```
module testeros1();

	// Inputs
	reg clk;
	reg rst;
	reg [0:8] i;

	// Outputs
	wire y;

	// Instantiate the Unit Under Test (UUT)
	eros1 uut (
		.clk(clk),
		.rst(rst),
		.i(i),
		.y(y)
	);

	initial
		// Initialize Inputs
		clk=1'b1;
		always #5 clk=~clk;
initial
begin
rst=1'b0;
#10 rst=1'b1;
end
initial
begin
   i=9'b000_000_000;
#10 i=9'b101_110_111;
#40 i=9'b111_111_111;
end

endmodule
```