```
module testmaineros;

	// Inputs
	reg clk;
	reg rst;
	reg [0:63] a;

	// Outputs
	wire [0:63] b;

	// Instantiate the Unit Under Test (UUT)
	maineros uut (
		.clk(clk),
		.rst(rst),
		.a(a),
		.b(b)
	);

initial
  clk=1'b1;
always #5 clk=~clk;

//declare inputs for rst
initial
 begin
  rst=1'b0;
  #10 rst=1'b1;
 end

 //declare inputs for i
initial
 begin

a=64'b00000000_00000000_00011000_00011000_00011000_00000000_00000000_00000000;
  //#20
a=64'b11101101_10010110_11110011_00000011_11000010_10111001_00011100_00010000;
  //#10
a=64'b01101101_10000110_11011011_00000011_11110010_10111001_01111100_01110000;
  //#10
a=64'b01101101_10000110_11011011_00000011_11110010_10111001_01111100_01110000;
  //#10 a=64'b0;
  //#10 a=64'b11111111_11111111_11111111_11111111_11111111_11111111_11111111_11111111;
end
```

```
initial
 begin
 $monitor("The input image matrix is\n");
 $monitor($time,"a=%b",a);
 $monitor($time,"b=%b",b);
end
endmodule
```