```
module tb_dilation();
//inputs as reg
reg clk,rst;
reg [0:8]i;
//outpus as wire
wire y;
//module instantiation
 dilation a0(clk,rst,i,y);
 //declare inputs for clk

initial
  clk=1'b1;
always #5 clk=~clk;

//declare inputs for rst
initial
 begin
  rst=1'b1;
  #10 rst=1'b0;
 end

//declare inputs for i

initial
 begin
  i=9'b111_111_111;
  #20 i=9'b000_000_000;
  #40 i=9'b011_100_110;
 end
initial
#100 $stop;
endmodule
```