Name: Aditya Bhalotia / Entry No.: 2021EE30698 / Course: ELL856. (Advanced topics in Power electronics)

Assignment: 1

(a) There are three available PSFBs i.e., diode ~~brig~~ bridge, centre tap rectifier ~~to and~~ based and current double rectifier.

Let us analyse each of these under the specs given!

(i) Diode Bridge PSFB converter:

Specifications for the converter are [same for all PSFBs].

→ $V_{in} = 400\,V$ → $V_{out} = 200\,V$ to $336\,V$ ($296\,V$ nominal).

→ Load power = 3.6 kW (maxm.) → $\Delta i_L = 75\%$ of average curr.

→ $f_{sw} = 100\,kHz$.

Assumptions:

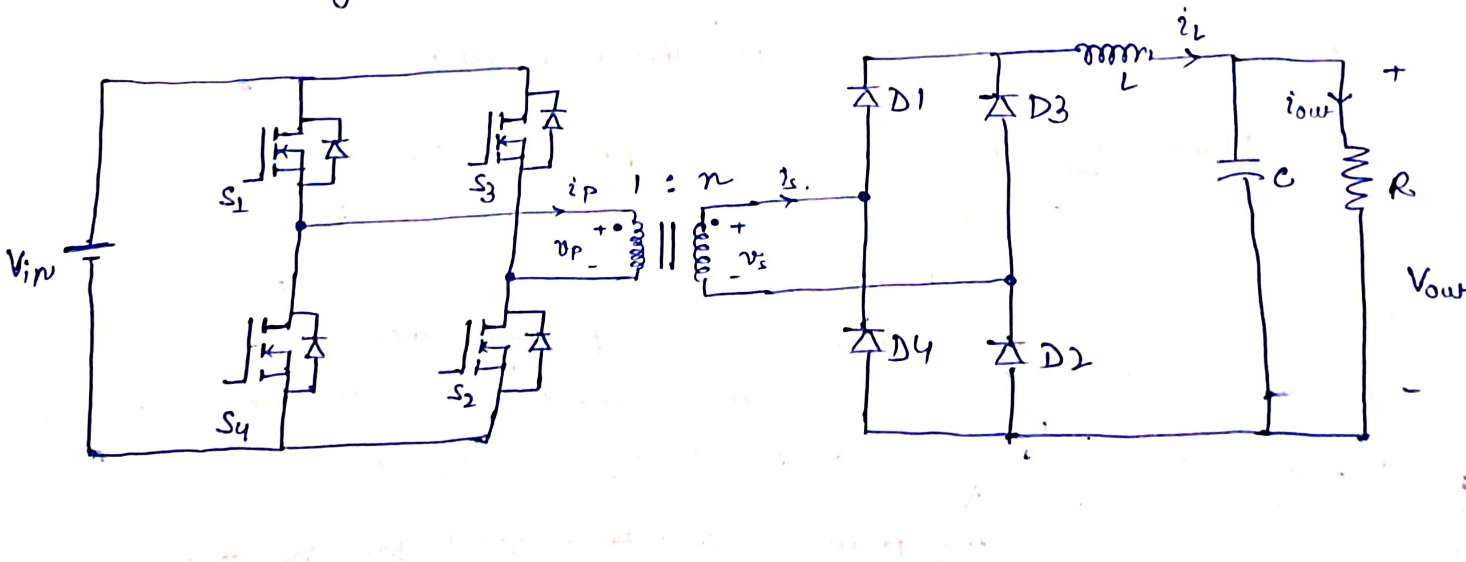
① Let us assume the switching frequency ripple in voltage to be 2V i.e., same for both totem pole and PSFB.

② Minimum power drawn from the converter be 360 W (0.1 pu).

③ Ideal elements while designing the converter.

④ Taken the input voltage capacitor as input voltage source.

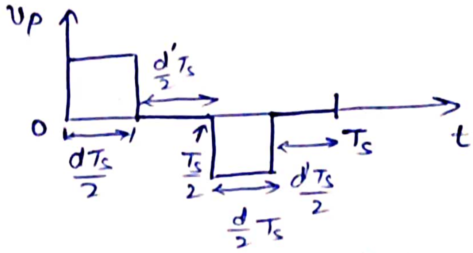
Circuit diagram:



We know that if voltage wave form, ~~at the~~ v_p looks like figure (a)

then

$$V_{out} = n D V_{in}$$



- Let us first choose the turns ratio.

Methodology: For choosing the turns ratio, we will limit the 'n' ~~dang~~ such that complete range of Vin can be achieved for different duty ratios.

Solution: $\because$ $200 \leq V_{out} \leq 336$

$$\Rightarrow \quad 0.5 \leq nD \leq 0.84$$

We can choose any value of $n \geq 1$. and $0.84 \leq n \leq$ ~~0.1~~ 1

Now if we choose $n < 1$, then value of D will be closer to 1 during some voltage range.

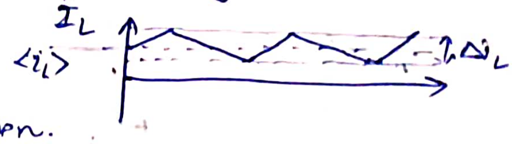
If we choose $n > 1$, then the voltage stress on diodes on secondary side will be more than Vin.

Thus, let us choose $n = 1$.

- Now, let us ~~choose~~. design the value of L::

Methodology: Allowed inductor ripple is 75% of average current:

Now, ~~the sho~~ if we can ensure that Δi_L is 75% when maximum ripple is possible then. in cases where ripple value is less, the contraint will automatically be satisfied.



~~Volt~~

Thus, inductor will be designed for the case when max^n ripple can occur and average current is mini

From the circuit diagram, we can conclude, that $I_L = I_{out}$ [$\because$ Capacitor absorbs the ripple current]

Now, during $0 \leq t \leq \frac{D}{2}T_s$, the inductor current rises,

$$\therefore \frac{L \Delta i_L}{\frac{D}{2}T_s} = nV_{in} - V_o \Rightarrow L = (nV_{in} - nDV_{in}) \frac{D}{2f_s} \cdot \frac{1}{\Delta i_L}$$

$$\Rightarrow \cancel{L = \frac{nV_{in}(1-D)D \, V_{out}}{2f_s \times 0.75 \times P_{out}}} \Rightarrow \cancel{L = \frac{n^2 V_{in}^2 D^2 (1-D)}{2f_s \times 0.75 P_{out}}}$$

$$\Delta i_L = \frac{nV_{in}(1-D)D}{2f_s \; L}.$$

Now, Δi_L will be max^m when $D = 0.5$.

$\therefore$ Inductor value should be ~~sh.~~ such that Δi_L is 75% of I_L at $D=0.5$.

$$I_L = \frac{P_{out}}{V_{out}} = \frac{P_{out}}{200} \text{ at } D = 0.5$$

$$\therefore \Delta I_L \Big|_{max} = 0.75 \times \frac{P_{out}|_{min}}{200} = 0.75 \times \frac{360}{200} = 1.35A.$$

$$\therefore L = 370.370 \mu H.$$

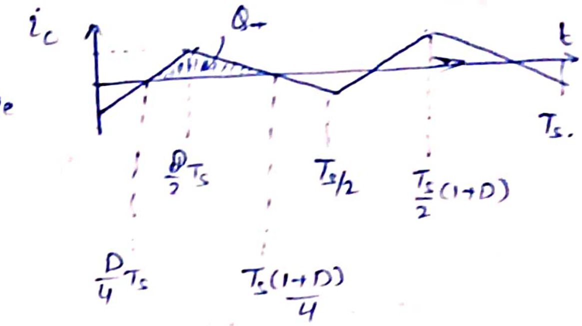
So, required value of inductance is $370.37 \mu H$. (we can round it up to $400 \mu H$).

- Now, let us design the Capacitor of PSFB:

Methodology: Observe that diode bridge PSFB is having same behaviour as a buck converter except the fact that 'n' is now also a parameter ($n=1$, in our case). So, the formula for computing the ripple is expected to be same as that of buck converter. So, we will use the concept of charge accumulated in capacitor to find ΔV_c and then calculate C.

Solution:

The current waveform in the Capacitor is



$Q_+ = C\frac{\Delta v_c}{2}$ where Δv_c is pk-pk ripple in output voltage.

$$\frac{C\Delta v_c}{2} = \frac{1}{2}\Delta i_L \times \frac{T_s}{4}$$

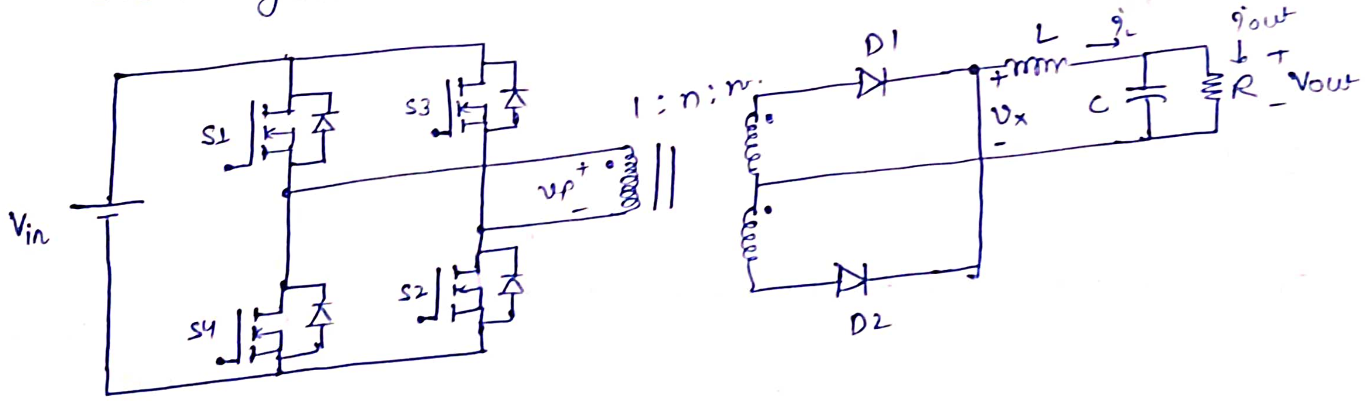
$$\Rightarrow C = \frac{\Delta i_L}{8 f_s (\Delta v_c/2)} = \frac{1.35}{8\times 100e3 \times (1)} = 1.6875\ \mu F$$

Thus, we have designed the passives for ~~an~~ diode bridge PSFB converter
$n=1$, $L = 370.37\ \mu H$, $C = 1.6875\ \mu F$

(ii) Centre tap PSFB converter:

Assumptions are same as that of ~~4-four~~ diode bridge PSFB.

Circuit diagram:



Methodology: We will avoid doing the whole calculation again and solve the circuit intuitively. Observe that potential v_x is same as the voltage produced by the diode bridge rectifier after it rectifies the pulsating v_s.

So, voltage relation remains same i.e., $V_{out} = nDV_{in}$.

Infact everything after v_x remains same. Thus, values of L and C remains unchanged given that $n=1$.

We will now use this fact to make further comments.

Solution: If $n = 1$, the rest of the passives remains same (i.e., values of L and C are same as diode bridge PSFB).

But the size of transformer secondary winding doubles. Thus the volume ~~doubles~~ increases for the transformer as centre tap PSFB will have twice the no. of windings as compared to diode bridge PFC.

Now, if we reduce n then to have the transformer sized same we would need $n = \frac{1}{2}$. But this is not possible.

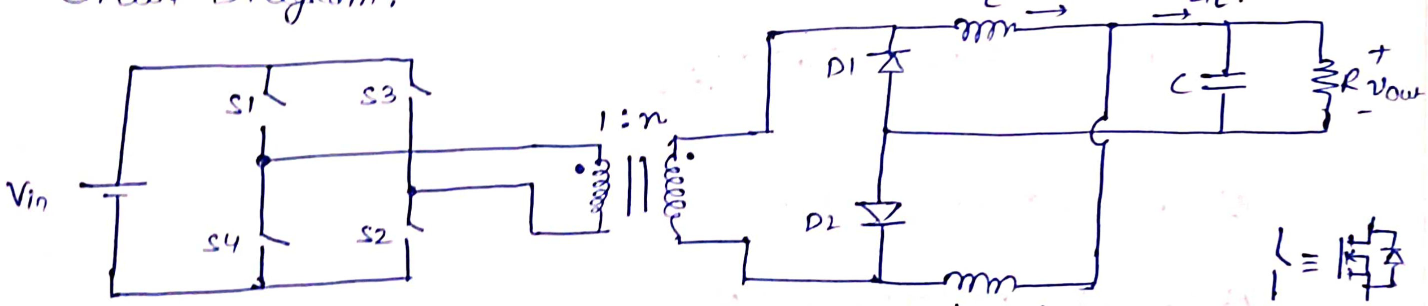
Reason: If $n = \frac{1}{2}$ then $nDV_{in} = 336$ would require $D = 1.68$ (not possible).

Thus, in terms of size we can reject centre tap PSFB.

(iii) Current Doubler Rectifier:-

Assumptions are same as those in the previous cases.

Circuit Diagram:



Methodology: Here also we will first find the value of n. ~~Now, if~~ Then we will calculate the value of L and C.

For the value of n we will use the relation b/w V_{in}, D, n and V_{out}. Then by using constraints on D ~~and~~ we will find the value of n.

Solution:

We know that $V_{out} = \frac{nDV_{in}}{2}$ for current doubler rectifier.

Now, to have same D as the diode bridge PSFB, $n = 2$.

At best we can take n such that

$$\frac{n V_{in}}{2} = 336 \Rightarrow n = 1.68.$$

So, we cannot reduce n as compared to the diode bridge PSFB.

We will take $n = 2$, to have $0.5 \le D \le 0.84$.

Now, let us design inductor of current doubler rectifier.

Methodology: We will find the expression of value of Δi_L and then find the point where maximum ripple occurs and the use that point to get appropriate L.

Solution:

$$\frac{L \Delta i_{L_0}}{\left(\frac{D}{2} T_s\right)} = nV_{in} - V_o.$$

$$\Delta i_L = nV_{in}(1 - D/2)\, D/2f_s L$$

Δi_L is max^m when $D = 1$

Since inductors are ideal,

$$I_{L_1} = I_{L_2} = I_{out}/2.$$

V_o =

Note that $D = 1$ is never possible as $n = 2$ and $0.5 < D < 0.84$.

So, actual $\Delta i_L|_{max}$ will occur at $D = 0.84$.

$$\Delta i_L|_{max} = \frac{1.9488 \times 10^{-3}}{L_1}$$

$$\Delta i_L|_{max} = 0.75\, I_L|_{min} = 0.75 \times \frac{I_o|_{min}}{2} = 0.375 \times \frac{P_{out}|_{min}}{V_{out}|_{max}} \quad [\because D = 0.84]$$

$$\Rightarrow \Delta i_L|_{max} = 0.375 \times \frac{360}{336} = 0.40178$$

$$\therefore L_1 = \frac{1.9488 \times 10^{-3}}{0.40178} = 4.850\ mH. = L_2.$$

So, not only size of transformer, size of inductors is also too large as compared to diode bridge PSFB.

Thus, we will use diode bridge PSFB with

$n = 1$, $L = 370.37\ \mu H$ and

$C = 1.6875\ \mu F$.

- Design of passives of totem pole PFC.

~~Design of inductor of totem pole PFC:~~

Inductors need to be designed to have ripple such that at maximum point of Δi_L the value should be in given limit.

Capacitors needs to designed to filter out 2ω ripple.

Q: Specs of totem pole PFC converter:

→ V_{ac} = 85V to 265V (rms)

→ freq., f_{ac} = 45 – 65 (Hz)

→ Power factor > 0.99.

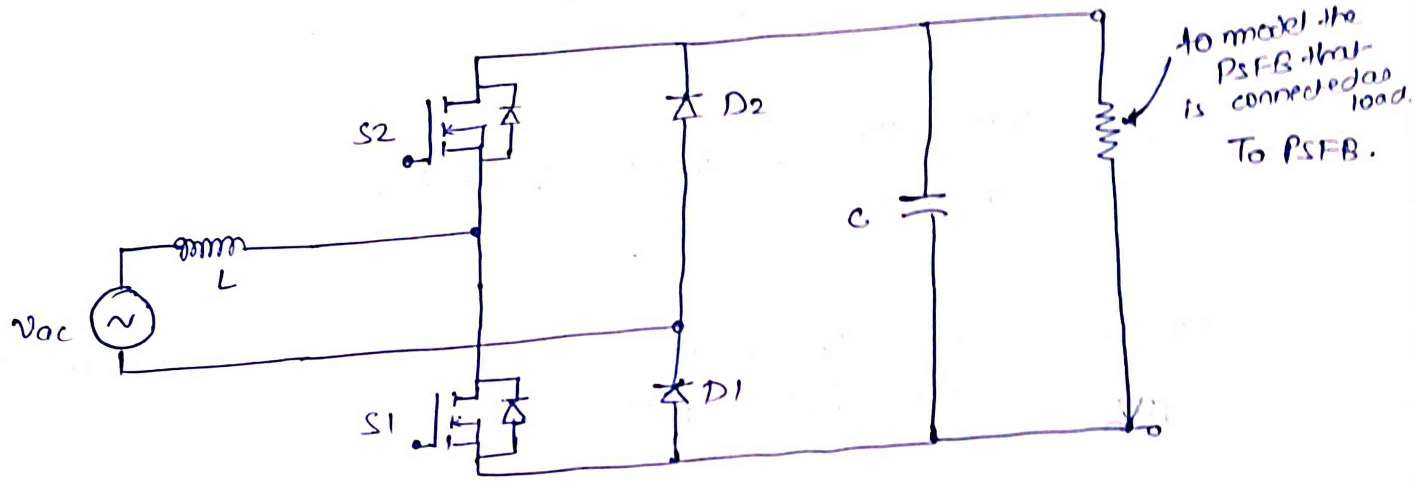
→ Δi_L = 25% of peak current.

→ V_{dc} = 400V (nominal)

→ $\Delta V_{dc\,2\omega}$ = 20V.

→ f_{sw} = 50kHz.

Circuit diagram of totem pole PFC:



Assumption:

~~Δi_L is 25% of maximum peak current.~~

Δi_L is 25% of peak current at maximum voltage and maximum power (to have smaller inductor size).

- **Design of inductor:**

Methodology: Determine the maximum possible ripple and it should be 25% of peak current.

Solution.

$$\frac{L\,\Delta i_L}{DT_s} = V_{in} \Rightarrow \frac{L\,\Delta i_L}{DT_s} = (1-D)\,V_{out}$$

$$\Rightarrow \Delta i_L = \frac{D(1-D)\,V_{out}}{f_s L}$$

$\Delta i_L|_{max}$ happens at D = 0.5.

$$\Delta i_L|_{max} = 2\times 10^{-3}/L$$

$\Delta i_L|_{max} = 25\%$ of $I_{ac}|_{pk}|_{min} = \frac{25}{100} \times \frac{2 P_{out}|_{max}}{V_M|_{max}}$

$= 4.803.$

$\therefore L = 416.406\ \mu H.$

- Capacitor design for totem pole PFC:

The capacitor needs to be ~~dis~~ designed to filter out twice the line frequency.

$$C_{totem} = \frac{P_{out\,max}}{\Delta V_{dc} \times V_{dc} \times 2\pi f_{ac}|_{min}} = \frac{3600}{20 \times 400 \times 2\pi \times 45} = 1.5915\ mF$$

$$\approx 1.6\ mF$$

Thus, the totem pole PFC passive components values are:

$L = 416.406\ \mu H$ and $C = 1.6\ mF$.

(b) Let us calculate the stress on devices:

For totem pole:

Voltage stress on all the devices is dc voltage at output.

$\therefore$ All switches should be rated for, $(400 \times 2) = 800V.$

$\uparrow$ safety factor

[600V if 1.5 is safety factor]

The max currents the each switch carry $= \left[\frac{2 \times 3600}{85\sqrt{2}}\right] \times 2 = 120A.$

$\uparrow$ safety factor

[90A if 1.5 is safety factor]

Switching frequency of high frequency switch = 50KHz.
Switching frequency of low frequency leg = 50Hz.

Thus, MOSFETs should be rated for 800V-600V, 120A, 50KHz switching frequency.
Diodes should be rated for 800V-600V, 120A, 50Hz switching frequency.
for totem pole PFC.

For diode bridge PSFB:

The primary side switches should be rated to block (400V×2) = 800V.

Similarly secondary side should be rated for 800V as well since $n = 1$.

On primary side as well as secondary side, current ratings should also be same because $n = 1$.

$\therefore$ Current rating $= 2 \times \frac{3600}{200} = 36A$, 27A with 1.5 safety factor

Hence, all the mosfets and diodes should be rated to block 800V-600V and carry 36A with switching frequency of 100 KHz.

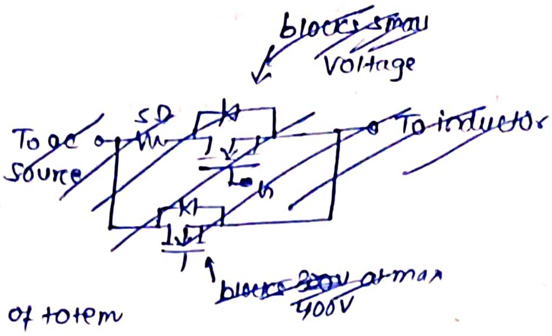
Now, since we know the device ratings, we will search for the appropriate devices.

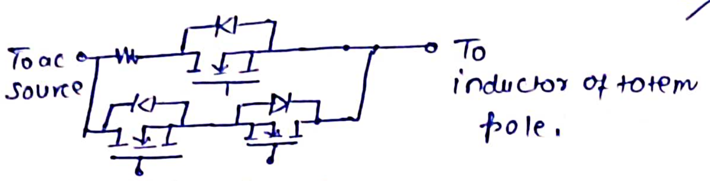
Also, on running the simulation, it was observed that in totem pole PFC during transients the peak current was 250A which is quite high. To reduce this a resistor is being introduced in the current path to limit the current to 80A.
So, instead of 120A rated diodes and mosfets we can choose devices rated at ~~80~~ 85 - 90A.

~~These~~
Also, two more kinds of devices ~~can be~~ needs to be chosen to have this introduction of resistors possible. Among These MOSFETS, one will block voltage whose max^m magnitude is 400V and another will block very small voltage. (say 10-20V)

Both mosfets should carry 80A current

Lower mosfet can be a Si or SiC MOSFET. upper MOSFET can be Si MOSFET





MOSFET for current limiting in Totem Pole:

Upper Leg : PSMN5R0-40MLH

Reason: Small voltage blocking, high current conduction satisfied by this. Lower power dissipation.

Lower leg : UF3C065030K4S + PSMN5R0-40MLH. [We did not use two MOSFETs rated at 650V as that would increase the cost].

Reason: Requisite blocking and conduction current satisfied.

MOSFETs for totem pole High Frequency Leg:

These are GaN devices that should be rated b/w 600-810V and to carry 85A of current at max. They should switch at high frequency.

Part No: TP65H015G5WS.

Reason: Satisfy stress limits. High frequency switching.

Diodes for totem pole low frequency leg:

These are low frequency switched SiC devices. They should handle a stress of about 600-800V and carry a peak current of 85A.

Part. No:- GD2x30MPS06D.

Reason: Satisfied the voltage and current stress limits at higher temperature as well.

MOSFETs for primary side of PSFB:

These are also SiC devices. But they are ~~designe~~ chosen to carry lower current values (36A at max, 27A at least considering safety factor). They are high frequency switched devices since $f_{sw}|_{PSFB} = 100kHz$

Part No: C3M0060065J

Reason: The required voltage and current stress are handled by the device even at higher temperatures.

- Diodes on secondary side of PSFB:

These diodes are also high frequency switched diode. ~~They block 400V and~~ They should be rated for 600-800 V and 27-36A of current.

Part No:- FEP30JP-E3.

Reason: Ultrafast recovery helps in faster switching.

And voltage and current stresses are as per requirements.

(c) Controller Design:

We need to design the following controllers:

1. Current controller for inner loop of totem pole PFC.
2. Voltage controller for outer loop of totem pole PFC.
3. Current Controller for inner loop of ~~fixed~~ diode bridge PSFB.
4. Voltage controller for outer loop of diode bridge PSFB.

One more logic needs to be designed that will choose whether we need to control i using current loop i.e., CC mode or whether we need to control voltage using voltage mode i.e., CV mode in PSFB.

These needs to be designed depending on the battery SoC profile.

① Current controller for totem Pole PFC:

We know that,

$$G_{id}(s) = \frac{V_{out}}{sL}$$

Let us say that Vout is tightly controlled and maintained at 400V which will be done by voltage controller.

$L = 416.406\,\mu H$.

Following assumptions have been made while designing all the controllers:

- Reference voltage can be 5V at maximum value of concerned quantity.
- The PWM block has carrier of ~~1~~ 5V.
- $v_{control}$ can vary ~~from~~ upto ~~10V~~ 15V at max. ~~at steady~~

Now let us start the design of current controller:

$$T_{ui}(s)\Big|_{\text{totem pole}} = R_{sense}\,\frac{1}{V_M}\,\frac{V_{out}}{sL}$$ [Uncompensated loop gain]

$$R_{sense} = \frac{5V}{i_L|_{max}} = \frac{5V}{\frac{\sqrt{2}\times 3600}{85}} = 83.5\,m\Omega.$$

$V_M = 5V$.

$$\therefore\ T_{ui}(s)\Big|_{\text{totem pole}} = \frac{16042.0359}{s}$$

Let us say we want a bandwidth of 5KHz ($\frac{1}{10}$th of f_{sw}|totem pole) and a phase margin of roughly 50°. and zero steady state error.

∴ A PI controller is sufficient to acheive this as uncompensated loop has 90° of phase margin and we need phase reduction.

Let $G_{ci}(s)\Big|_{\text{totem pole}} = G_{c\infty}\left(1 + \frac{w_L}{s}\right)$

$f_c = 5000$

$$\measuredangle T_{ui}(j2\pi f_c) + \measuredangle G_{ci}(2\pi f_c j) = -130°$$

$$\Rightarrow \measuredangle G_{ci}(2\pi f_c j) = -130° + 90°$$

$$\Rightarrow -\tan^{-1}\left(\frac{w_L}{2\pi f_c}\right) = -40°$$

$$\Rightarrow w_L = 2\pi f_c \times \tan 40° \Rightarrow w_L = 26361.092 \text{ rad/s.}$$

and $\quad \|T_{ui}(j2\pi f_c)\| \, \|G_{ci}(j2\pi f_c)\| = 1$

$$\Rightarrow \frac{16042.0359}{2\pi \times 5000} \times G_{c\infty}\sqrt{1 + \left(\frac{26361.092}{2\pi \times 5000}\right)^2} = 1$$

$$\Rightarrow G_{c\infty} = 1.50018.$$

∴ PI compensator for current controller loop is

$$G_{ci}(s)\Big|_{\text{totem pole}} = 1.50078\left(1 + \frac{26361.092}{\cancel{10000} \cdot s}\right)$$

(2) Voltage controller for totem pole :

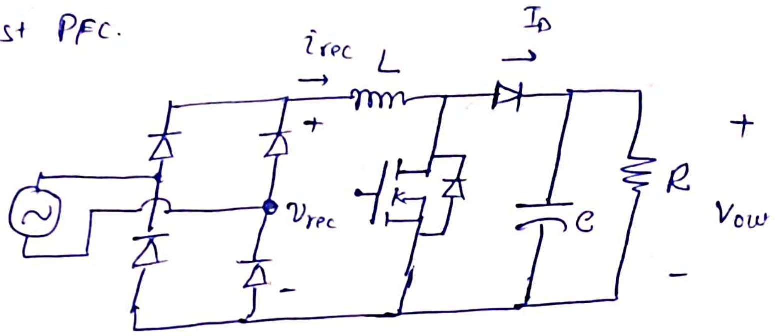
Let us try to find the plant transfer function of voltage loop :

~~Let i_D be the diode current~~.

We can say that totem pole PFC is nothing but a circuit equivalent to boost PFC.

So, the transfer functions will also remain same.

Now let us consider a boost PFC.



We know that

$\cancel{v_{rec}(t)\, i_{rec}(t) = v_{out}\, i_D}$.

$\Rightarrow \cancel{v_{rec} \dfrac{k_x v_{control}(t)\, v_{rec}(t)}{V_M^2}} = \cancel{v_{out}(t)\, i_D(t)}$.

$$P_{out}\big|_{avg} = \langle v_{out} \rangle_{T_s/2} \langle i_D \rangle_{T_s/2}$$

$$\Rightarrow \frac{V_M}{\sqrt{2}} \cdot \frac{I_M}{\sqrt{2}} = (V_{out} + \tilde{v}_{out})(I_D + \tilde{i}_D)$$

[V_M = Peak of ac voltage
I_M = Peak of ac current]

$$\Rightarrow \frac{V_M}{2} \times \frac{k_x V_M \langle v_{control} \rangle_{T_s/2}}{R_{sense} V_M^2} = (V_{out} + \tilde{v}_{out})(I_D + \tilde{i}_D)$$

$$\Rightarrow \frac{k_x}{2R_{sense}} [V_{control} + \tilde{v}_{control}] = [V_{out} + \tilde{v}_{out}][I_D + \tilde{i}_D]$$

$$\Rightarrow \frac{k_x}{2R_{sense}} \tilde{v}_{control} = \tilde{v}_{out} I_D + \tilde{i}_D V_{out}.$$

Where 'k_x', R_{sense}, $v_{control}$ are standard notations used in boost PFC.

and $\tilde{v}_{out} = ~~R_{eq}~~ (R \parallel 1/sC)\, \tilde{i}_D$

$$\therefore \frac{k_x}{2R_{sense}} \tilde{v}_{control} = \tilde{v}_{out} I_D + V_{out} \frac{\tilde{v}_{out}}{(R \parallel 1/sC)}$$

In ~~are~~ DC sense $V_{out} = I_D R$

$$\therefore \frac{k_x \tilde{v}_{control}}{2R_{sense}} = \tilde{v}_{out} \left[\frac{V_{out}}{R} + \frac{V_{out}(sRC+1)}{R} \right]$$

$$\Rightarrow \tilde{v}_{control} \frac{k_x}{2R_s} = \tilde{v}_{out} \left[\frac{1+sRC/2}{R/2} \right] V_{out}$$

$$\Rightarrow \frac{\tilde{v}_{out}}{\tilde{v}_{control}} = \frac{k_x}{2R_{sense} V_{out}} \frac{R/2}{1+sRC/2}$$

Note that voltage loop will generate $V_{control}$ and gave V_{out} as the output.

Thus, our plant transfer function is $\frac{k_x}{2R_{sense} V_{out}} \frac{R/2}{1+sRC/2}$

Now let us find k_x.

Let us say that at ~~Peak~~ $P_{out} = 3600W$, $V_{control} = 12V$,

Although we assumed that $V_{control}$ goes upto 15V we set 12V as the maximum power control voltage.

$V_{control}$ is kept till 15V to reduce the settling time of ~~loop~~. voltage at the output of totem pole.

So, $P_{out} = \dfrac{k_x\, v_{control}}{2 R_{sense}} \Rightarrow 3600 = \dfrac{k_x \times 12}{2 \times 0.0835}$

$$\Rightarrow \boxed{R_x = 50.1}$$

Hence we set $R_x = 50.1$ for the multiplier block.

Also, note that R varies depending on the output power being drawn.

$$R_{min} = \frac{R \cdot V_{out}^2}{P_{out\,max}} = \frac{400 \times 400}{3600} = 44.444\,\Omega \qquad R_{max} = \frac{V_{out}^2}{P_{out\,min}} = \frac{400 \times 400}{360} = 444.44\,\Omega.$$

$\therefore$ ~~Also~~ R varies b/w $44.444\,\Omega$ to $444.444\,\Omega$.

Let us know find voltage sensor gain, $H = \frac{5}{400} = 0.0125.$

Now,

$$T_{uv}(s)\Big|_{\substack{totem \\ at\ R_{min}}} = \frac{50.1 \times 22.222}{2 \times 0.0835 \times 400} \cdot \frac{1}{1 + s\left[\frac{44.444 \times 1.6 \times 10^{-3}}{2}\right]} \cdot \underbrace{0.0125}_{H}$$

$$= \frac{0.2083312 5}{1 + \left(s/28.27436\right)}$$

$$T_{uv}(s)\Big|_{\substack{totem \\ at\ R_{max}}} = \frac{50.1 \times 222.222}{2 \times 0.0835 \times 400} \times 0.0125 \cdot \frac{1}{1 + s\left[222.222 \times 1.6 \times 10^{-3}\right]}$$

$$= \frac{2.0833125}{1 + s/2.827436}$$

So, we need to design the controller for worst case.

On plotting the bode plots (attached in PDF), we observe that if we design the controller to acheive a bandwidth of 20 Hz and phase margin of roughly 50° for R_{max}, the we can acheive a stable response for all other values of R.

Observe that the voltage loop bandwidth is much less than twice the line frequency. Reason being we do not want our voltage loop to react to any voltage reference ~~more~~ which asks me to vary the voltage with half lime cycle.

Now, the plant transfer function is of 1st order.

So, a PI compensator will work to acheive required bandwidth and phase margin.

$$\text{Let } G_{cv} = G_{cv\infty}\left(1 + \frac{\omega_{Lv}}{s}\right)$$

$f_c = 20\,Hz$

$$\angle T_{uv}(j2\pi f_c)_{\substack{totem \\ R_{max}}} + \angle G_{cv}(j2\pi f_c) = -130^\circ$$

$$\Rightarrow -\tan^{-1}\left(\frac{40\pi}{2.827436}\right) - \tan^{-1}\left(\frac{\omega_{Lv}}{2\pi \times 20}\right) = -130^\circ$$

$$\Rightarrow \omega_{Lv} = 2\pi \times 20 \tan(41.288^\circ)$$

$$\Rightarrow \omega_{Lv} = 110.3206 \text{ rad/s.}$$

$$\|T_{uv}(j2\pi f_c)\| \, \|G_{cv}(j2\pi f_c)\| = 1$$

$$\Rightarrow \frac{2.0833125}{\sqrt{1+\left(\frac{40\pi}{2.827436}\right)^2}} \cdot G_{cv\infty}\sqrt{1+\left(\frac{110.3206}{40\pi}\right)^2} = 1. \quad \Rightarrow G_{cv\infty} = 16.036.$$

∴ Transfer function of voltage controller for totem pole is:

$$G_{cv} = 16.036\left(1 + \frac{110.3206}{s}\right).$$

Note: This controller was designed keeping in mind that no ~~be~~ filtering of 2ω ripple is being done. We can use filtering and design another controller that will have higher bandwidth.

(3) Current controller design for diode bridge PSFB:-

Let us first write the plant transfer function.

Observe that the diode bridge PSFB has same dynamic equation as that of buck converter. [This was discussed in class] except for the fact that V_{in} is replaced by nV_{in}.

$$G_{id}\Big|_{PSFB}(s) = \frac{nV_{IN}}{R} \frac{1+sRC}{1+\frac{sL}{R}+s^2LC}$$

∵ Totem Pole PFC is controlled using a properly designed ~~to~~ voltage controller.

∴ At steady state, $V_{IN} = 400V$.

Also, R varies as voltage at the output and power output changes.

$V_{out}|_{min} = 200V$, $V_{out}|_{max} = 336V$

$P_{out}|_{min} = 360W$ $P_{out}|_{max} = 3600W$.

$$\therefore R_{min} = \frac{V_{out}^2|_{min}}{P_{out}|_{max}} = \frac{200\times200}{3600} = 11.111\Omega$$

$$R_{max} = \frac{V_{out}^2{}_{max}}{P_{out\,min}} = \frac{336\times336}{360} = 313.6\Omega.$$

$$\therefore\ G_{id}(s)\Big|_{\substack{PSFB\\ \text{at } R_{min}}} = \frac{400}{11.111} \cdot \frac{1 + s \cdot 11.111 \times 1.6875 \times 10^{-6}}{1 + s \times \frac{370.370 \times 10^{-6}}{11.111} + s^2 (1.6875 \times 370.370 \times 10^{-12})}$$

$$= 36.00036 \frac{\left(1 + s/53333.38667\right)}{1 + s/29999.73 + \left(s/40000.02\right)^2}$$

$$G_{id}(s)\Big|_{\substack{PSFB\\ \text{at } R_{max}}} = \frac{400}{313.6} \frac{(1 + s \cdot 313.6 \times 1.6875 \times 10^{-6})}{1 + s\left(\frac{370.370 \times 10^{-6}}{313.6}\right) + s^2 (1.6875 \times 370.370 \times 10^{-12})}$$

$$= 1.275510 \frac{\left(1 + s/1889.6447\right)}{1 + \left(s/846720.8467\right) + \left(s/40000.02\right)^2}$$

Now, let us find the value of sensor gain for current loop,

$$R_{sense}\Big|_{PSFB} = 5/I_{L}|_{max} = \frac{5}{\frac{Pout|_{max}}{Vout_{min}}} = \frac{5 \times 200}{3600}$$

$$= 277.78\,m\Omega.$$

$$\therefore\ T_{ui}(s) = \frac{R_{sense}}{V_M} \times G_{id}(s).$$

On plotting the bode plot for both the $G_{id}(s)$, we observed that if we design to controller to acheive a bandwidth of 20KHz and phase margin of 50° for the R_{max} case then we will get a stable response for all other cases.

So, $T_{ui}(s)$ for designing the controller is,

$$T_{ui}(s) = \frac{0.27778}{5} \times 1.275510 \; \frac{1 + s/1889.6447}{1 + s/846720.8467 + (s/40000.02)^2}$$

One can observe that the phase goes to $-90°$ at the very least.
So, a PI compensator will be sufficient to get the required bandwidth and phase margins.

Let $G_{ci}(s)\Big|_{PSFB} = G_{c\infty}\left(1 + \frac{\omega_{Li}}{s}\right)$.

$f_c = 20$ kHz [$1/5$th of f_{sw} of PSFB].

$\angle G_{ci}(j2\pi f_c) + \angle T_{ui}(j2\pi f_c) = -180° + 50°$

$\Rightarrow -\tan^{-1}\left(\frac{\omega_{Li}}{2\pi \times 20000}\right) = -40°$

$\Rightarrow \omega_{Li} = 2\pi \times 20000 \tan 40°$

$= 105444.3695$ rad/s.

$\|T_{ui}(j2\pi f_c)\| \, \|G_{ci}(j2\pi f_c)\| = 1$

$$\Rightarrow \frac{0.27778}{5} \times 1.275510 \times \frac{(40000.02)^2}{2\pi \times 20000 \times 1889.6447} \cdot G_{c\infty}\sqrt{1 + \tan^2 40} = 1$$

$\Rightarrow G_{c\infty} = 1.60438.$

Thus, the required PI compensator for the current controller for PSFB is,

$$G_c\Big|_{PSFB} = 1.60438\left(1 + \frac{105444.3695}{s}\right)$$

(4) Voltage controller for the voltage loop of PSFB:

Let us first write the plant transfer function.

$$\frac{\tilde{v}_{out}}{\tilde{i}_{ref}} = \frac{\tilde{v}_{out}/\tilde{d}}{\tilde{i}_{out}/\tilde{d}} \times \frac{\tilde{i}_{out}}{\tilde{i}_{ref}}$$

and,

$$\tilde{v}_{out}/\tilde{d} = \frac{nV_{in}}{1 + sL/R + s^2LC}$$

for PSFB since the dynamic equation is same as buck converter.

$$\therefore \frac{\tilde{v}_{out}}{\tilde{i}_{ref}} = \frac{nV_{in}}{nV_{in}/R\,(1+sRC)} \cdot \frac{1}{R_{sense}}$$

$$= \frac{R}{R_{sense}} \cdot \frac{1}{1+sRC} = G_{vv}(s)$$

This is the required plant transfer function because, the voltage loop will give v_{out} as output by controlling the current reference.

$\therefore\ T_{uv}(s) = H_{PSFB} \cdot G_{vv}(s)$

Where $H_{PSFB} = \frac{5}{336} = 0.014881.$

$$G_{vv}(s)\Big|_{at\ R_{max}} = \frac{313.6}{0.27778} \cdot \frac{1}{1+ s/1889.6447}$$

$$= \frac{1128.9509}{1+ s/1889.6447}.$$

$$G_{vv}(s)\Big|_{at\ R_{min}} = \frac{39.996.760}{1+ s/53333.32667}$$

BW of voltage loop $= \frac{1}{10}$ th of BW of current loop $= 2000$ Hz.

On plotting the bode plot, it was observed that if we can acheive a bandwidth of 2kHz and phase margin of 50° for R_{max} case then the loop will be stable for ~~both~~ all the values of R_o.

So, T_{uv} for controller design is:

$$T_{uv}(s) = \frac{16.799918}{1+ s/18809.6447.}$$

Observe that the ~~closed loop~~ loop gain is a 1st order t.f.

So, PI compensator is sufficient to acheive the required specs

Let $G_{cv} = G_{cm}\left(1+ \frac{N_{Lvv}}{s}\right)$

$f_c = 2000\ Hz$

$$\measuredangle T_{uv}(j2\pi f_c) + \measuredangle G_{cv}(j2\pi f_c) = -130^\circ$$

$$\Rightarrow -\tan^{-1}\left(\frac{2\pi \times 2000}{18889.4447}\right) - \tan^{-1}\left(\frac{W_{Lvv}}{2\pi f_c}\right) = -130^\circ$$

$$\Rightarrow W_{Lvv} = 14229.09056\ rad/sec$$

and $\|T_{uv}(j2\pi f_c)\| \, \|G_{cv}(j2\pi f_c)\| = 1$

$$\Rightarrow \frac{16.799918}{\sqrt{1 + \left(\frac{\cancel{14229}\ 4000\pi}{1889.4447}\right)^2}} \cdot G_{c\infty}\sqrt{1 + \left(\frac{14229.09056}{4000\pi}\right)^2} = 1$$

$$\Rightarrow G_{c\infty} = 0.26500.$$

Thus, the required controller for voltage loop is,

$$G_{cv}(s)\Big|_{PSFB.} = 0.26500\left(1 + \frac{14229.09056}{s}\right)$$

Thus, we have designed all the controllers.

Next step is to sense SoC from the BMS and ~~do~~ decide whether to activate voltage loop or not in the PSFB stage.
One of the ways could be to sense the current going into the battery and integrate it over time to get the amount of charge that the battery has drawn. We know the full capacity of battery. Now if this SoC is b/w 20 % to 80 %, then instead of generating the current reference from voltage controller, ~~and~~ we will set the current reference by

Design of notch filter for totem pole PFC:

Designing Bandpass:

From the bode plot of MATLAB, I decide $Q = 2$ to have significant ~~reject~~ acceptance in 90-130Hz bandwidth in the bandpass stage, so that on having subtraction from the output voltage, we can reject 90-130Hz component.

Centre frequency was chosen as; $\omega_0 = 100\text{ Hz} = 200\pi$ rad/s.

$$\therefore G_{bandpass}(s) = \frac{s/2\times 200\pi}{1 + s/400\pi + (s/200\pi)^2}$$

Thus,

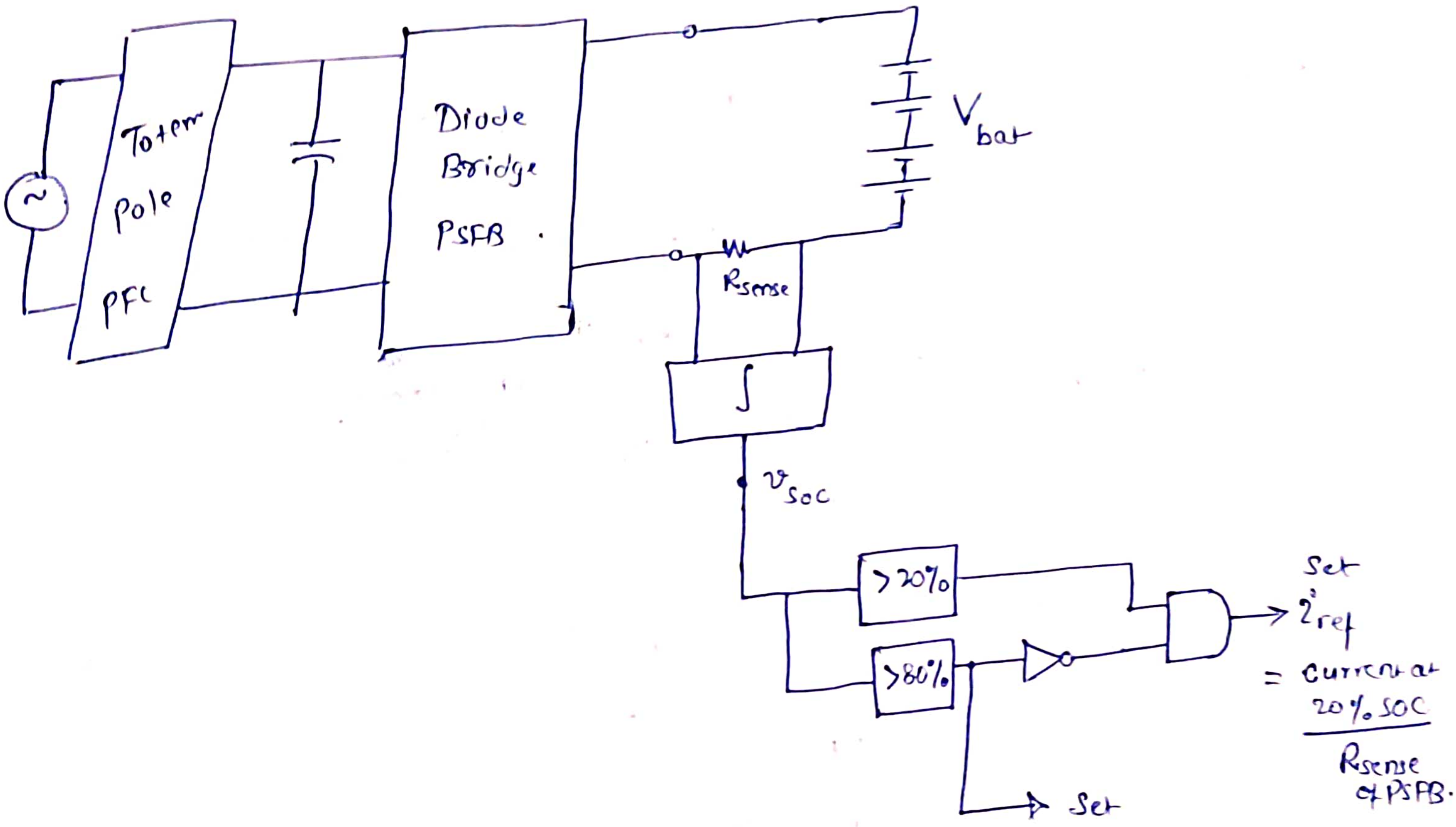
$$G_{notch}(s) = 1 - G_{bandpass}(s)$$

$$= \frac{1 + (s/200\pi)^2}{1 + s/400\pi + (s/200\pi)^2}.$$

The simulation includes this notch filter and the phase response of voltage controller was appropriately adjusted to get the phase margin of 50° ~~at~~ and bandwidth of 20Hz.

Sensing the current from BMS. If SoC > 80%, then the voltage loop will be used to get the current reference, where a fixed voltage reference will be given to the voltage loop.

Circuit Diagram explaining the idea:



$V_{ref} = \frac{\text{Voltage at 80\% SoC}}{H_{PSFB}}$

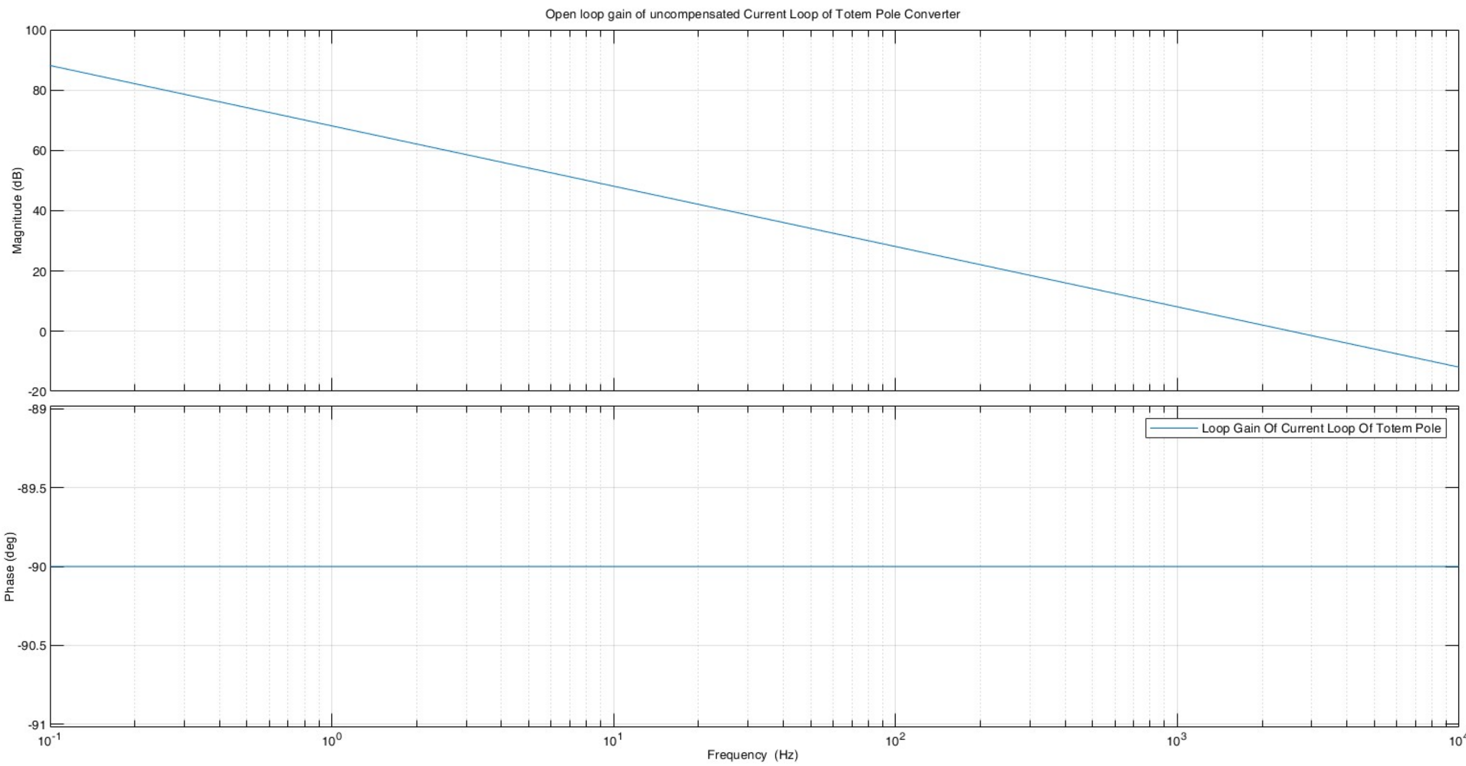
Also, instead of connecting the voltage controller output directly to the i_{ref}, we can connect it to a mux/switch to select whether i_{ref} is constant or will be generated from voltage loop.

~~while determining the~~

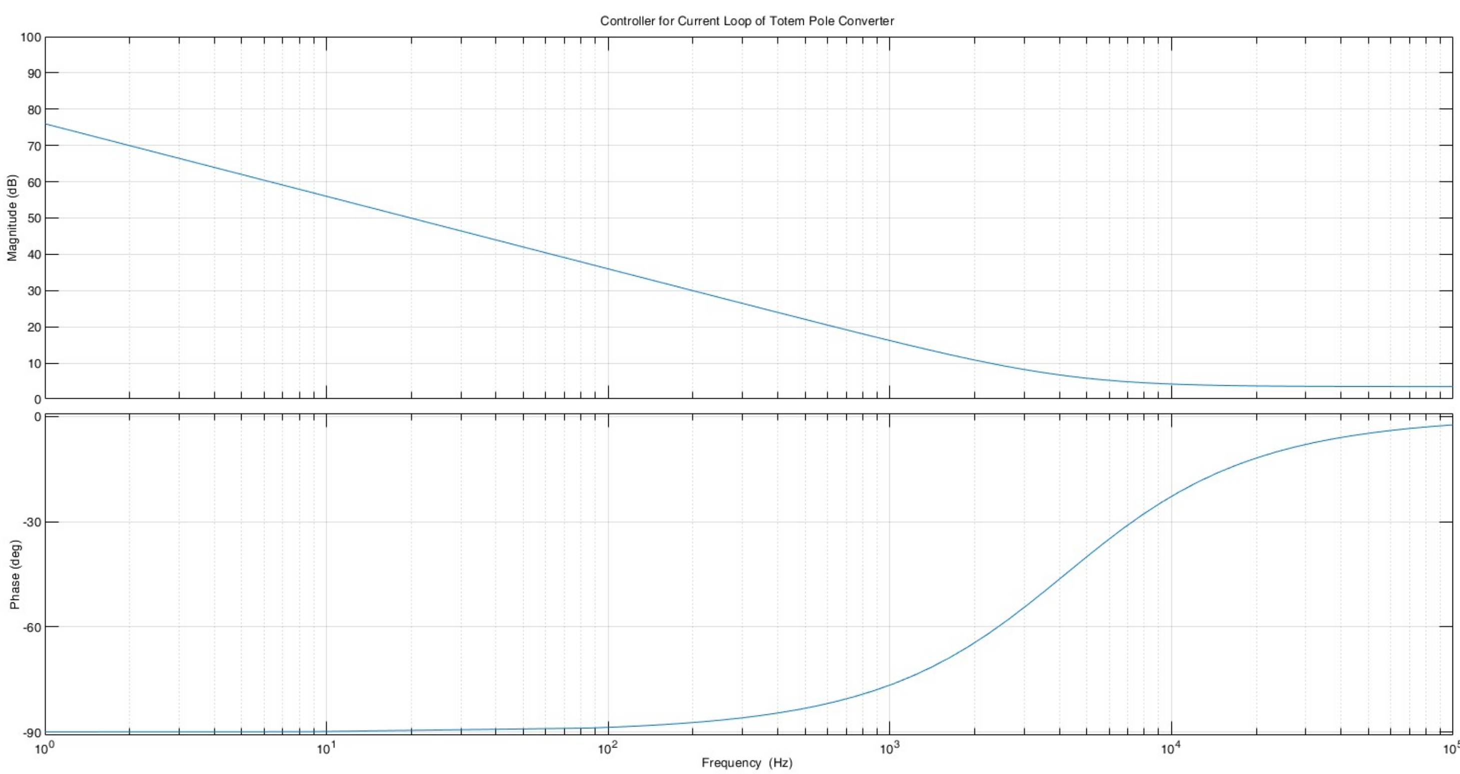
Another way could be to assume that 296 V (nominal output voltage) occurs at 80% SoC and 200V at 20% SoC. Then voltage sensing would be enough to comment on SoC and decide the state of controller.

(c) **1. Totem Pole converter:**

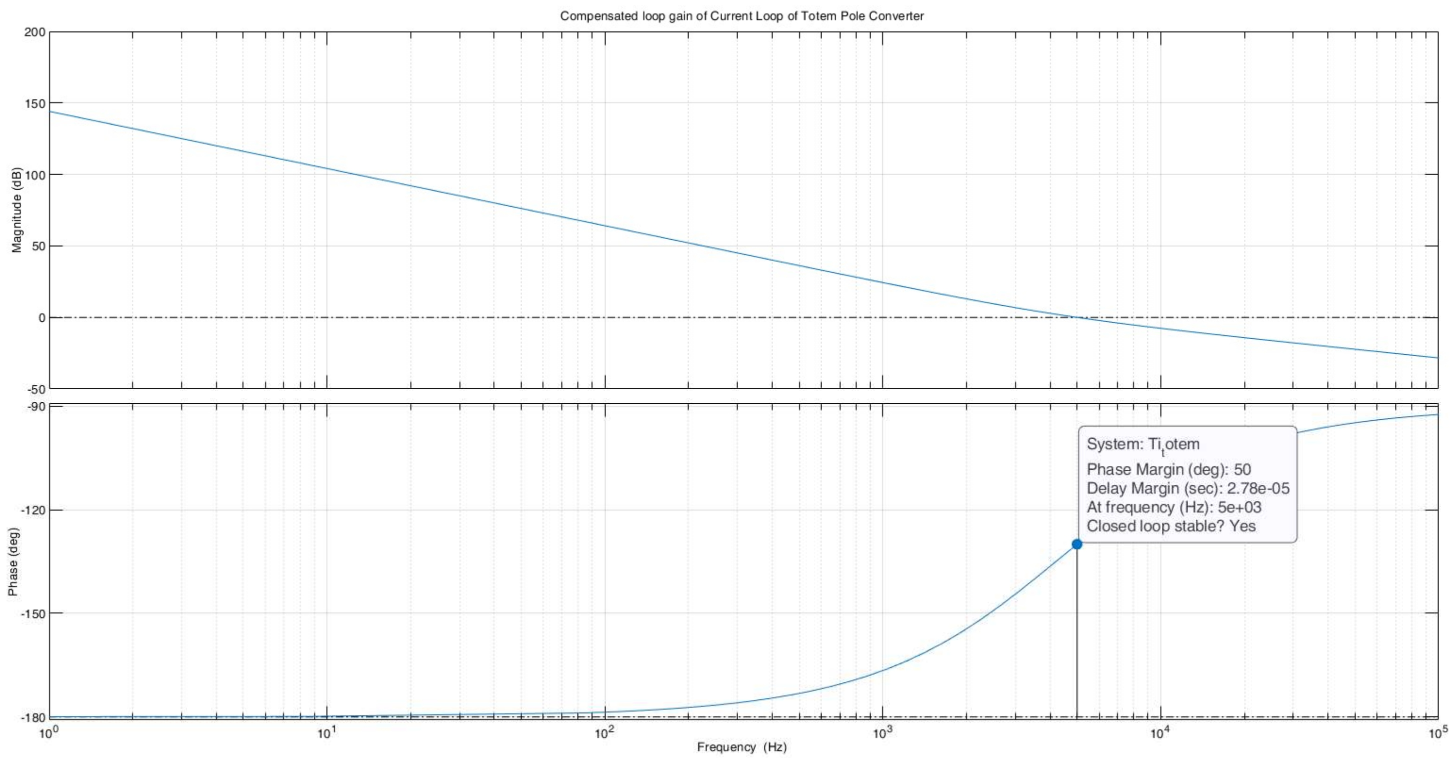
<u>Bode plot for uncompensated current loop:</u>



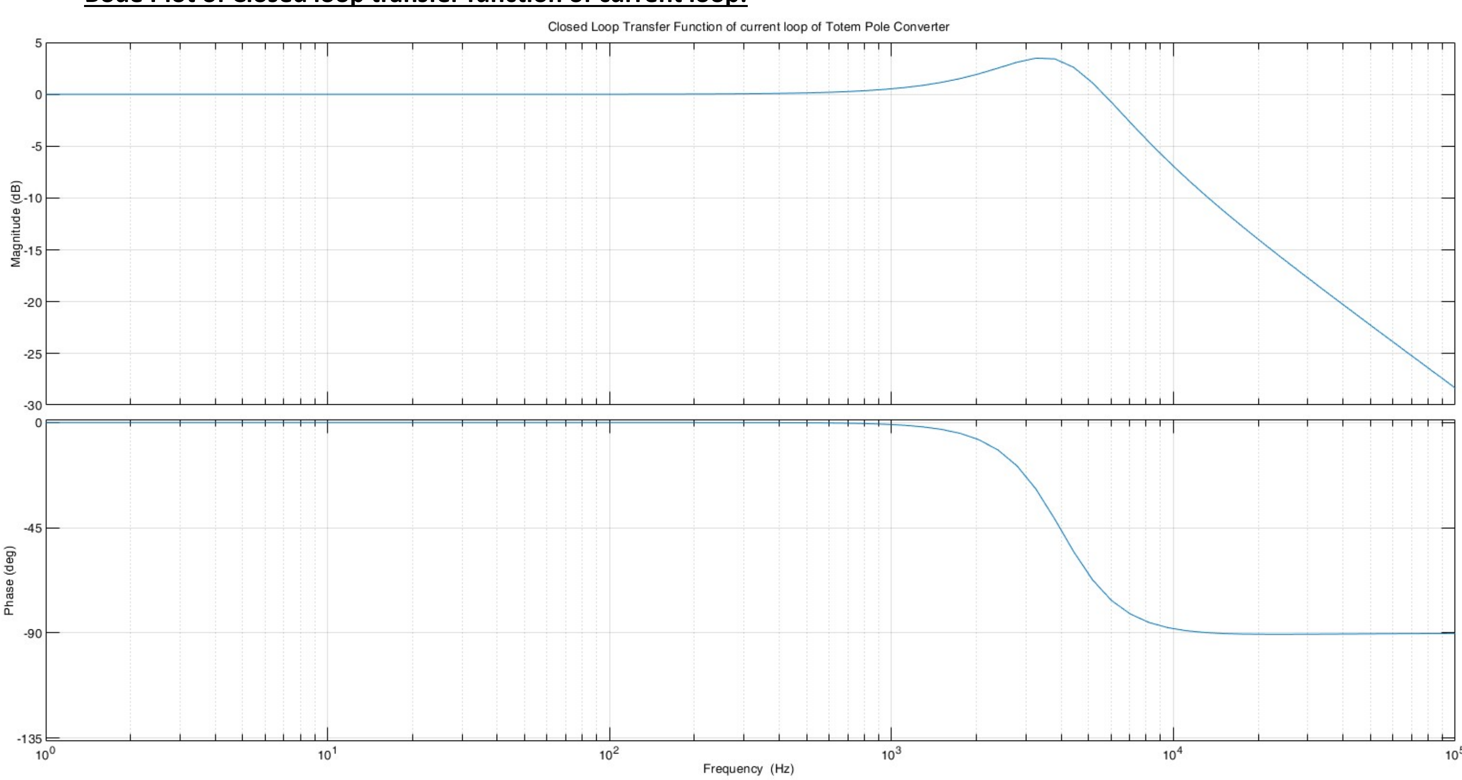
<u>Bode Plot of current controller:</u>



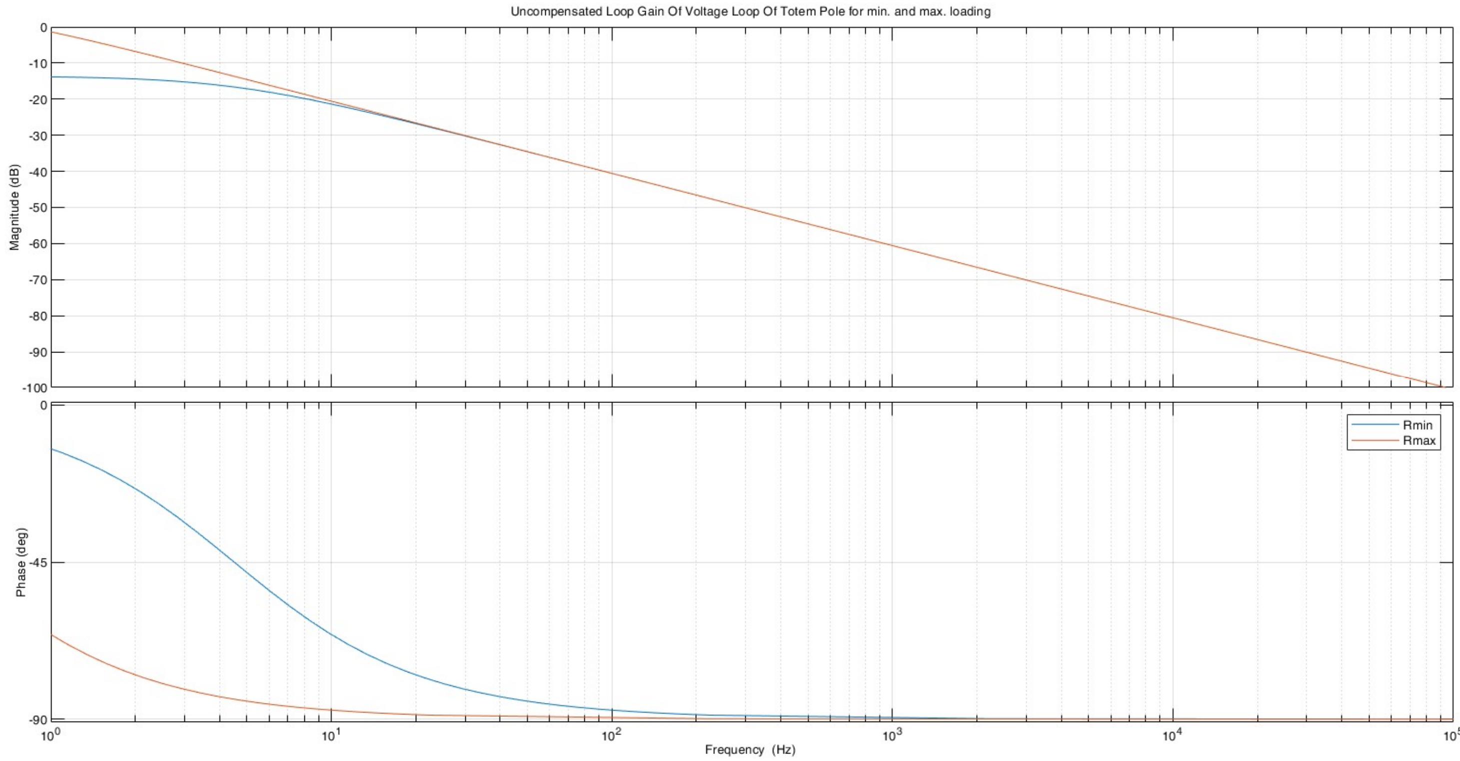
Bode plot of compensated current loop:



Bode Plot of Closed loop transfer function of current loop:

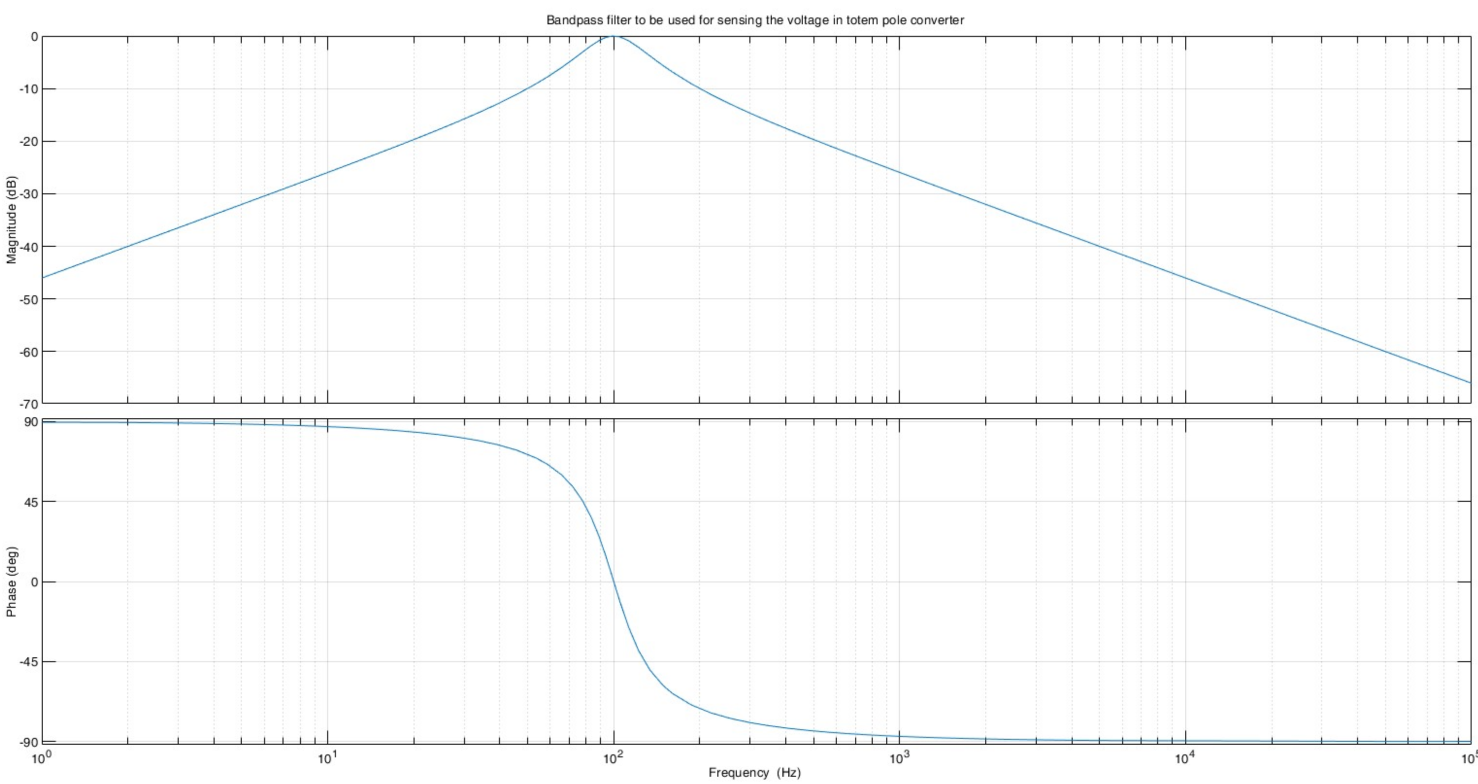


Bode Plots for uncompensated Voltage loop:

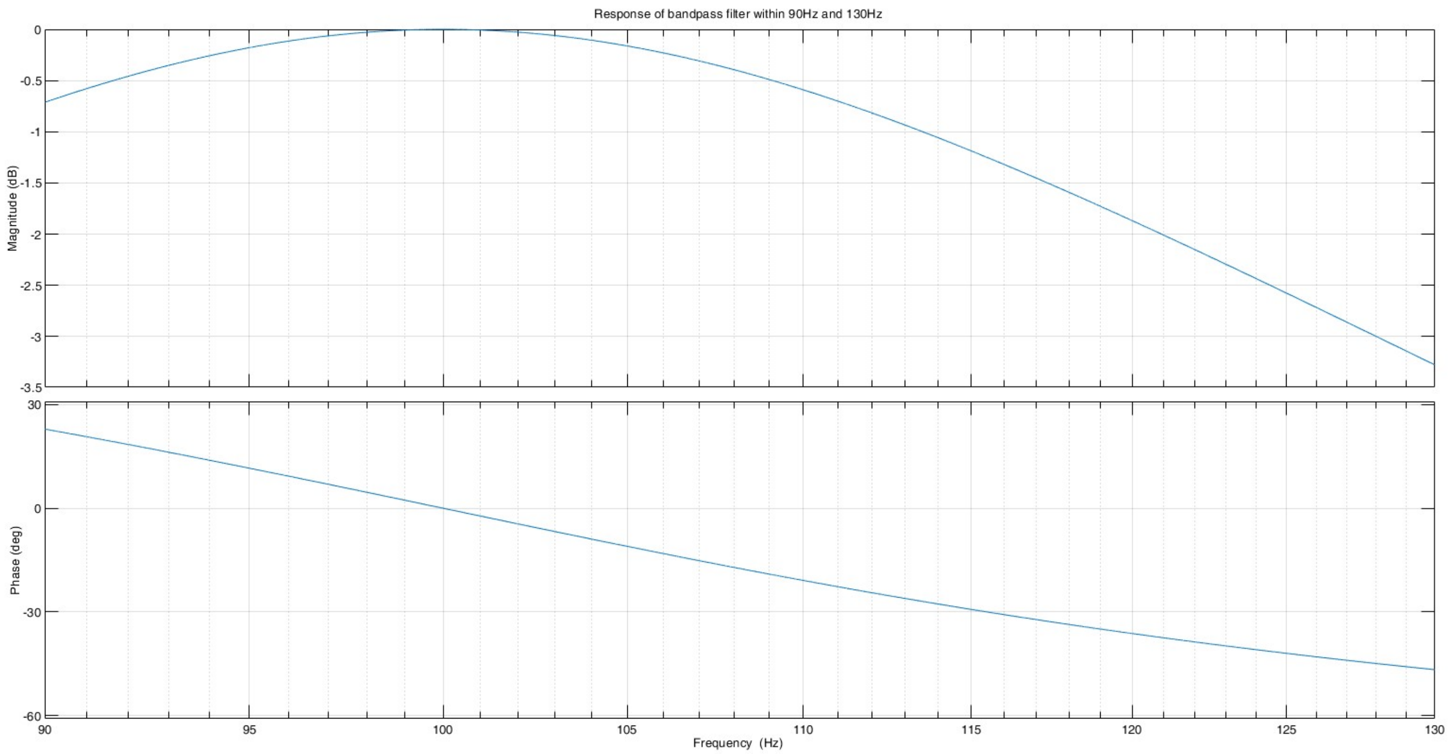


NOTE: Rmin and Rmax denotes the minimum and maximum effective load resistance that the totem pole converter drives. Since power varies between 360W to 3600W, I have considered the load variation in plant transfer function.

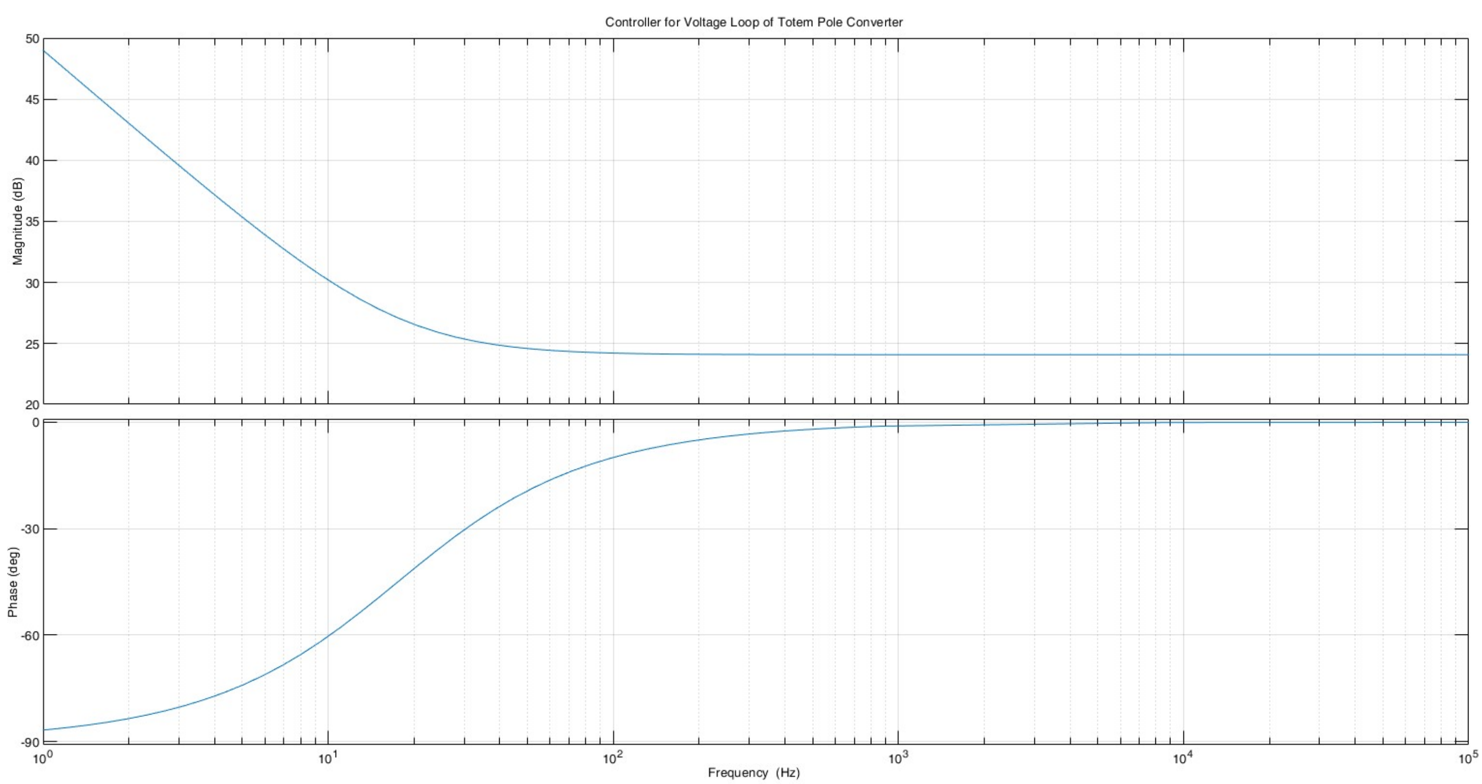
Bode Plot for bandpass filter for rejecting the 90-130Hz component:



Response of bandpass filter withing 90-130Hz band:

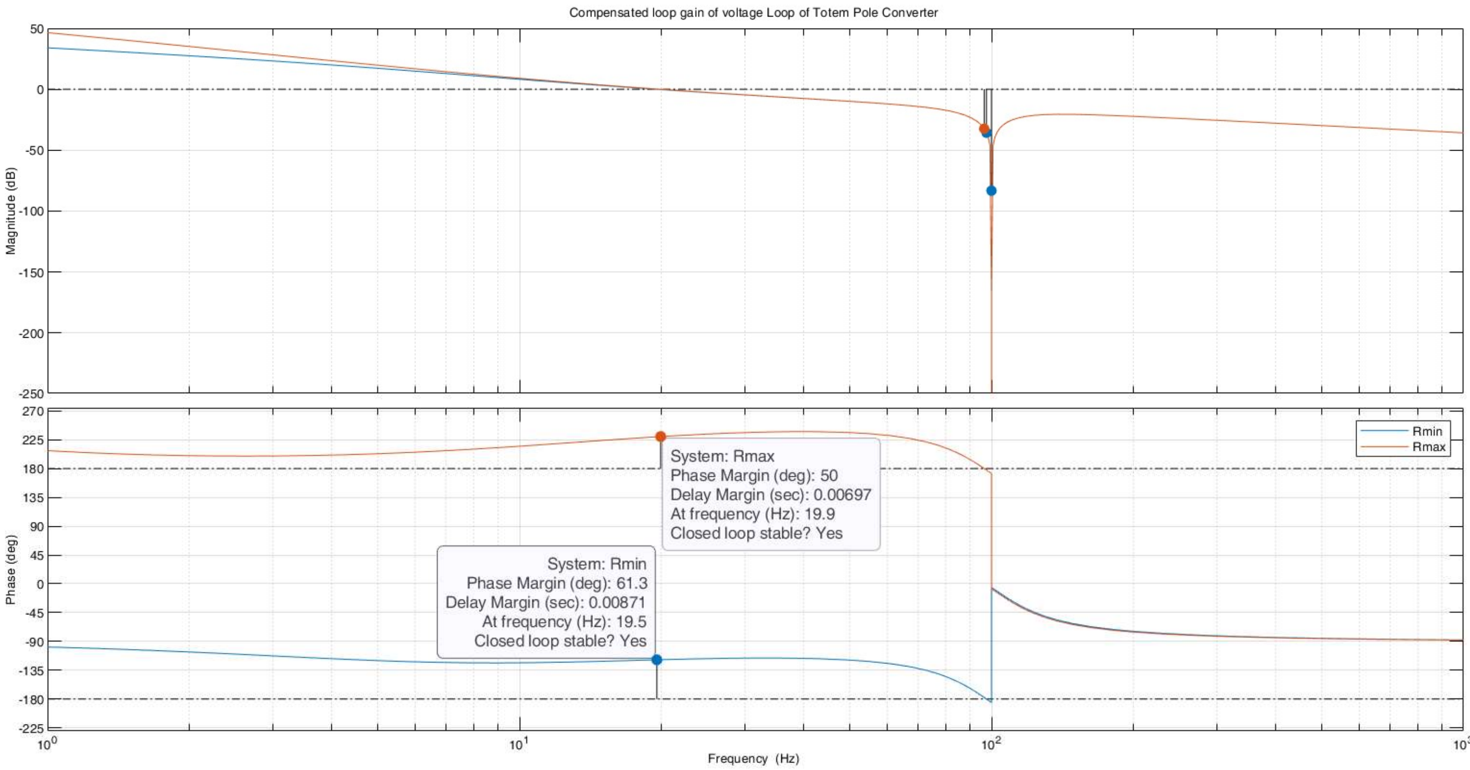


Bode Plot of Controller Transfer function for the voltage loop:

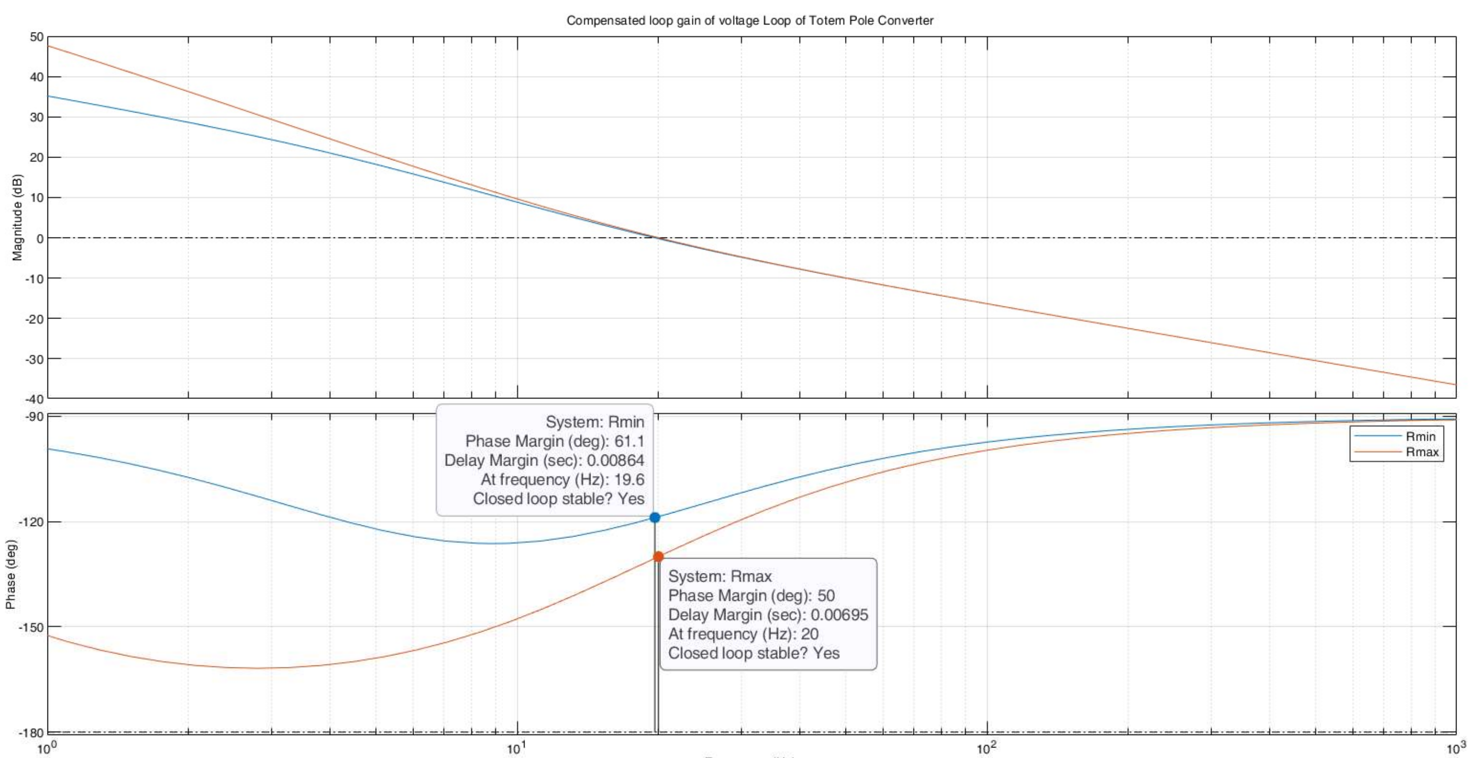


Bode plot of compensated loop gain for voltage loop of totem pole converter:

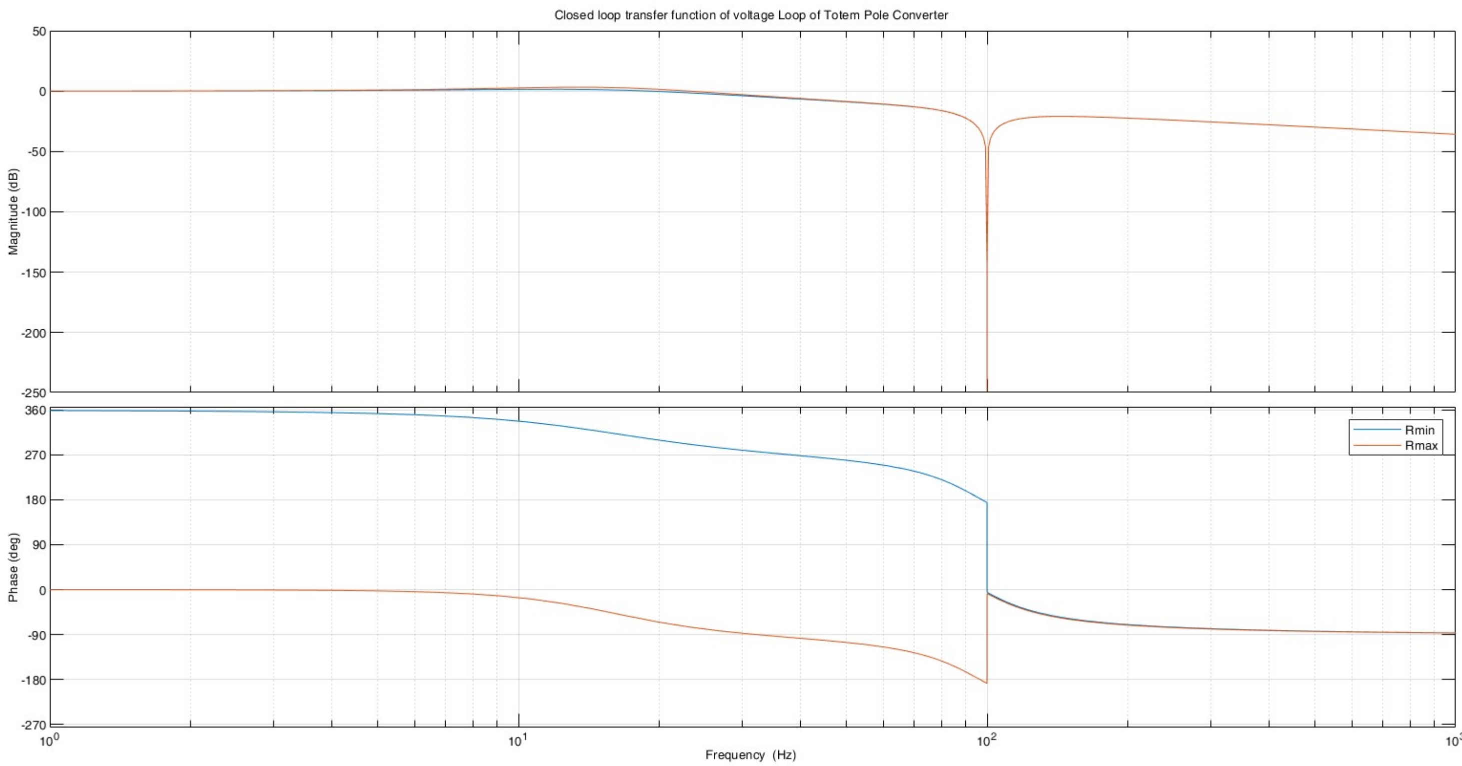
(a) With notch filter:



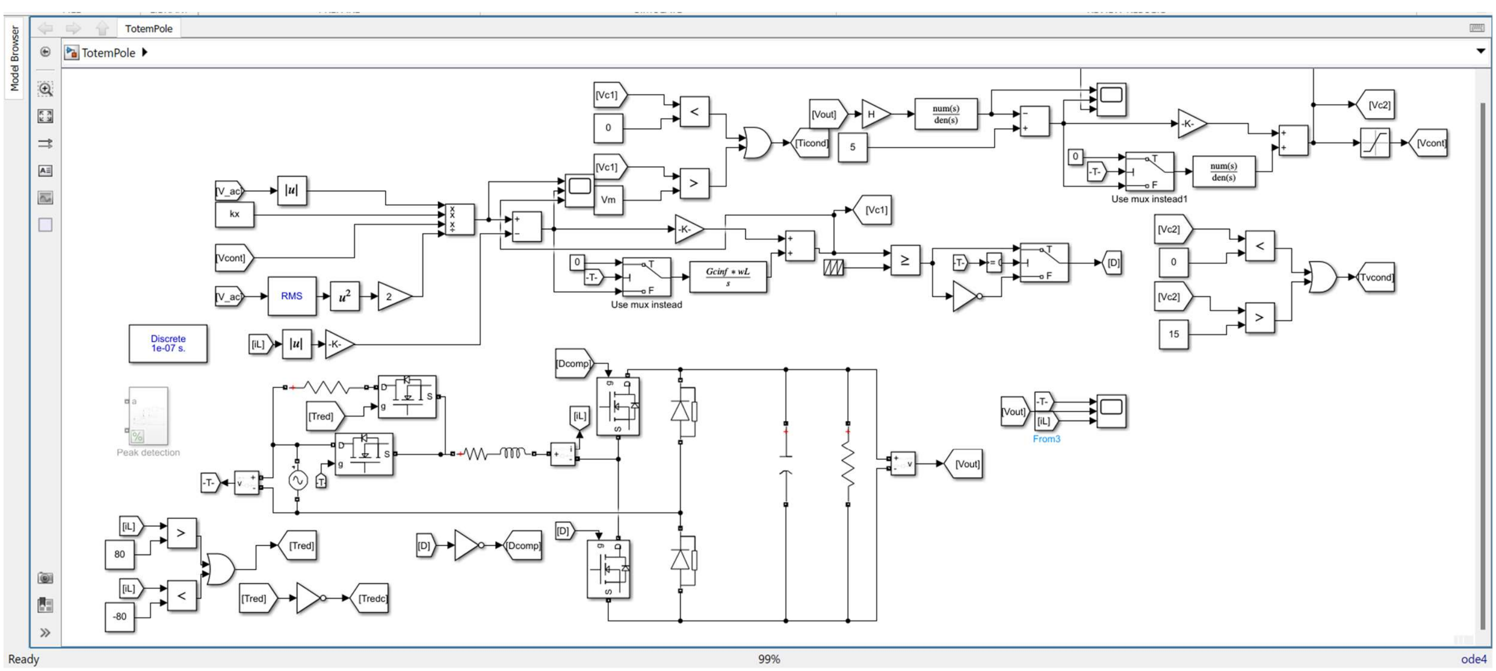
(b) Without notch filter:



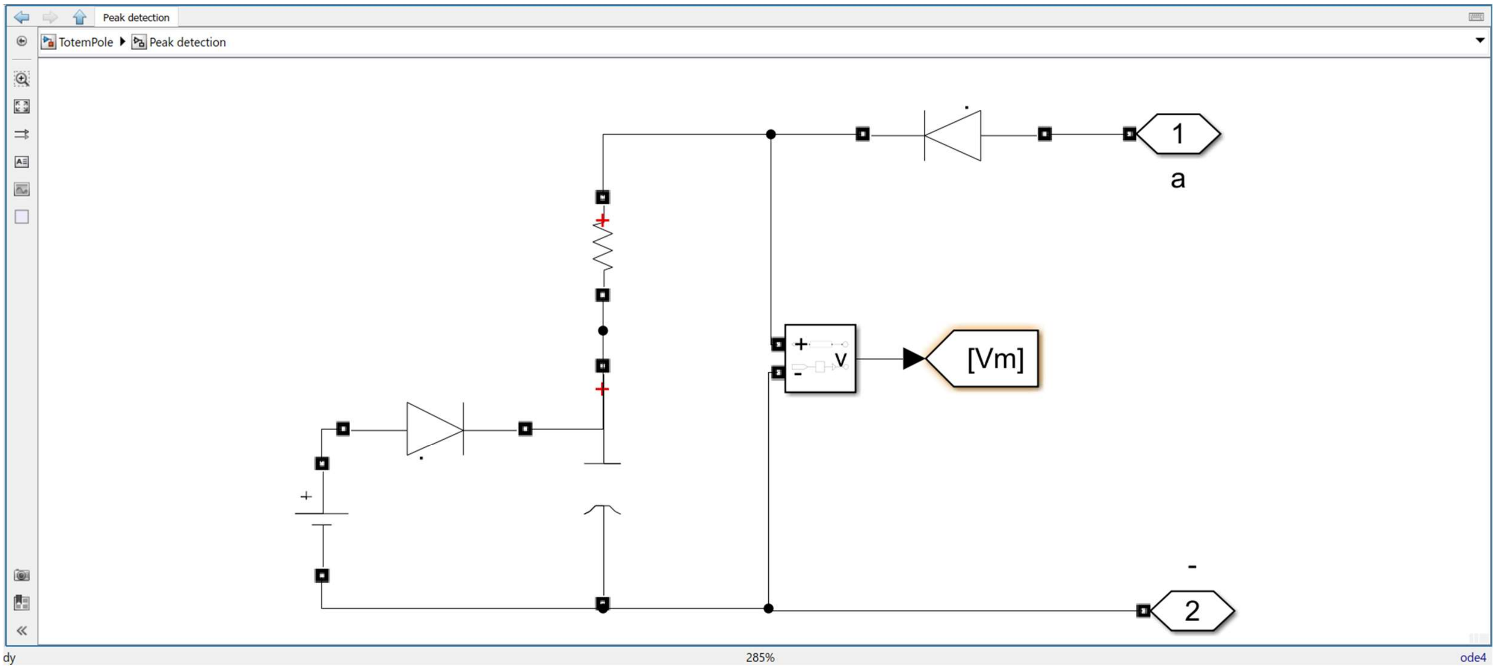
Bode Plot of Closed loop transfer function of voltage loop:



2. Circuit schematic of totem pole converter:



Circuit schematic of peak detection circuit:

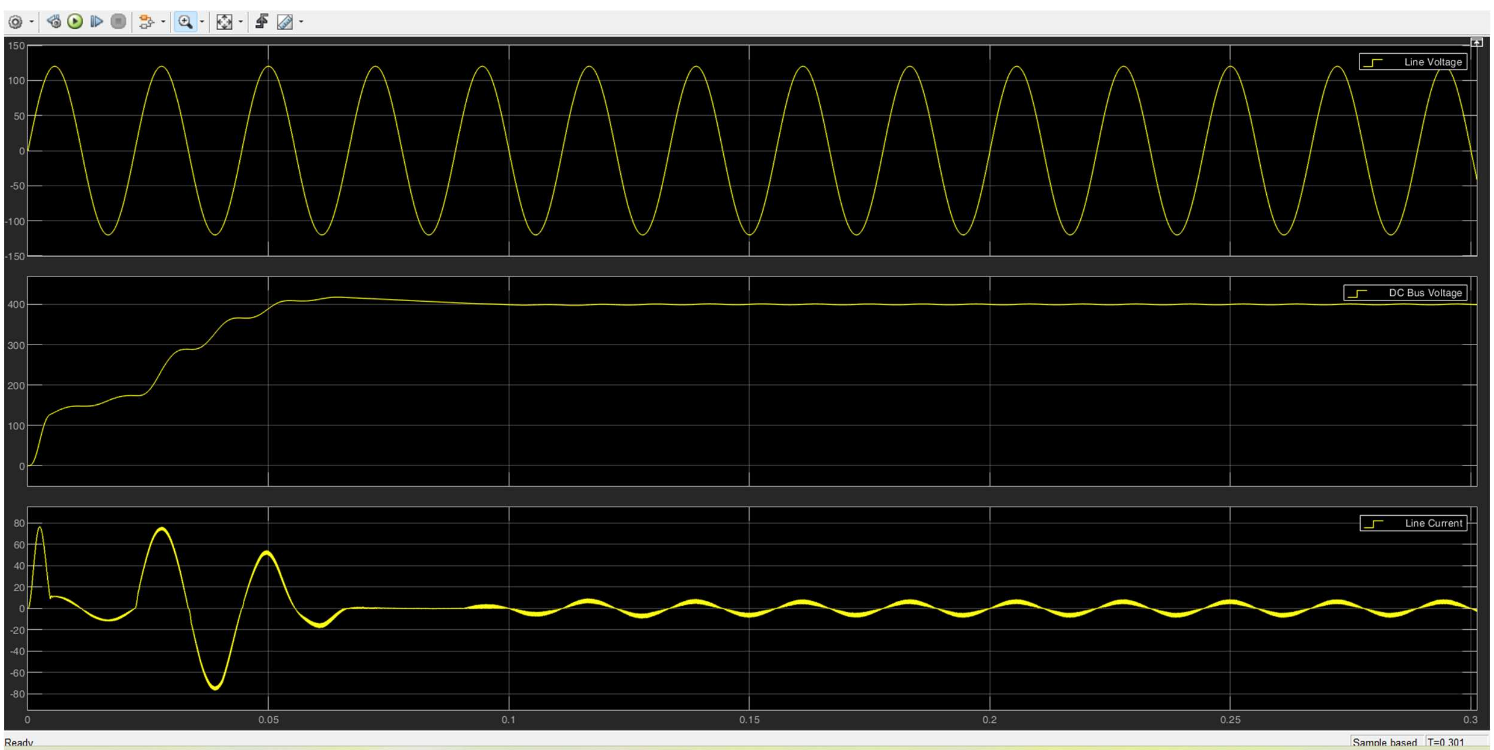


NOTE: The peak detection circuit was not used in the final simulation and RMS block was used to get the peak and this value was square later on.

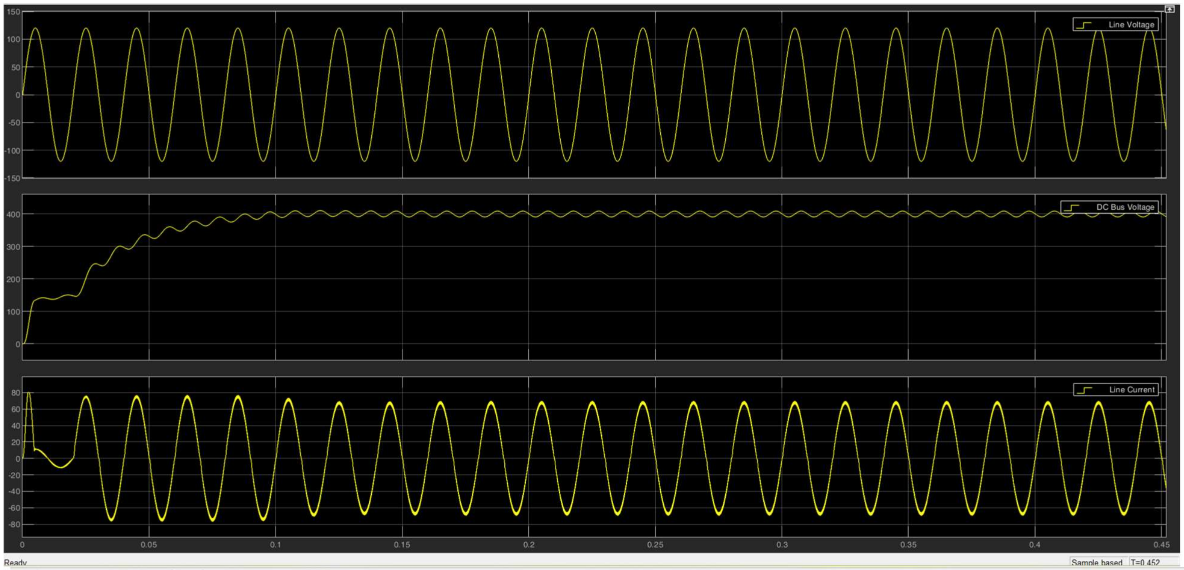
Waveforms for the totem pole converter:

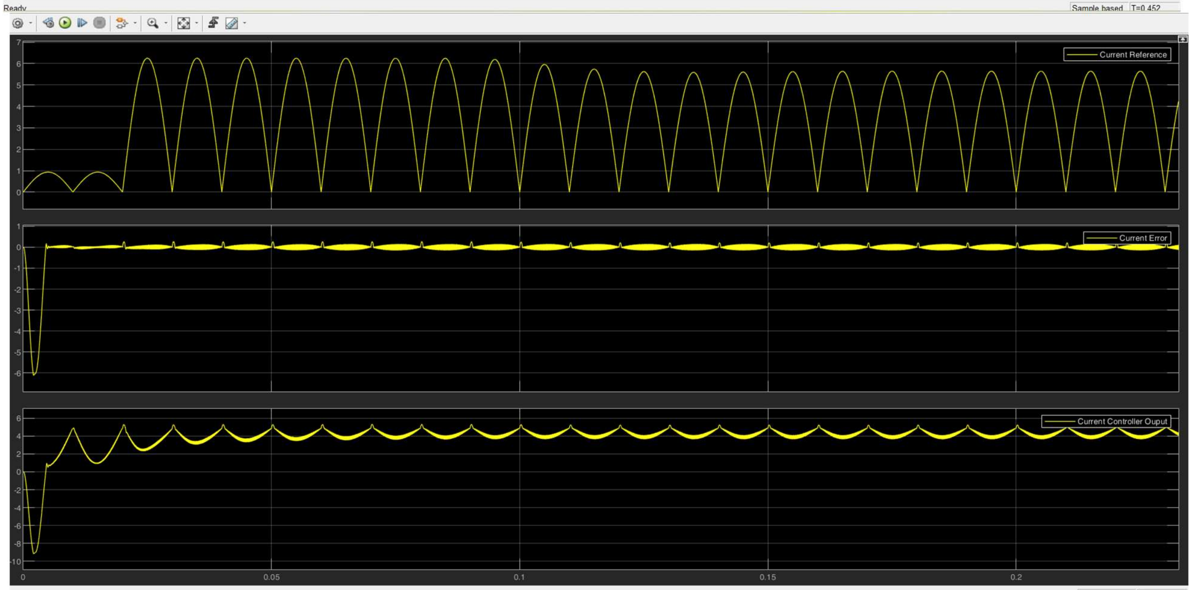
I have added controller output and input waveforms for few cases.

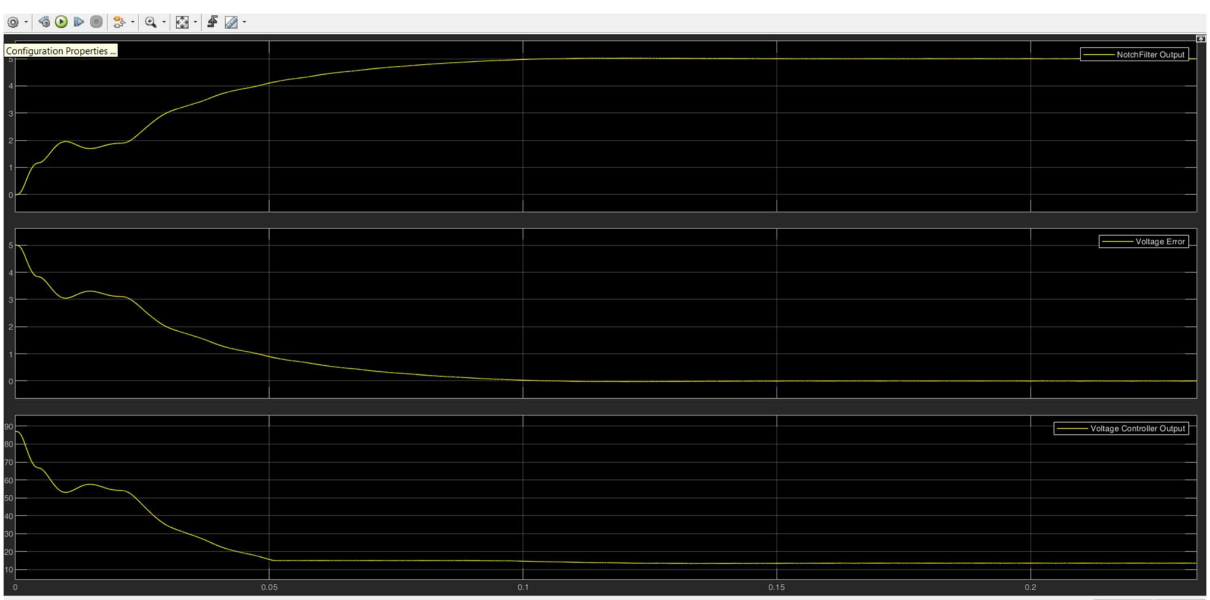
1. **At Vac = 85V (rms), 45Hz, Pout = 360W**



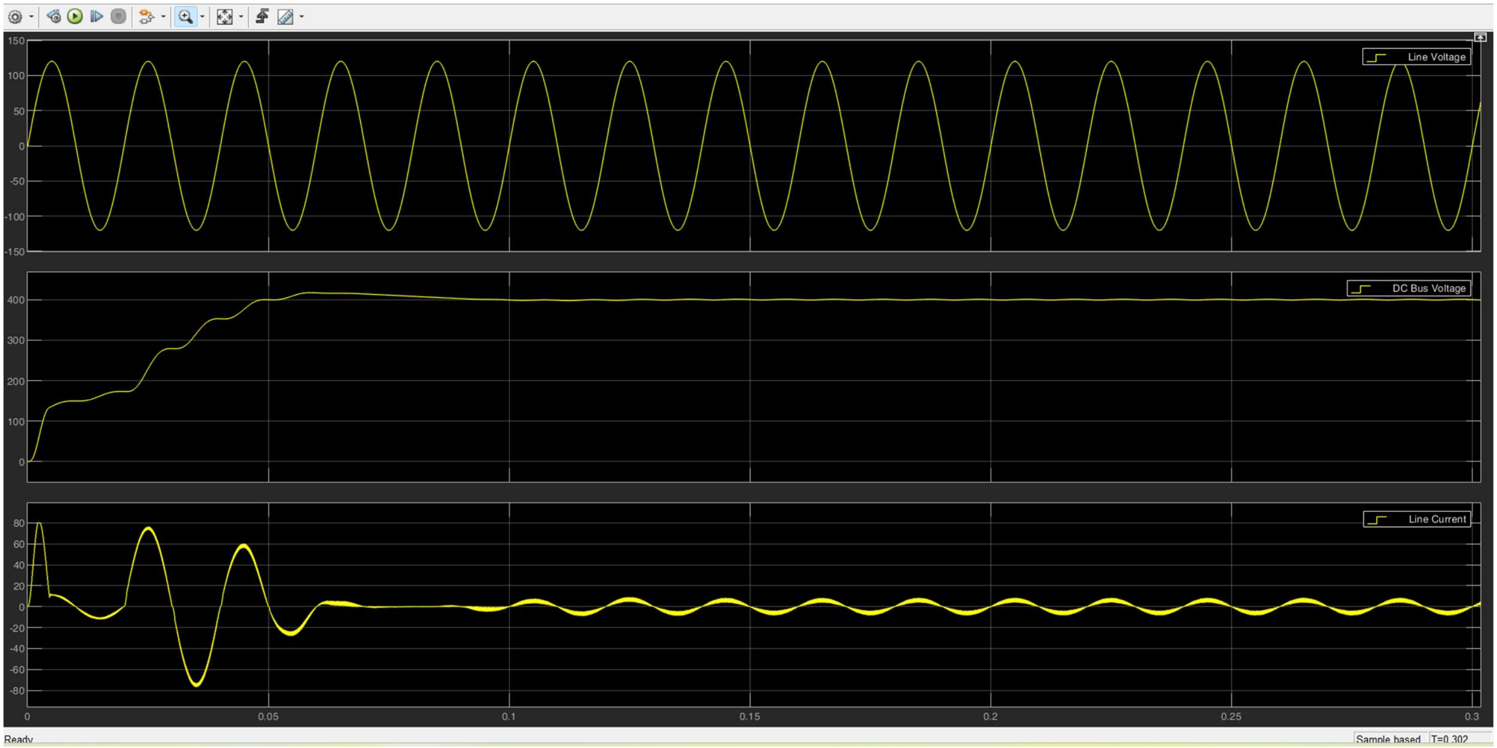
2. **At Vac = 85V (rms), 50Hz, Pout = 3600W (The graph of controllers waveform has been added later)**



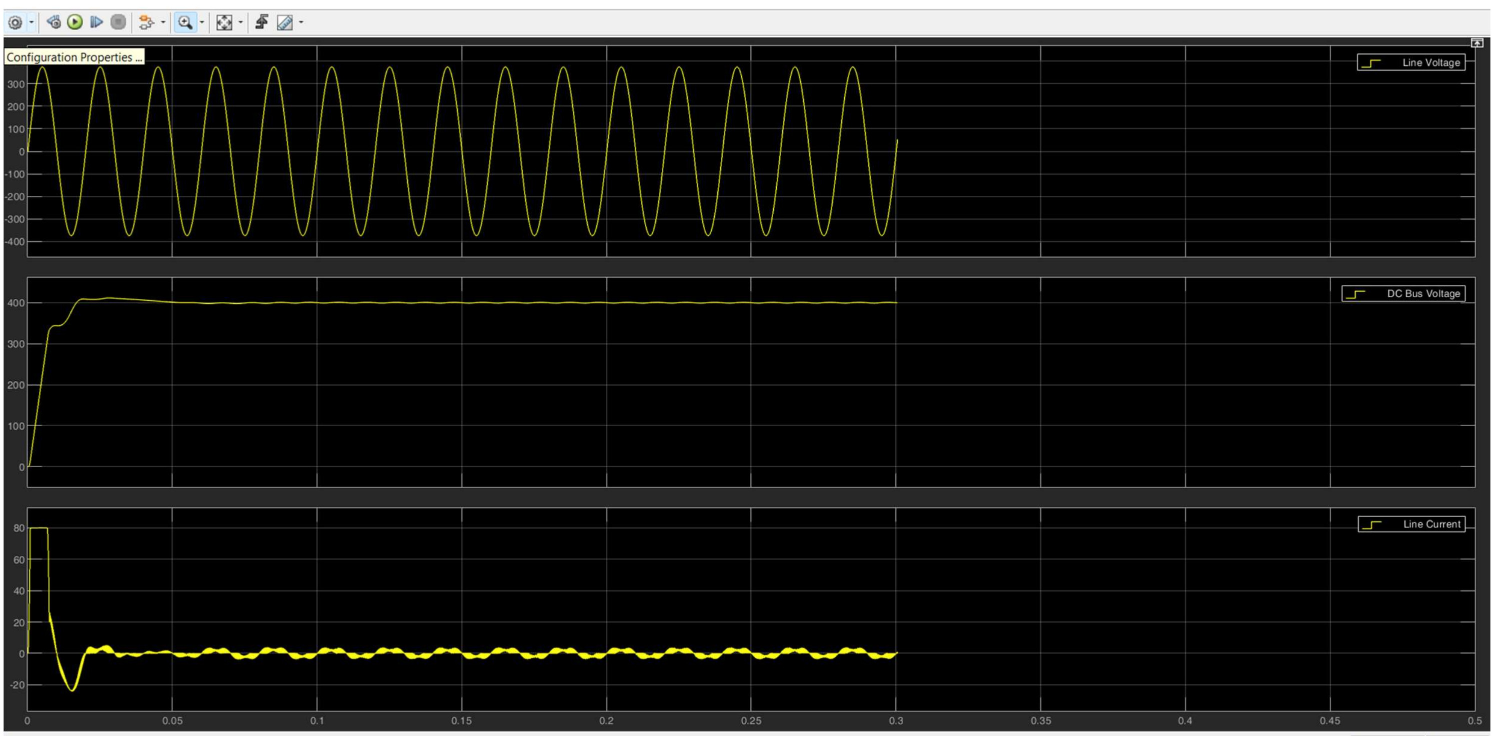




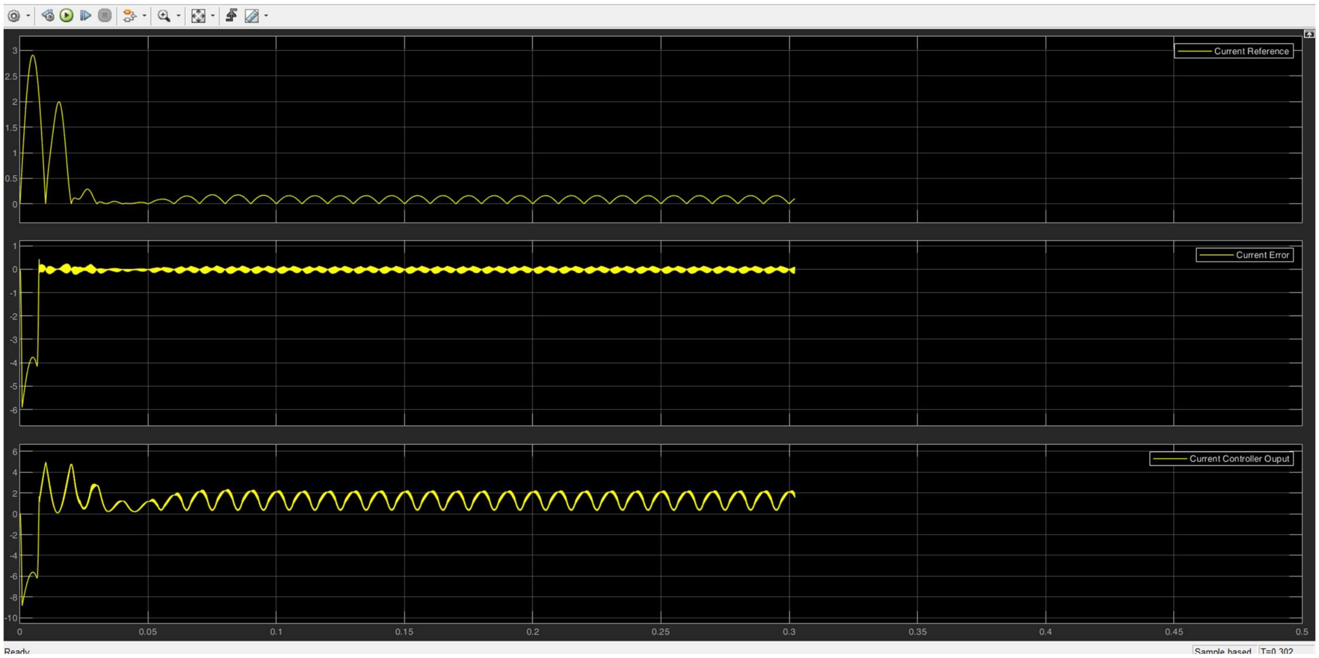
3. **At Vac = 85V (rms), 50Hz, Pout = 360W**

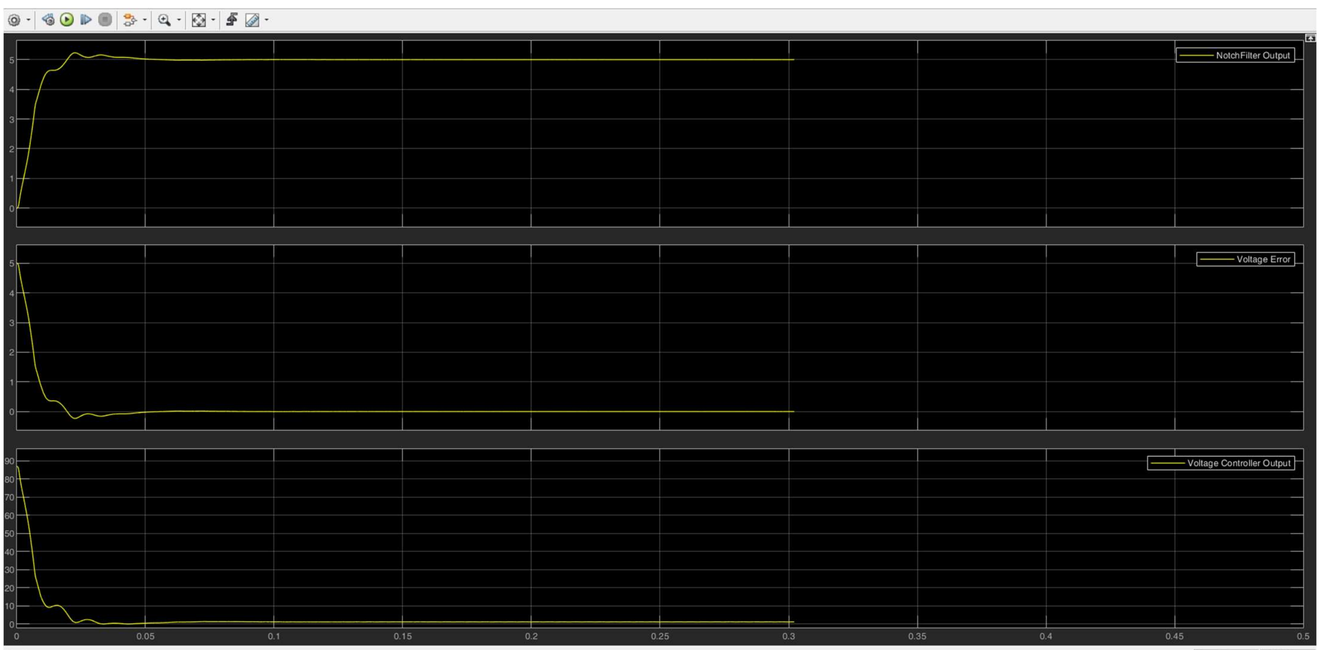


4. **At Vac = 265V (rms), 50Hz, Pout = 360W**

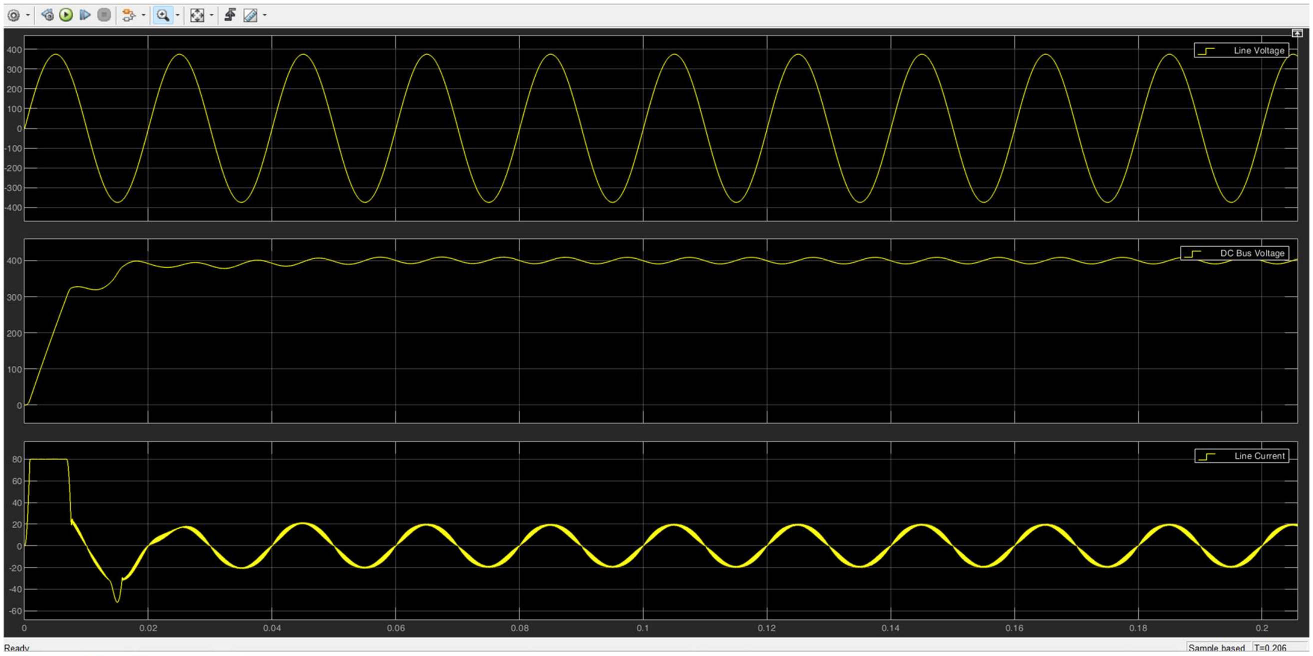


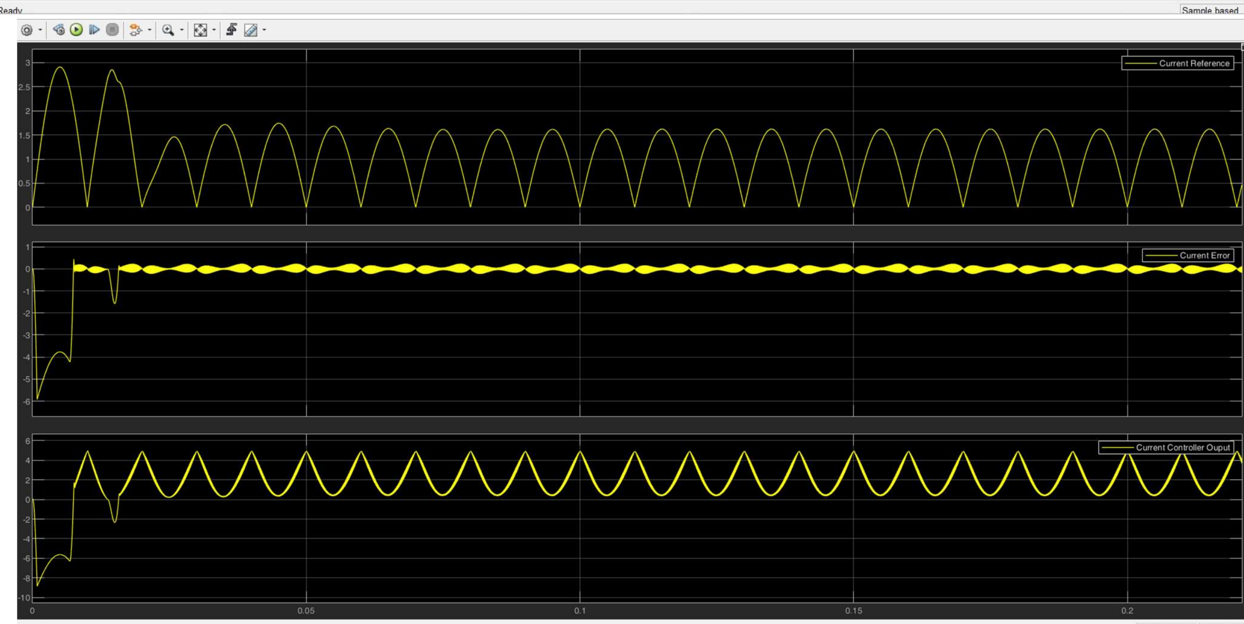
Controller output on next page.

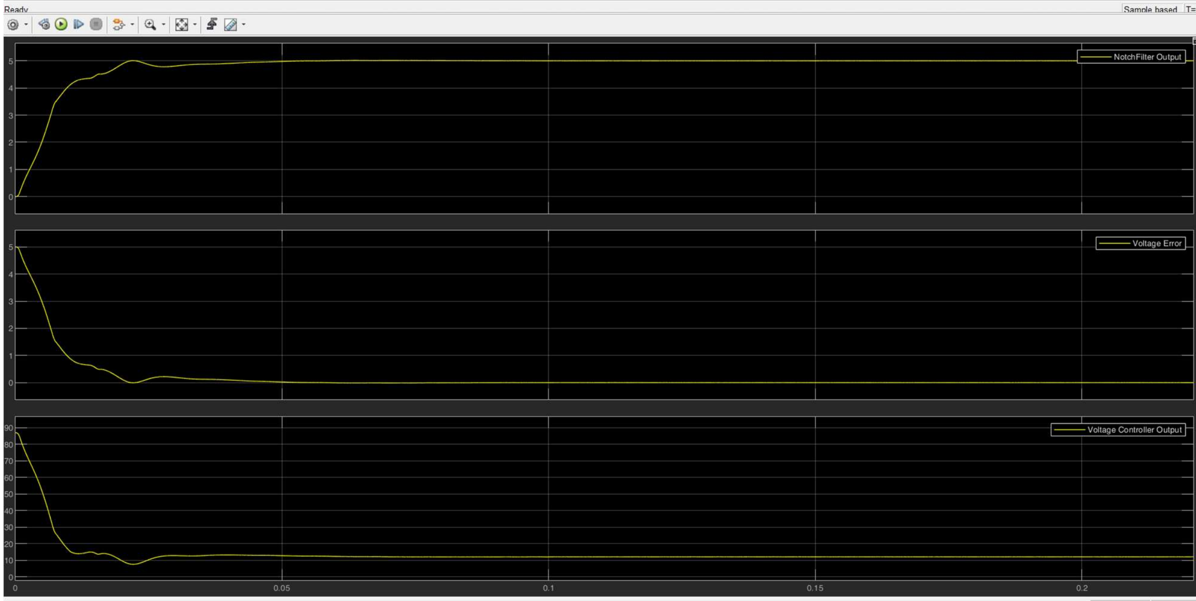

Current Reference
Current Error
Current Controller Ouput
Ready
Sample based
T=0.302


NotchFilter Output
Voltage Error
Voltage Controller Output
Ready
Sample based
T=0.302

5. At Vac = 265V (rms), 50Hz, Pout = 3600W (with controller output)

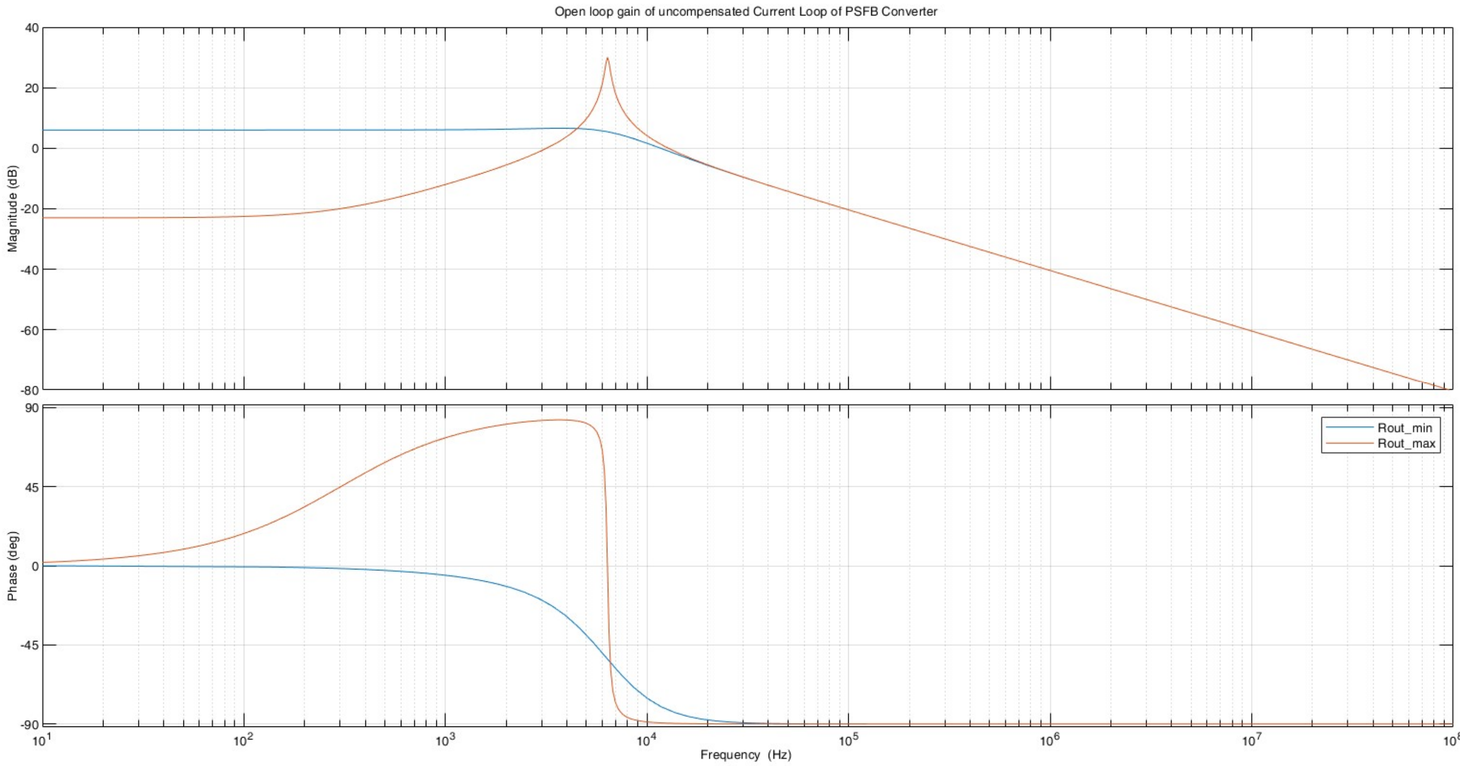






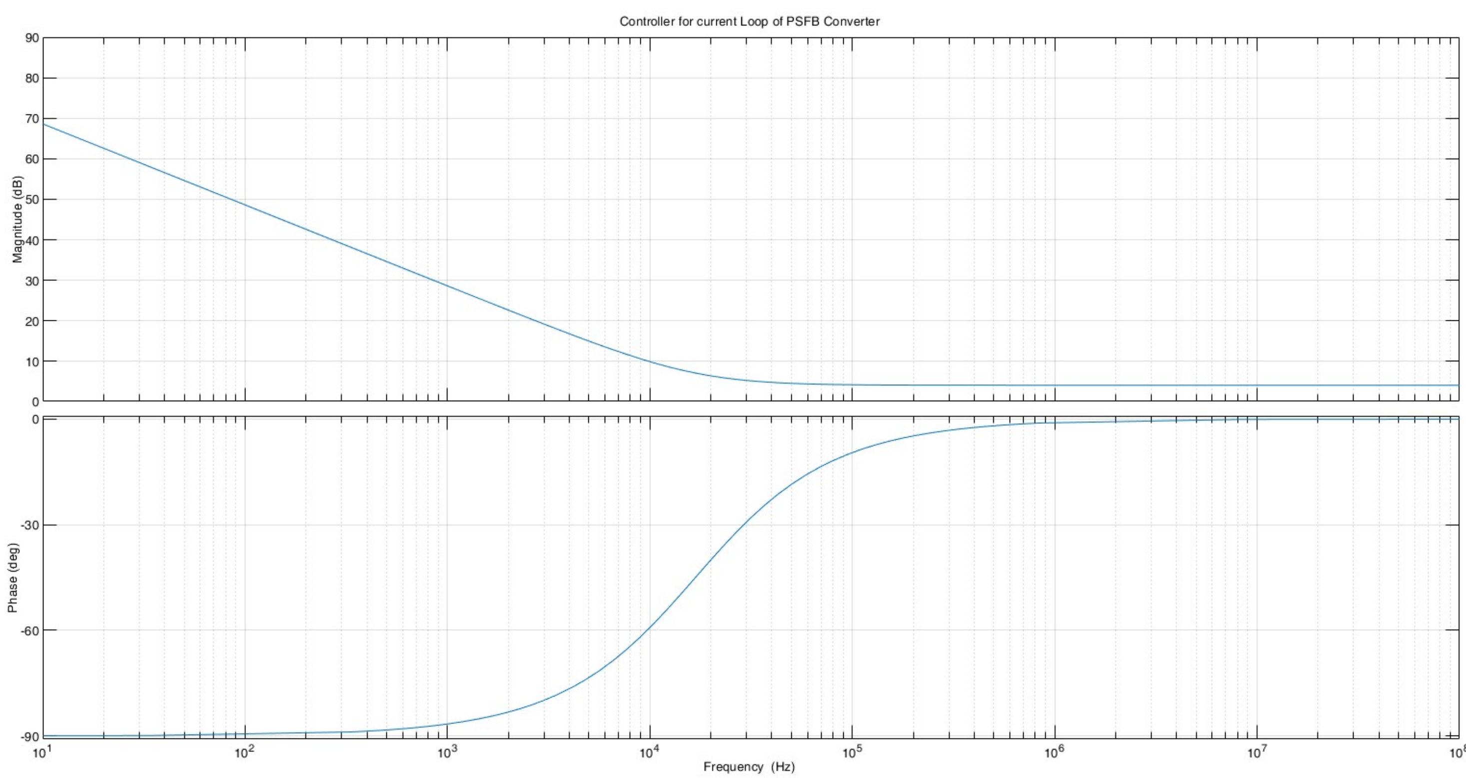
2. Diode bridge PSFB converter:

Bode plot for uncompensated current loop of PSFB:

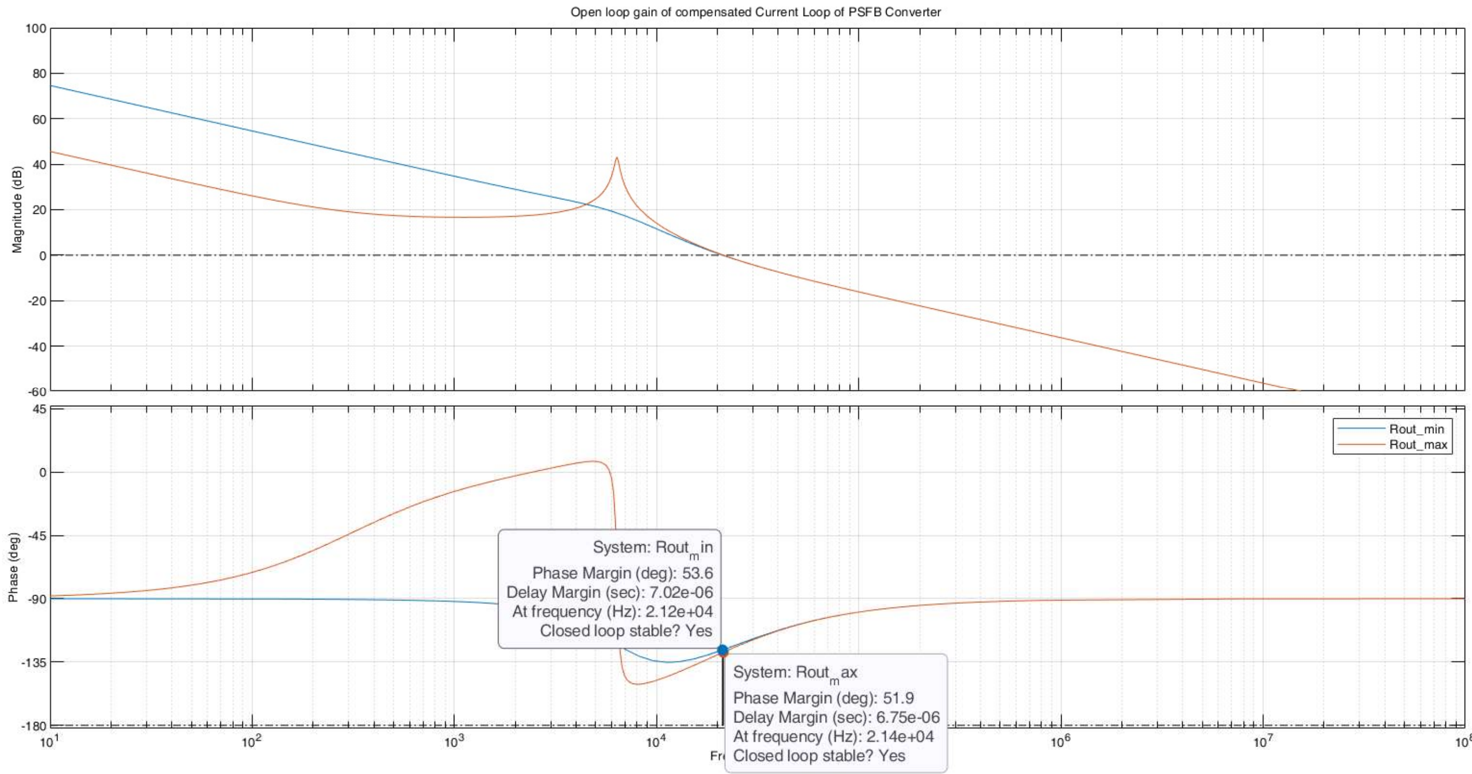


NOTE: Rout_min and Rout_max denotes the minimum and maximum effective load resistance that the PSFB converter drives. Since power varies between 360W to 3600W and output voltage varies between 200V to 336V, I have considered the load variation in plant transfer function.

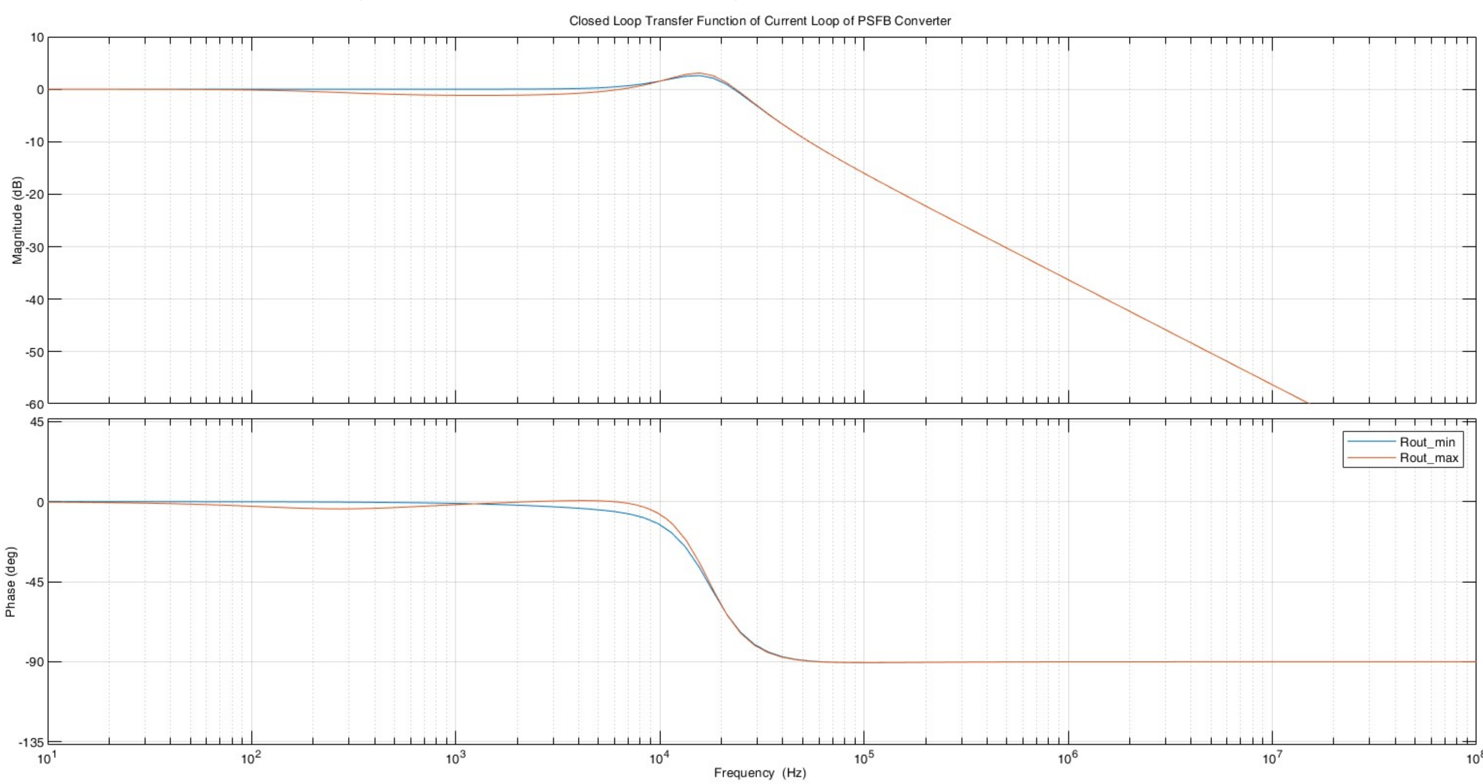
Bode Plot of current controller for PSFB:



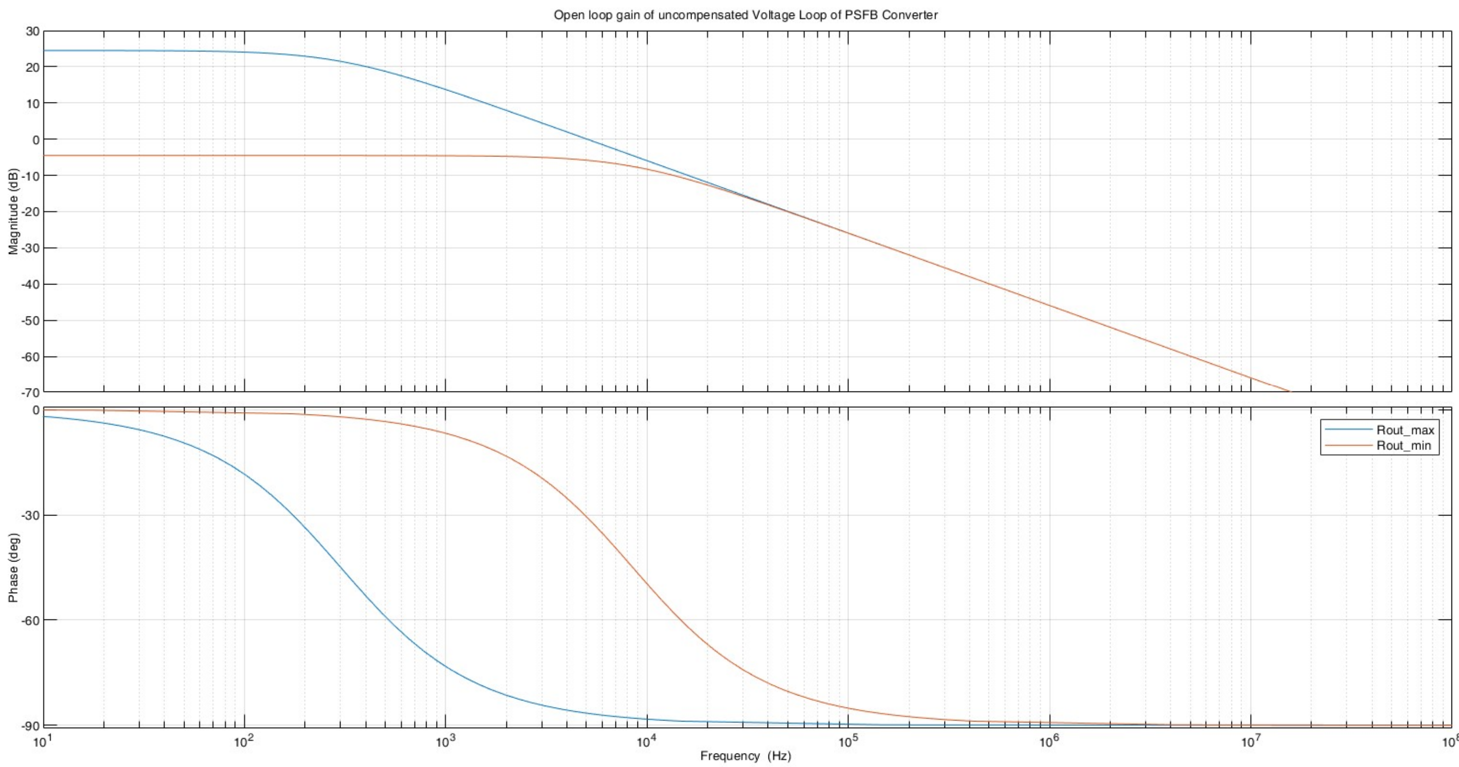
Bode plot of compensated current loop of PSFB:



Bode Plot of Closed loop transfer function of current loop of PSFB:

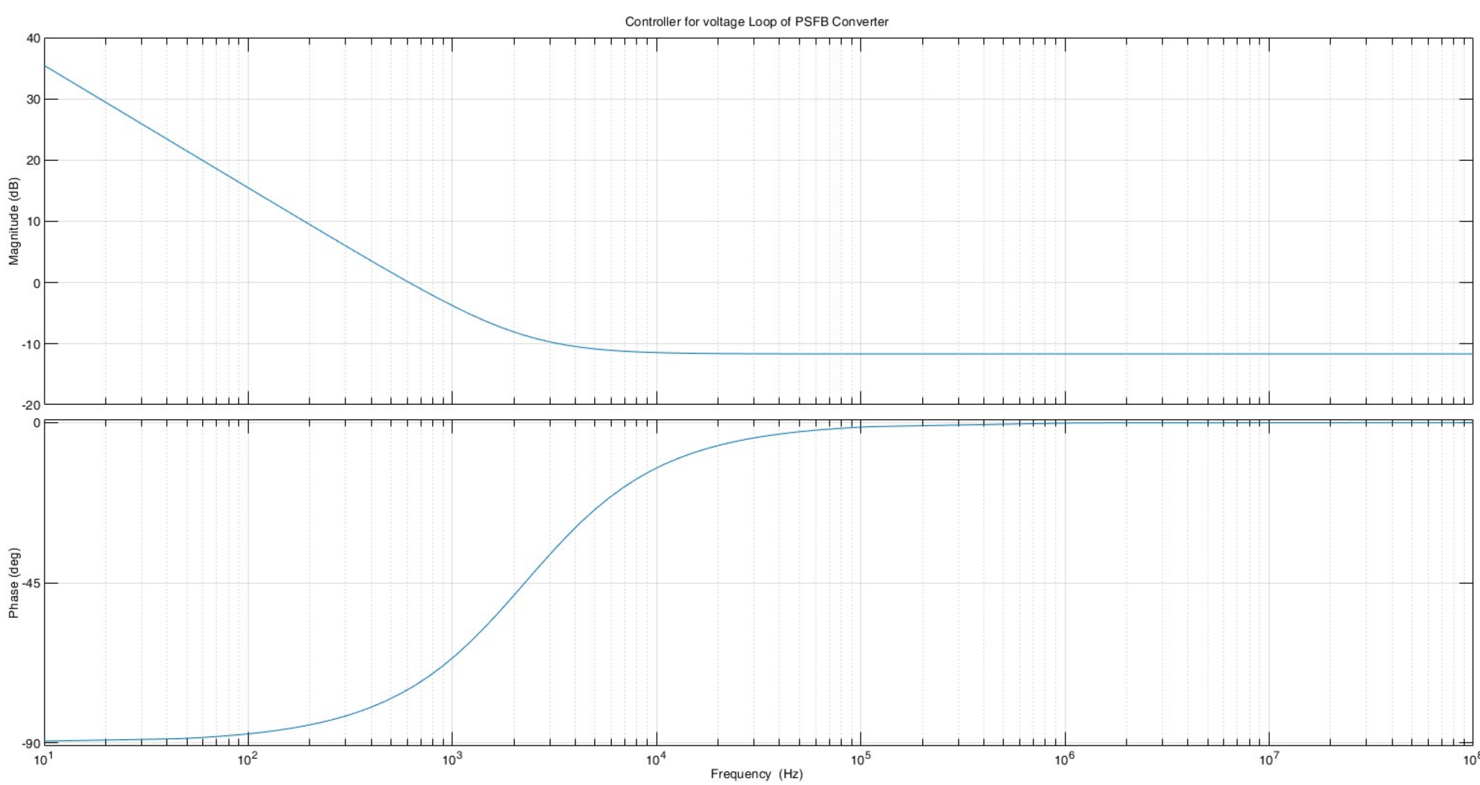


Bode Plots for uncompensated Voltage loop of PSFB:

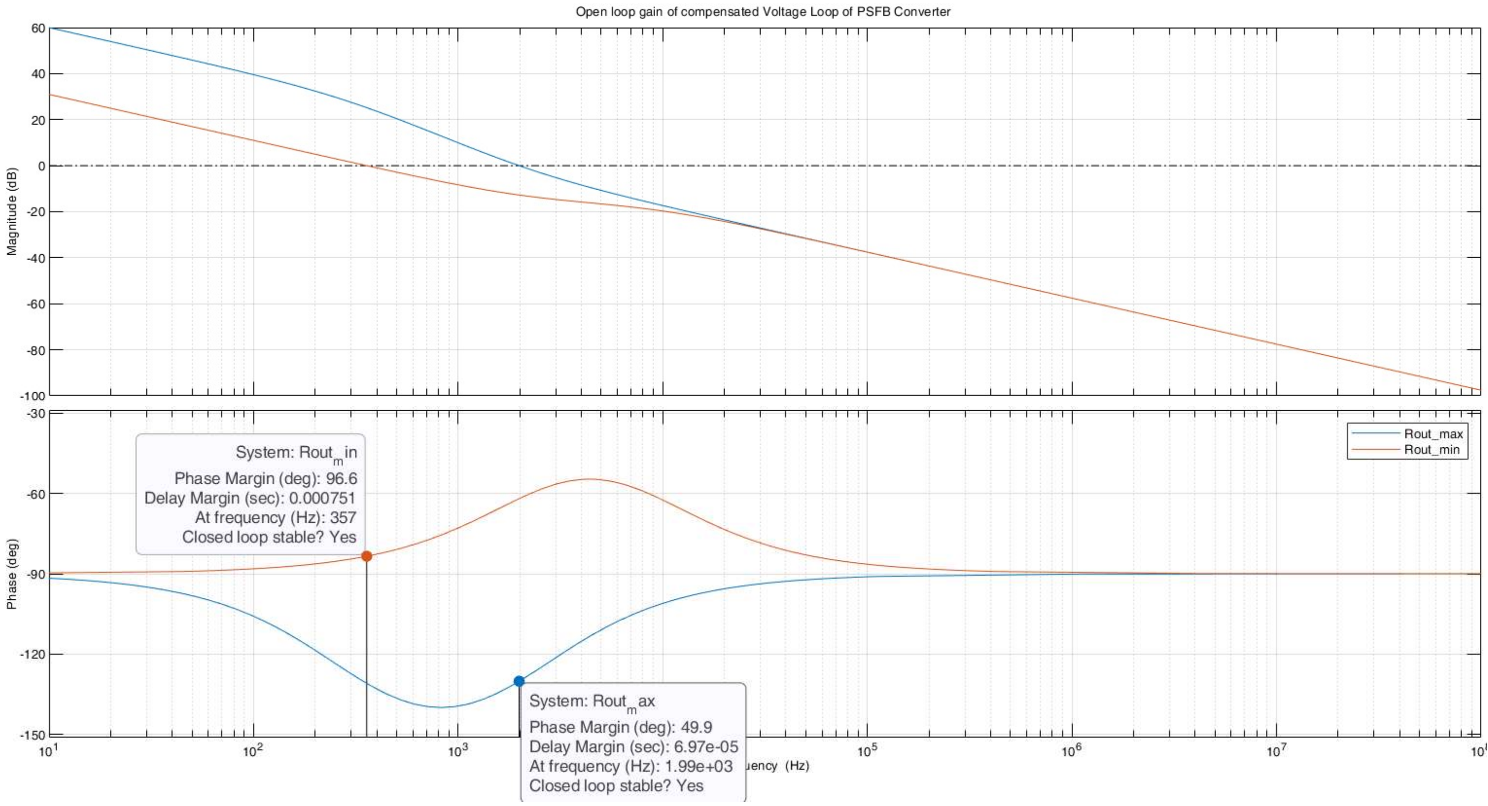


NOTE: Rout_min and Rout_max denotes the minimum and maximum effective load resistance that the PSFB converter drives. Since power varies between 360W to 3600W and output voltage varies between 200V to 336V, I have considered the load variation in plant transfer function.

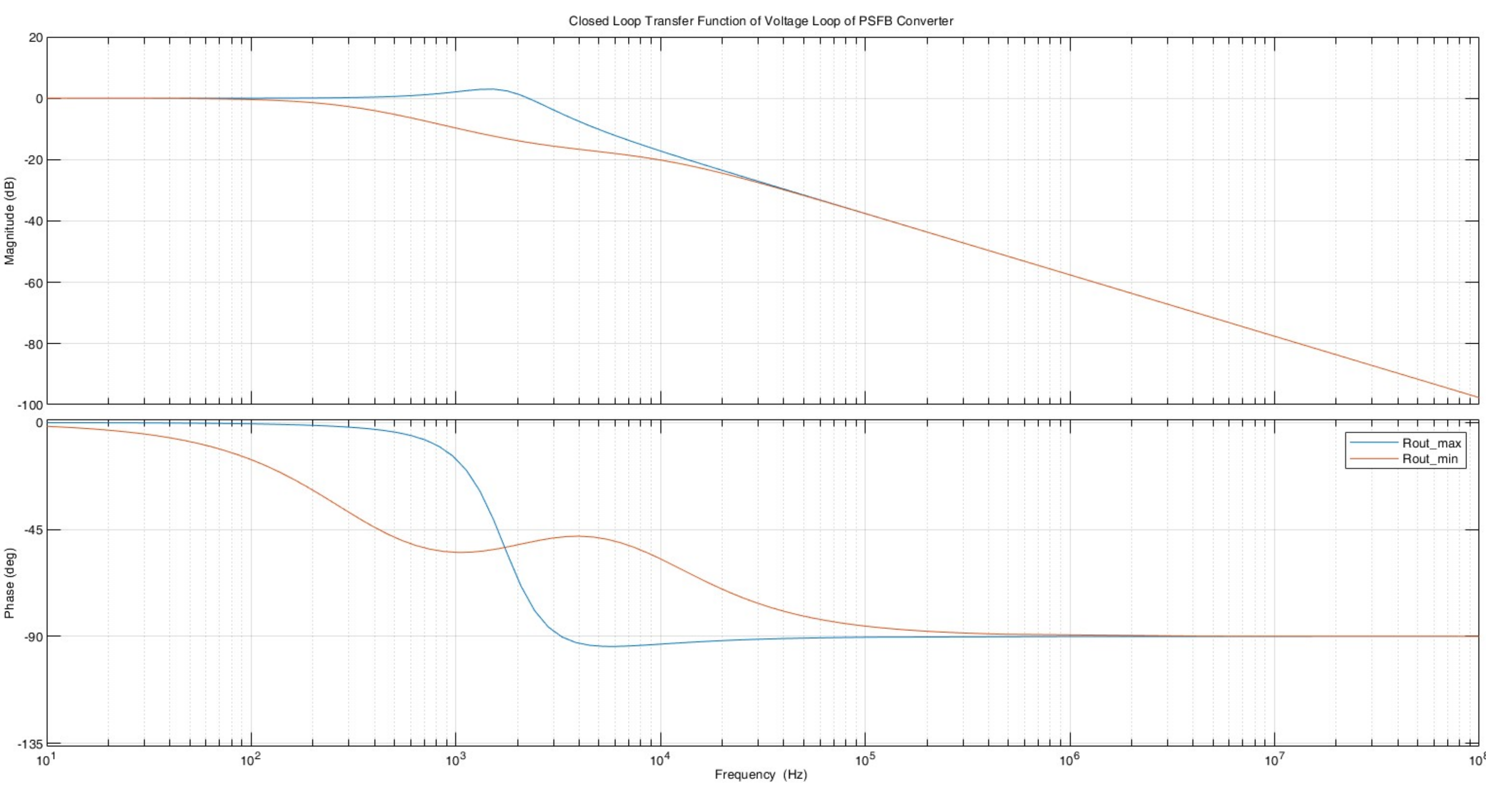
Bode Plot of Controller Transfer function for the voltage loop of PSFB:



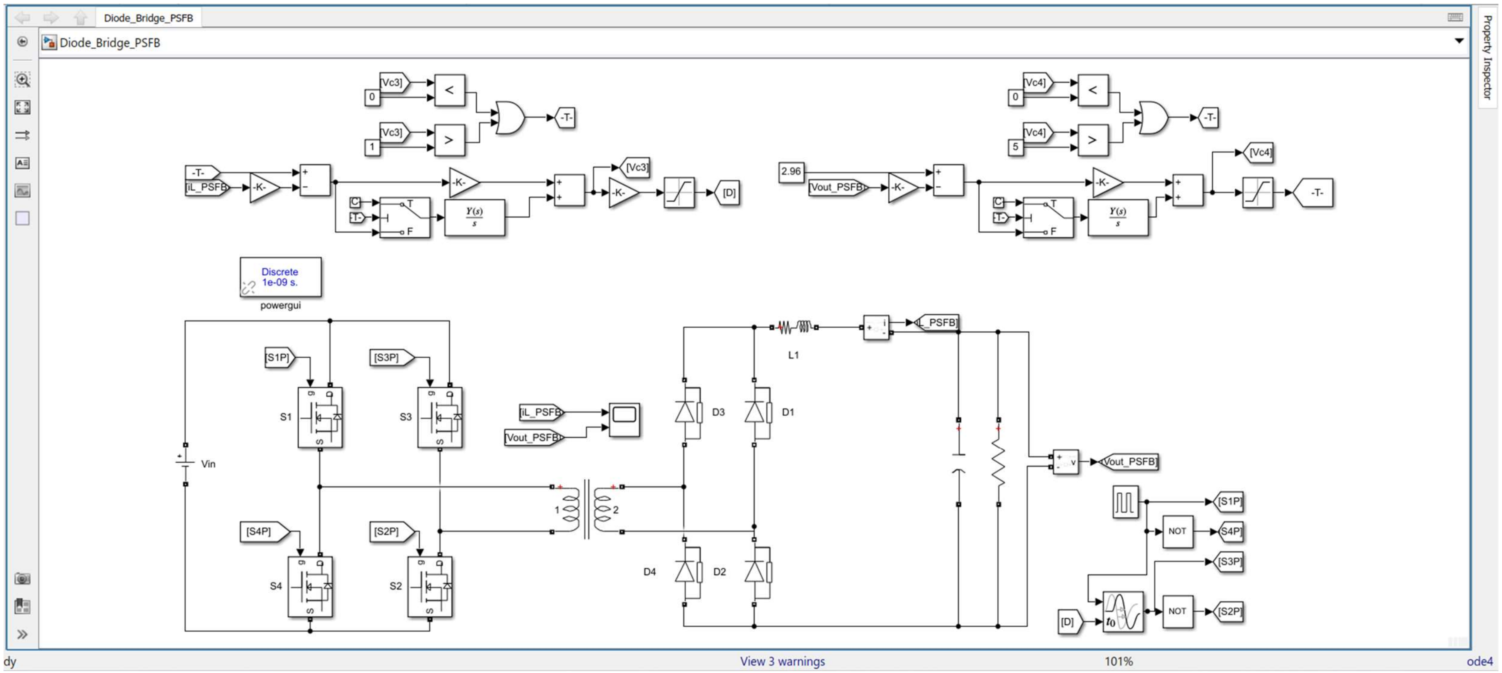
Bode plot of compensated loop gain for voltage loop of PSFB:



Bode Plot of Closed loop transfer function of voltage loop of PSFB:

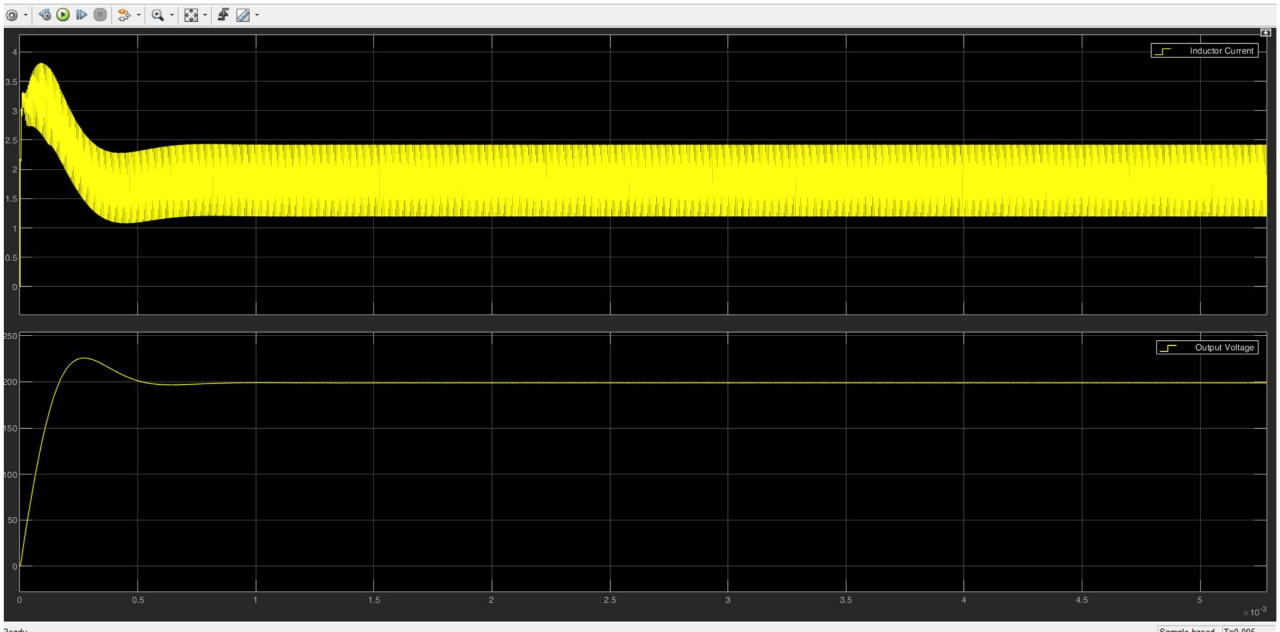


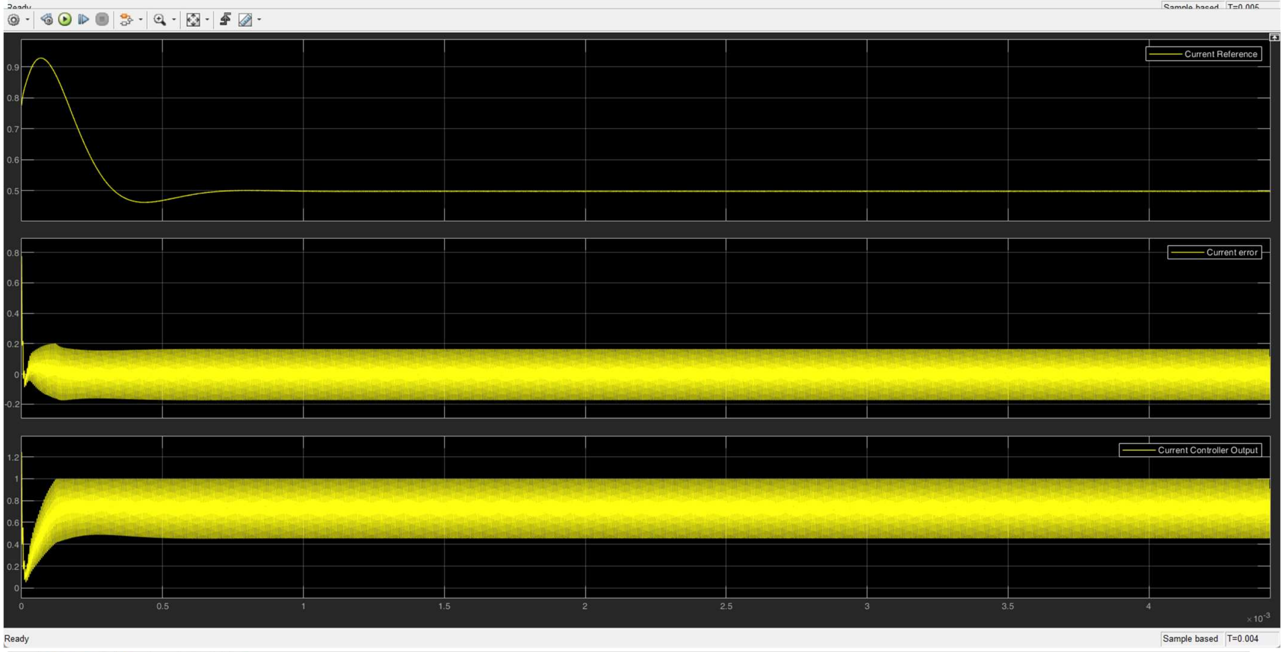
Schematic of the circuit for PSFB:

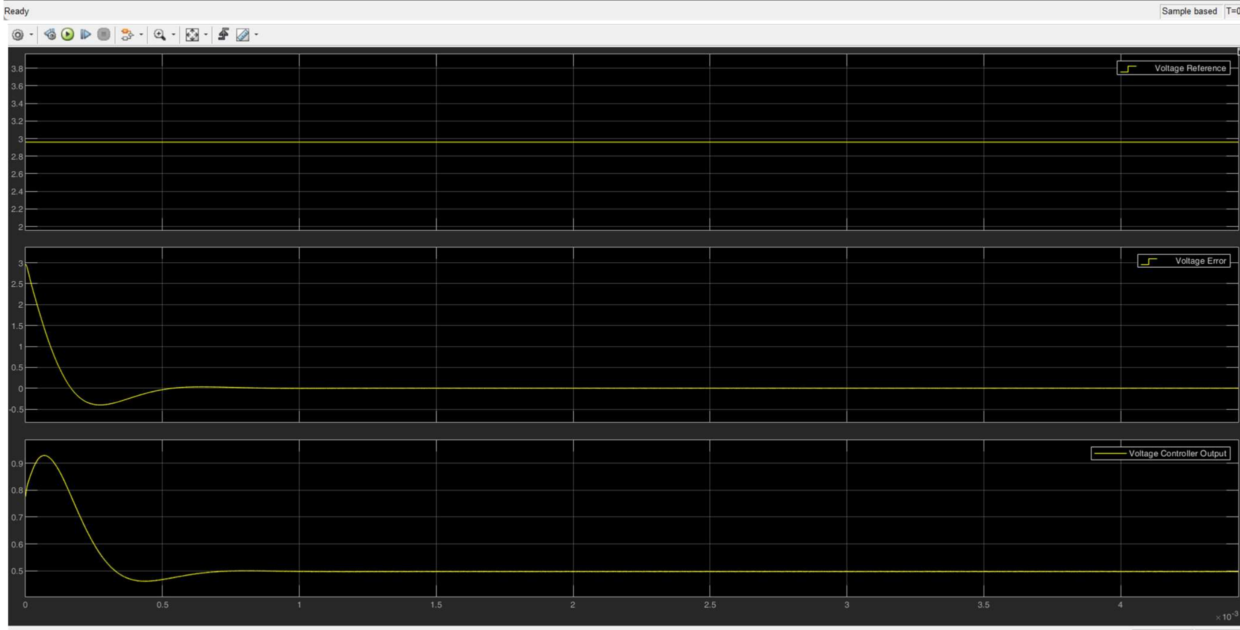


Waveforms of the PSFB converter:
The waveforms have been attached on next few pages.

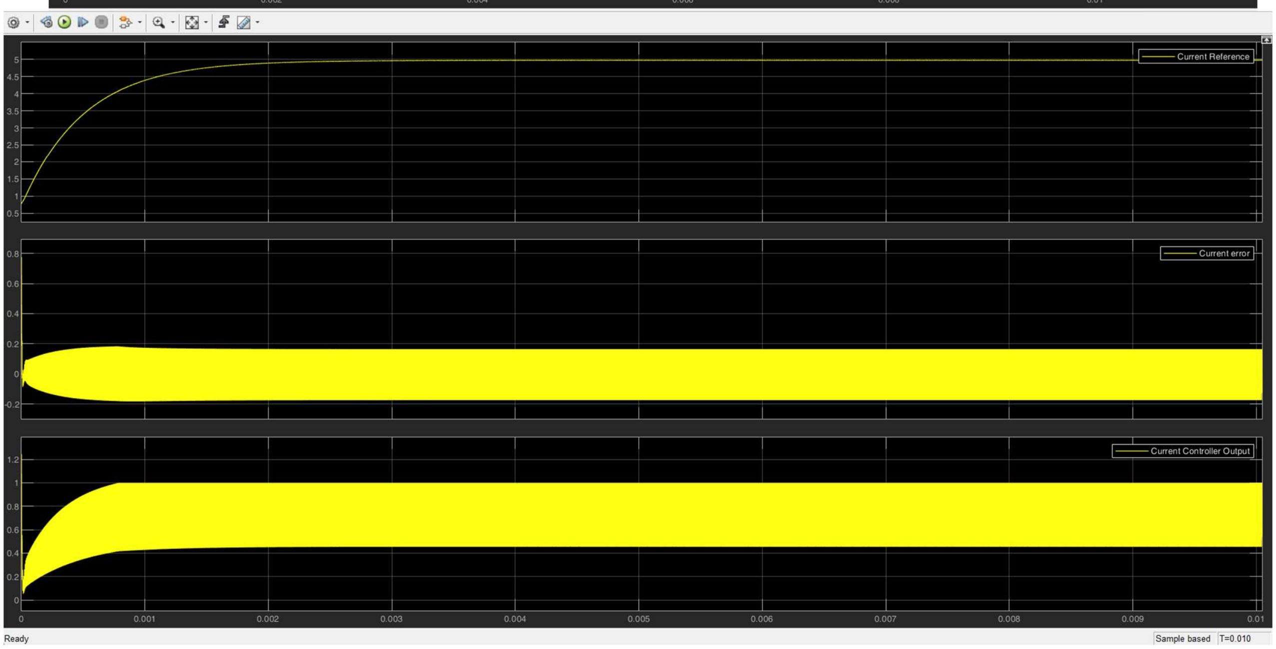
(a) At Vout = 200V, Pout = 360W

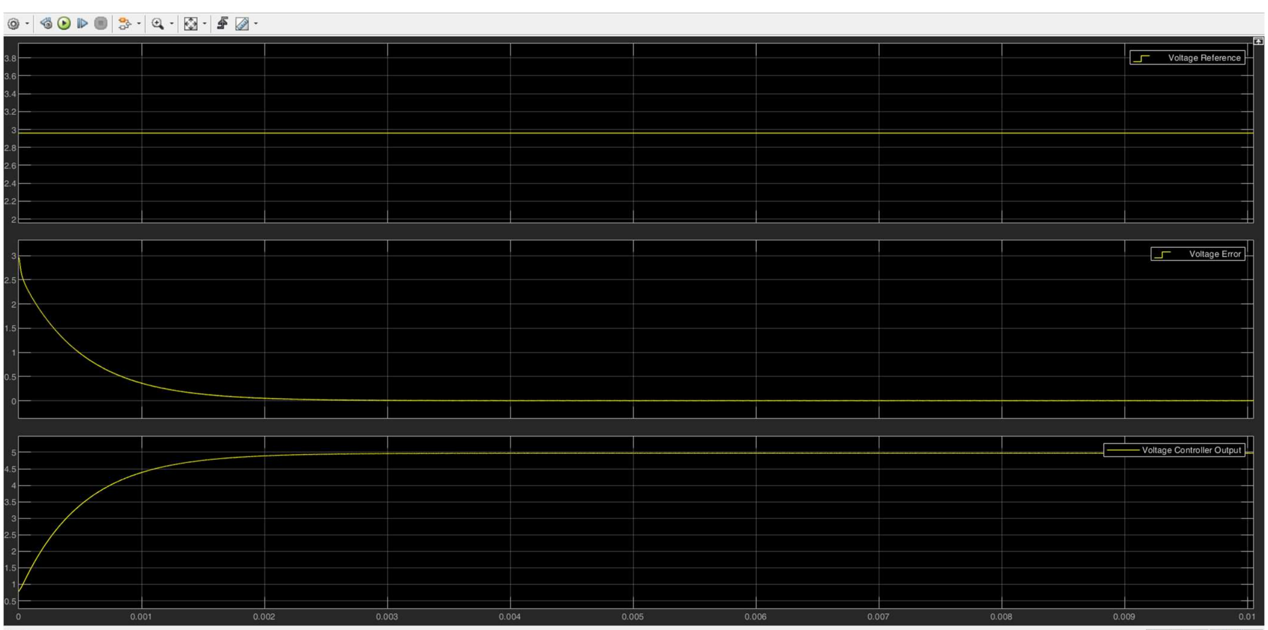




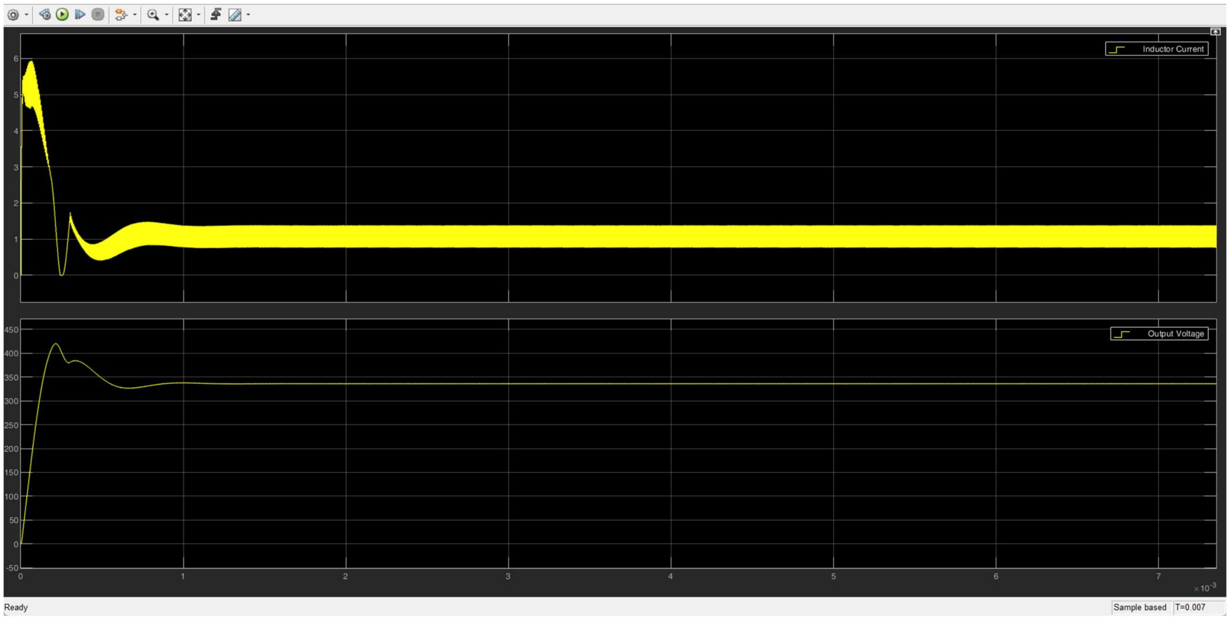


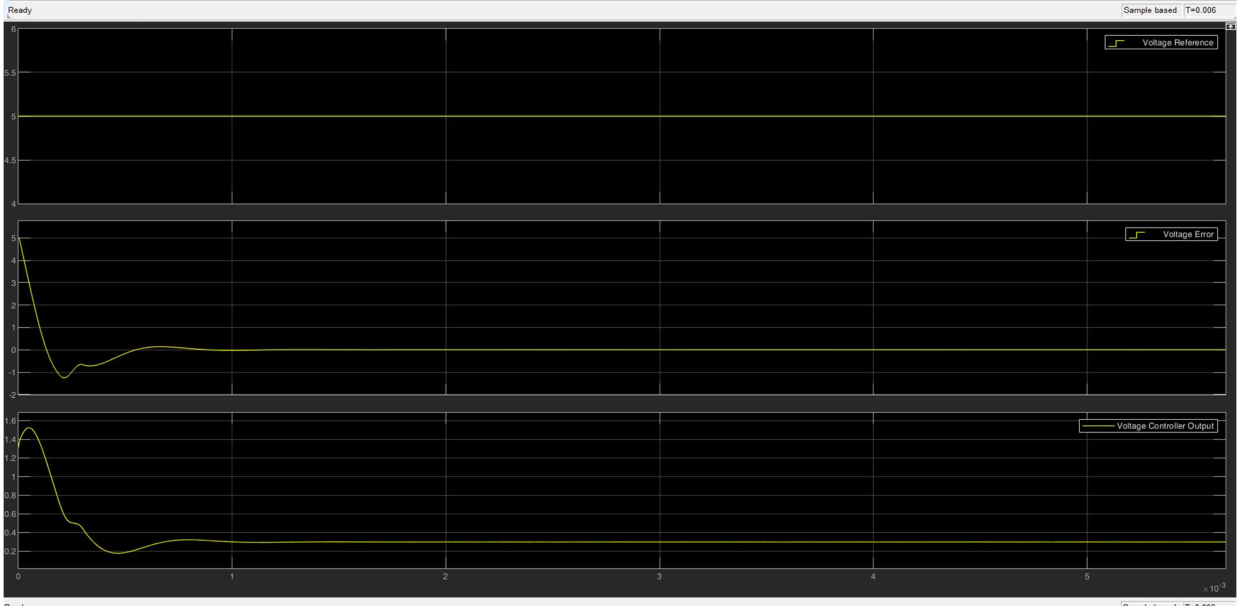
(b) At Vout = 200V, Pout = 3600W



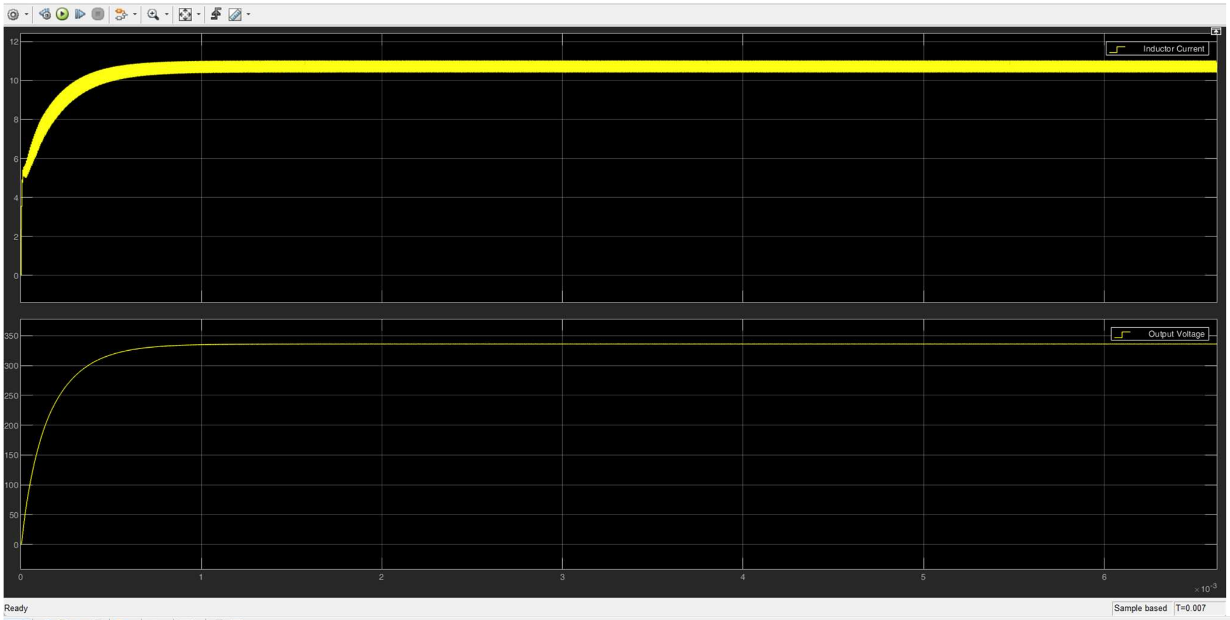


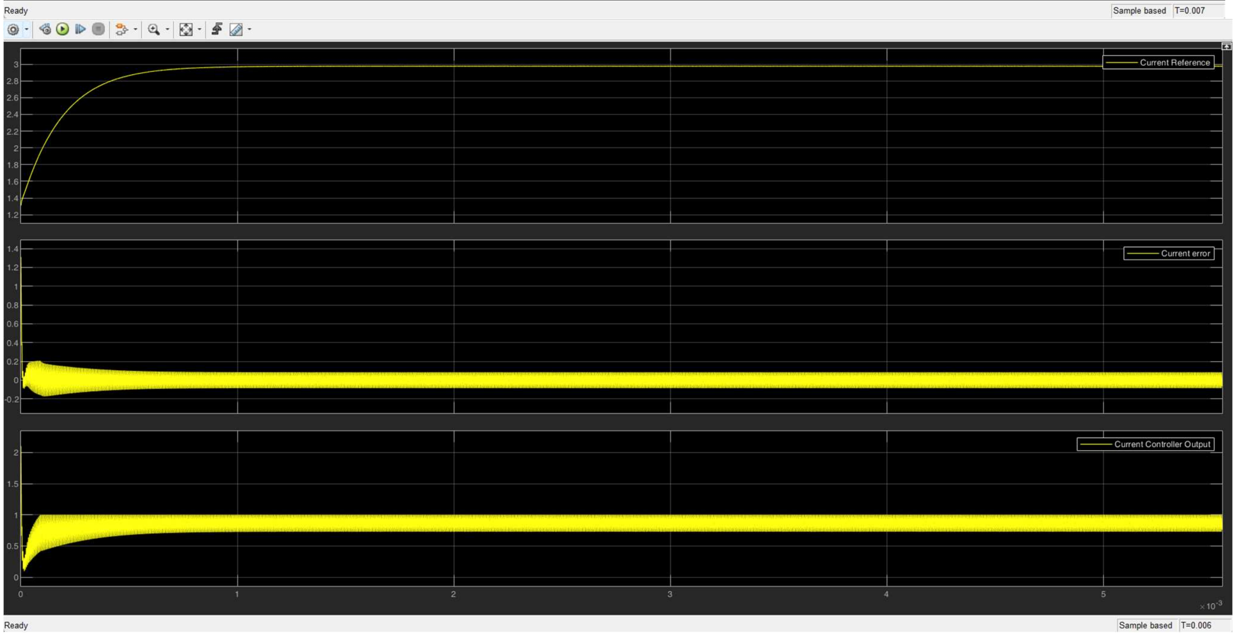
(c) At Vout = 336V, Pout = 360W

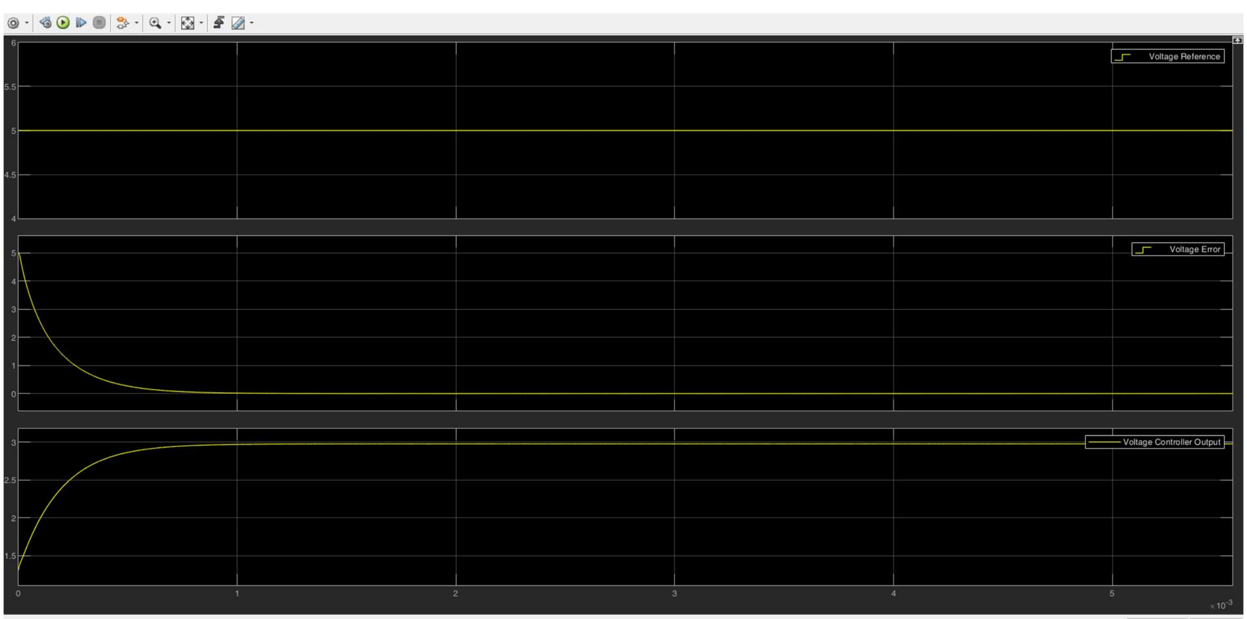




(d) At Vout = 336V, Pout = 3600W

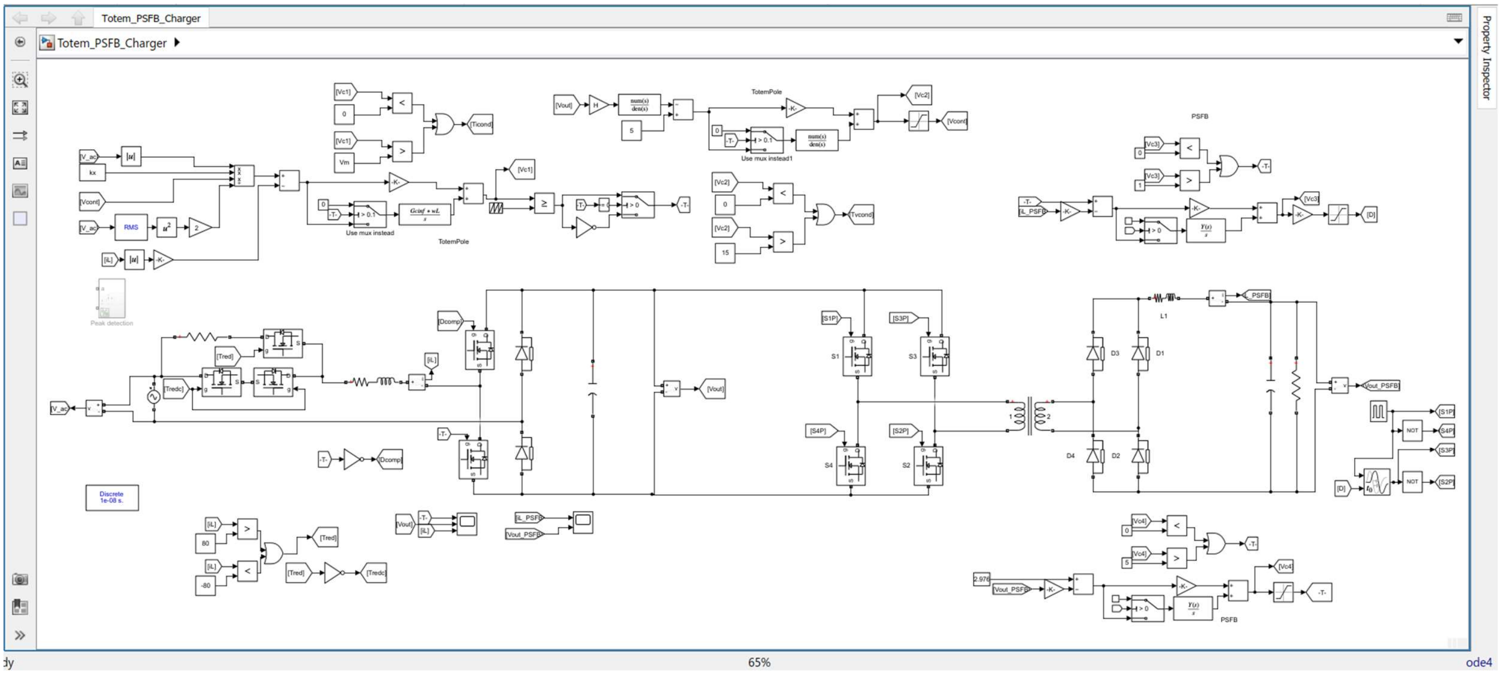






Now, let us combine these two converters as specified in the problem statement and check whether it is functioning correctly or not at different operating conditions.

Circuit schematic for charger (i.e., Totem Pole and PSFB converter connected as specified):



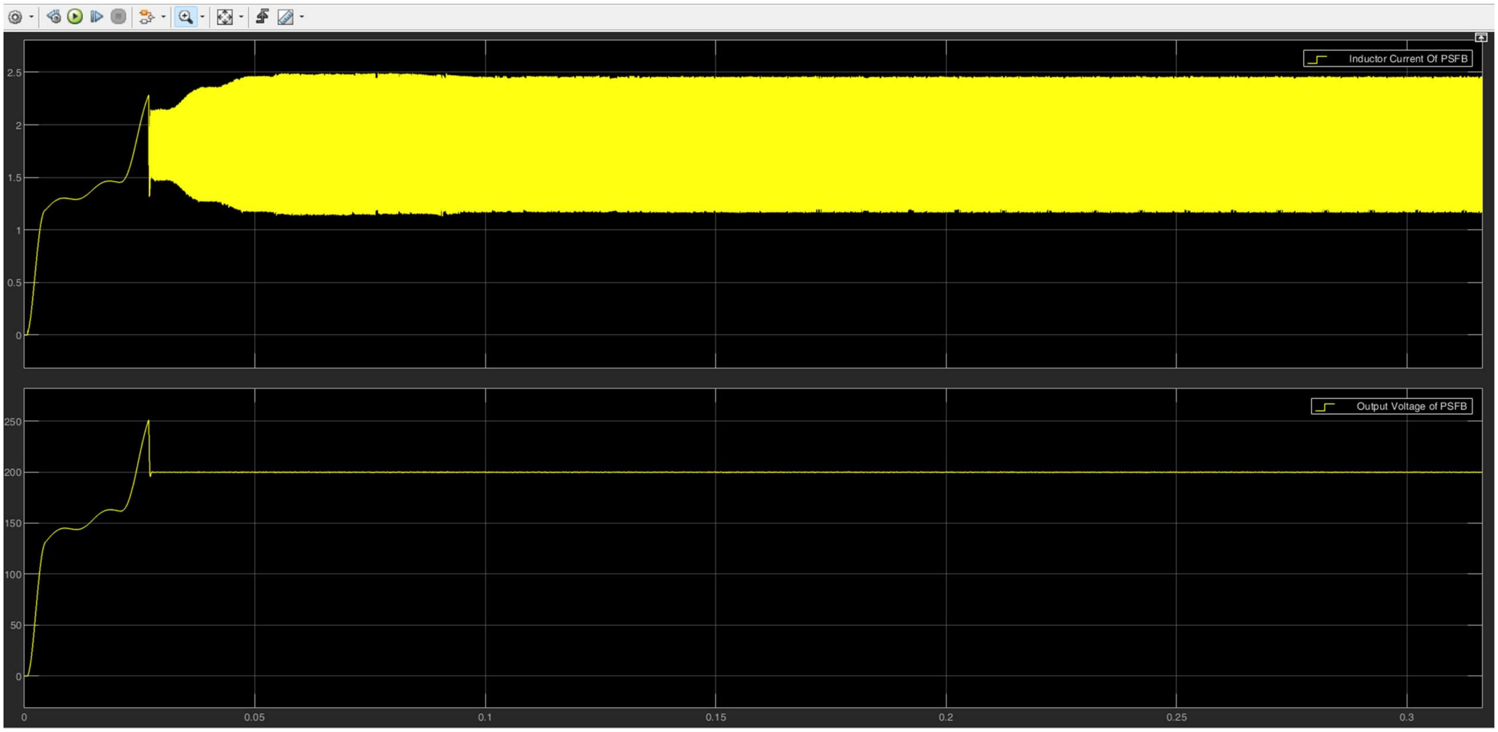
NOTE: The simulation has to be ran at a step size of 1e-09s or 1e-08s for avoiding distortion in the PSFB waveform. But due to excessive time consumption at lower step size, I used a step size of 1e-07s. One can run this simulation at any step size if needed.
Also, the waveforms for controllers are not shown as on trying recording data on many scopes my laptop crashed. So, I can show the waveform as a demo.

Waveforms are on next few pages

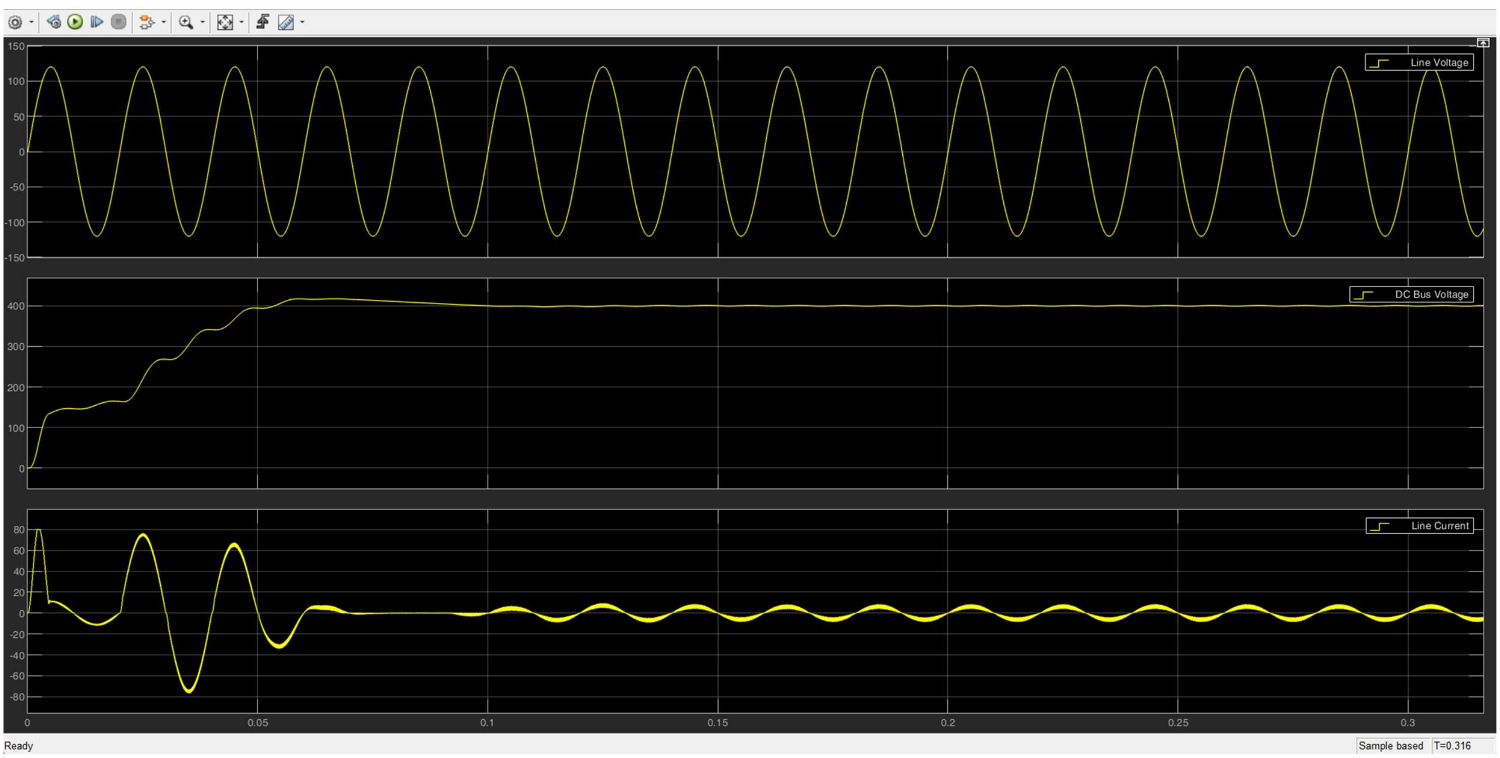
Waveforms at different operating conditions:

(a) **At Vac = 85V (rms), fac = 50Hz, Vout = 200V, Pout = 360W**

PSFB waveform:

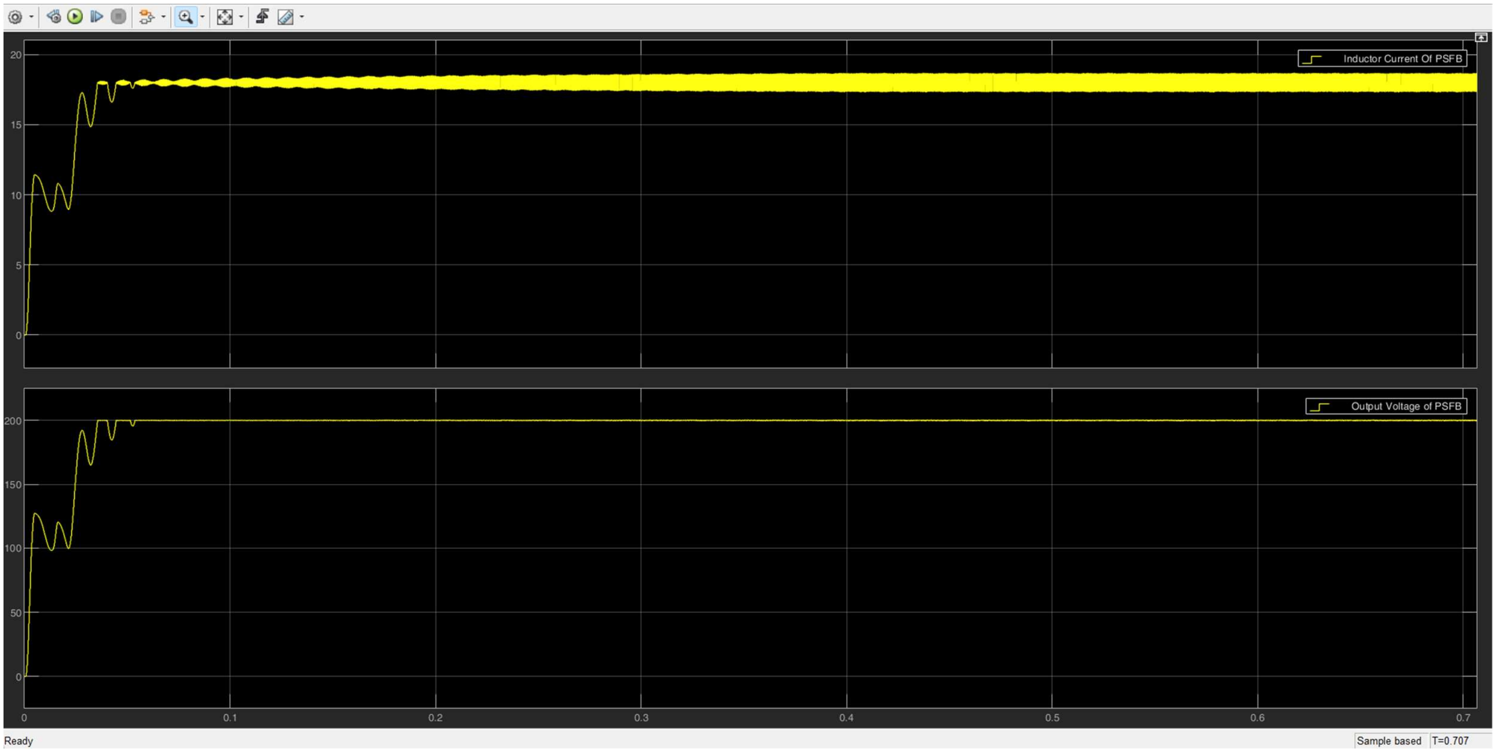


Totem Pole Waveforms:

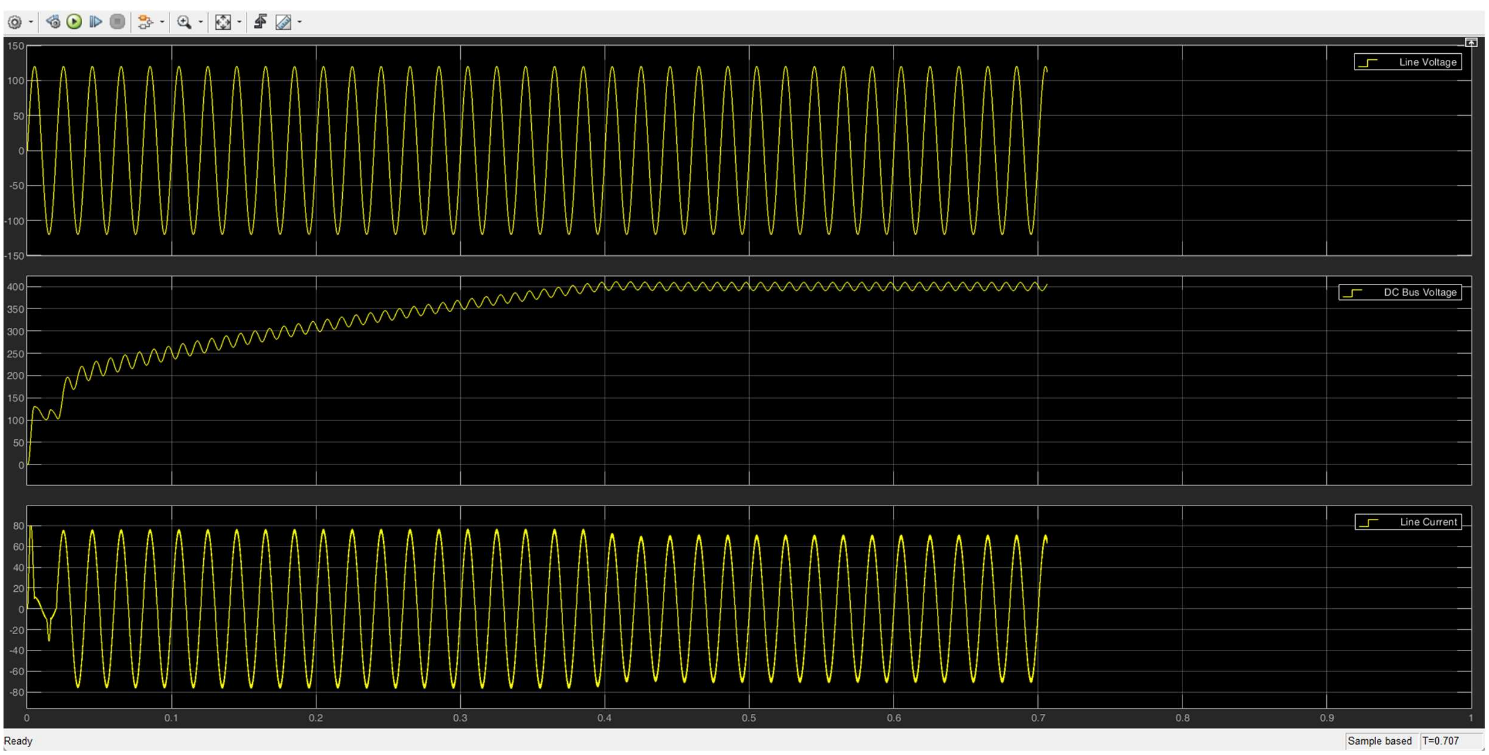


(b) <u>At Vac = 85V (rms), fac = 50Hz, Vout = 200V, Pout = 3600W (maximum loading on converter)</u>

PSFB waveform:

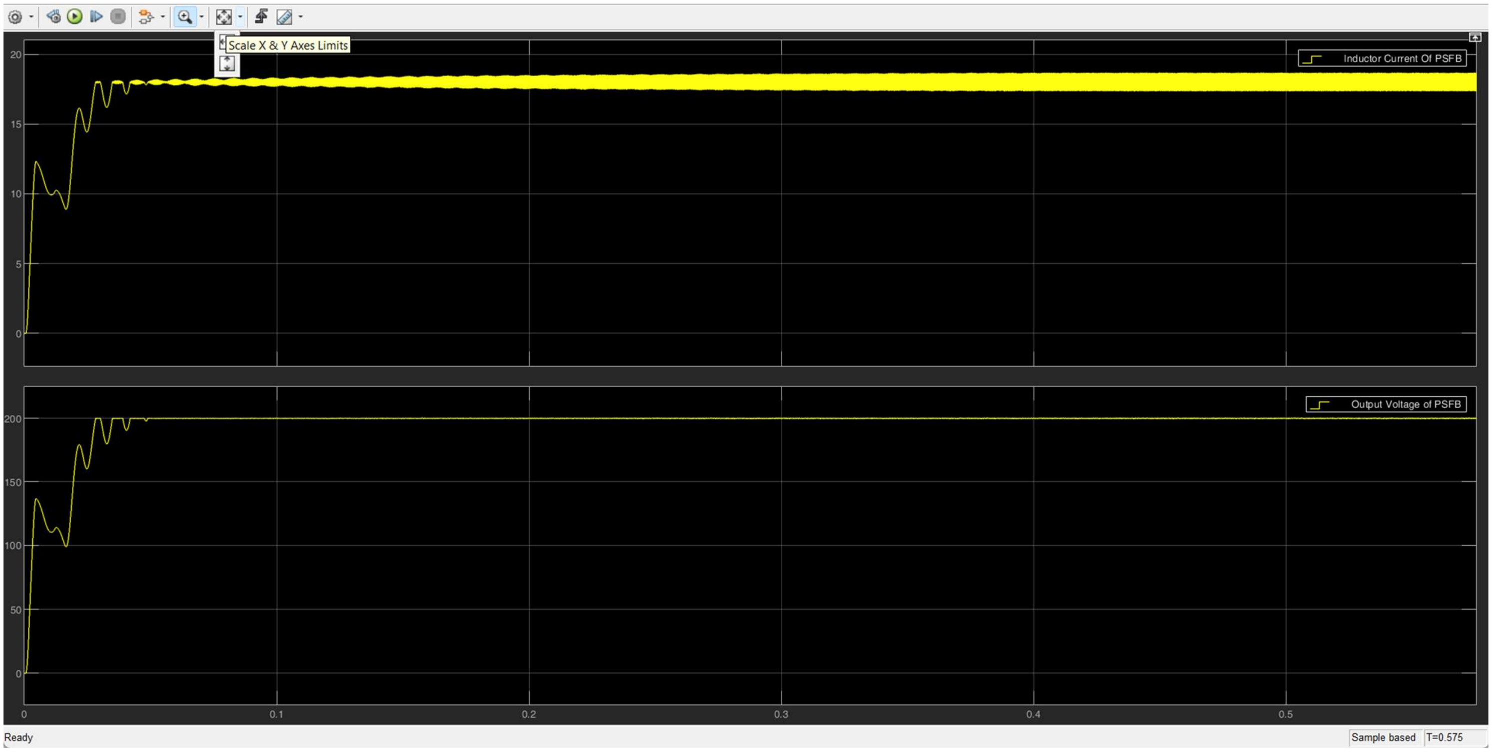


Totem Pole converter:

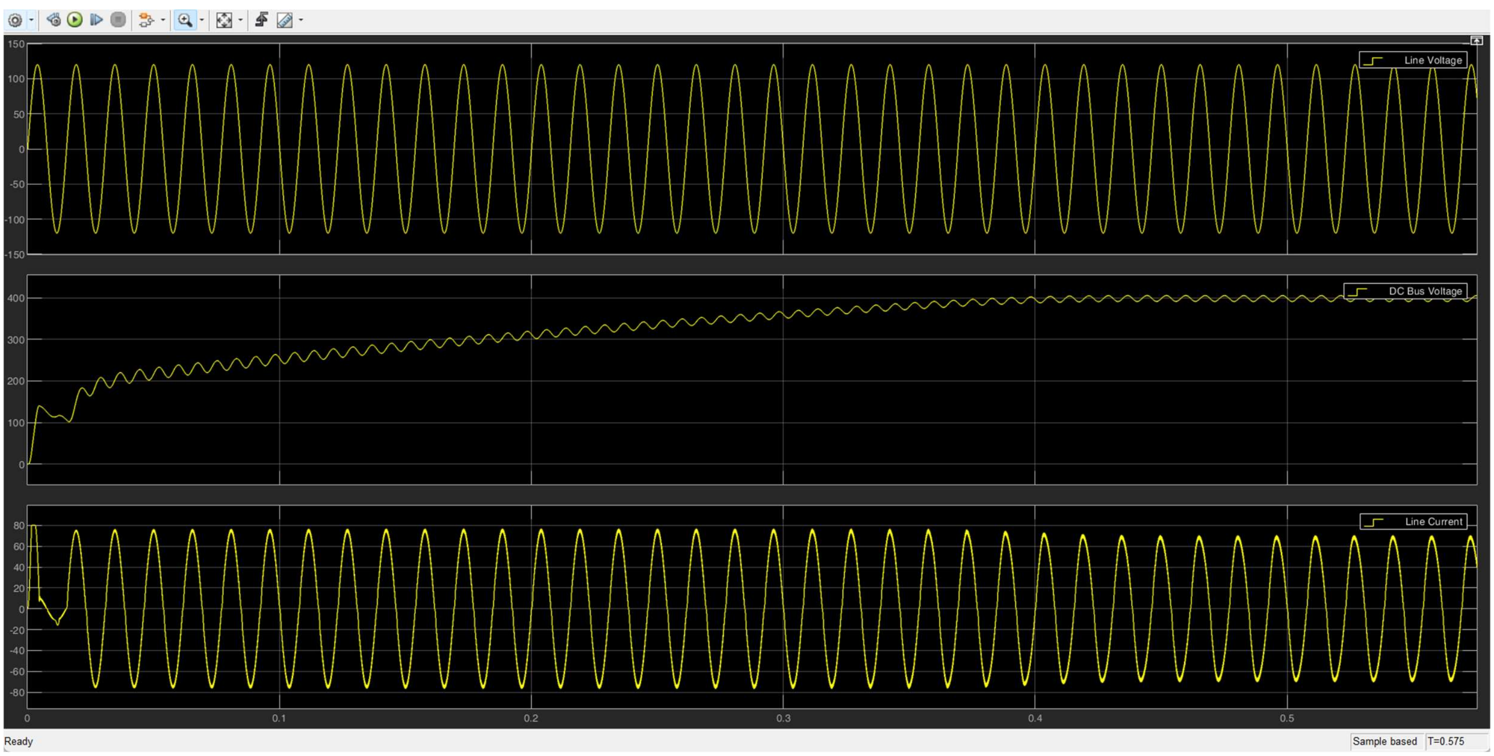


(c) At Vac = 85V (rms), fac = 65Hz, Vout = 200V, Pout = 3600W (maximum loading on converter)

PSFB Converter:

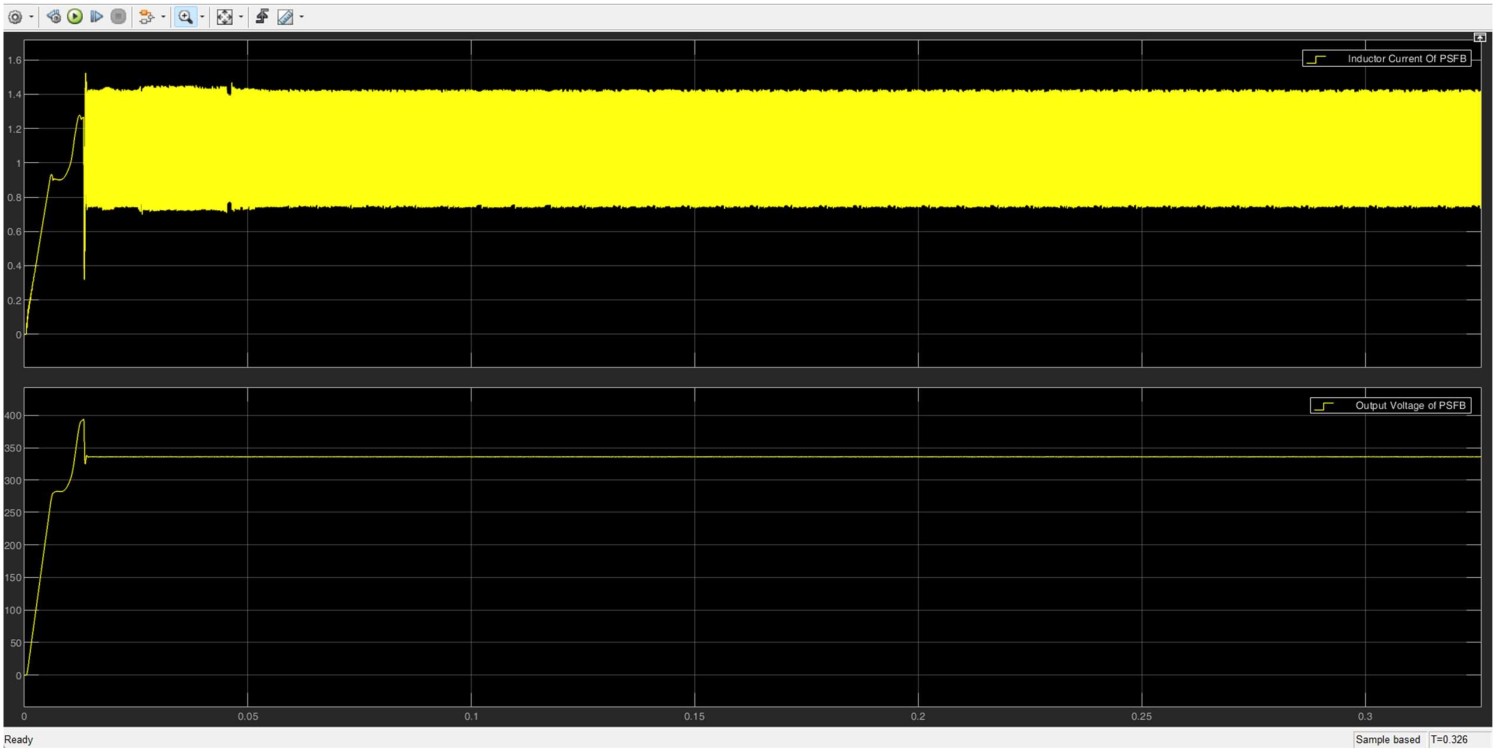


Totem Pole converter:

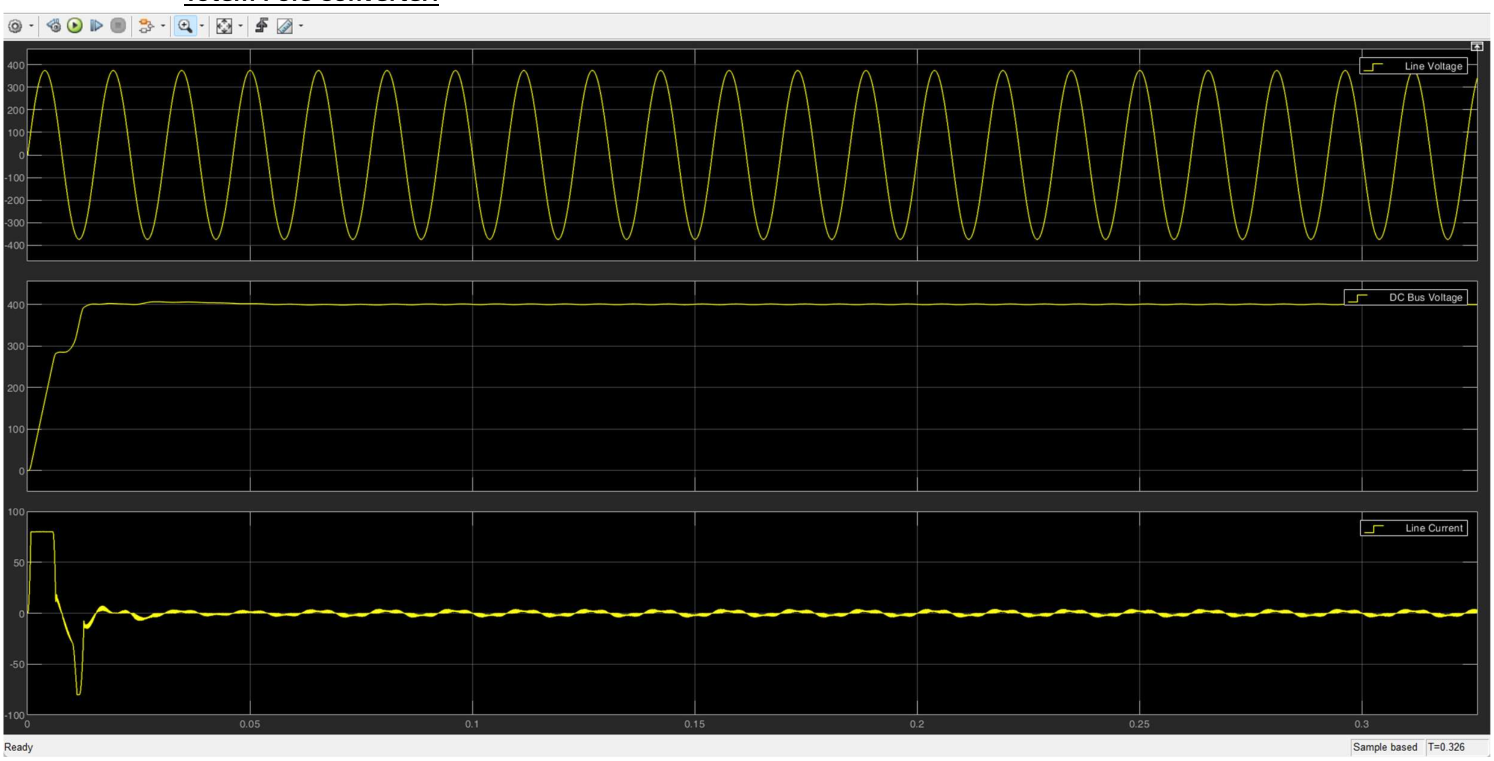


(d) At Vac = 265V (rms), fac = 65Hz, Vout = 336V, Pout = 360W (minimum loading on converter)

PSFB Converter:

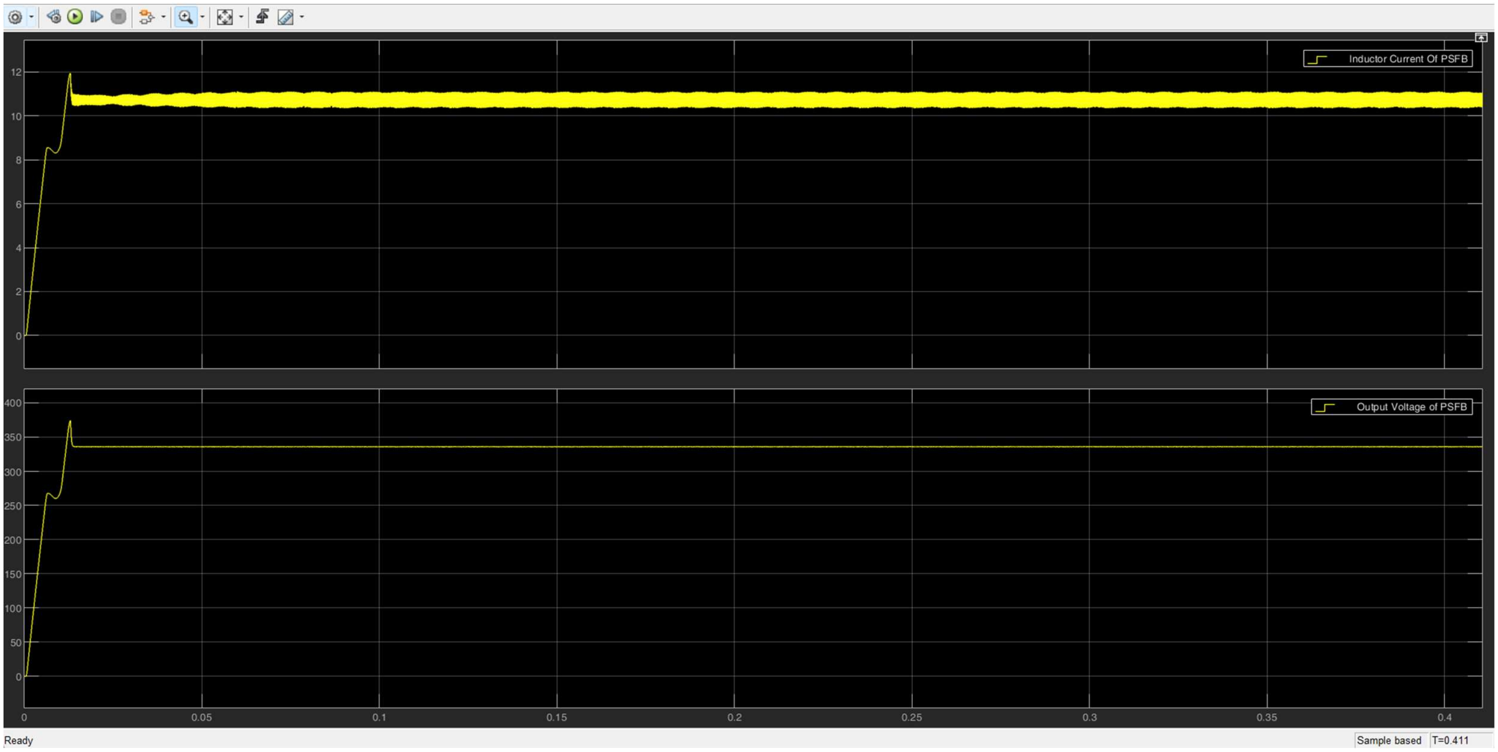


Totem Pole Converter:



(e) At Vac = 265V (rms), fac = 65Hz, Vout = 336V, Pout = 3600W

PSFB Converter:



Totem Pole converter: