PROJECT 2

EE739: - Processor Design

Department of Electrical Engineering

(IIT Bombay)

Submitted By: -

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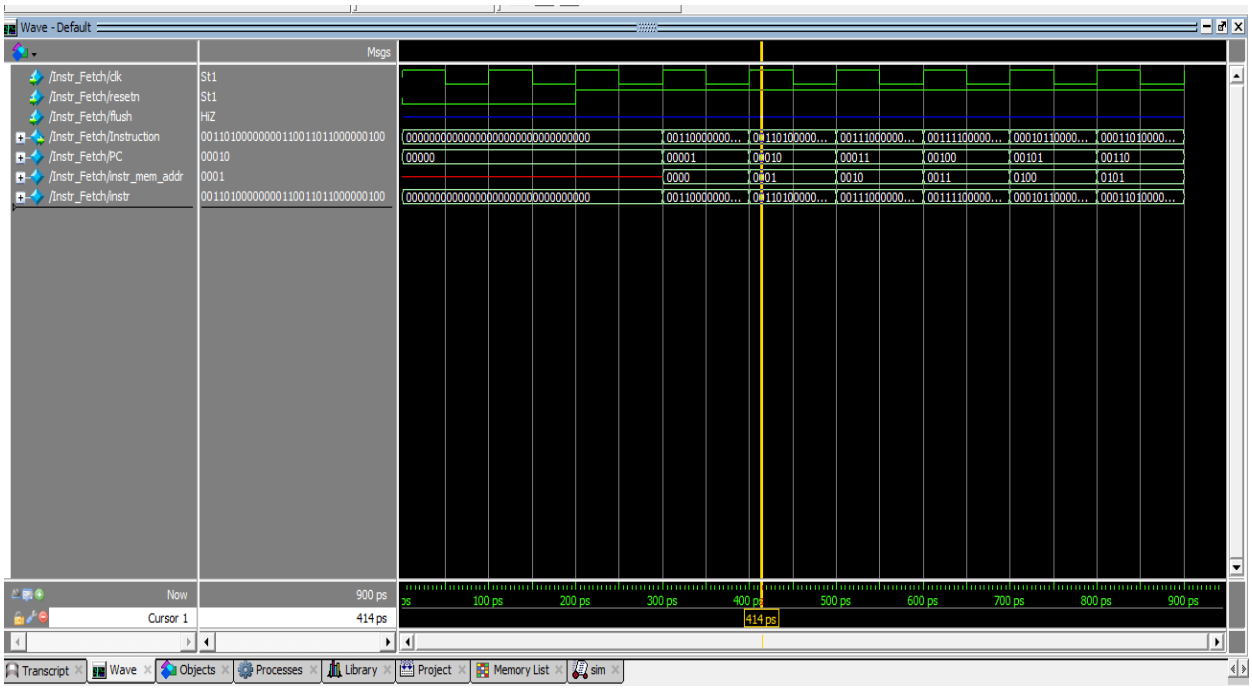
Introduction: -

Here, in this project we have implemented 2-way fetch superscalar processor which is 16-bit computer with 8 registers. We fetch two instructions at a time in the Fetch Unit. We then decode the instructions two at a time and pass the control bits to the Dispatch Unit. The Dispatch Unit then passes the instructions to the respective Reservation Stations for the ALU, Memory units. The Reservation Station manages the dispatching of the instructions stored in its buffer to the respective execution units. The outputs of the execution unit are then next fed to the storage buffer.

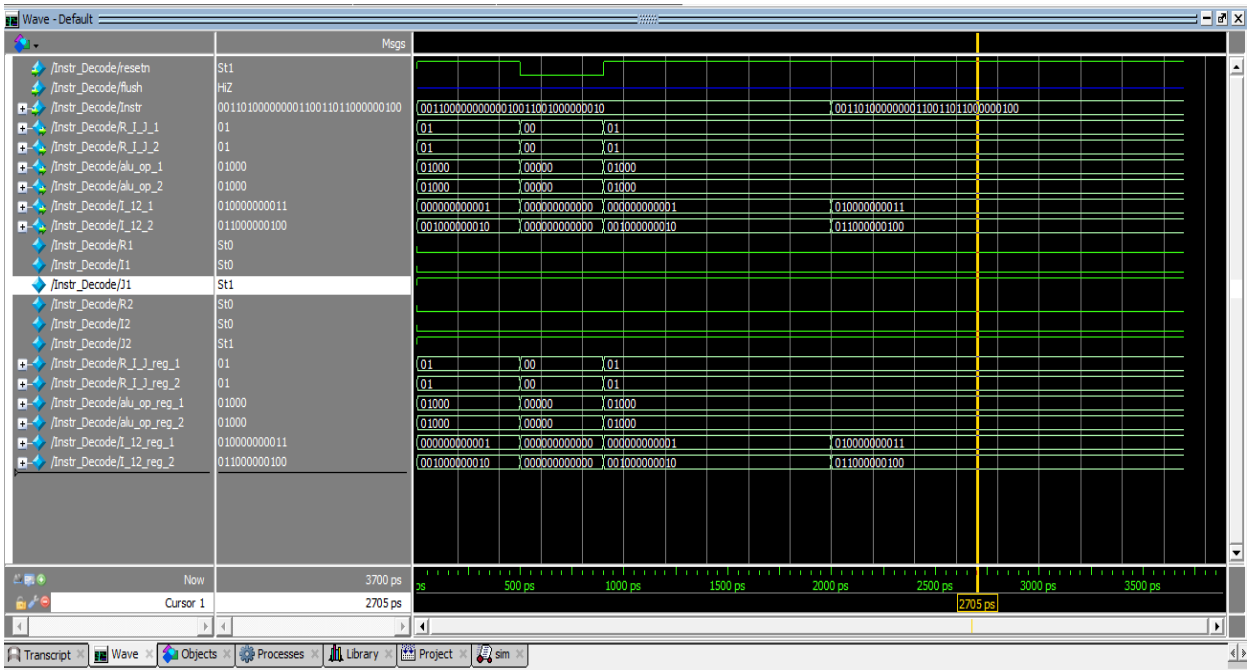
Instruction Fetch: -

The Fetch Unit requires an input of the Program Counter. This Program Counter is fed to the Fetch Unit via a Multiplexer which is responsible for selecting the next program counter. The two instructions each of 16-bit wide have been fetched at a time.



Instruction Decode: -

The Decode Stage is responsible to decode the instructions and send the corresponding register data and the architectural register tags for the destination and the operand registers along with the immediate operands (if any). It also sends control bits to be used by the different stages further in the pipeline.



Dispatch Stage: -

The Dispatch Stage is crucial for the Superscalar processor architecture. This stage is responsible for dispatching the instructions coming to it. Dispatch stage receives the decoded instruction from the decode stage. In the case of 2- way fetch superscalar, the dispatch stage receives two decoded instructions from decode stage. Each instruction has associated control signals and register Ids or immediate operand. The dispatch stage resolves the false dependencies by using register renaming. As the reservation stations are decentralized, dispatch unit sends the instruction to appropriate reservation station. Dispatch stage receives instruction, operands, control bits, source and destination registers from decode stage. Dispatch receives 2 instructions from decode, in each clock cycle. Dispatch unit sends each instruction along with its associated control signals, operands (or tag of operand), operand validity bits, tag of destination to the correct reservation station.

Reservation Station: -

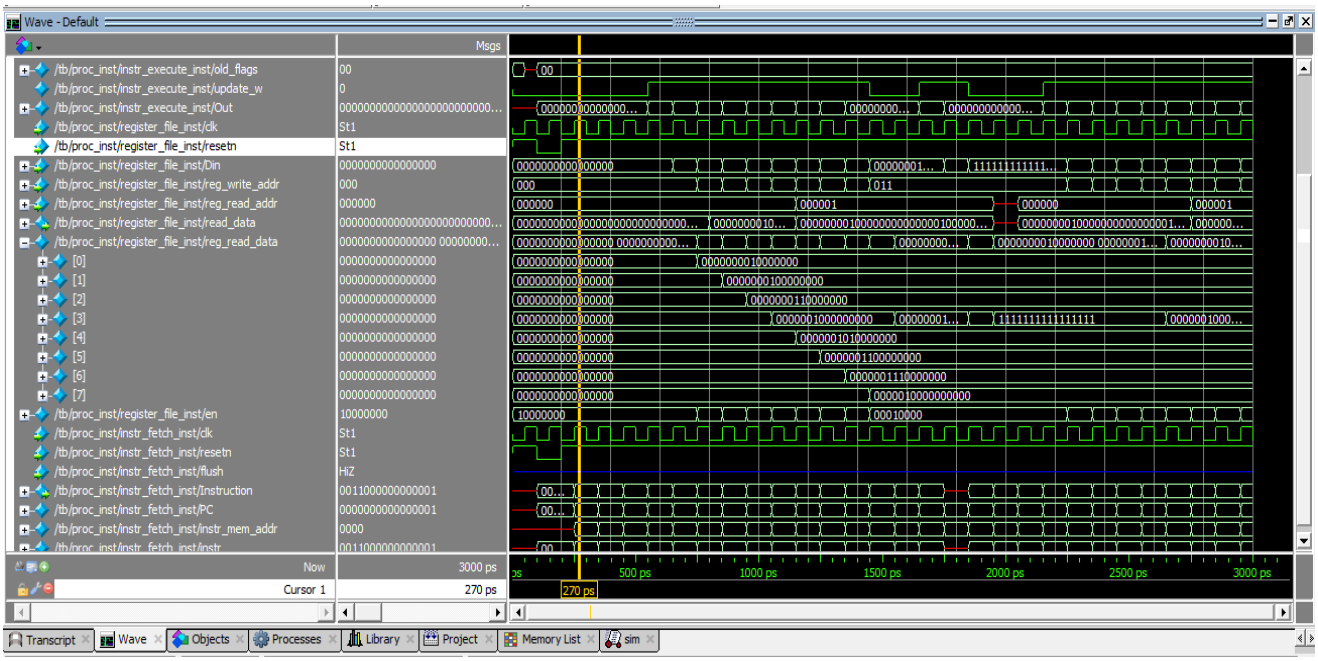
Instructions wait in the reservation station till their operands are ready. We have designed decentralized reservation stations, with each execution unit having its own reservation station. Thus, there are 2 reservation stations, one each for ALU, Memory units. The reservation station sends the instruction to execution unit once its operands are ready. Each reservation gets the instruction, control bits, operands, operand validity bits, tag of destination register of the instruction from the dispatch stage. Reservation station sends the instruction, control bits, destination register tag to the execution unit. The instruction, control bits and operands are used by the execution units as desired.

Execution: -

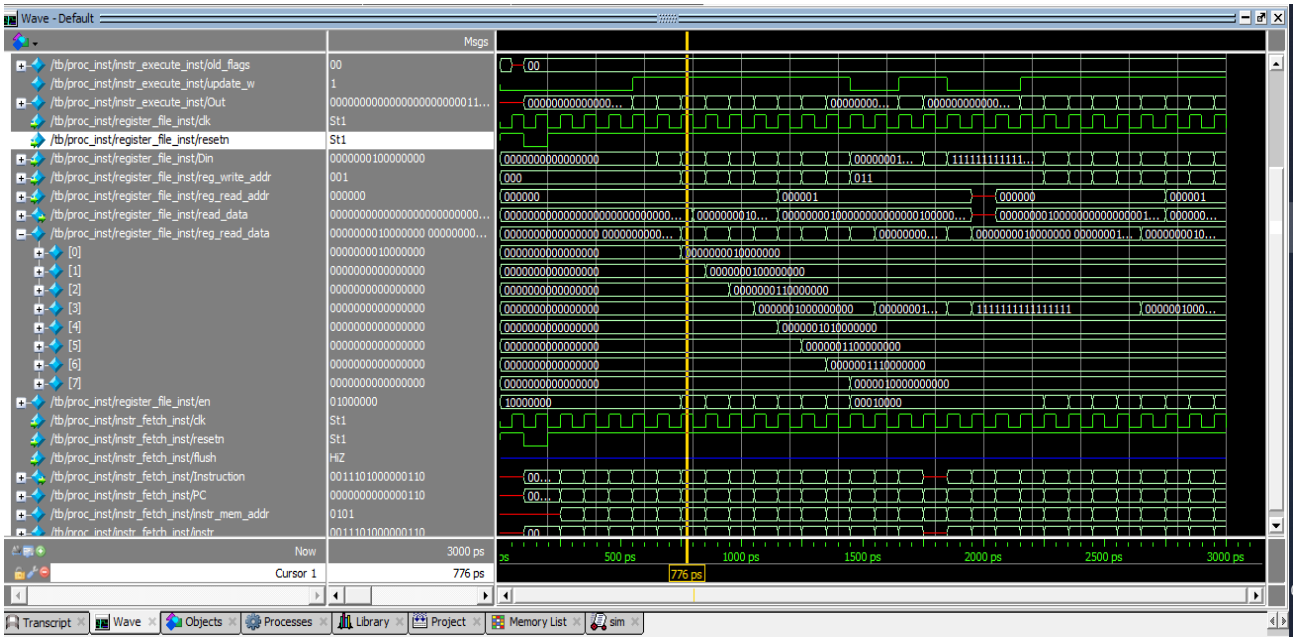
In this stage the execution of the instruction takes place according to the operands defined in the instruction like whether it is ADD, ADC, NDU, LHI, LW, SW, etc. and the results have been produced. The execution stage contains mostly the ALU & Memory operations.

LHI R0, 000000001 (1st Instruction From program_instr.hex)

Input: -

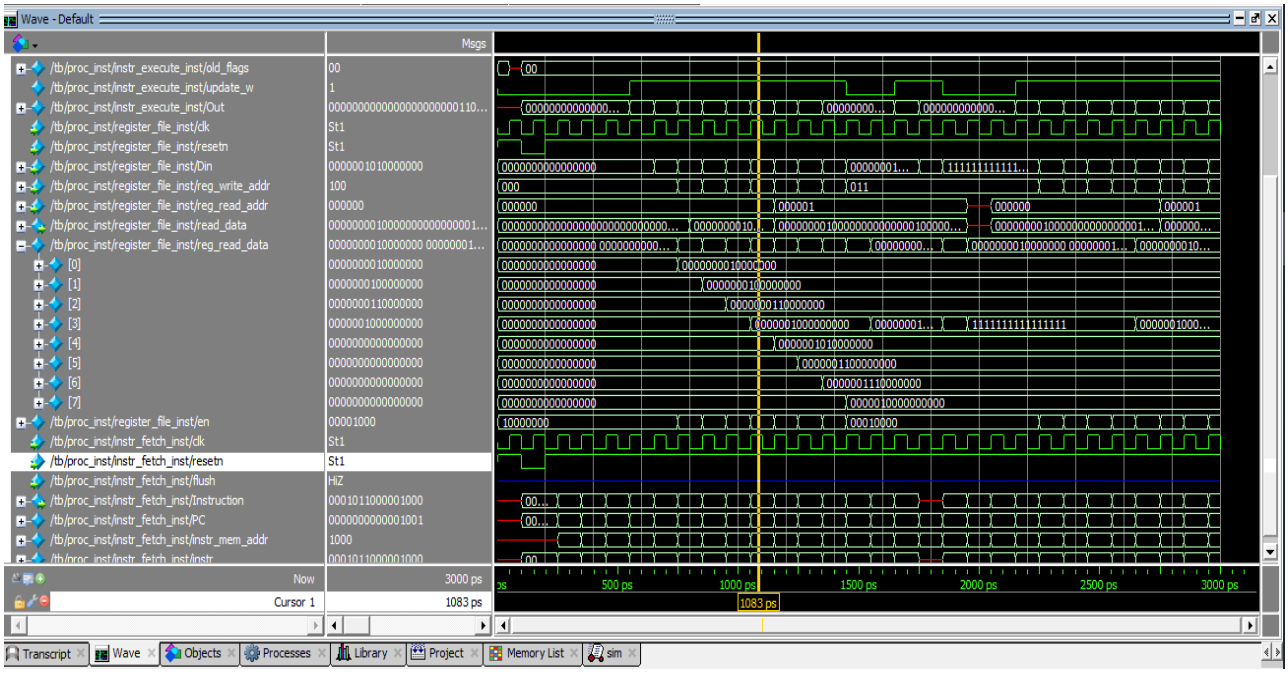


Output: -

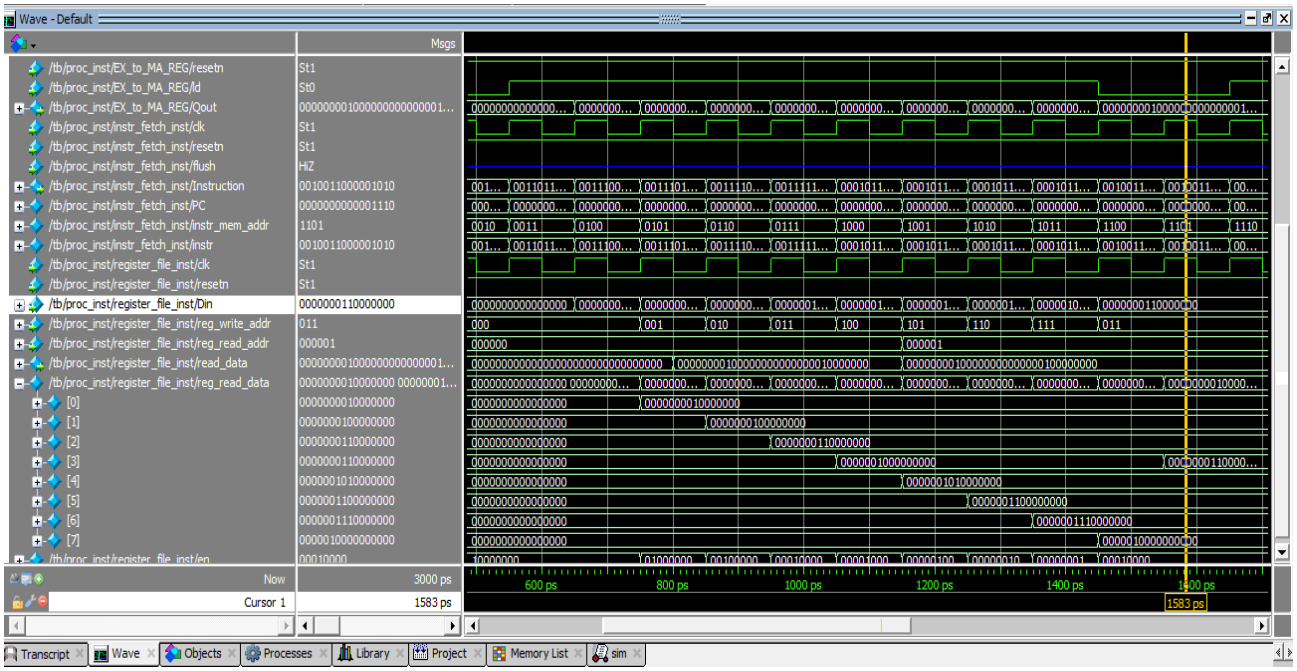


ADD R3, R0, R1 Instruction: -

Input: -

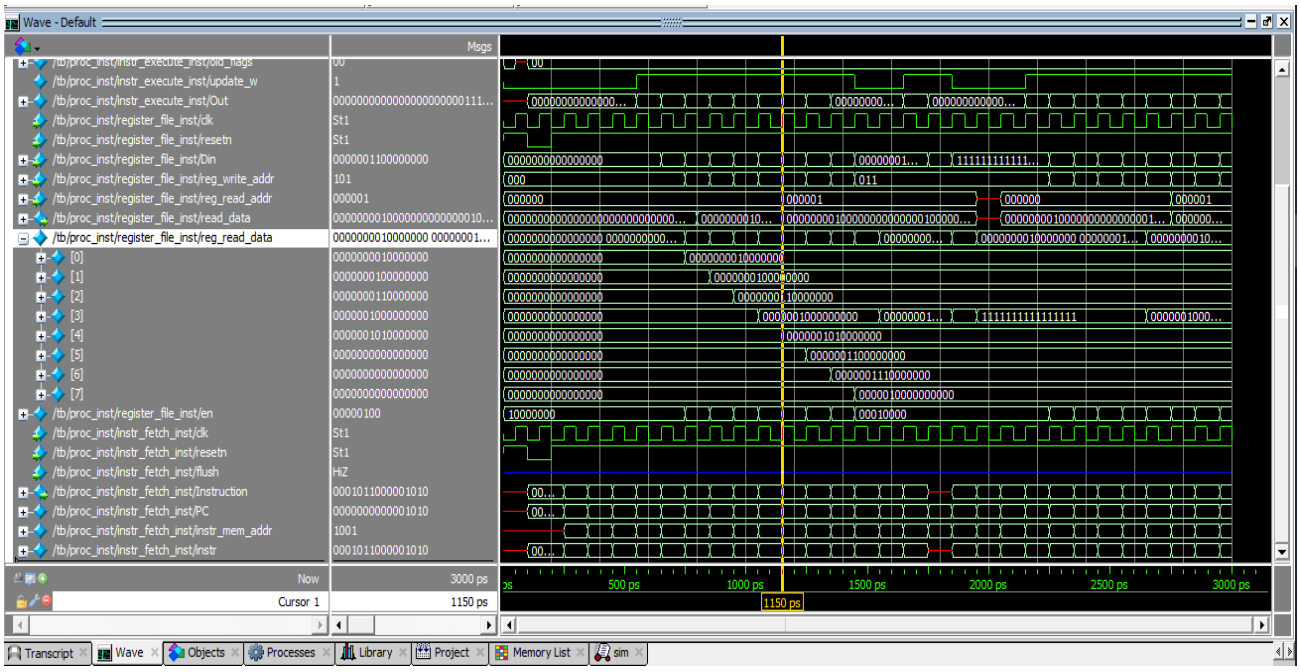


Output: -

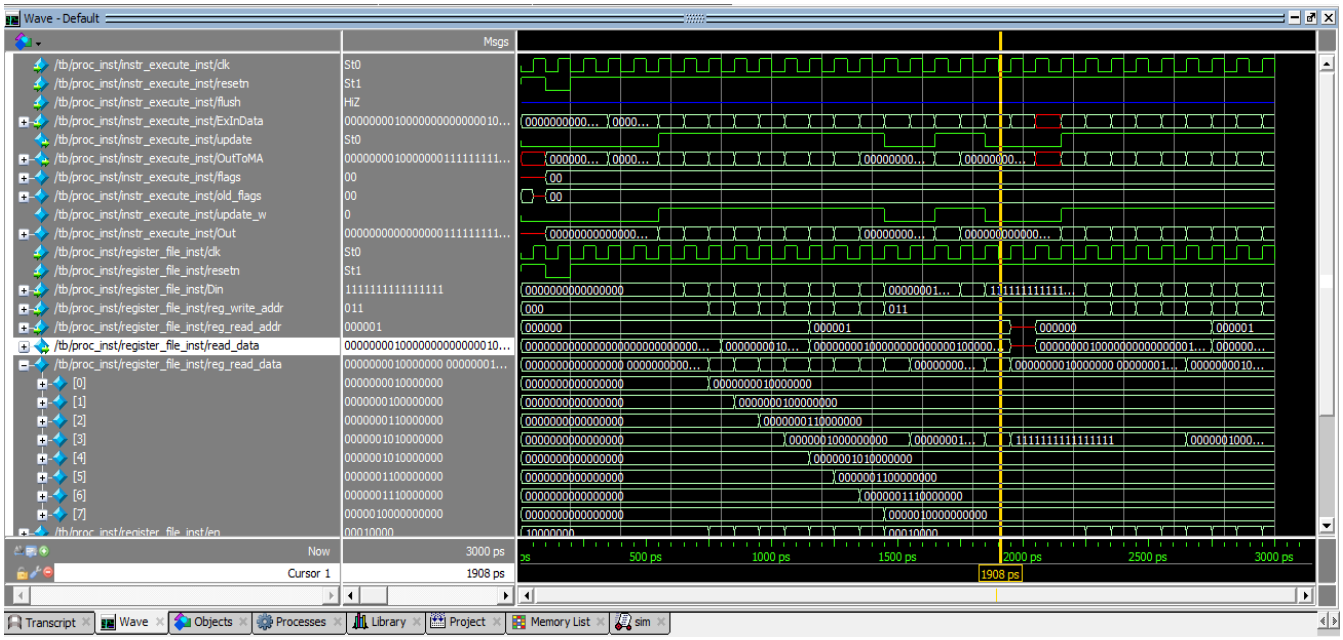


ADC R4, R0, R1 Instruction: -

Input: -

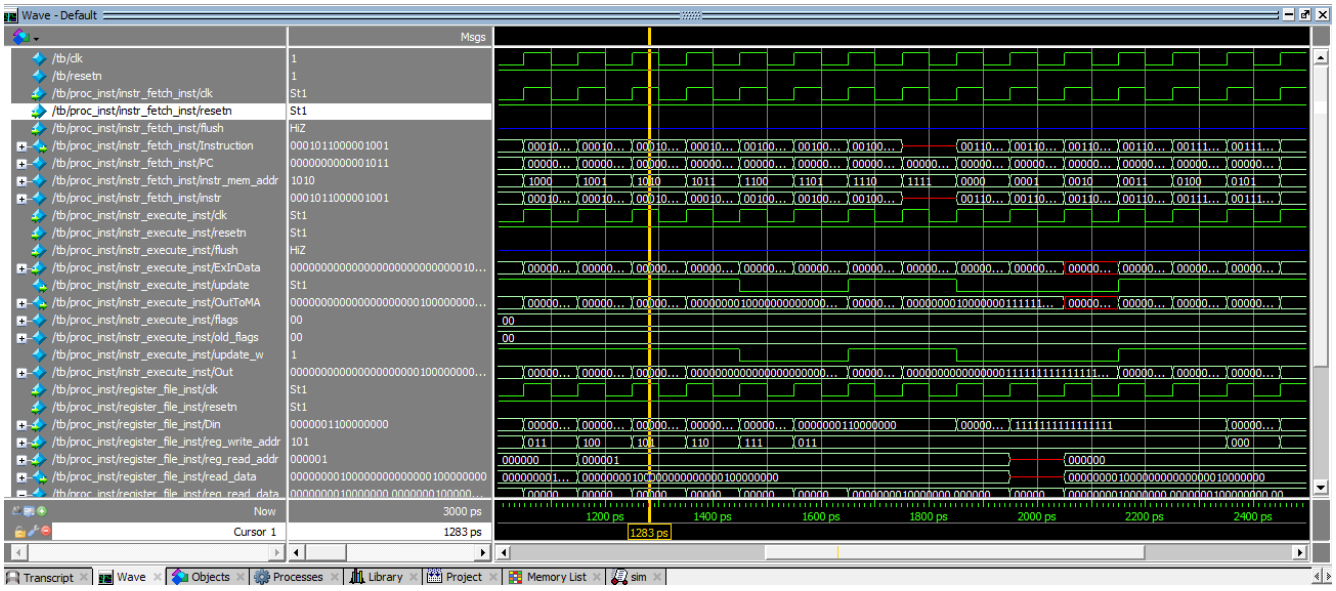


Output: -

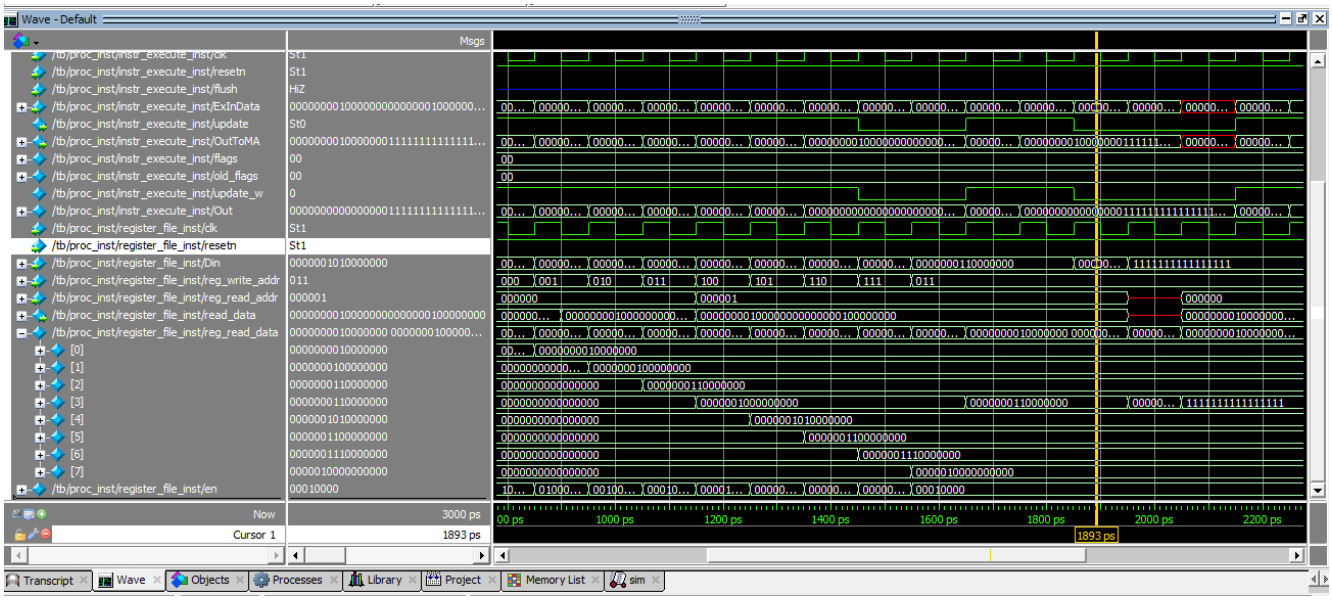


ADZ R5, R0, R1 Instruction: -

Input: -

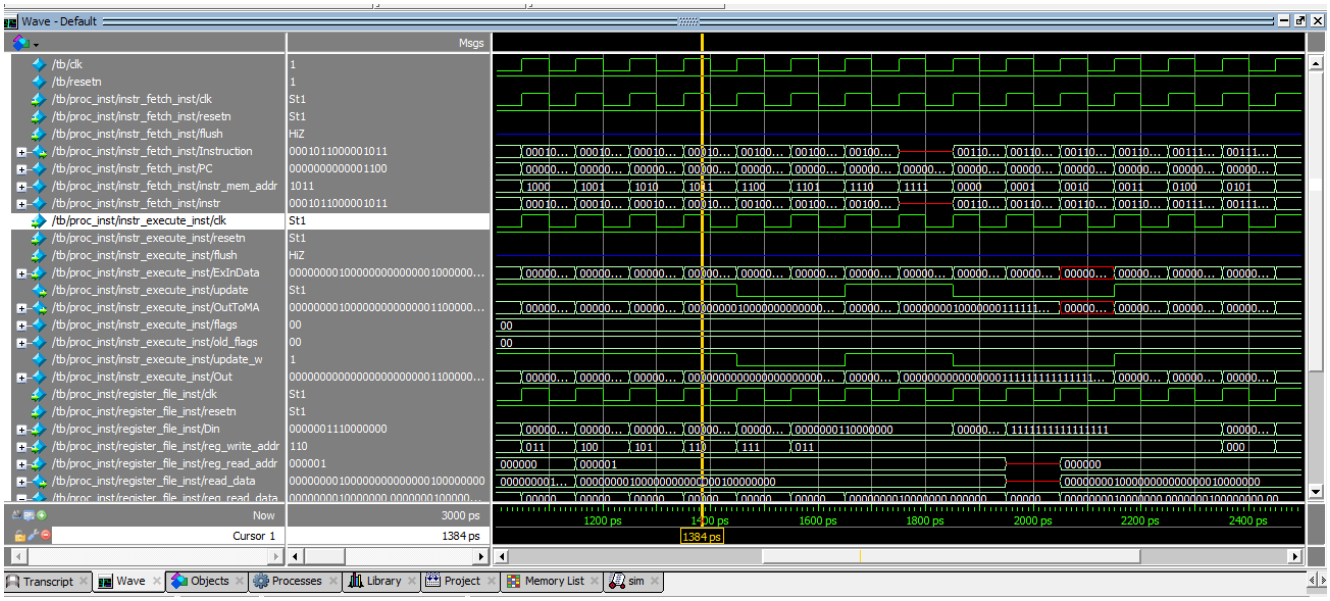


Output: -

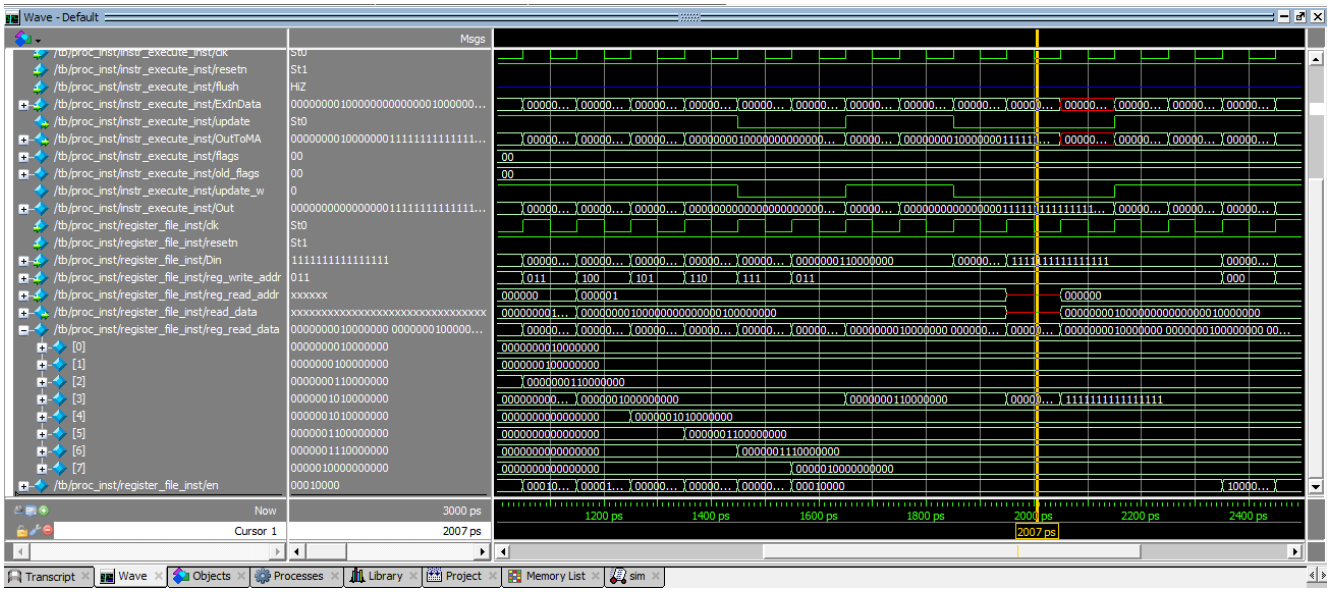


ADL R6, R0, R1 Instruction: -

Input: -

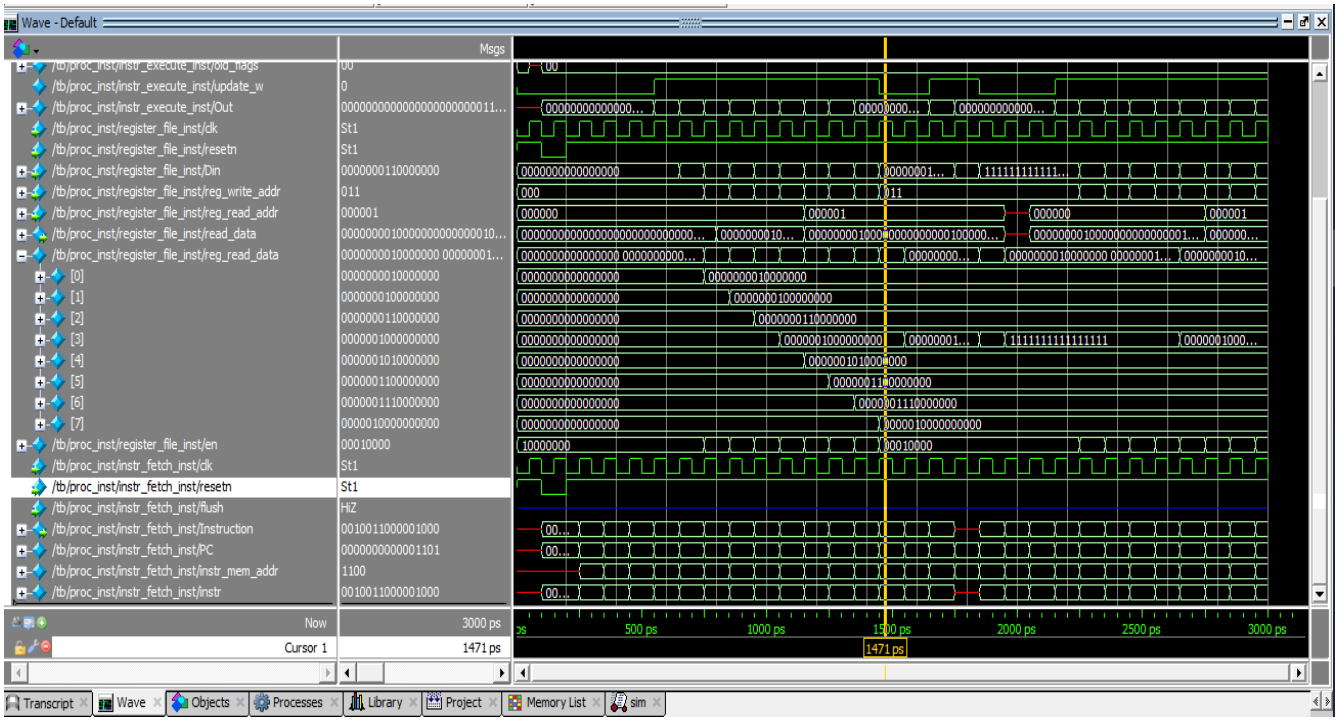


Output: -

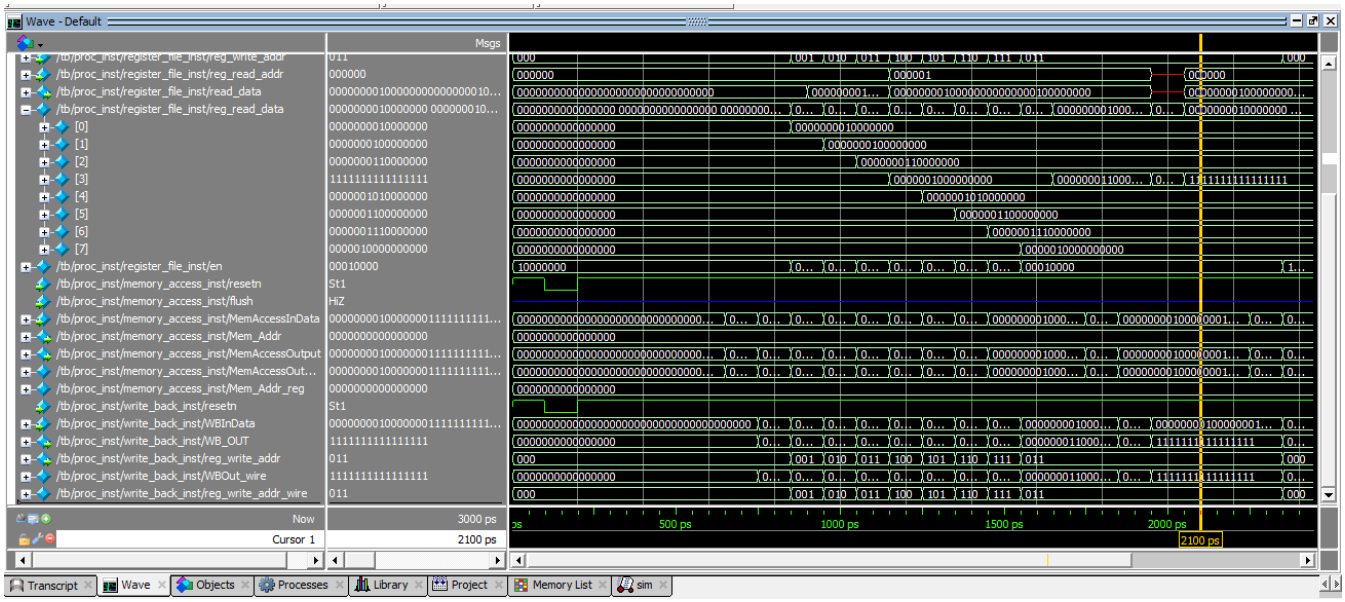


NDU R3, R0, R1 Instruction: -

Input: -

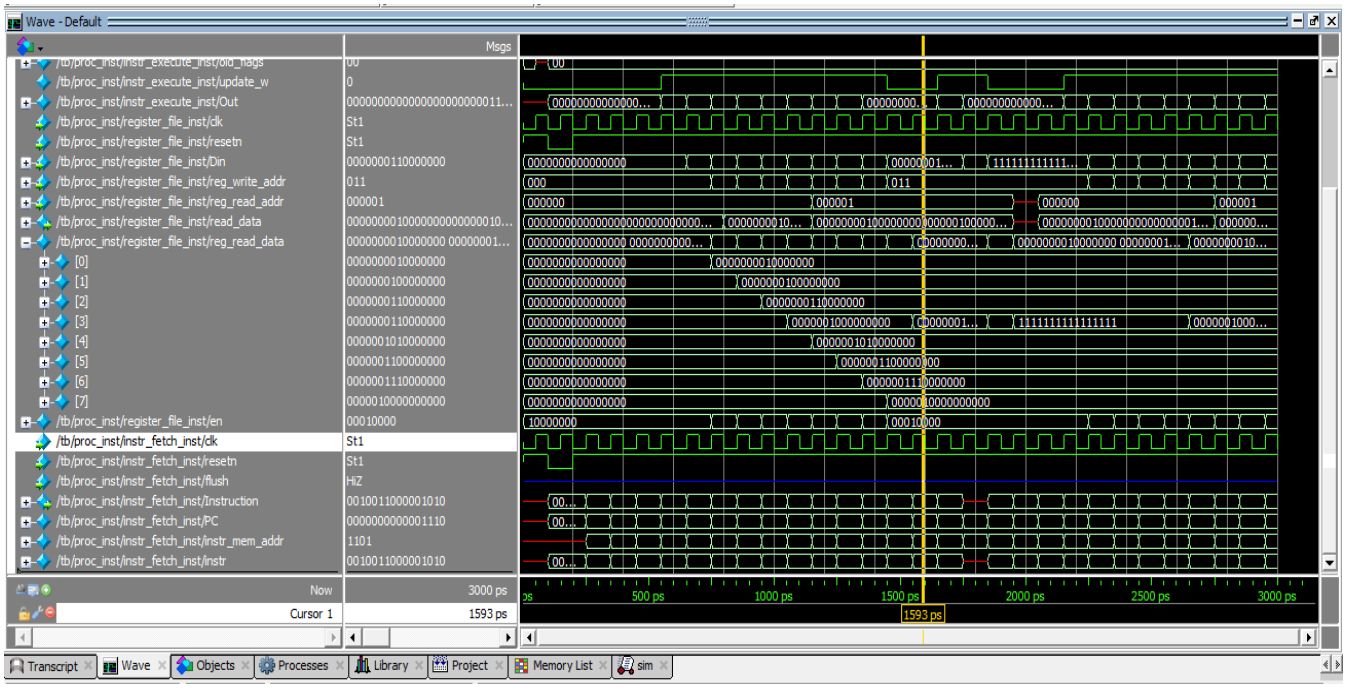


Output: -

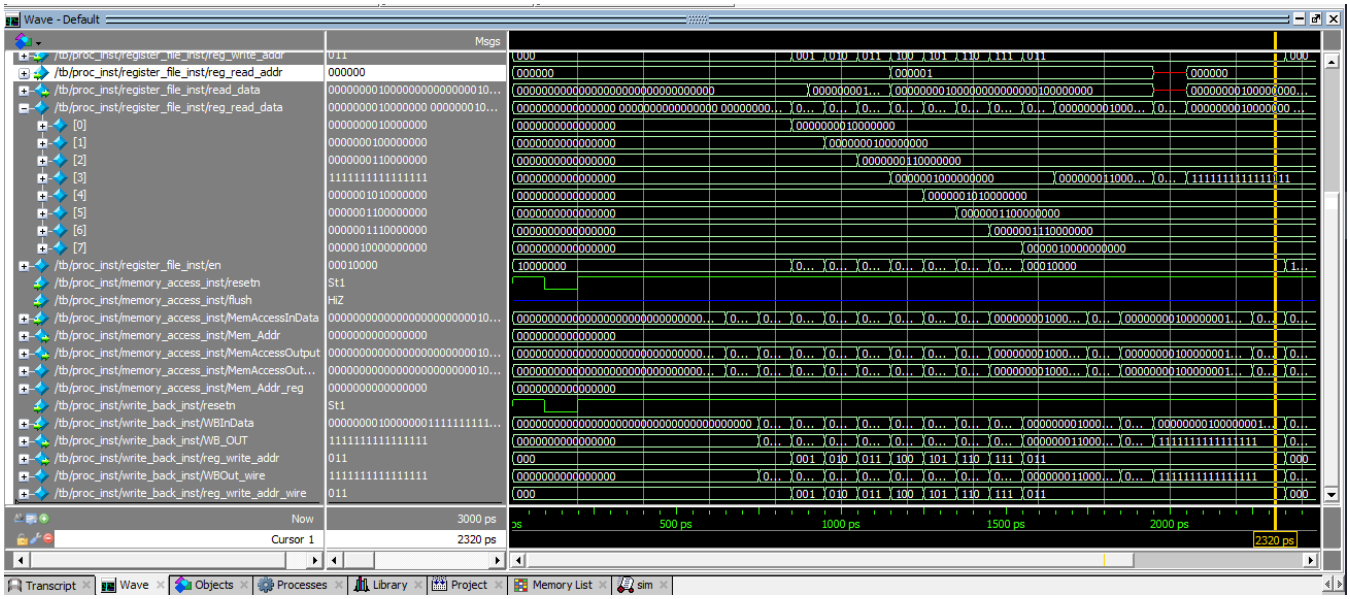


NDC R2, R0, R1 Instruction: -

Input: -

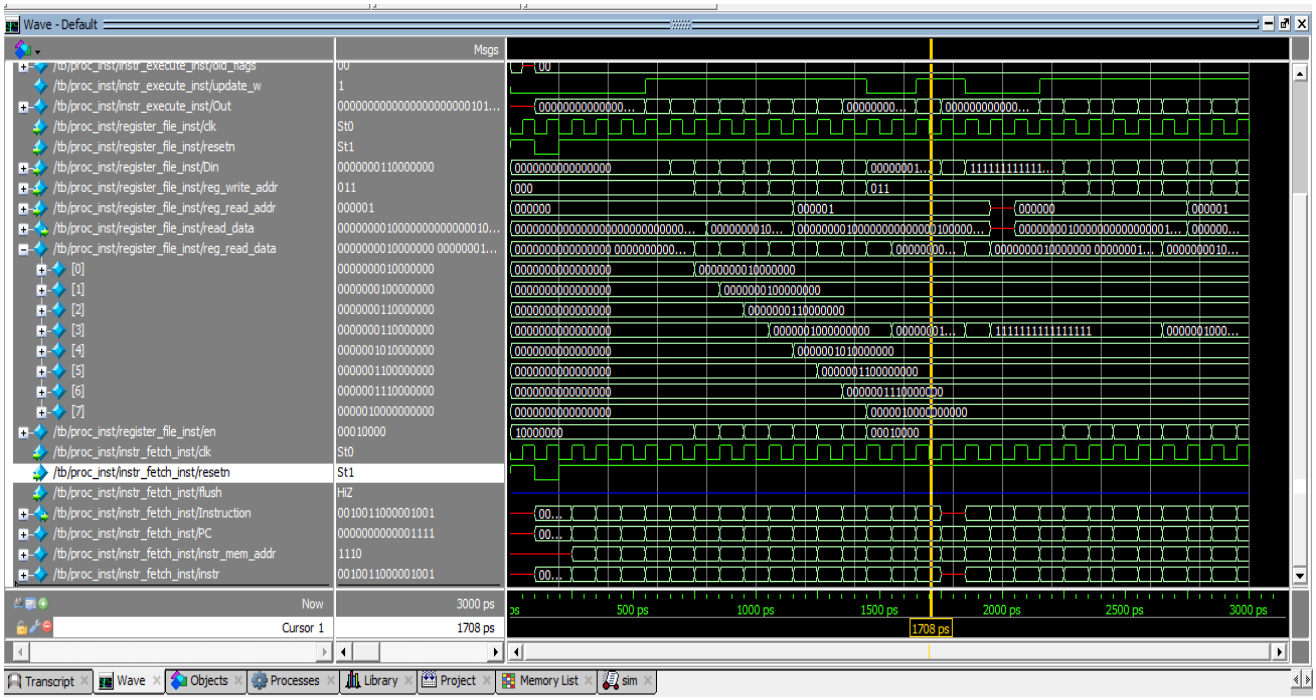


Output: -

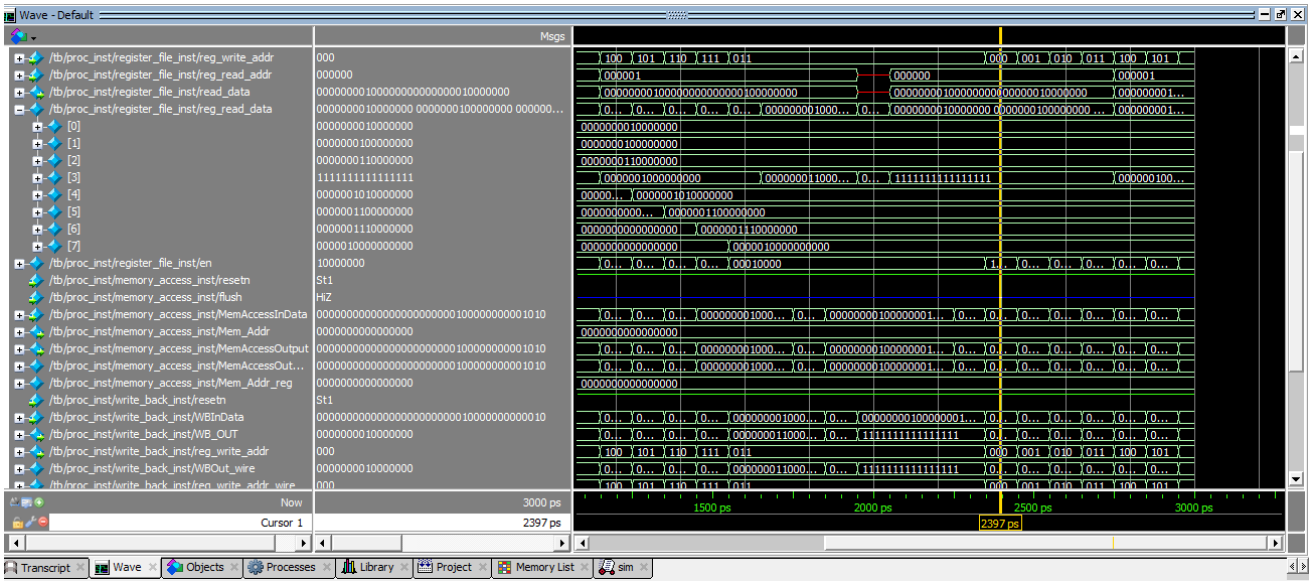


NDZ R4, R0, R1 Instruction: -

Input: -



Output: -



Completion Stage: -

The Completion Stage is mainly concerned with memory writeback. Memory writeback occurs using the store buffer via a store commit signal upon the commit of a memory store instruction. Whenever a memory writeback needs to occur, a store commit signal is enabled and the Store Buffer location for that particular instruction (obtained from the memory unit itself upon execution) is sent to the Store Buffer wherein the data and the memory address stored at the sent location is written back to the memory. This data and memory address was stored into the Store Buffer by the Memory Unit upon successful execution.

Conclusion: -

We have designed and verified the 2-way fetch superscalar processor design which is 16-bit computer, 8 registers with 16-bit each and it has been optimized by performance.