

# Assignment 2

## EE599- Accelerated Computing Using FPGA

Spring 2020

**GitHub Repo Link:**

[https://github.com/Aditya-Pharande/EE599\\_Pharande\\_2739814954](https://github.com/Aditya-Pharande/EE599_Pharande_2739814954)

- Aditya Rajendra Pharande
- USCID: 2739814954
- pharande@usc.edu

## Task 1: Barrel Shifter

Barrel shifter take  $N$  clock cycles to shift  $2^N$  elements by given shift value. We can shift input elements by 0 to  $2^N-1$  elements using an implementation similar to below where \* elements ( $2^3$ ) elements can be shifted by 0-7 elementst

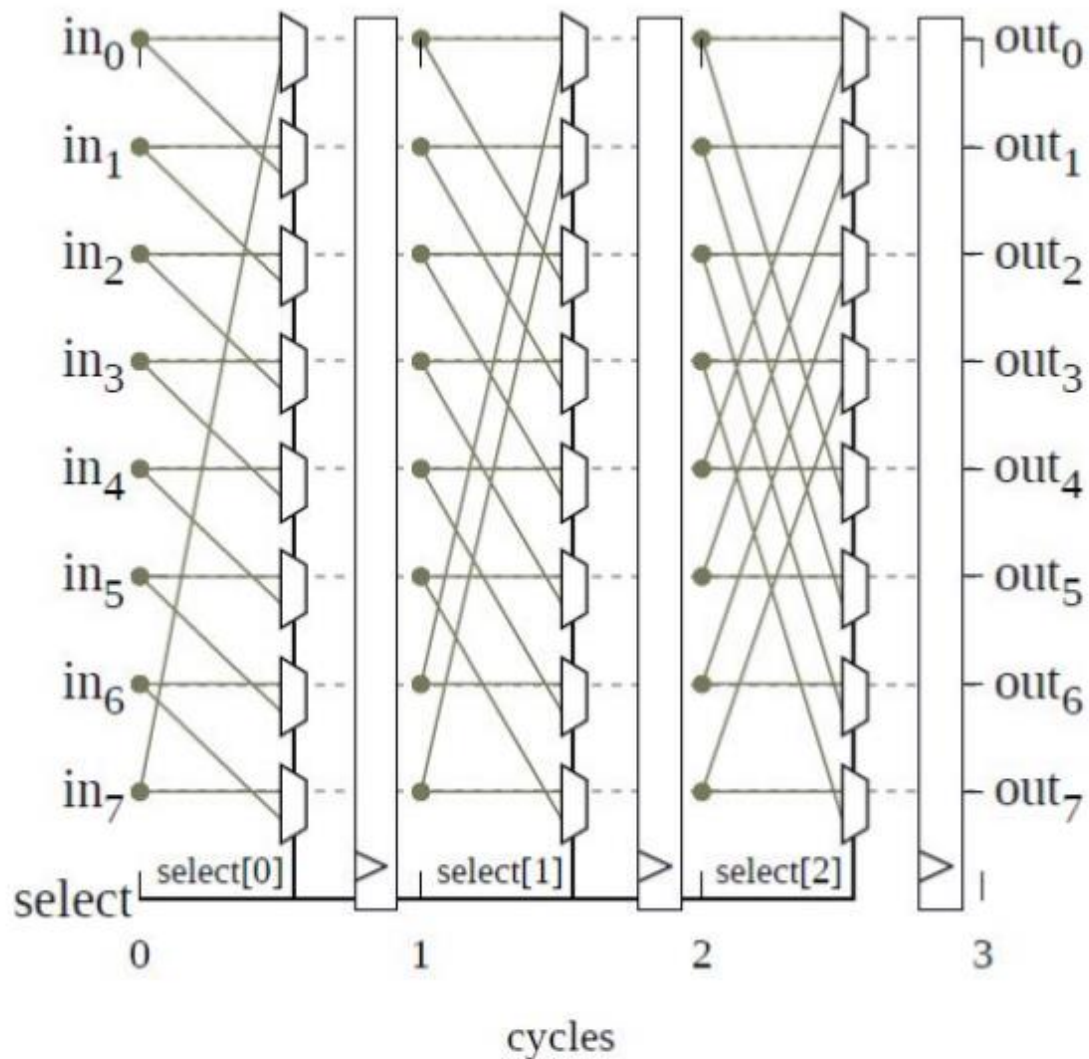
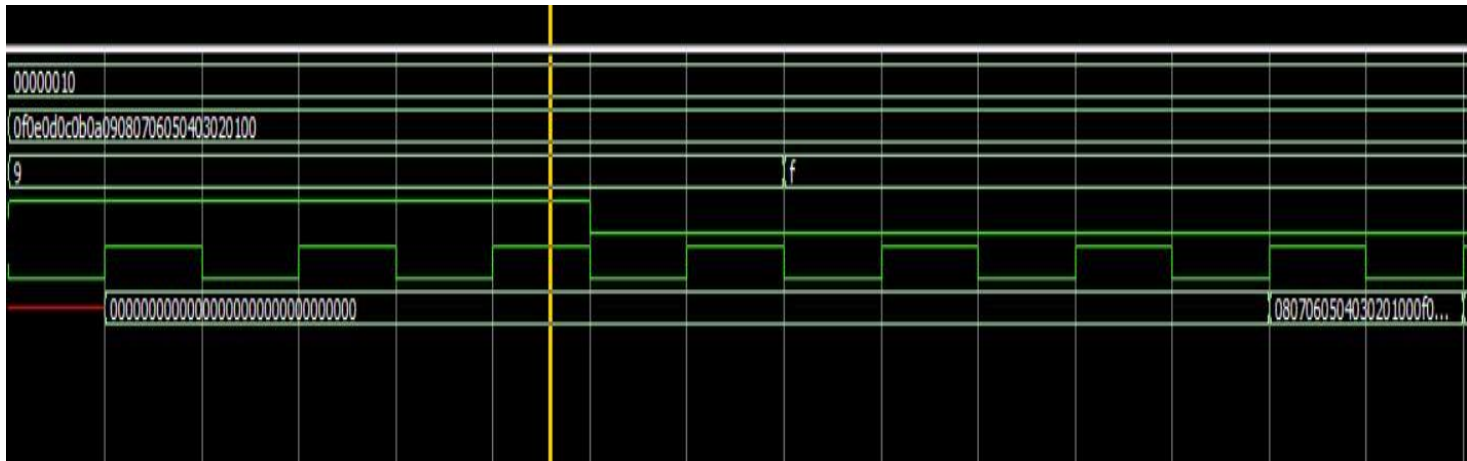


Figure 1: An Example Pipeline Barrel Shifter

## I. 16 Elements Barrel Shifter Unit:

### Simulation Result:

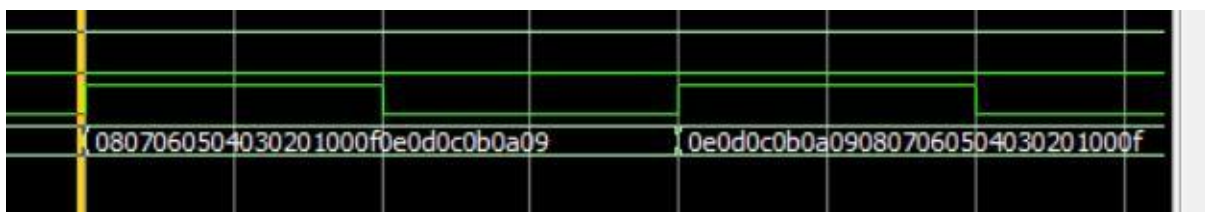
Given Input in hex = [0f, 0e, 0d, 0c, 0b, 0a, 09, 08, 07, 06, 05, 04, 03, 02, 01, 00]



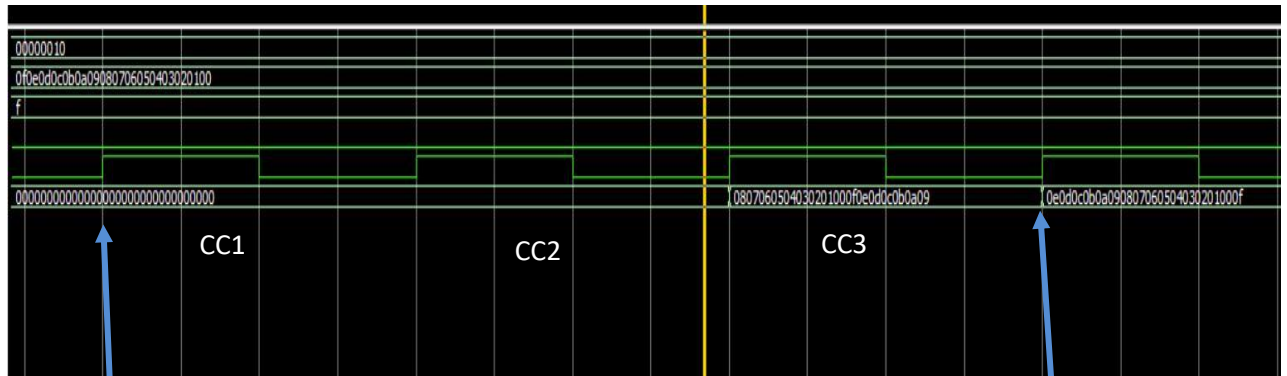
Active high reset= resets all values to zero



Two shift signals given back to back clock cycle: First was shift by 9 other was shift by 15(f)



Results gets after 3 clock cycles.



Data Getting Latch

Generated Output

### Elaborated Schematics:

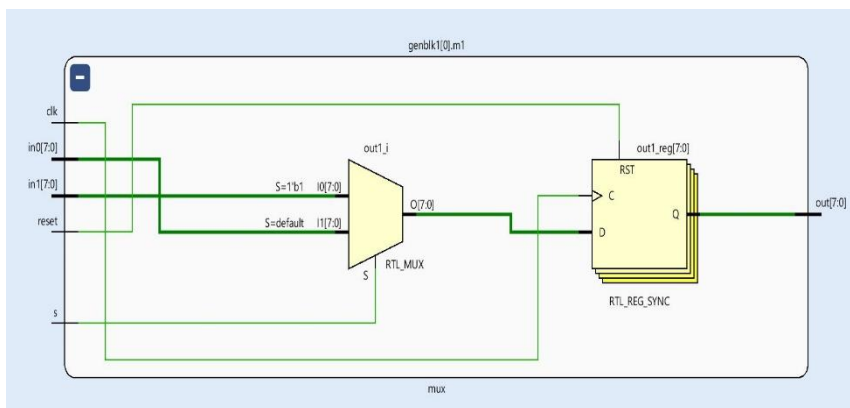


Figure 1: Mux 2\*1 Schematics

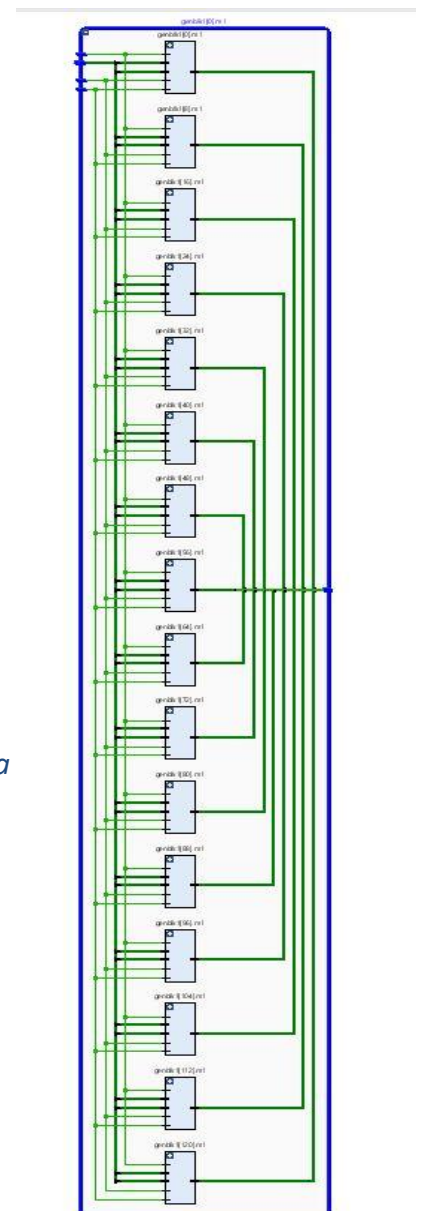


Figure 2: 16 Mux Array in a stage ->

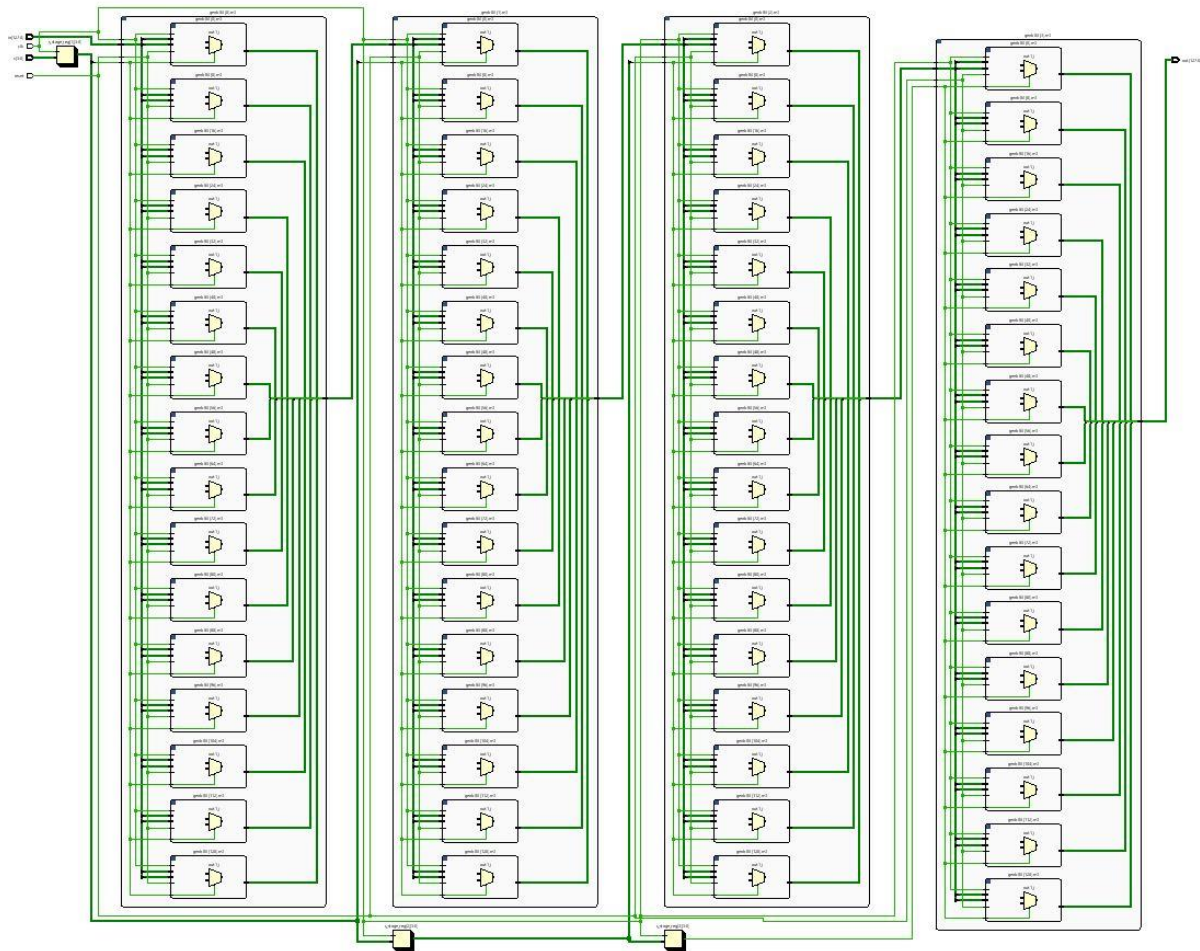


Figure 3: Barrel shifter 16 element (4 stage, each stage with 16muxes)

## Synthesized Schematics:

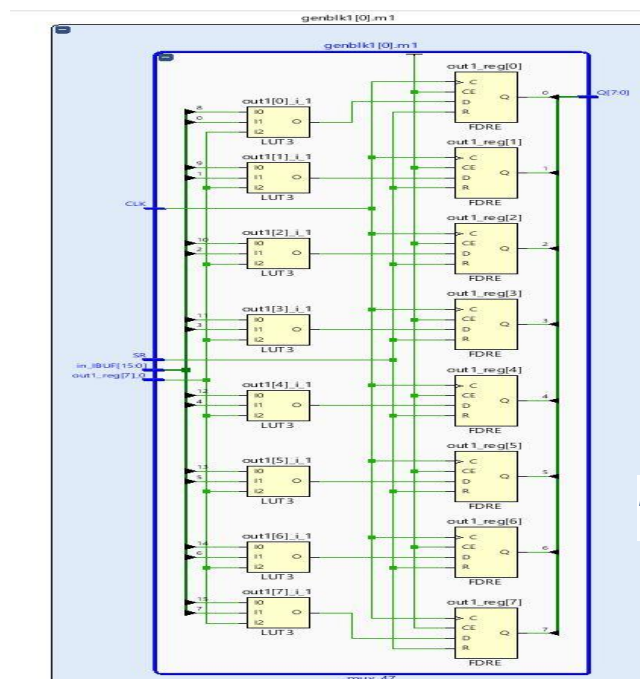


Figure 4: Mux 2\*1 synthesized schematics

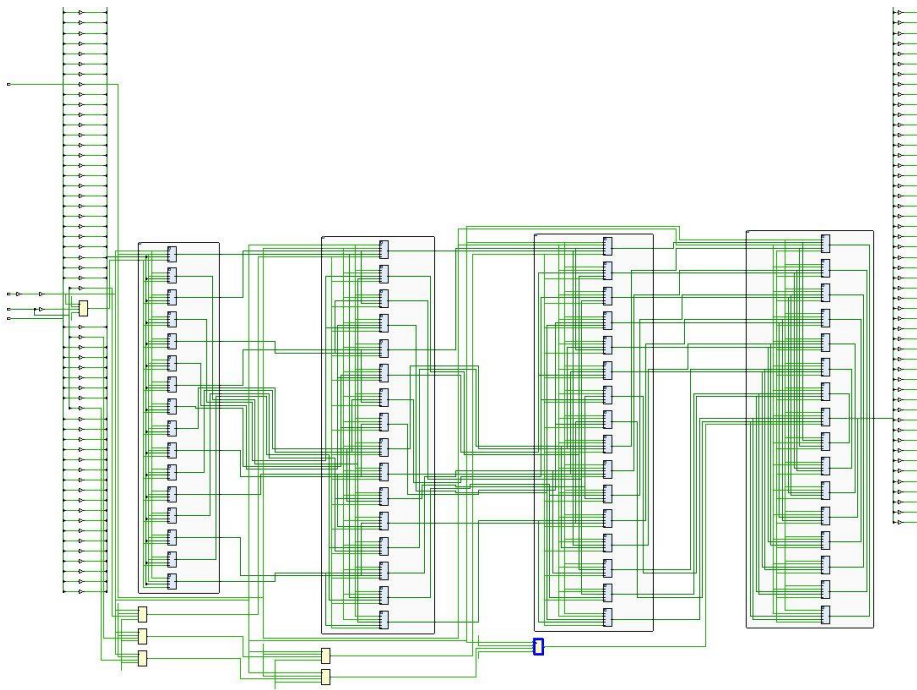


Figure 5: 16 element Barrel Shifter Synthesized Schematics

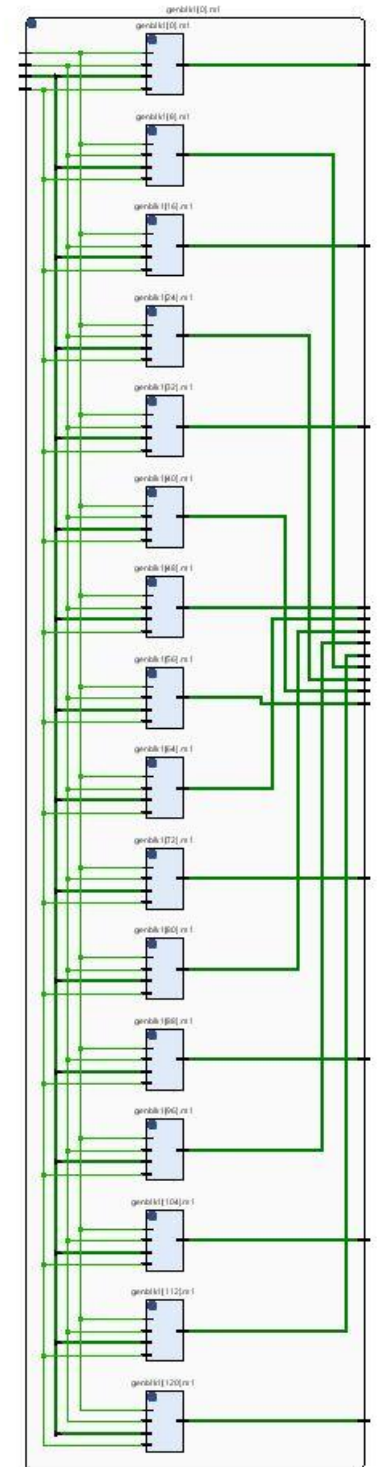


Figure 6: Mux Array in a stage of shifter



## Used Resource Estimation:

### 1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	256	0	63400	0.40
LUT as Logic	256	0	63400	0.40
LUT as Memory	0	0	19000	0.00
Slice Registers	519	0	126800	0.41
Register as Flip Flop	519	0	126800	0.41
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

### 4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	262	0	210	124.76
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

### 7. Primitives

Ref Name	Used	Functional Category
FDRE	519	Flop & Latch
LUT3	512	LUT
IBUF	134	IO
OBUF	128	IO
BUFG	1	Clock

## Timing Estimation:

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 8.293 ns	Worst Hold Slack (WHS): 0.152 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 515	Total Number of Endpoints: 515	Total Number of Endpoints: 520

All user specified timing constraints are met.

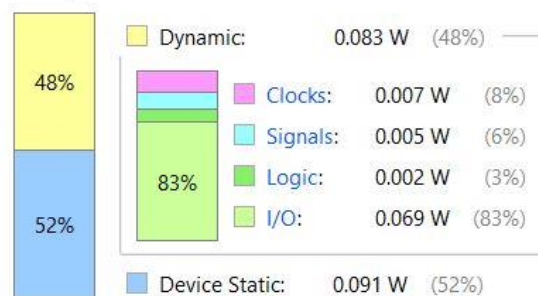
## Power Estimation:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

<b>Total On-Chip Power:</b>	<b>0.174 W</b>
<b>Design Power Budget:</b>	<b>Not Specified</b>
<b>Power Budget Margin:</b>	<b>N/A</b>
<b>Junction Temperature:</b>	<b>25.8°C</b>
Thermal Margin:	59.2°C (12.8 W)
Effective $\theta_{JA}$ :	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

### On-Chip Power





**II. 64 Element Barrel Shifter Unit:**  
**Elaborated Schematics:**

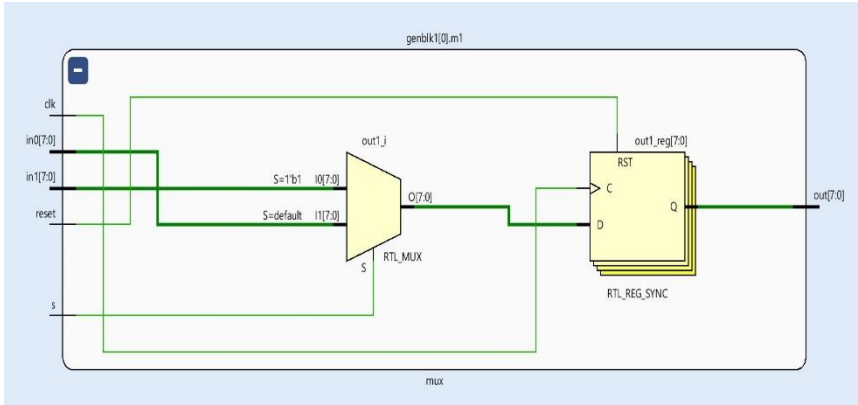


Figure 7: 2\*1 Mux Schematics

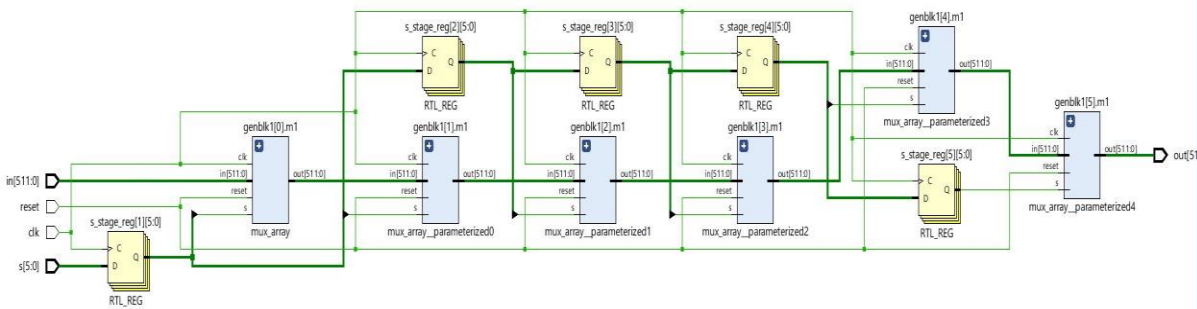
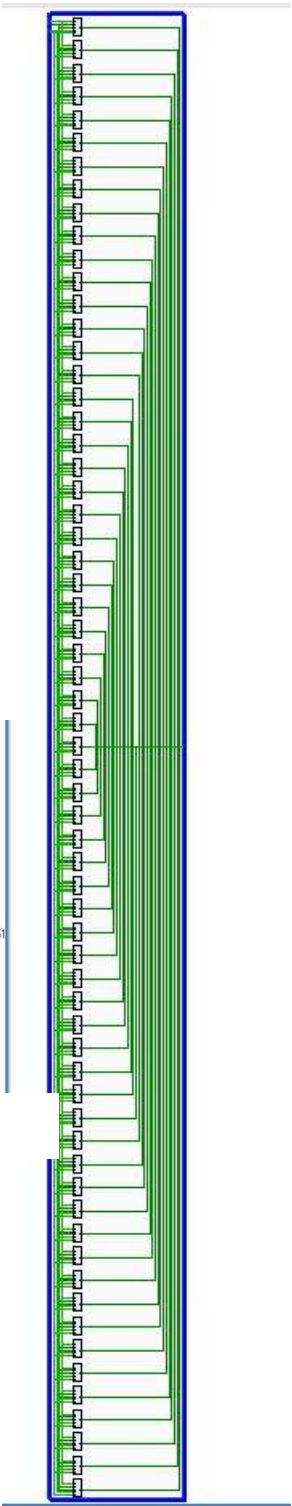


Figure 8: 64 Element barrel Shifter with 6 stages

Figure 9: 64 Muxes array in given stage ->



## Synthesized Schematics:

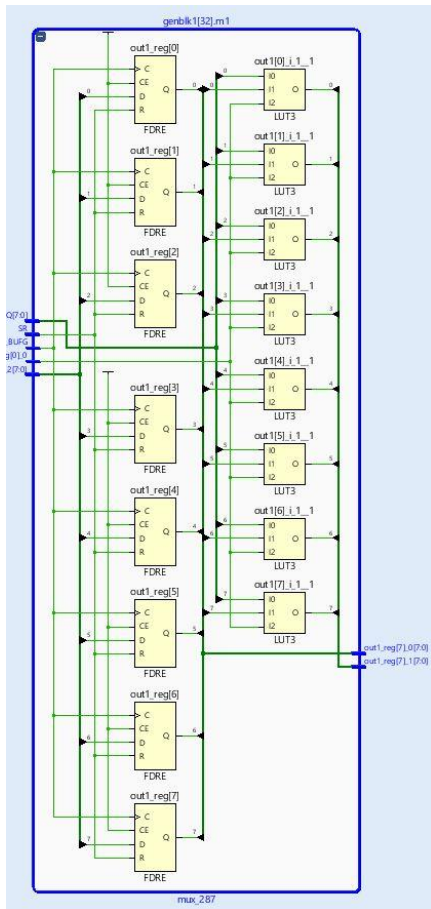


Figure 11: 2\*1 Mux synthesized schematics



Figure 10: Mux Array Synthesized Schematics

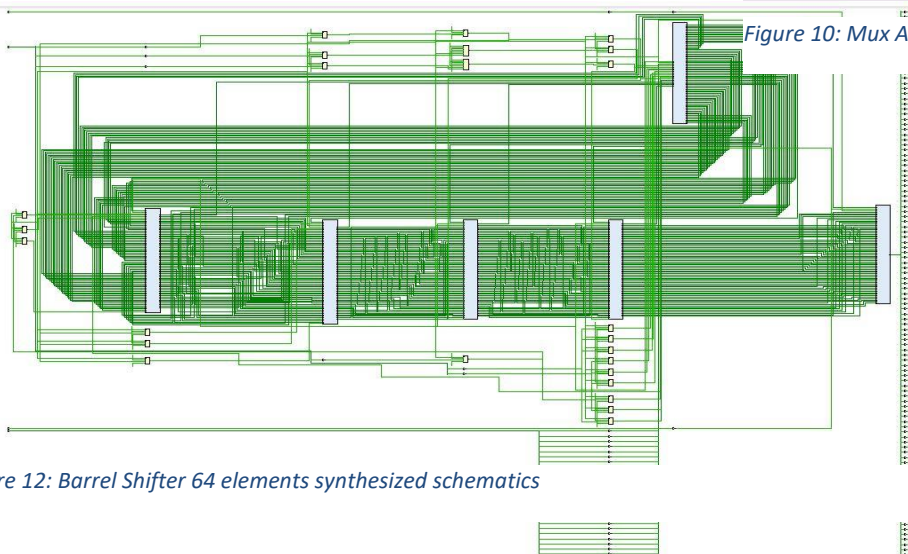


Figure 12: Barrel Shifter 64 elements synthesized schematics

## Used Resource Estimation:

### 1. Slice Logic

-----

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	1538	0	63400	2.43
LUT as Logic	1536	0	63400	2.42
LUT as Memory	2	0	19000	0.01
LUT as Distributed RAM	0	0		
LUT as Shift Register	2	0		
Slice Registers	3095	0	126800	2.44
Register as Flip Flop	3095	0	126800	2.44
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

\* Maximal LUTs and Flip Flop count after physical optimizations and full

### 4. IO and GT Specific

-----

Site Type	Used	Fixed	Available	Util%
Bonded IOB	1032	0	210	491.43
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

### 7. Primitives

-----

Ref Name	Used	Functional Category
FDRE	3095	Flop & Latch
LUT3	3072	LUT
IBUF	520	IO
OBUF	512	IO
SRL16E	2	Distributed Memory
BUFG	1	Clock

Timing Estimation:

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 8.288 ns	Worst Hold Slack (WHS): 0.079 ns	Worst Pulse Width Slack (WPWS): 4.020 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 3085	Total Number of Endpoints: 3085	Total Number of Endpoints: 3098
All user specified timing constraints are met.		

Power Estimation:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:0.486 W

Design Power Budget:Not Specified

Power Budget Margin:N/A

Junction Temperature:27.2°C

Thermal Margin:57.8°C (12.5 W)

Effective θJA:4.6°C/W

Power supplied to off-chip devices:0 W

Confidence level:Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

On-Chip Power

81%

19%

Dynamic:0.394 W (81%)

Clocks:0.028 W (7%)

Signals:0.024 W (6%)

Logic:0.015 W (4%)

I/O:0.326 W (83%)

Device Static:0.092 W (19%)

## Task 2: Systolic Array for Dense Matrix-Matrix Multiplication.

The Systolic Architecture consists of an array of processing elements, where data flows between neighboring elements, synchronously, from different directions. Processing element takes data from Top, Left, and output the results to Right, Bottom. Processing Unit for Matrix multiplication is Multiplier and Accumulator unit. Below diagram shows  $3 \times 3$  matrix multiplication systolic array. The matrix inputs must be aligned in time space properly.

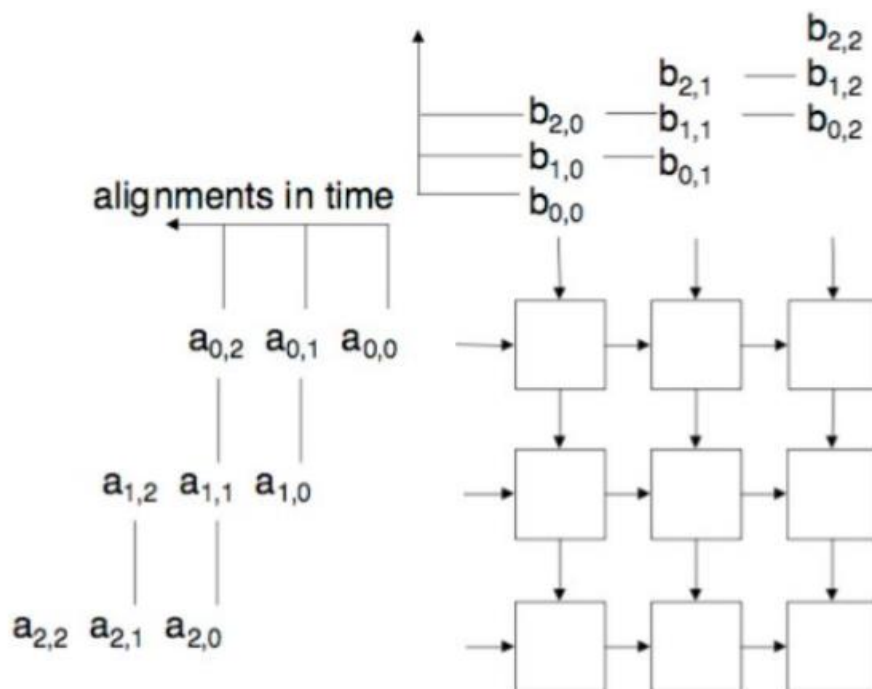


Figure 4: Example  $3 \times 3$  Systolic Array

[illegible]



Output Matrix= A\*B:

19840	23800	23664	23528	23392	23256	23120	22984	22848	22712	22576	22440	22304	22168	22032	21896
50560	58360	57968	57576	57184	56792	56400	56008	55616	55224	54832	54440	54048	53656	53264	52872
15744	27384	26736	26088	25440	24792	24144	23496	22848	22200	21552	20904	20256	19608	18960	18312
46464	61944	61040	60136	59232	58328	57424	56520	55616	54712	53808	52904	52000	51096	50192	49288
11648	30968	29808	28648	27488	26328	25168	24008	22848	21688	20528	19368	18208	17048	15888	14728
42368	65528	64112	62696	61280	59864	58448	57032	55616	54200	52784	51368	49952	48536	47120	45704
7552	34552	32880	31208	29536	27864	26192	24520	22848	21176	19504	17832	16160	14488	12816	11144
38272	3576	1648	65256	63328	61400	59472	57544	55616	53688	51760	49832	47904	45976	44048	42120
3456	38136	35952	33768	31584	29400	27216	25032	22848	20664	18480	16296	14112	11928	9744	7560
34176	7160	4720	2280	65376	62936	60496	58056	55616	53176	50736	48296	45856	43416	40976	38536
64896	41720	39024	36328	33632	30936	28240	25544	22848	20152	17456	14760	12064	9368	6672	3976
30080	10744	7792	4840	1888	64472	61520	58568	55616	52664	49712	46760	43808	40856	37904	34952
60800	45304	42096	38888	35680	32472	29264	26056	22848	19640	16432	13224	10016	6808	3600	392
25984	14328	10864	7400	3936	472	62544	59080	55616	52152	48688	45224	41760	38296	34832	31368
56704	48888	45168	41448	37728	34008	30288	26568	22848	19128	15408	11688	7968	4248	528	62344
21888	18168	14448	10728	7008	3288	65104	61384	57664	53944	50224	46504	42784	39064	35344	31624

Note: Since each element of output matrix has 2N bit space , there can be possibility of overflow.

Output from Verilog Code:

Matrix A:

/tb_systolic_array/MatA	{8'd1 8'd2 8'd3 8'd...	{1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16} {17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32}
[0]	8'd1 8'd2 8'd3 8'd...	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
[1]	8'd17 8'd18 8'd19 ...	17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
[2]	8'd33 8'd34 8'd35 ...	33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48
[3]	8'd49 8'd50 8'd51 ...	49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64
[4]	8'd65 8'd66 8'd67 ...	65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80
[5]	8'd81 8'd82 8'd83 ...	81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96
[6]	8'd97 8'd98 8'd99 ...	97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112
[7]	8'd113 8'd114 8'd...	113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128
[8]	8'd129 8'd130 8'd...	129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144
[9]	8'd145 8'd146 8'd...	145 146 147 148 149 150 151 152 153 154 155 156 157 158 159 160
[10]	8'd161 8'd162 8'd...	161 162 163 164 165 166 167 168 169 170 171 172 173 174 175 176
[11]	8'd177 8'd178 8'd...	177 178 179 180 181 182 183 184 185 186 187 188 189 190 191 192
[12]	8'd193 8'd194 8'd...	193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208
[13]	8'd209 8'd210 8'd...	209 210 211 212 213 214 215 216 217 218 219 220 221 222 223 224
[14]	8'd225 8'd226 8'd...	225 226 227 228 229 230 231 232 233 234 235 236 237 238 239 240
[15]	8'd241 8'd242 8'd...	241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 0
/tb_systolic_array/MatB	{8'd16 8'd15 8'd1...	{16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1} {32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1}
/tb_systolic_array/MatOut	{16'd19840 16'd2...	{19840 23800 23664 23528 23392 23256 23120 22984 22848 22712 22576 22440 22304 22168 22032 21896 21760 21624 21488 21352 21216 21080 20944 20808 20672 20536 20400 20264 20128 20000 19864 19728 19592 19456 19320 19184 19048 18912 18776 18640 18504 18368 18232 18096 17960 17824 17688 17552 17416 17280 17144 17008 16872 16736 16600 16464 16328 16192 16056 15920 15784 15648 15512 15376 15240 15104 14968 14832 14696 14560 14424 14288 14152 14016 13880 13744 13608 13472 13336 13200 13064 12928 12792 12656 12520 12384 12248 12112 11976 11840 11704 11568 11432 11296 11160 11024 10888 10752 10616 10480 10344 10208 10072 9936 9800 9664 9528 9392 9256 9120 8984 8848 8712 8576 8440 8304 8168 8032 7896 7760 7624 7488 7352 7216 7080 6944 6808 6672 6536 6400 6264 6128 5992 5856 5720 5584 5448 5312 5176 5040 4904 4768 4632 4496 4360 4224 4088 3952 3816 3680 3544 3408 3272 3136 3000 2864 2728 2592 2456 2320 2184 2048 1912 1776 1640 1504 1368 1232 1096 960 824 688 552 416 280 144 0}

## Matrix B:

/tb_systolic_array/MatA	{8'd1 8'd2 8'd3 8'...	{1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16} {17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32} {
/tb_systolic_array/MatB	{8'd16 8'd15 8'd1...	{16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1} {32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17} {
[0]	8'd16 8'd15 8'd14 ...	16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
[1]	8'd32 8'd31 8'd30 ...	32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17
[2]	8'd48 8'd47 8'd46 ...	48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33
[3]	8'd64 8'd63 8'd62 ...	64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49
[4]	8'd80 8'd79 8'd78 ...	80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65
[5]	8'd96 8'd95 8'd94 ...	96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81
[6]	8'd112 8'd111 8'd...	112 111 110 109 108 107 106 105 104 103 102 101 100 99 98 97
[7]	8'd128 8'd127 8'd...	128 127 126 125 124 123 122 121 120 119 118 117 116 115 114 113
[8]	8'd144 8'd143 8'd...	144 143 142 141 140 139 138 137 136 135 134 133 132 131 130 129
[9]	8'd160 8'd159 8'd...	160 159 158 157 156 155 154 153 152 151 150 149 148 147 146 145
[10]	8'd176 8'd175 8'd...	176 175 174 173 172 171 170 169 168 167 166 165 164 163 162 161
[11]	8'd192 8'd191 8'd...	192 191 190 189 188 187 186 185 184 183 182 181 180 179 178 177
[12]	8'd208 8'd207 8'd...	208 207 206 205 204 203 202 201 200 199 198 197 196 195 194 193
[13]	8'd224 8'd223 8'd...	224 223 222 221 220 219 218 217 216 215 214 213 212 211 210 209
[14]	8'd240 8'd239 8'd...	240 239 238 237 236 235 234 233 232 231 230 229 228 227 226 225
[15]	8'd0 8'd255 8'd25...	0 255 254 253 252 251 250 249 248 247 246 245 244 243 242 241
/tb_systolic_array/MatOut	{16'd19840 16'd2...	{19840 23800 23664 23528 23392 23256 23120 22984 22848 22712 22576 22440 22304 22168 22032 21896} {50560 58360 57920 57480 57040 56600 56160 55720 55280 54840 54400 53960 53520 53080 52640 52200 51760 51320 50880 50440 50000 49560 49120 48680 48240 47800 47360 46920 46480 46040 45600 45160 44720 44280 43840 43400 42960 42520 42080 41640 41200 40760 40320 39880 39440 39000 38560 38120 37680 37240 36800 36360 35920 35480 35040 34600 34160 33720 33280 32840 32400 31960 31520 31080 30640 30200 29760 29320 28880 28440 28000 27560 27120 26680 26240 25800 25360 24920 24480 24040 23600 23160 22720 22280 21840 21400 20960 20520 20080 19640 19200 18760 18320 17880 17440 17000 16560 16120 15680 15240 14800 14360 13920 13480 13040 12600 12160 11720 11280 10840 10400 9960 9520 9080 8640 8200 7760 7320 6880 6440 6000 5560 5120 4680 4240 3800 3360 2920 2480 2040 1600 1160 720 280 160 80 40 20 10 5 2 1 0

## Output Matrix= A\*B:

/tb_systolic_array/clock	1'd1	
/tb_systolic_array/reset	1'd0	
/tb_systolic_array/MatA	{8'd1 8'd2 8'd3 8'...	{1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16} {17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32} {33 34 35 36 37 38 39 40 41 42 43 44 45
/tb_systolic_array/MatB	{8'd16 8'd15 8'd1...	{16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1} {32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17} {48 47 46 45 44 43 42 41 40 39 38 37 36
/tb_systolic_array/MatOut	{16'd19840 16'd2...	{19840 23800 23664 23528 23392 23256 23120 22984 22848 22712 22576 22440 22304 22168 22032 21896} {50560 58360 57920 57480 57040 56600 56160 55720 55280 54840 54400 53960 53520 53080 52640 52200 51760 51320 50880 50440 50000 49560 49120 48680 48240 47800 47360 46920 46480 46040 45600 45160 44720 44280 43840 43400 42960 42520 42080 41640 41200 40760 40320 39880 39440 39000 38560 38120 37680 37240 36800 36360 35920 35480 35040 34600 34160 33720 33280 32840 32400 31960 31520 31080 30640 30200 29760 29320 28880 28440 28000 27560 27120 26680 26240 25800 25360 24920 24480 24040 23600 23160 22720 22280 21840 21400 20960 20520 20080 19640 19200 18760 18320 17880 17440 17000 16560 16120 15680 15240 14800 14360 13920 13480 13040 12600 12160 11720 11280 10840 10400 9960 9520 9080 8640 8200 7760 7320 6880 6440 6000 5560 5120 4680 4240 3800 3360 2920 2480 2040 1600 1160 720 280 160 80 40 20 10 5 2 1 0
[0]	16'd19840 16'd2...	19840 23800 23664 23528 23392 23256 23120 22984 22848 22712 22576 22440 22304 22168 22032 21896
[1]	16'd50560 16'd5...	50560 58360 57920 57480 57040 56600 56160 55720 55280 54840 54400 53960 53520 53080 52640 52200 51760 51320 50880 50440 50000 49560 49120 48680 48240 47800 47360 46920 46480 46040 45600 45160 44720 44280 43840 43400 42960 42520 42080 41640 41200 40760 40320 39880 39440 39000 38560 38120 37680 37240 36800 36360 35920 35480 35040 34600 34160 33720 33280 32840 32400 31960 31520 31080 30640 30200 29760 29320 28880 28440 28000 27560 27120 26680 26240 25800 25360 24920 24480 24040 23600 23160 22720 22280 21840 21400 20960 20520 20080 19640 19200 18760 18320 17880 17440 17000 16560 16120 15680 15240 14800 14360 13920 13480 13040 12600 12160 11720 11280 10840 10400 9960 9520 9080 8640 8200 7760 7320 6880 6440 6000 5560 5120 4680 4240 3800 3360 2920 2480 2040 1600 1160 720 280 160 80 40 20 10 5 2 1 0
[2]	16'd15744 16'd2...	15744 27384 26736 26088 25440 24792 24144 23496 22848 22200 21552 20904 20256 19608 18960 18312
[3]	16'd46464 16'd6...	46464 61944 61040 60136 59232 58328 57424 56520 55616 54712 53808 52904 52000 51096 50192 49288
[4]	16'd11648 16'd3...	11648 30968 29808 28648 27488 26328 25168 24008 22848 21688 20528 19368 18208 17048 15888 14728
[5]	16'd42368 16'd6...	42368 65528 64112 62696 61280 59864 58448 57032 55616 54200 52784 51368 49952 48536 47120 45704
[6]	16'd7552 16'd34...	7552 34552 32880 31208 29536 27864 26192 24520 22848 21176 19504 17832 16160 14488 12816 11144
[7]	16'd38272 16'd3...	38272 3576 1648 65256 63328 61400 59472 57544 55616 53688 51760 49832 47904 45976 44048 42120
[8]	16'd3456 16'd38...	3456 38136 35952 33768 31584 29400 27216 25032 22848 20664 18480 16296 14112 11928 9744 7560
[9]	16'd34176 16'd7...	34176 7160 4720 2280 65376 62936 60496 58056 55616 53176 50736 48296 45856 43416 40976 38536
[10]	16'd64896 16'd4...	64896 41720 39024 36328 33632 30936 28240 25544 22848 20152 17456 14760 12064 9368 6672 3976
[11]	16'd30080 16'd1...	30080 10744 7792 4840 1888 64472 61520 58568 55616 52664 49712 46760 43808 40856 37904 34952
[12]	16'd60800 16'd4...	60800 45304 42096 38888 35680 32472 29264 26056 22848 19640 16432 13224 10016 6808 3600 392
[13]	16'd25984 16'd1...	25984 14328 10864 7400 3936 472 62544 59080 55616 52152 48688 45224 41760 38296 34832 31368
[14]	16'd56704 16'd4...	56704 48888 45168 41448 37728 34008 30288 26568 22848 19128 15408 11688 7968 4248 528 62344
[15]	16'd21888 16'd1...	21888 18168 14448 10728 7008 3288 65104 61384 57664 53944 50224 46504 42784 39064 35344 31624



## Elaborated Schematics:

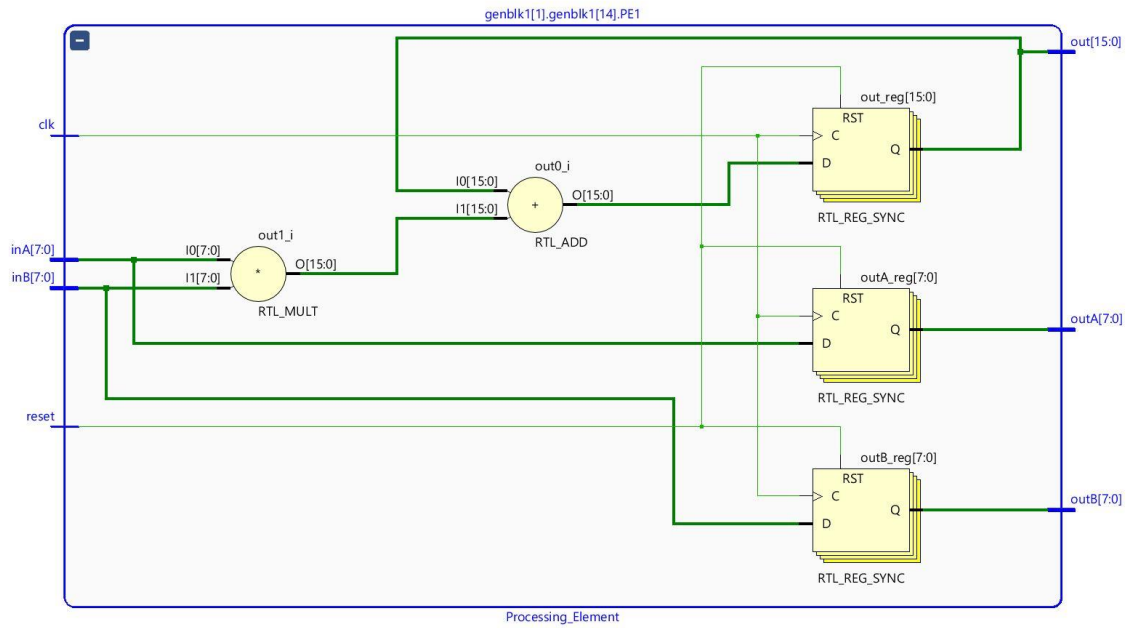


Figure 13: Processing Element (MAC) Schematics

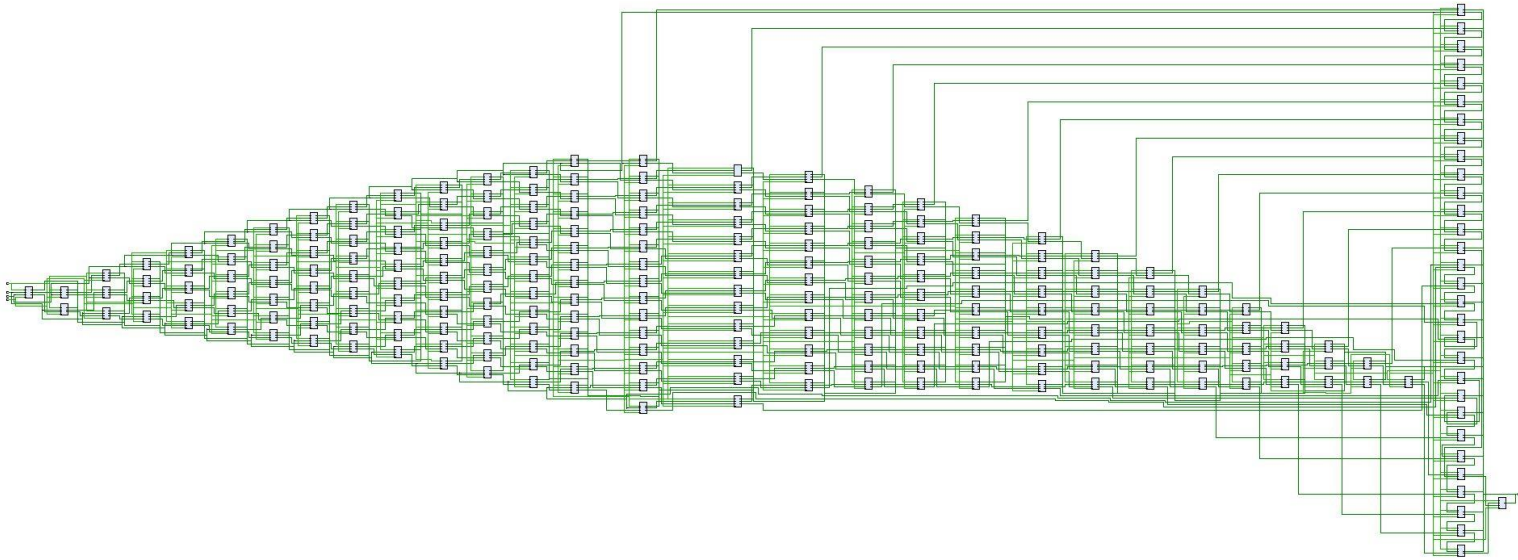


Figure 14: Systolic array for 16\*16 matrix multiplication. Total 256 PE

## **Synthesized Schematics:**

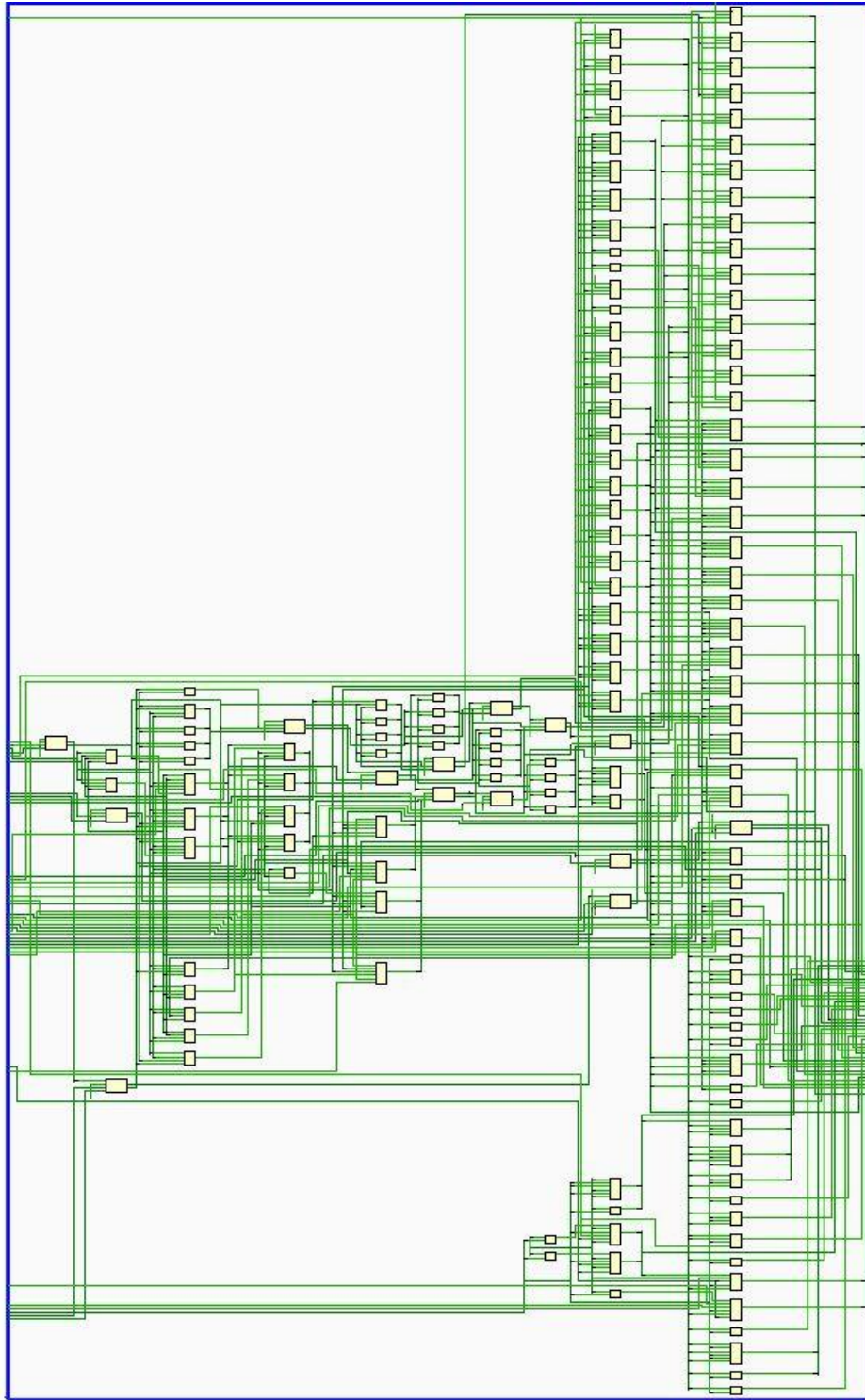
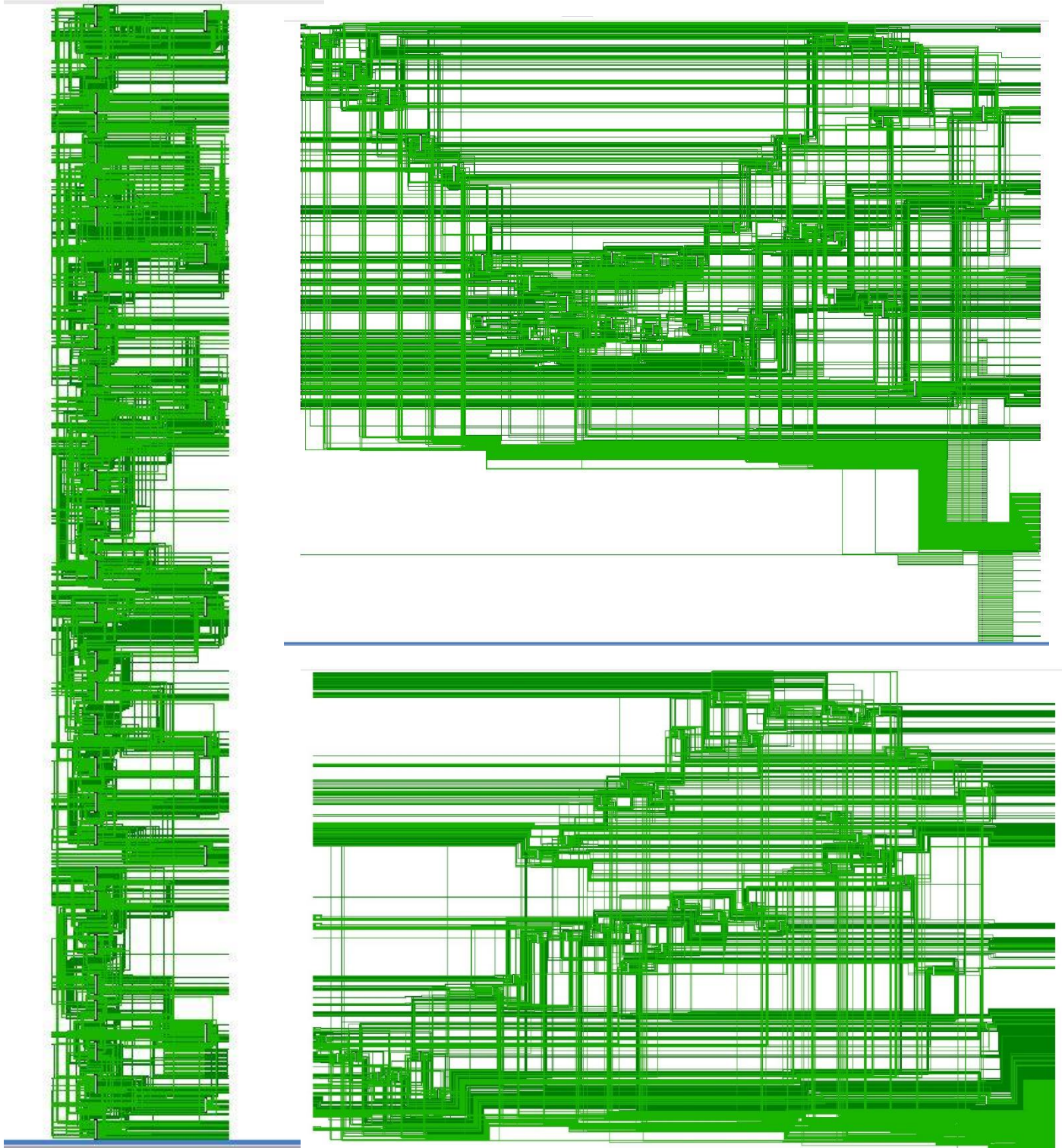


Figure 15: Synthesized PE Schematics



*Figure 16 Parts of Synthesized Schematics of Systolic Array*

## Used Resource Estimation:

### 1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	22258	0	63400	35.11
LUT as Logic	22258	0	63400	35.11
LUT as Memory	0	0	19000	0.00
Slice Registers	7936	0	126800	6.26
Register as Flip Flop	7936	0	126800	6.26
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

### 4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	4354	0	210	2073.33
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

### 7. Primitives

Ref Name	Used	Functional Category
LUT2	9728	LUT
LUT6	9098	LUT
FDRE	7936	Flop & Latch
OBUF	4096	IO
LUT4	4096	LUT
CARRY4	3584	CarryLogic
LUT5	2304	LUT
LUT3	630	LUT
IBUF	258	IO
BUFG	1	Clock



Timing Estimation:

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 2.580 ns	Worst Hold Slack (WHS): 0.118 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 7680	Total Number of Endpoints: 7680	Total Number of Endpoints: 7937

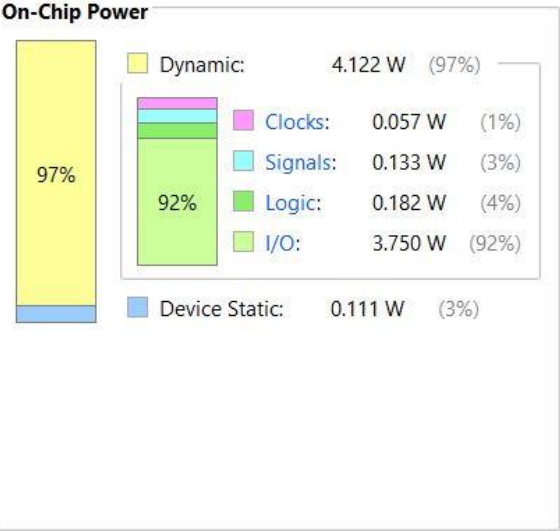
All user specified timing constraints are met.

Power Estimation:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	4.233 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	44.3°C
Thermal Margin:	40.7°C (8.8 W)
Effective $\theta$ JA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



# I. 32\*32 Matrix Multiplication

## Elaborated Schematics:

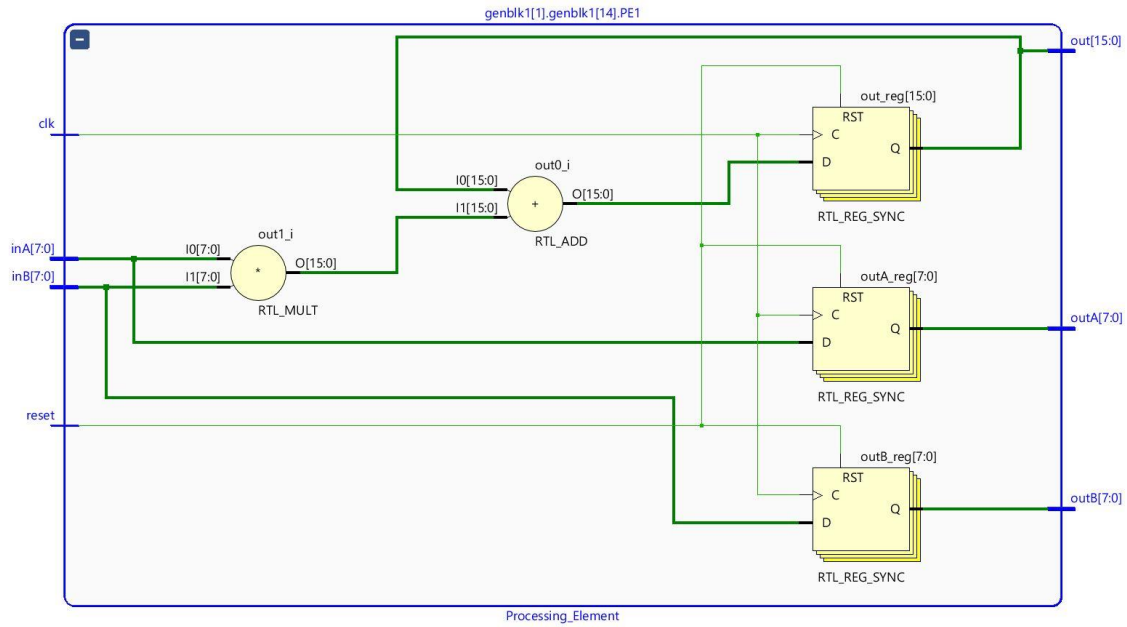


Figure 17: Processing Element (MAC) Schematics

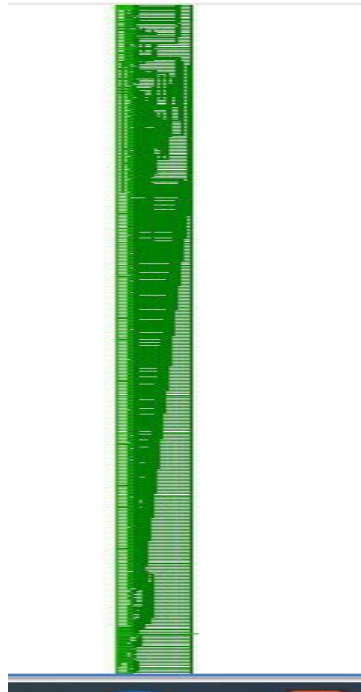


Figure 18: Systolic array for 32\*32 matrix multiplication. Total 1024 PE

## **Synthesized Schematics:**

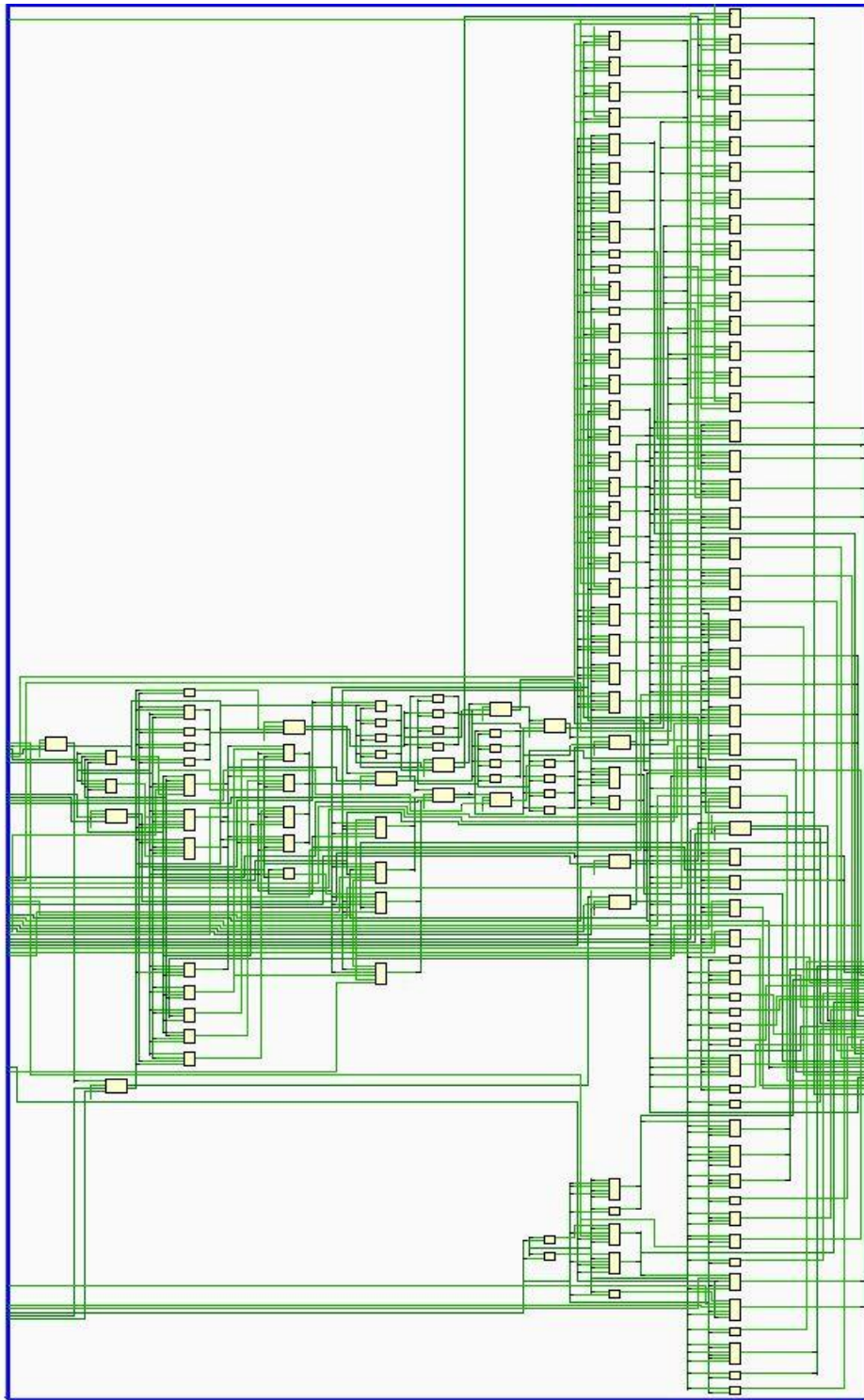
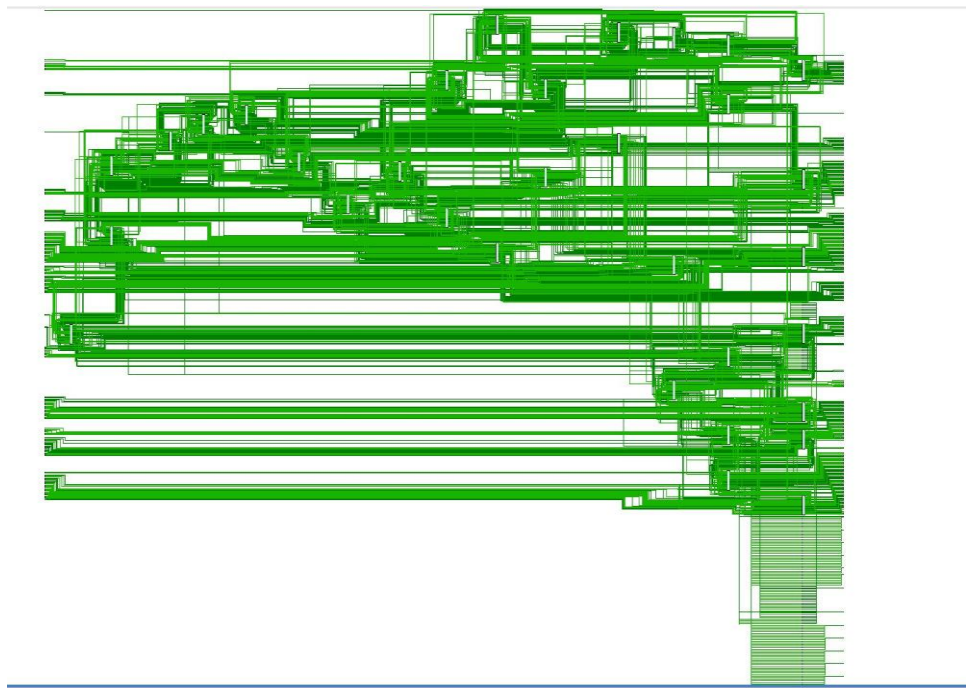
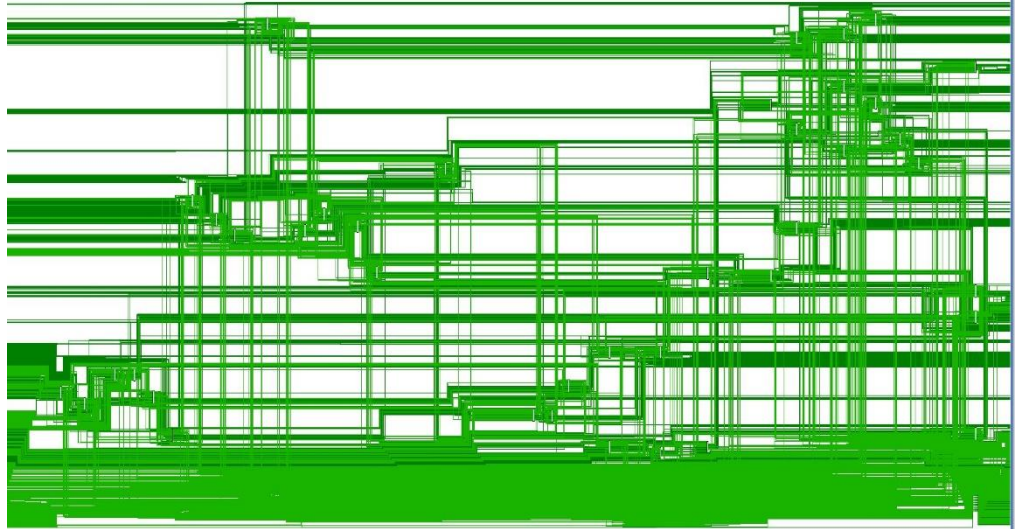
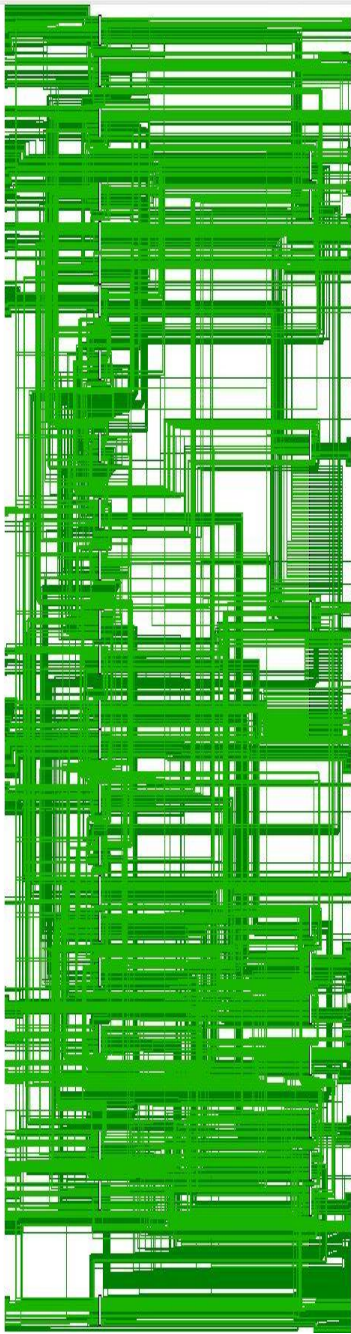


Figure 19: Synthesized PE Schematics



*Figure 20 Parts of Synthesized Schematics of Systolic Array*

## Used Resource Estimation:

### 1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	90048	0	63400	142.03
LUT as Logic	90048	0	63400	142.03
LUT as Memory	0	0	19000	0.00
Slice Registers	32256	0	126800	25.44
Register as Flip Flop	32256	0	126800	25.44
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

### 4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	16898	0	210	8046.67
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

### 7. Primitives

Ref Name	Used	Functional Category
LUT2	40960	LUT
LUT6	37888	LUT
FDRE	32256	Flop & Latch
LUT4	21504	LUT
OBUF	16384	IO
CARRY4	14336	CarryLogic
LUT3	4096	LUT
LUT5	3072	LUT
IBUF	514	IO
BUFG	1	Clock



## Timing Estimation:

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 2.641 ns	Worst Hold Slack (WHS): 0.118 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 31744	Total Number of Endpoints: 31744	Total Number of Endpoints: 32257

All user specified timing constraints are met.

## Power Estimation:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

<b>Total On-Chip Power:</b>	<b>16.817 W (Junction temp exceeded!)</b>
<b>Design Power Budget:</b>	<b>Not Specified</b>
<b>Power Budget Margin:</b>	<b>N/A</b>
<b>Junction Temperature:</b>	<b>101.7°C</b>
Thermal Margin:	-16.7°C (-3.5 W)
Effective $\theta_{JA}$ :	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

### On-Chip Power

