Assignment 2

EE599- Accelerated Computing Using FPGA

Spring 2020

GitHub Repo Link:

https://github.com/Aditya-Pharande/EE599_Pharande_2739814954

- Aditya Rajendra Pharande
- USCID: 2739814954
- pharande@usc.edu

Task 1: Barrel Shifter

Barrel shifter take N clock cycles to shift 2^N elements by given shift value. We can shift input elements by 0 to 2^N-1 elements using an implementation similar to below where * elements (2^3) elements can be shifted by 0-7 elemenst

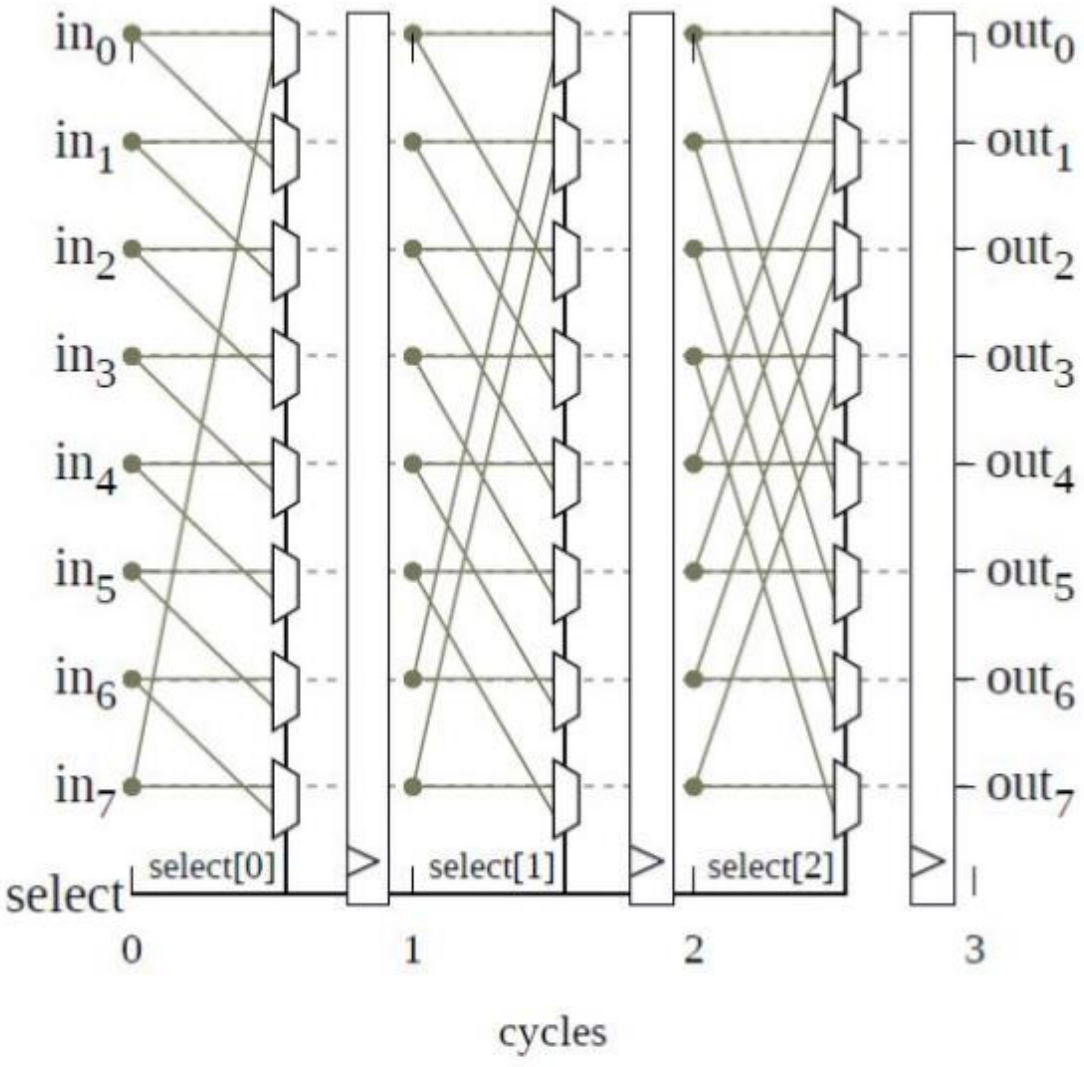
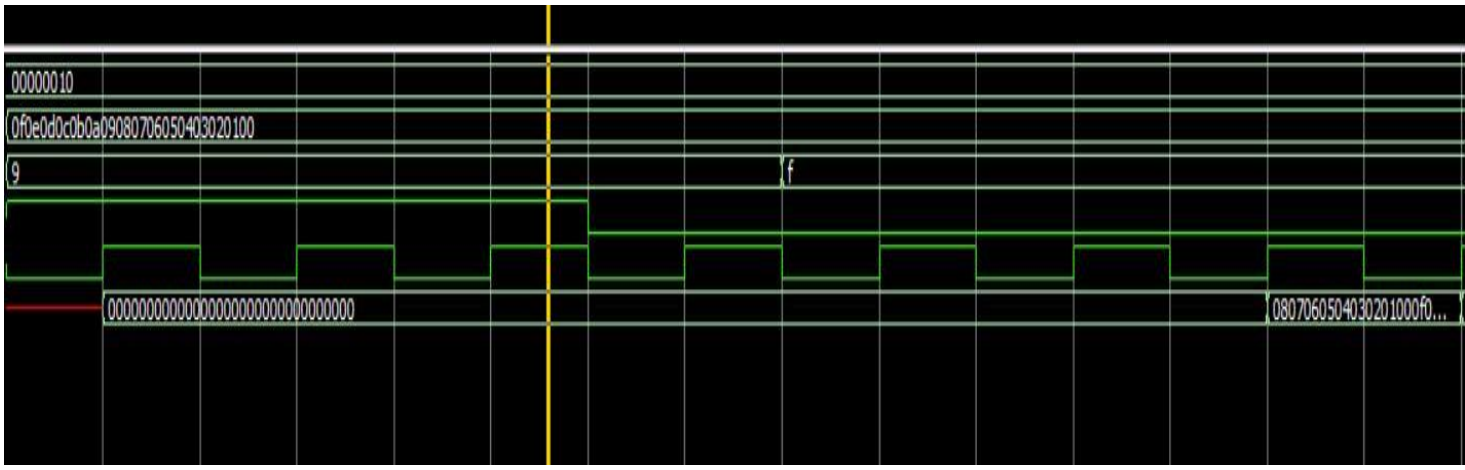


Figure 1: An Example Pipeline Barrel Shifter

I. 16 Elements Barrel Shifter Unit:

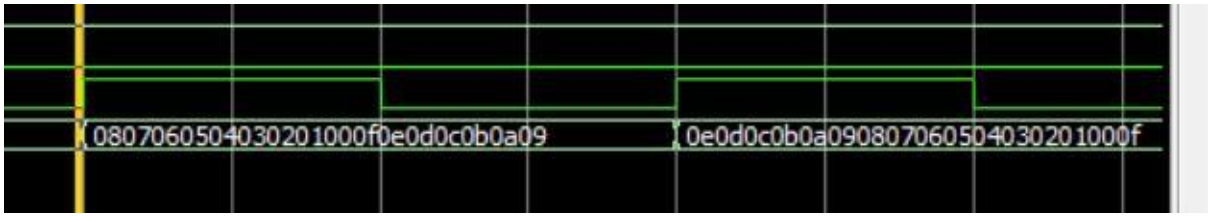
Simulation Result:

Given Input in hex = [0f, 0e, 0d, 0c, 0b, 0a, 09, 08, 07, 06,05,04,03,02,01 ,00]

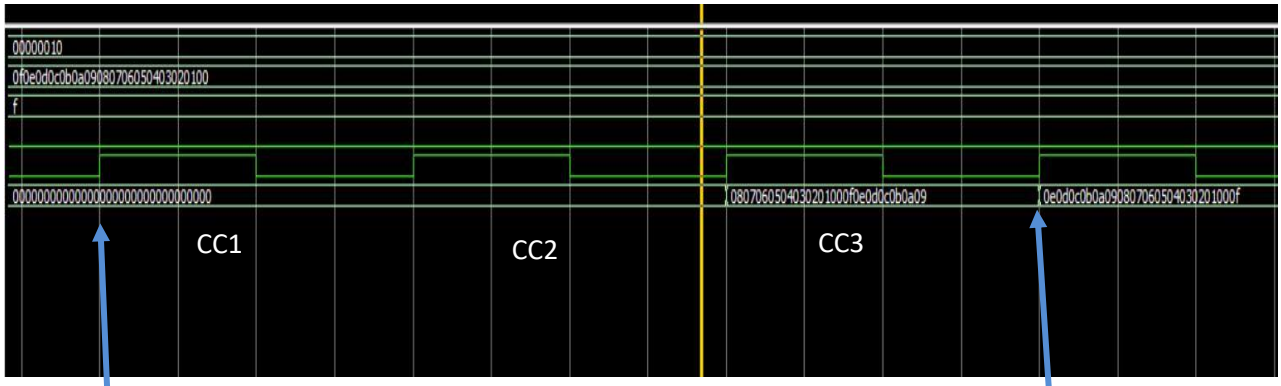


Active high reset= resets all values to zero

Two shift signals given back to back clock cycle: First was shift by 9 other was shift by 15(f)



Results gets after 3 clock cycles.



Data Getting Latch

Generated Output

Elaborated Schematics:

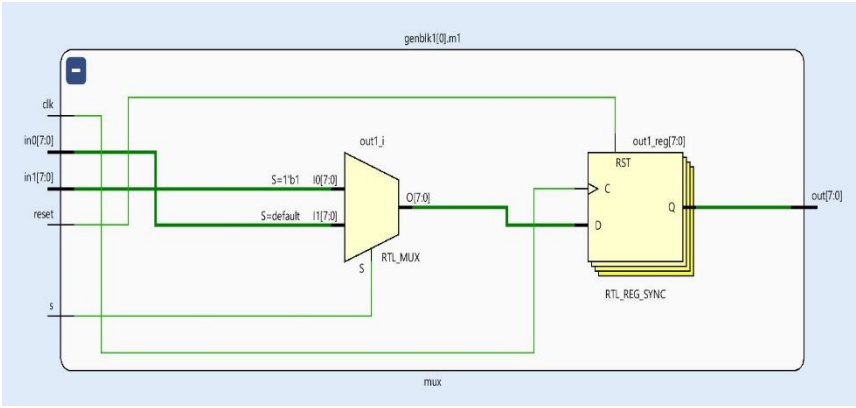
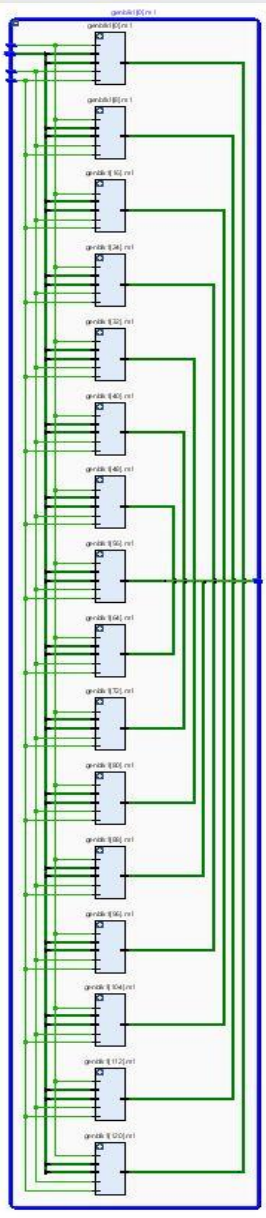


*Figure 1: Mux 2*1 Schematics*

Figure 2: 16 Mux Array in a stage ->



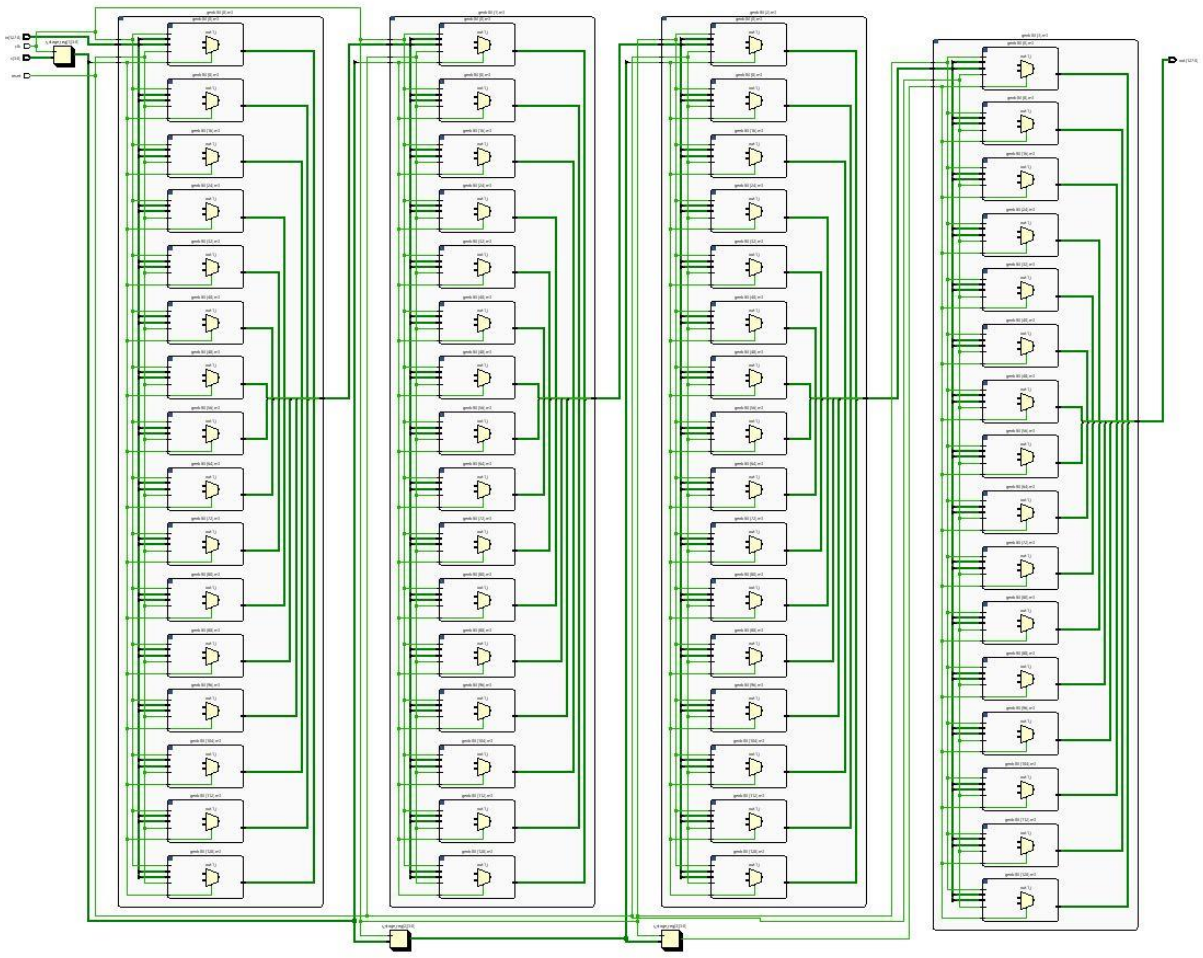


Figure 3: Barrel shifter 16 element (4 stage, each stage with 16muxes)

Synthesized Schematics:

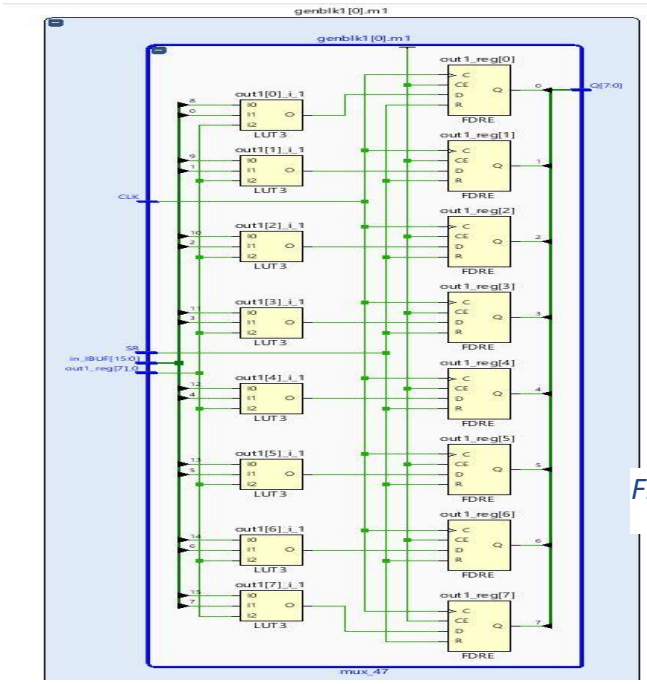


*Figure 4: Mux 2*1 synthesized schematics*

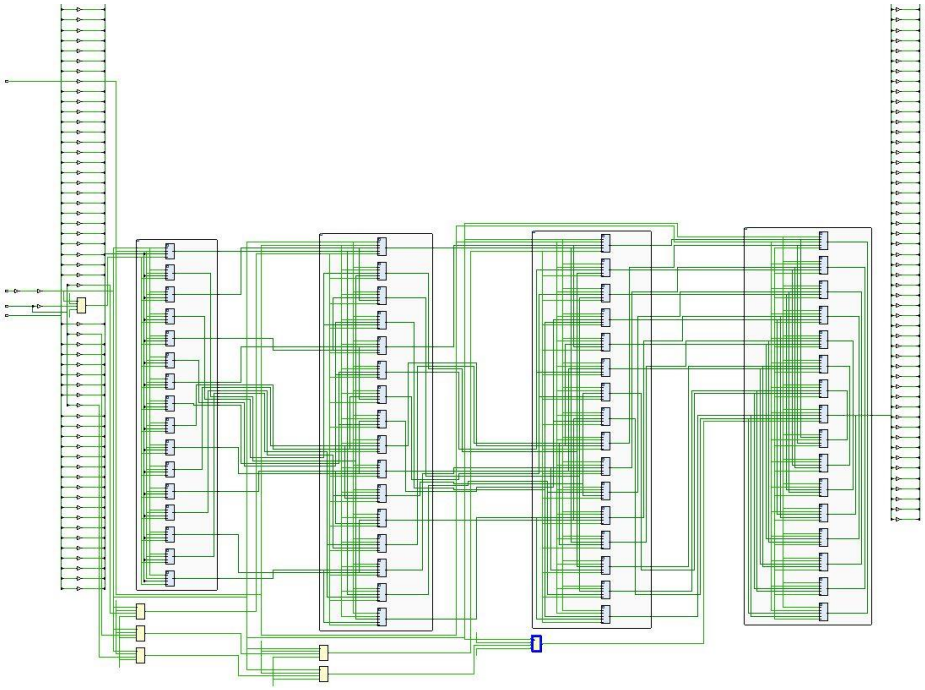


Figure 5: 16 element Barrel Shifter Synthesized Schematics

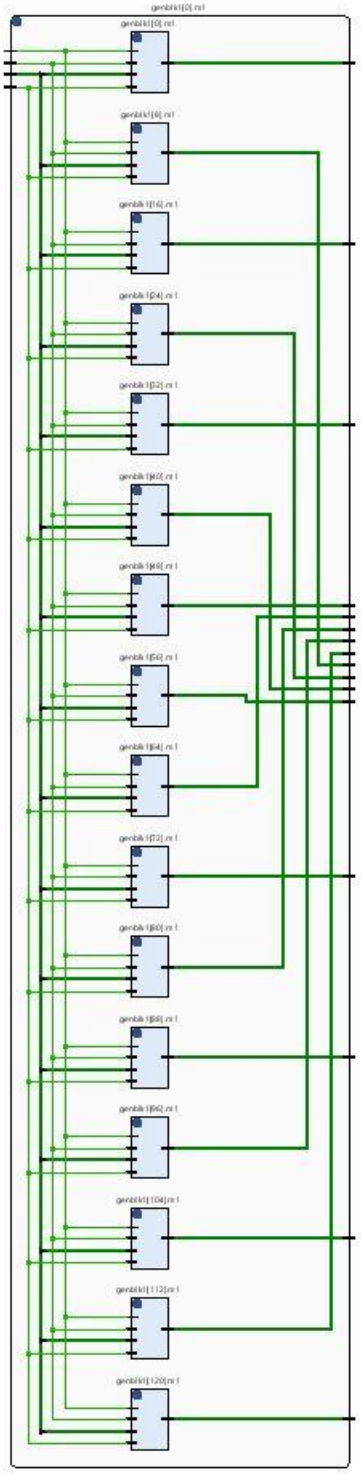


Figure 6: Mux Array in a stage of shifter

Used Resource Estimation:

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	256	0	63400	0.40
LUT as Logic	256	0	63400	0.40
LUT as Memory	0	0	19000	0.00
Slice Registers	519	0	126800	0.41
Register as Flip Flop	519	0	126800	0.41
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	262	0	210	124.76
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

7. Primitives

Ref Name	Used	Functional Category
FDRE	519	Flop & Latch
LUT3	512	LUT
IBUF	134	IO
OBUF	128	IO
BUFG	1	Clock

Timing Estimation:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.293 ns	Worst Hold Slack (WHS):	0.152 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	515	Total Number of Endpoints:	515	Total Number of Endpoints:	520

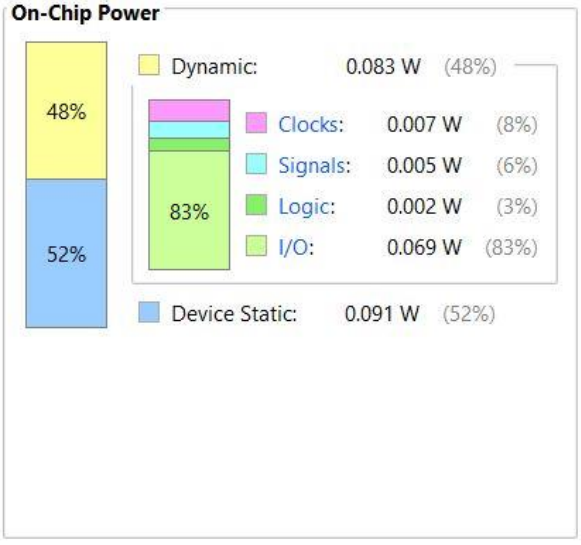
All user specified timing constraints are met.

Power Estimation:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.174 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.8°C**
Thermal Margin:	59.2°C (12.8 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



II. 64 Element Barrel Shifter Unit:

Elaborated Schematics:

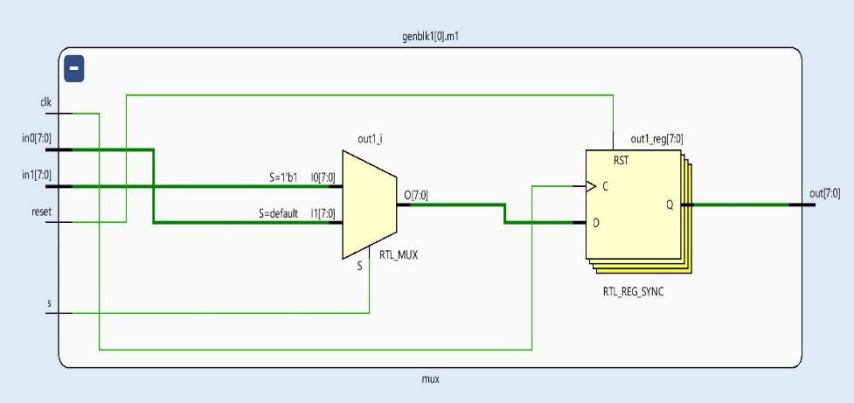


*Figure 7: 2*1 Mux Schematics*

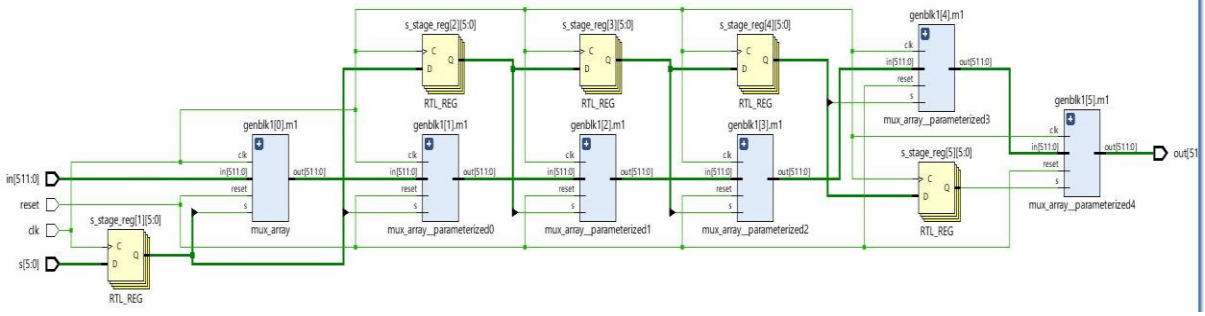


Figure 8: 64 Element barrel Shifter with 6 stages

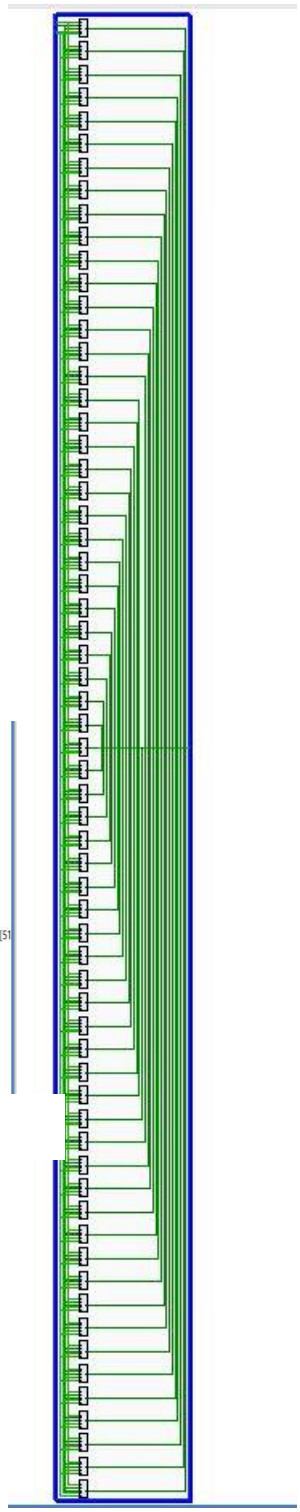


Figure 9: 64 Muxes array in given stage ->

Synthesized Schematics:

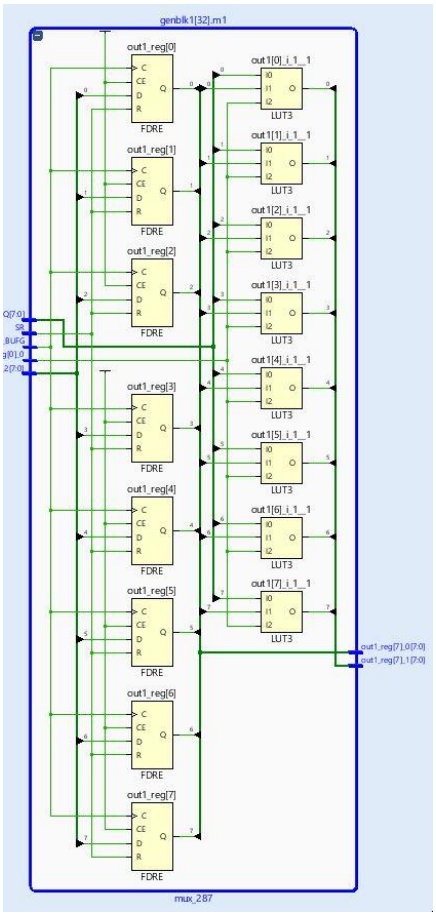


*Figure 11: 2*1 Mux synthesized schematics*

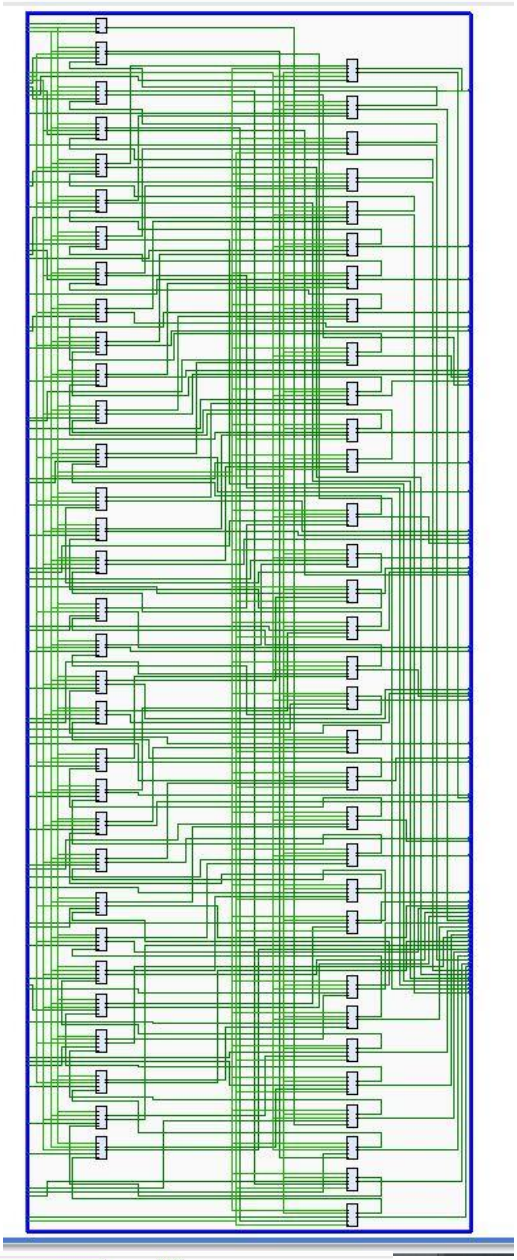


Figure 10: Mux Array Synthesized Schematics

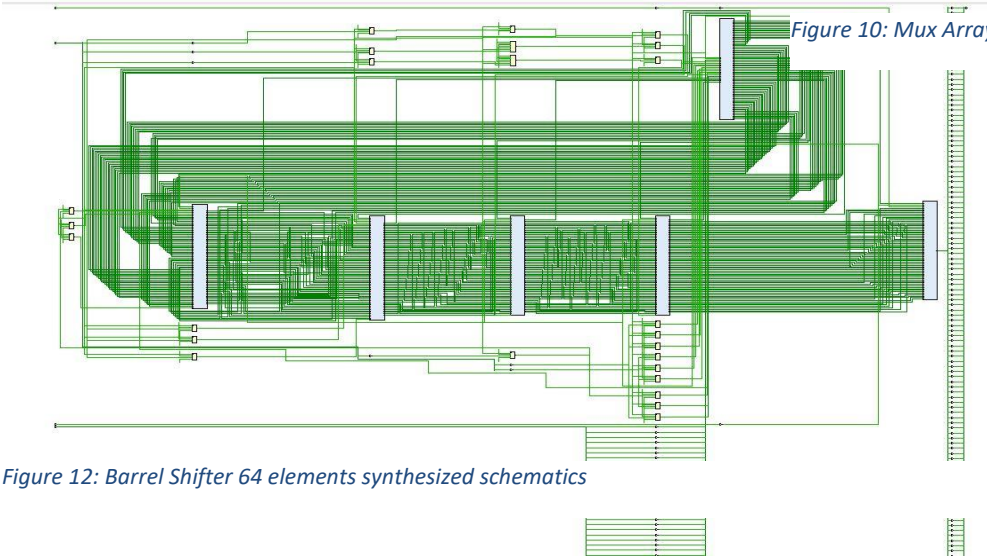


Figure 12: Barrel Shifter 64 elements synthesized schematics

Used Resource Estimation:

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	1538	0	63400	2.43
LUT as Logic	1536	0	63400	2.42
LUT as Memory	2	0	19000	0.01
LUT as Distributed RAM	0	0		
LUT as Shift Register	2	0		
Slice Registers	3095	0	126800	2.44
Register as Flip Flop	3095	0	126800	2.44
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

* Warning! The Final LUT count, after physical optimizations and full

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	1032	0	210	491.43
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

7. Primitives

Ref Name	Used	Functional Category
FDRE	3095	Flop & Latch
LUT3	3072	LUT
IBUF	520	IO
OBUF	512	IO
SRL16E	2	Distributed Memory
BUFG	1	Clock

Timing Estimation:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.288 ns	Worst Hold Slack (WHS):	0.079 ns	Worst Pulse Width Slack (WPWS):	4.020 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	3085	Total Number of Endpoints:	3085	Total Number of Endpoints:	3098

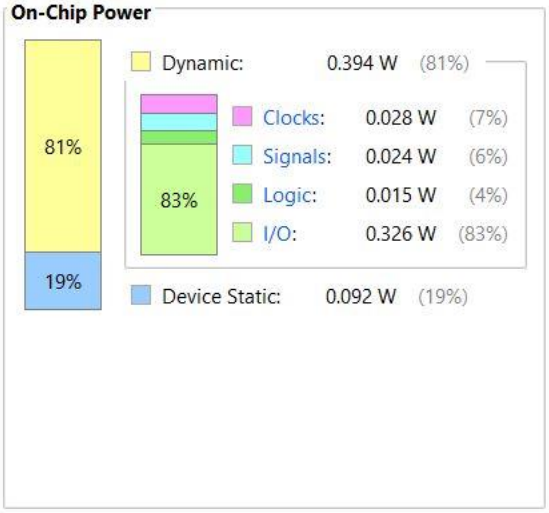
All user specified timing constraints are met.

Power Estimation:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.486 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.2°C**
Thermal Margin:	57.8°C (12.5 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Task 2: Systolic Array for Dense Matrix-Matrix Multiplication.

The Systolic Architecture consists of an array of processing elements, where data flows between neighboring elements, synchronously, from different directions. Processing element takes data from Top, Left, and output the results to Right, Bottom. Processing Unit for Matrix multiplication is Multiplier and Accumulator unit. Below diagram shows 3*3 matrix multiplication systolic array. The matrix inputs must be aligned in time space properly.

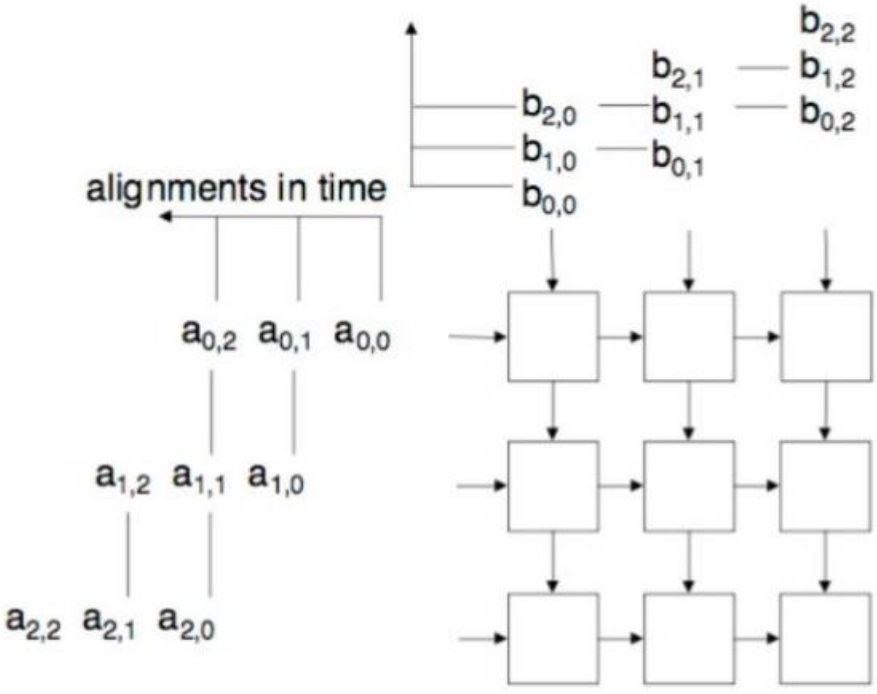


Figure 4: Example 3 × 3 Systolic Array

I. 16*16 Matrix Multiplication

Simulation Result:

To check the correctness, similar matrix generation unit is used in both Matlab and testbench file. And results are compared.

From Matlab: Matrix A:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96
97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112
113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128
129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144
145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160
161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176
177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192
193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208
209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224
225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240
241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	0

Matrix B:

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33
64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49
80	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65
96	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81
112	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97
128	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113
144	143	142	141	140	139	138	137	136	135	134	133	132	131	130	129
160	159	158	157	156	155	154	153	152	151	150	149	148	147	146	145
176	175	174	173	172	171	170	169	168	167	166	165	164	163	162	161
192	191	190	189	188	187	186	185	184	183	182	181	180	179	178	177
208	207	206	205	204	203	202	201	200	199	198	197	196	195	194	193
224	223	222	221	220	219	218	217	216	215	214	213	212	211	210	209
240	239	238	237	236	235	234	233	232	231	230	229	228	227	226	225
0	255	254	253	252	251	250	249	248	247	246	245	244	243	242	241

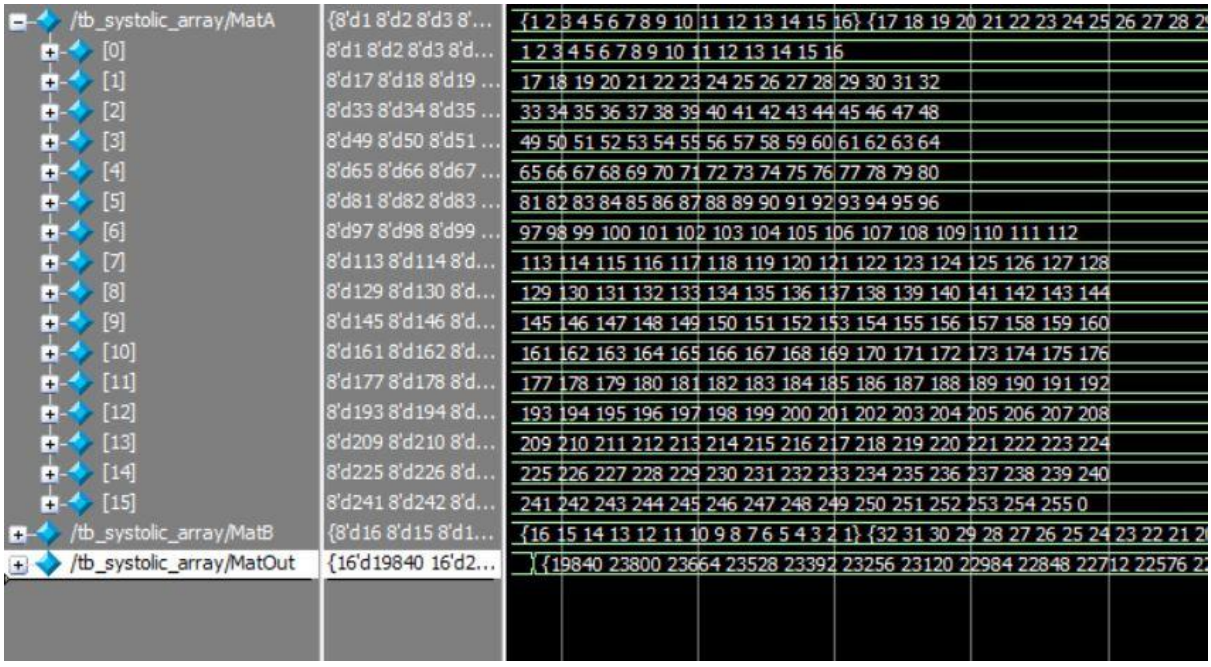
Output Matrix= A*B:

19840	23800	23664	23528	23392	23256	23120	22984	22848	22712	22576	22440	22304	22168	22032	21896
50560	58360	57968	57576	57184	56792	56400	56008	55616	55224	54832	54440	54048	53656	53264	52872
15744	27384	26736	26088	25440	24792	24144	23496	22848	22200	21552	20904	20256	19608	18960	18312
46464	61944	61040	60136	59232	58328	57424	56520	55616	54712	53808	52904	52000	51096	50192	49288
11648	30968	29808	28648	27488	26328	25168	24008	22848	21688	20528	19368	18208	17048	15888	14728
42368	65528	64112	62696	61280	59864	58448	57032	55616	54200	52784	51368	49952	48536	47120	45704
7552	34552	32880	31208	29536	27864	26192	24520	22848	21176	19504	17832	16160	14488	12816	11144
38272	3576	1648	65256	63328	61400	59472	57544	55616	53688	51760	49832	47904	45976	44048	42120
3456	38136	35952	33768	31584	29400	27216	25032	22848	20664	18480	16296	14112	11928	9744	7560
34176	7160	4720	2280	65376	62936	60496	58056	55616	53176	50736	48296	45856	43416	40976	38536
64896	41720	39024	36328	33632	30936	28240	25544	22848	20152	17456	14760	12064	9368	6672	3976
30080	10744	7792	4840	1888	64472	61520	58568	55616	52664	49712	46760	43808	40856	37904	34952
60800	45304	42096	38888	35680	32472	29264	26056	22848	19640	16432	13224	10016	6808	3600	392
25984	14328	10864	7400	3936	472	62544	59080	55616	52152	48688	45224	41760	38296	34832	31368
56704	48888	45168	41448	37728	34008	30288	26568	22848	19128	15408	11688	7968	4248	528	62344
21888	18168	14448	10728	7008	3288	65104	61384	57664	53944	50224	46504	42784	39064	35344	31624

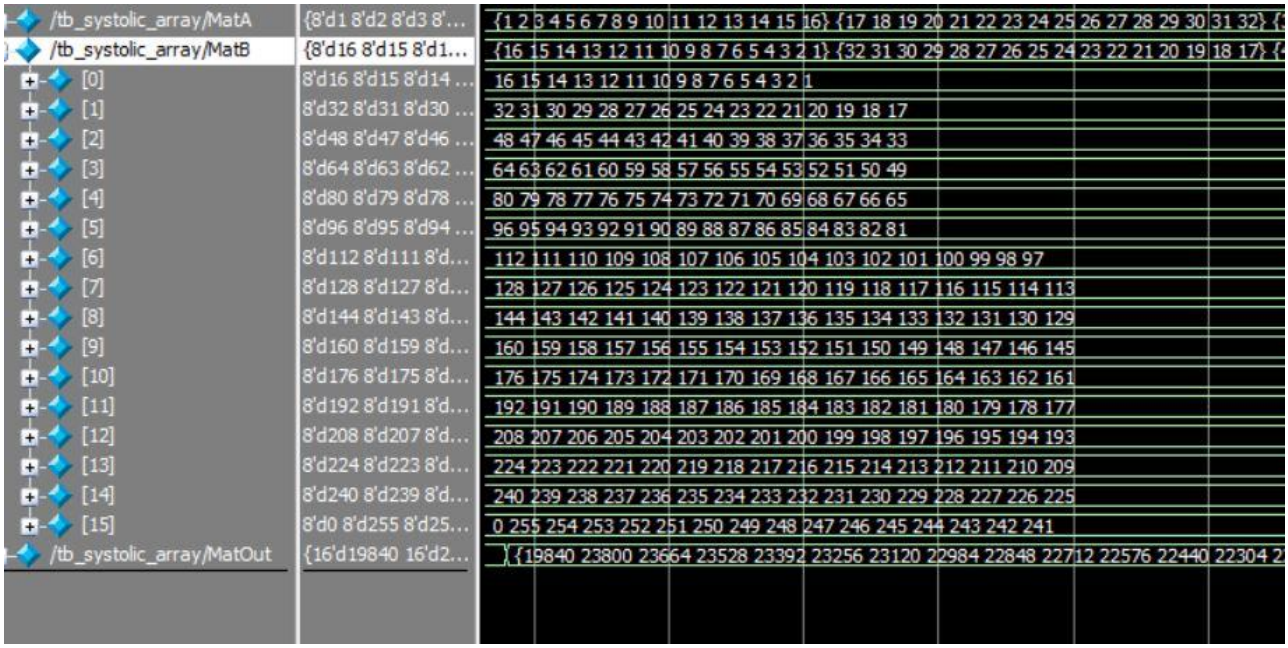
Note: Since each element of output matrix has 2N bit space , there can be possibility of overflow.

Output from Verilog Code:

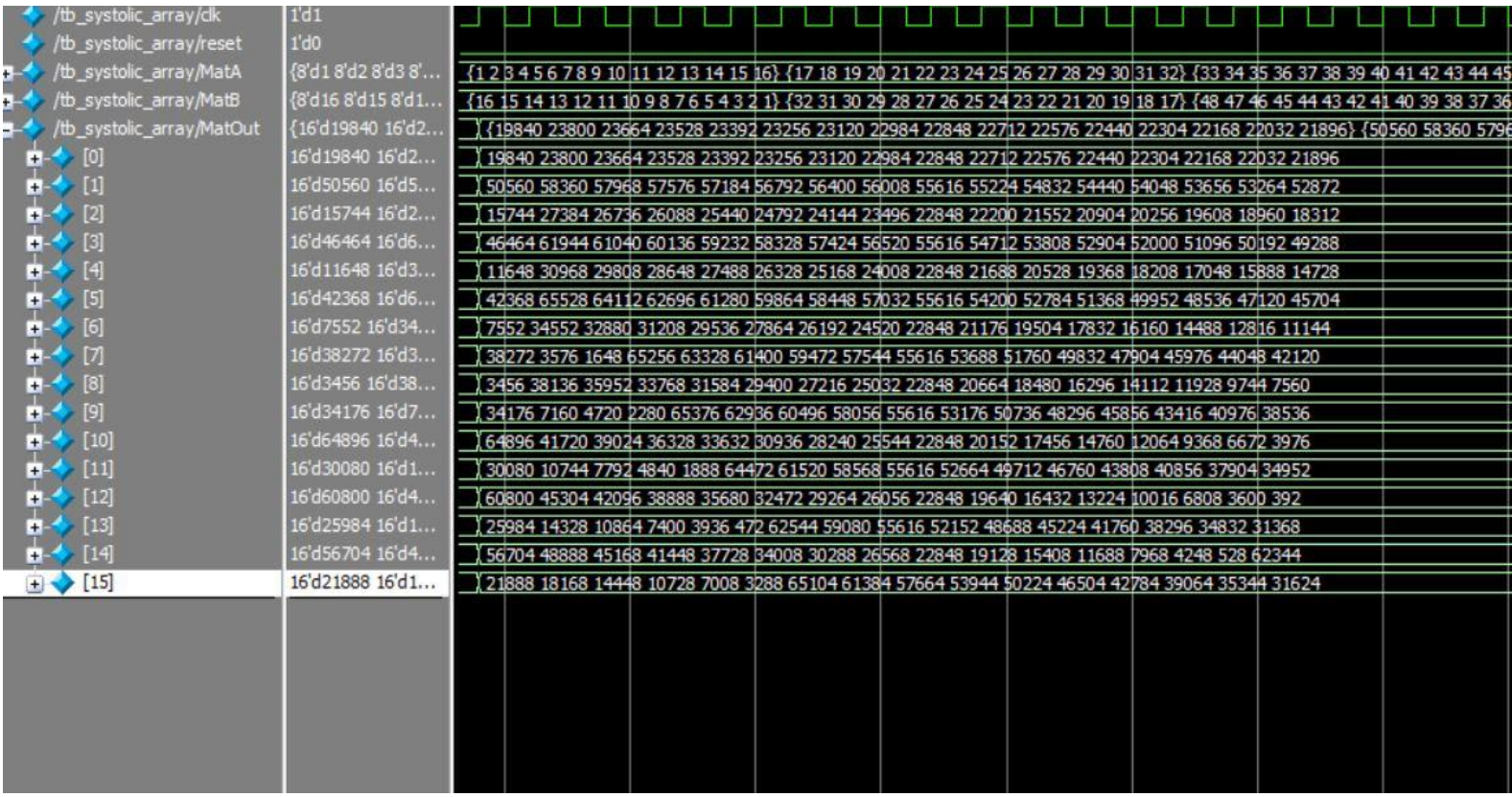
Matrix A:



Matrix B:



Output Matrix= A*B:



Elaborated Schematics:

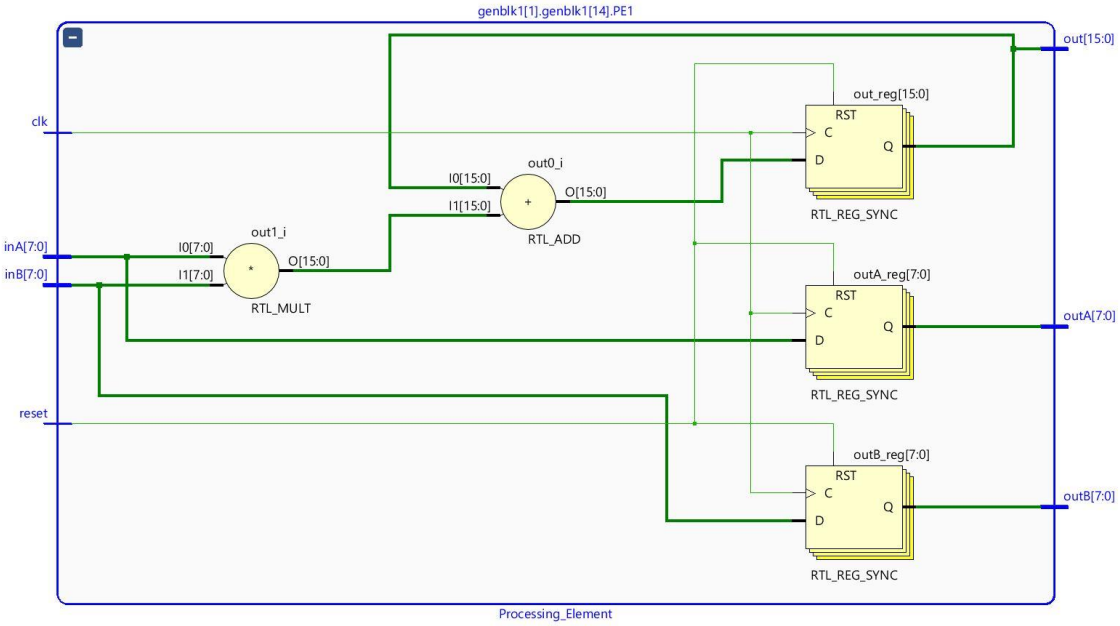


Figure 13: Processing Element (MAC) Schematics

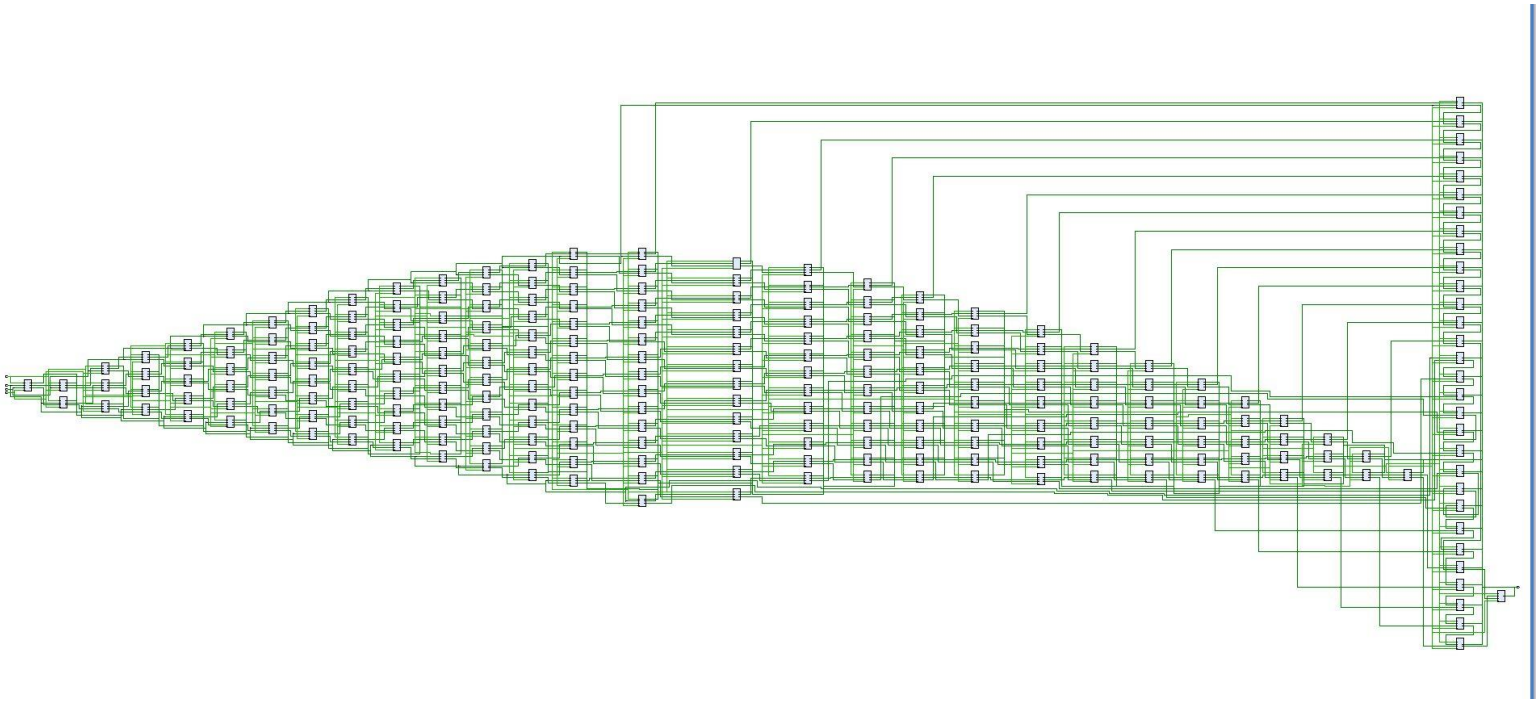


*Figure 14: Systolic array for 16*16 matrix multiplication. Total 256 PE*

Synthesized Schematics:

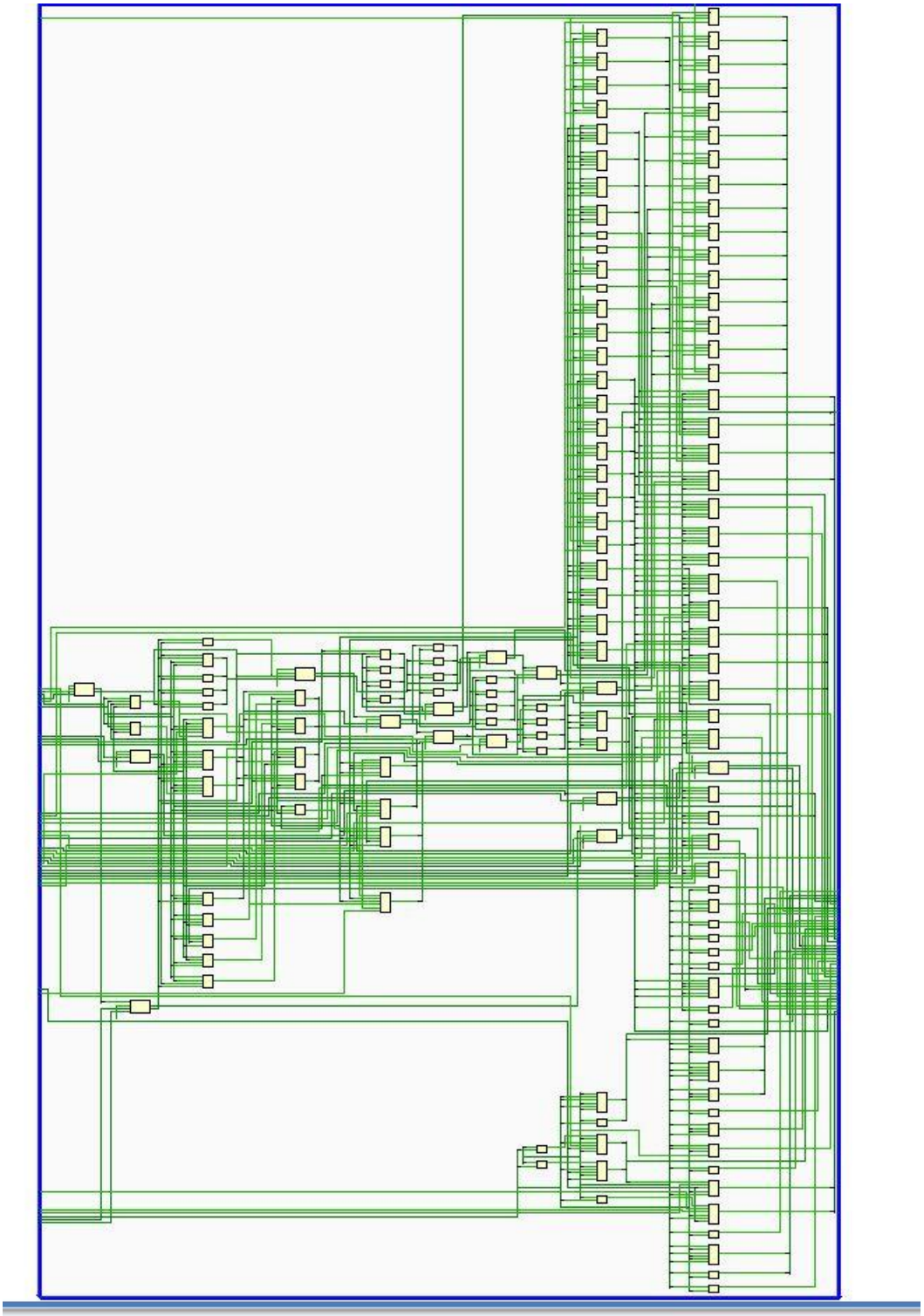


Figure 15: Synthesized PE Schematics

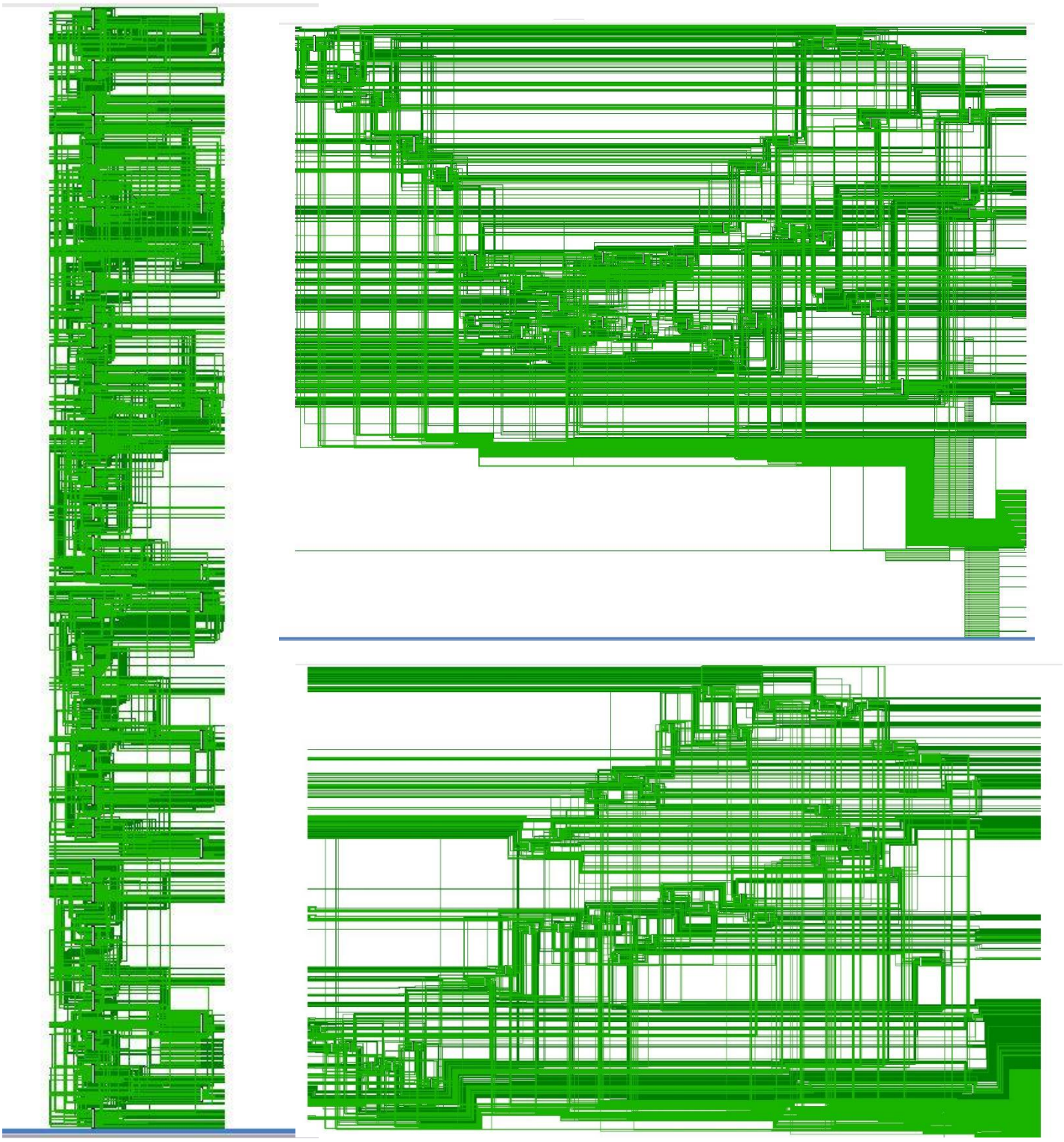


Figure 16 Parts of Synthesized Schematics of Systolic Array

Used Resource Estimation:

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	22258	0	63400	35.11
LUT as Logic	22258	0	63400	35.11
LUT as Memory	0	0	19000	0.00
Slice Registers	7936	0	126800	6.26
Register as Flip Flop	7936	0	126800	6.26
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	4354	0	210	2073.33
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT2	9728	LUT
LUT6	9098	LUT
FDRE	7936	Flop & Latch
OBUF	4096	IO
LUT4	4096	LUT
CARRY4	3584	CarryLogic
LUT5	2304	LUT
LUT3	630	LUT
IBUF	258	IO
BUFG	1	Clock

Timing Estimation:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.580 ns	Worst Hold Slack (WHS):	0.118 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	7680	Total Number of Endpoints:	7680	Total Number of Endpoints:	7937

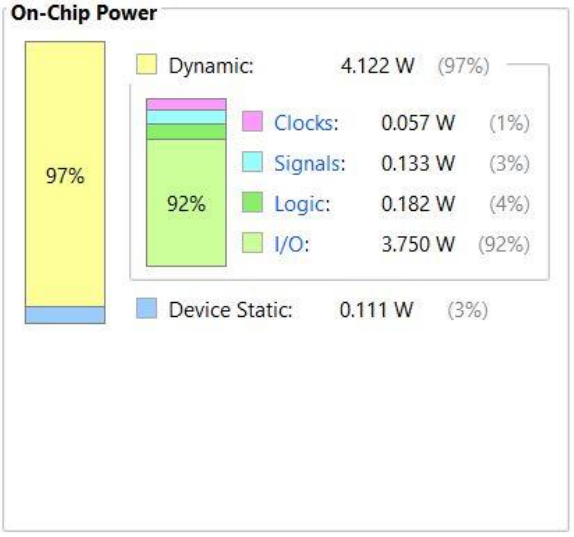
All user specified timing constraints are met.

Power Estimation:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**4.233 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**44.3°C**
Thermal Margin:	40.7°C (8.8 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



I. 32*32 Matrix Multiplication

Elaborated Schematics:

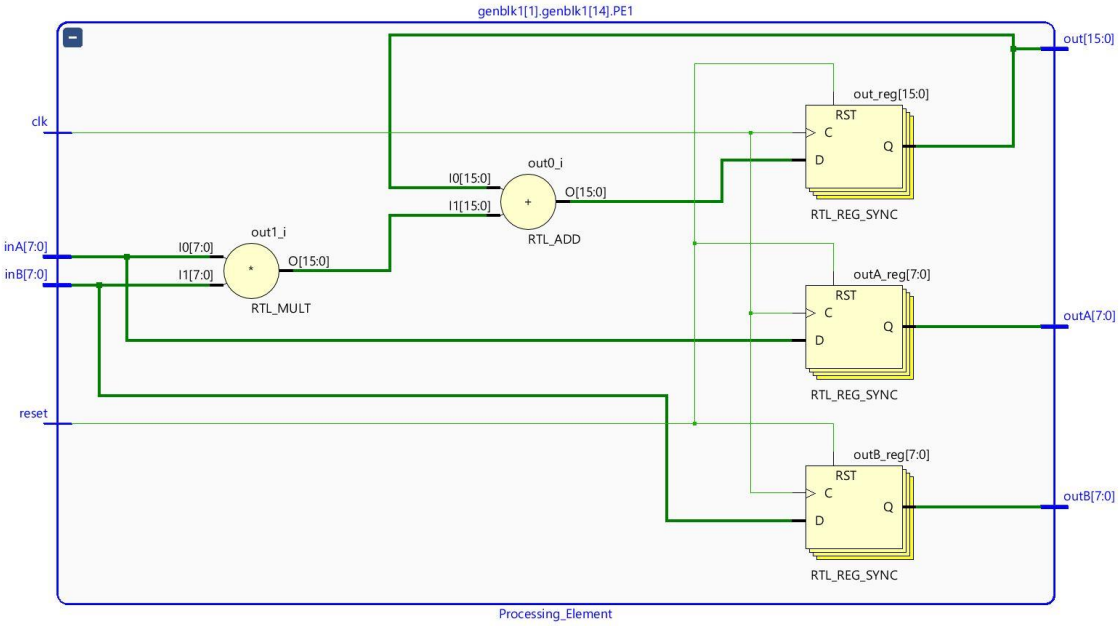


Figure 17: Processing Element (MAC) Schematics

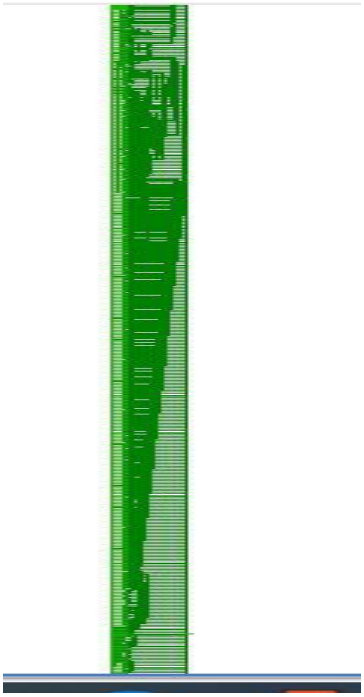


*Figure 18: Systolic array for 32*32 matrix multiplication. Total 1024 PE*

Synthesized Schematics:

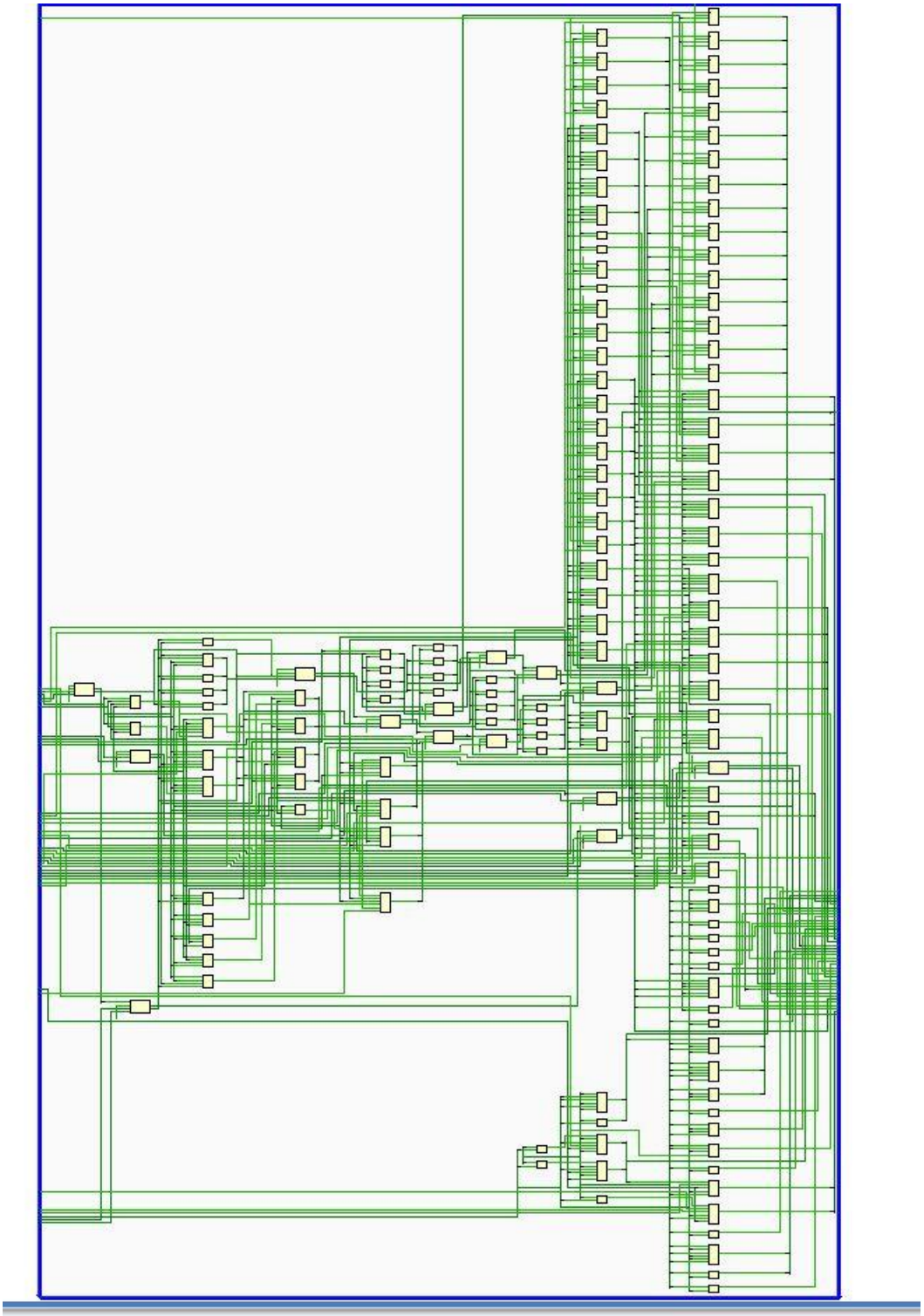


Figure 19: Synthesized PE Schematics

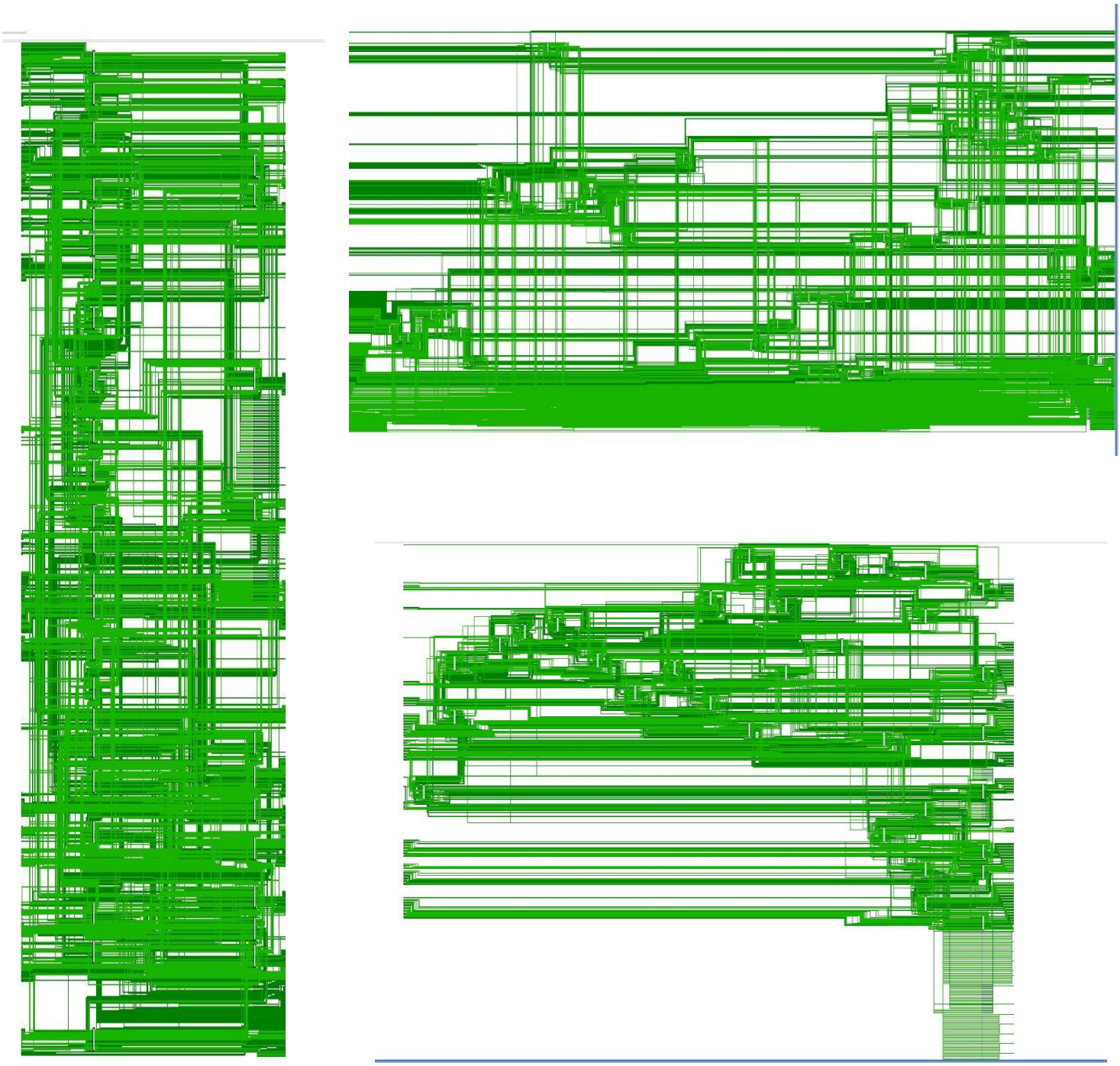


Figure 20 Parts of Synthesized Schematics of Systolic Array

Used Resource Estimation:

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	90048	0	63400	142.03
LUT as Logic	90048	0	63400	142.03
LUT as Memory	0	0	19000	0.00
Slice Registers	32256	0	126800	25.44
Register as Flip Flop	32256	0	126800	25.44
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	16898	0	210	8046.67
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT2	40960	LUT
LUT6	37888	LUT
FDRE	32256	Flop & Latch
LUT4	21504	LUT
OBUF	16384	IO
CARRY4	14336	CarryLogic
LUT3	4096	LUT
LUT5	3072	LUT
IBUF	514	IO
BUFG	1	Clock

Timing Estimation:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.641 ns	Worst Hold Slack (WHS):	0.118 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	31744	Total Number of Endpoints:	31744	Total Number of Endpoints:	32257

All user specified timing constraints are met.

Power Estimation:

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**16.817 W (Junction temp exceeded!)**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**101.7°C**
Thermal Margin:	-16.7°C (-3.5 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity