SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT
ELECTRONICS ENGINEERING DEPARTMENT

Expt. No:	2	Diode Clipper Circuits
Date:		

U20CS100_ADITYA_RAJ

AIM: To implement various diode clamper circuits and verify its performance using Multi-Sim software

SOFTWARE TOOLS / OTHER REQUIREMENTS:

1. Multisim Simulator/Circuit Simulator

THEORY:

A clamper is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal.

Additional shifts can also be obtained by introducing a dc supply to the basic structure. The resistor and capacitor of the network must be chosen such that the time constant determined by τ=RC is sufficiently large to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is not conducting. Throughout the analysis we assume that for all practical purposes the capacitor fully charges or discharges in five-time constants. The simplest of clamper networks is shown in figure below.

Clamping networks have a capacitor connected directly from input to output with a resistive element in parallel with the output signal. The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.

Six type of clamper circuits are as follows:

1. POSITIVE CLAMPER

2. POSITIVE CLAMPER WITH POSITIVE VT

3. POSITIVE CLAMPER WITH NEGATIVE VT

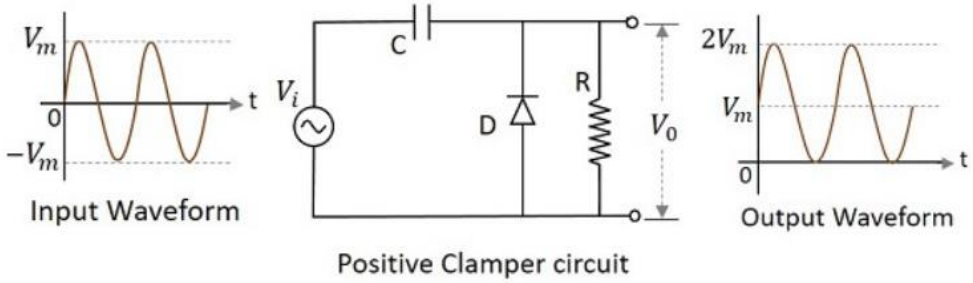
4. NEGATIVE CLAMPER

5 NEGATIVE CLAMPER WITH POSITIVE VT

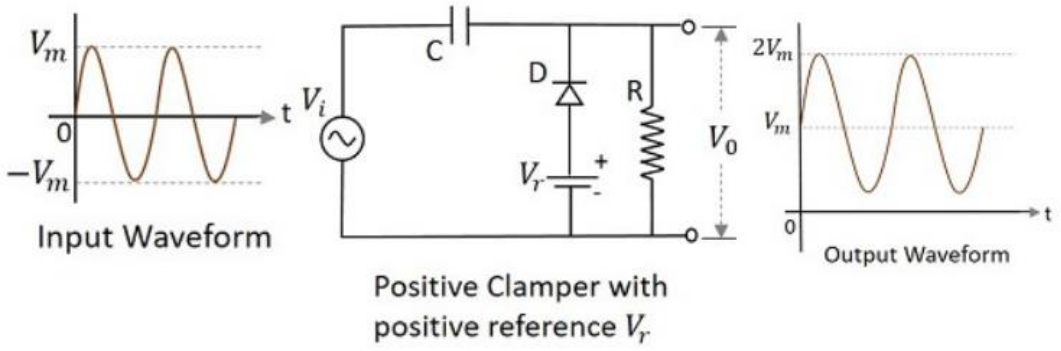
6 NEGATIVE CLAMPER WITH NEGATIVE VT

CIRCUIT DIAGRAMS

1. POSITIVE CLAMPER CIIRCUIT:

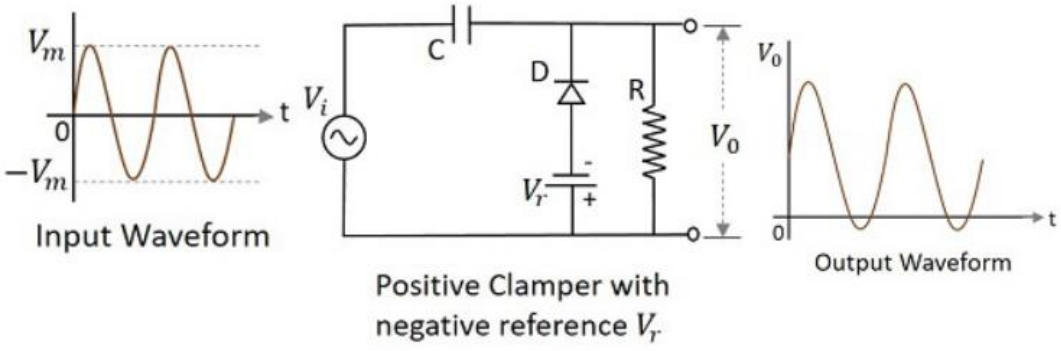


2. POSITIVE CLAMPER WITH POSITIVE VT



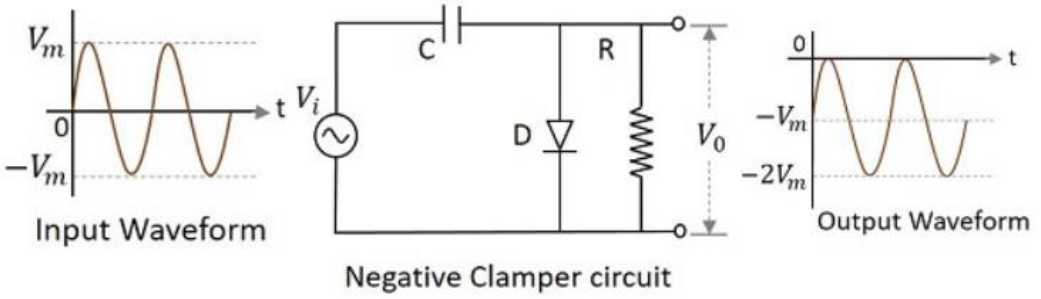
Positive Clamper with positive reference V_r

3. POSITIVE CLAMPER WITH NEGATIVE VT



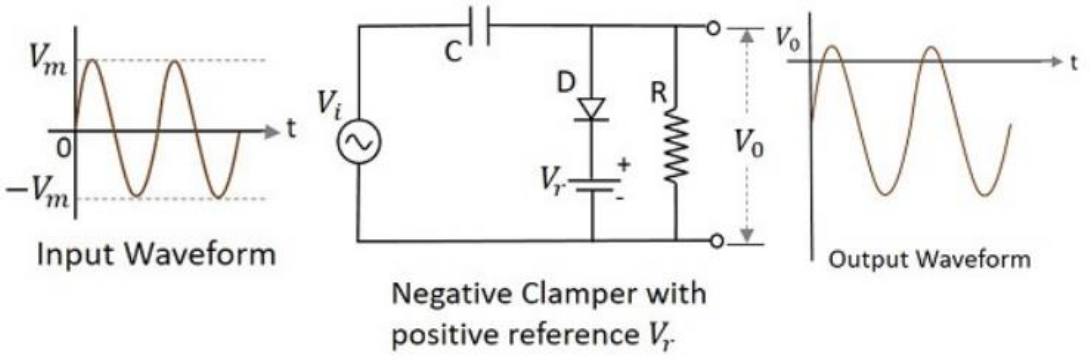
Positive Clamper with negative reference V_r

4. NEGATIVE CLAMPER

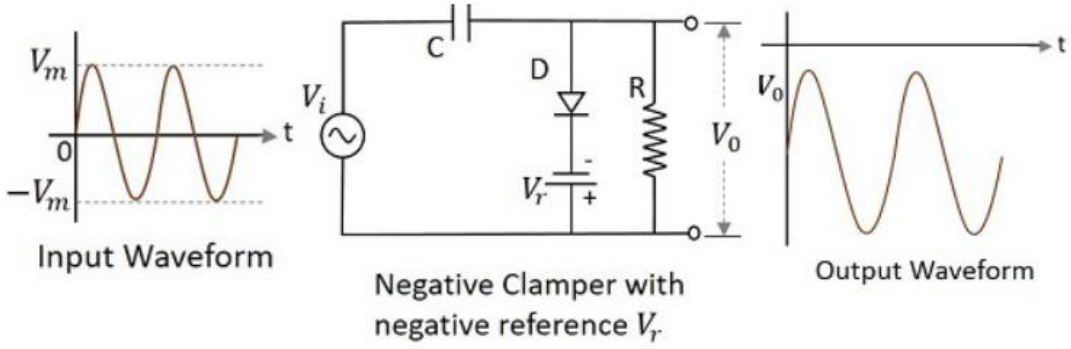


Negative Clamper circuit

5 NEGATIVE CLAMPER WITH POSITIVE VT

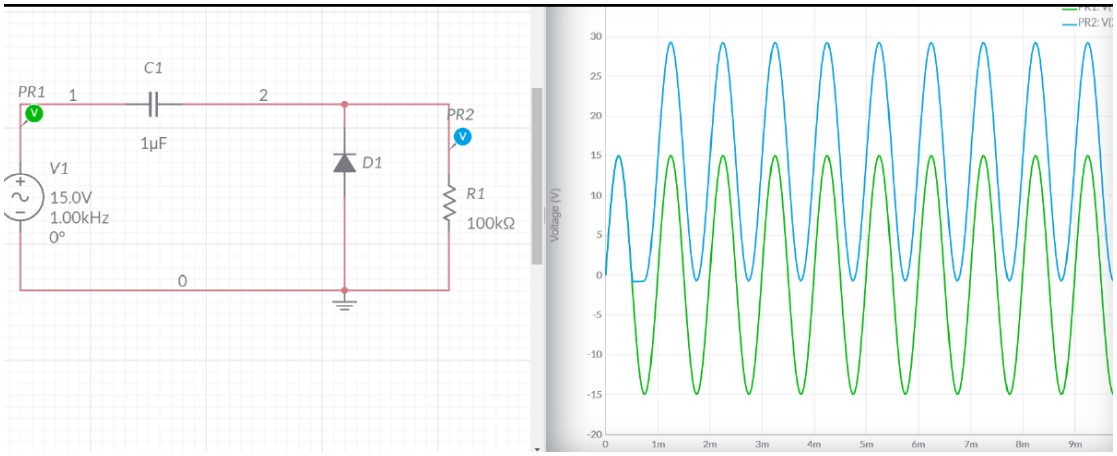


6 NEGATIVE CLAMPER WITH NEGATIVE VT



1) POSITIVE CLAMPER

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



CALCULATIONS:

Let V_c be the voltage of capacitor:

CASE 1: For interval 0<t<T/2

Diode is reversed biased, so it will act like open circuit in ideal condition.

By applying Kirchhoff's voltage law:

Vi + Vc - Vo = 0

Vo = Vi + Vi

Vo = 2Vi =30V

CASE 2: For interval T/2<t<T

Diode is forward biased, so it will act like short circuit in ideal condition.

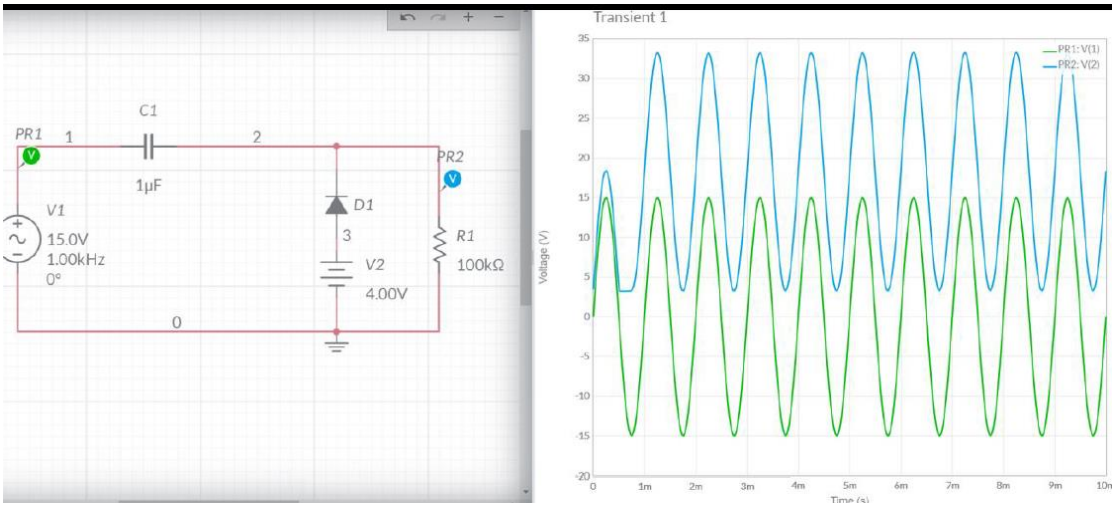
By applying Kirchhoff's voltage law:

-Vi + Vc - Vo = 0

Vc = 15V

2) POSITIVE CLAMPER CIRCUIT WITH POSITIVE REFERENCE

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



CALCULATIONS

CASE 1: For interval 0<t<T/2

Diode is reversed biased, so it will act like open circuit in ideal condition.

By applying Kirchhoff's voltage law:

Vi + Vc - Vo = 0

$V_o = V_c + V_i$

= 15V + 19V = 34V

CASE 2: For interval T/2<t<T

Diode is forward biased, so it will act like short circuit in ideal condition.

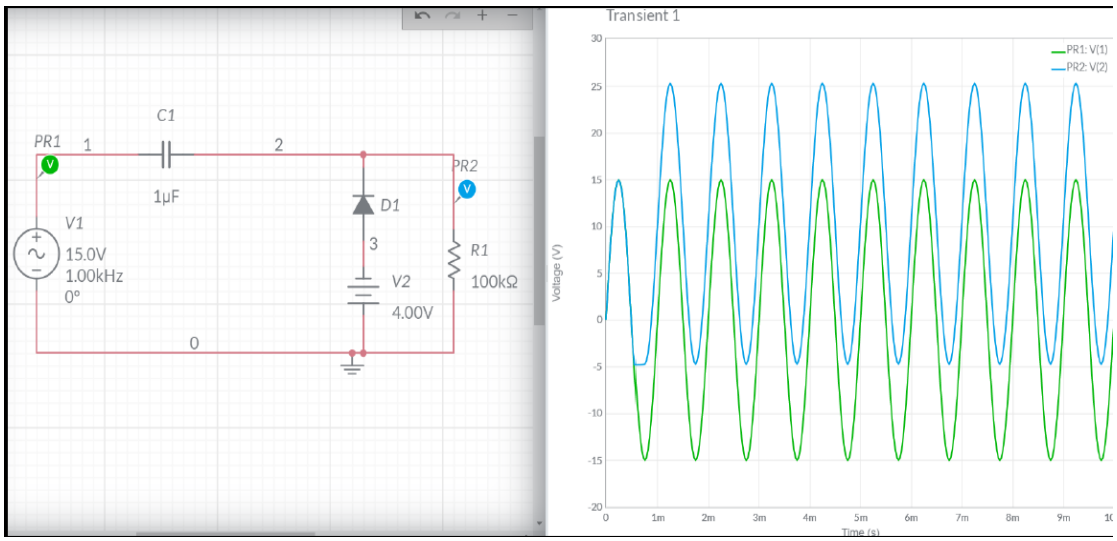
Assume that capacitor will charge p instantaneously to a voltage level determined by the surrounding network. As diode is short circuited Vo = Vr = 4V

Applying KVL: -Vi + Vc - Vo = 0

Vc = 19V

3) POSITIVE CLAMPER CIRCUIT WITH NEGATIVE REFERENCE

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



CALCULATIONS:

CASE 1: For interval 0<t<T/2

Diode is reversed biased so will act as open circuit.

Applying KVL:

$V_i + V_c - V_o = 0$

$V_o = 15V + 11V = 26V$

CASE 2: For interval 0<t<T/2

Diode is forward biased.

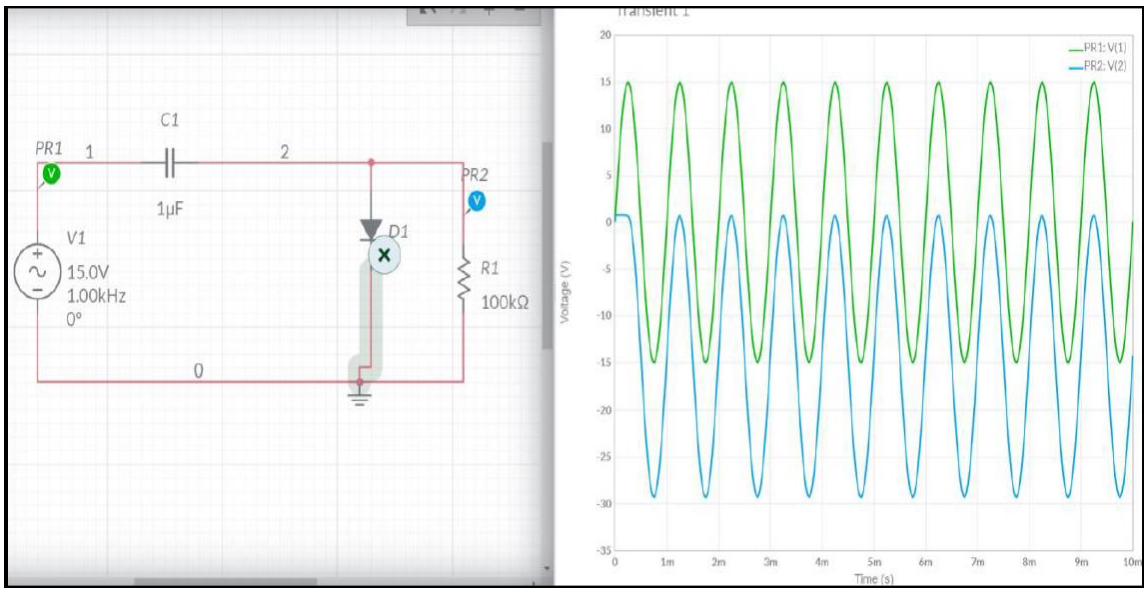
Assume that capacitor will charge p instantaneously to a voltage level determined by the surrounding network. As diode is short circuited Vo = Vr = -4V

Applying KVL: -Vi + Vc - Vo = 0

Vc=11V

4) NEGATIVE CLAMPER

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



CALCULATIONS:

Case-1: For interval 0<t<T

Assume that capacitor will charge p instantaneously to a voltage level determined by the surrounding network. As diode is short circuited Vo = 0

Voltage across capacitor Vc : Applying KVL: Vi - Vc - Vo = 0

$$Vc = -15V$$

Case-2) For interval T/2<t

Diode is reverse bias.

As diode is open circuited

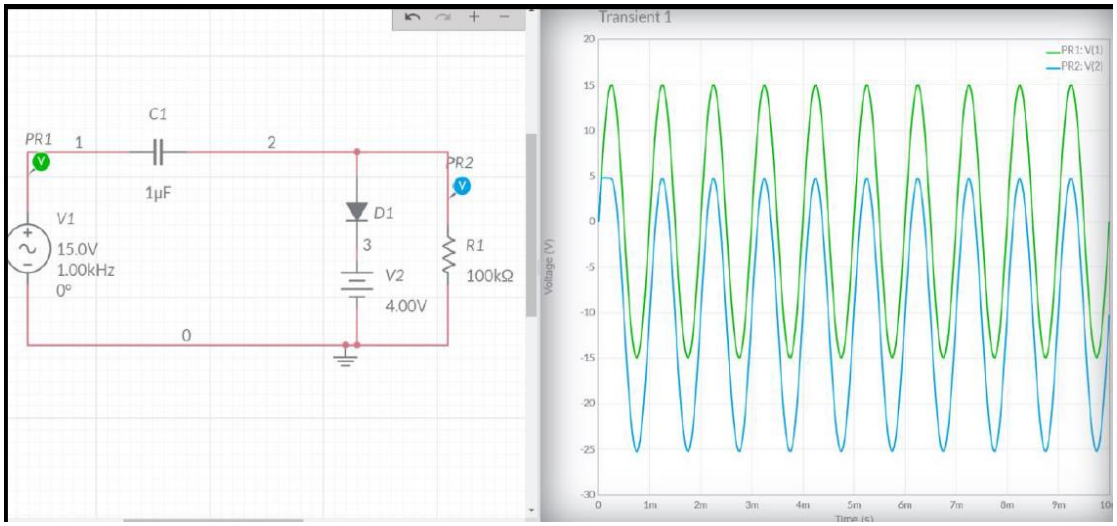
Applying KVL : -Vi - Vc - Vo = 0

$$Vo = -Vi - Vi$$

$$Vo = -2Vi = -30V$$

5) NEGATIVE CLAMPER CIRCUIT WITH POSITIVE REFERENCE

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



CALCULATIONS:

Case-1) For interval 0<t<T/2

Diode is forward bias. Assume that capacitor will charge p instantaneously to a voltage level determined by the surrounding network.

As diode is short circuited Vo = Vr = 4V

Voltage across capacitor Vc :

Applying KVL: Vi - Vc - Vo = 0

Vc = 11V

Case2: For interval T/2<t<T

Diode is reversed biased.

As diode is open circuited.

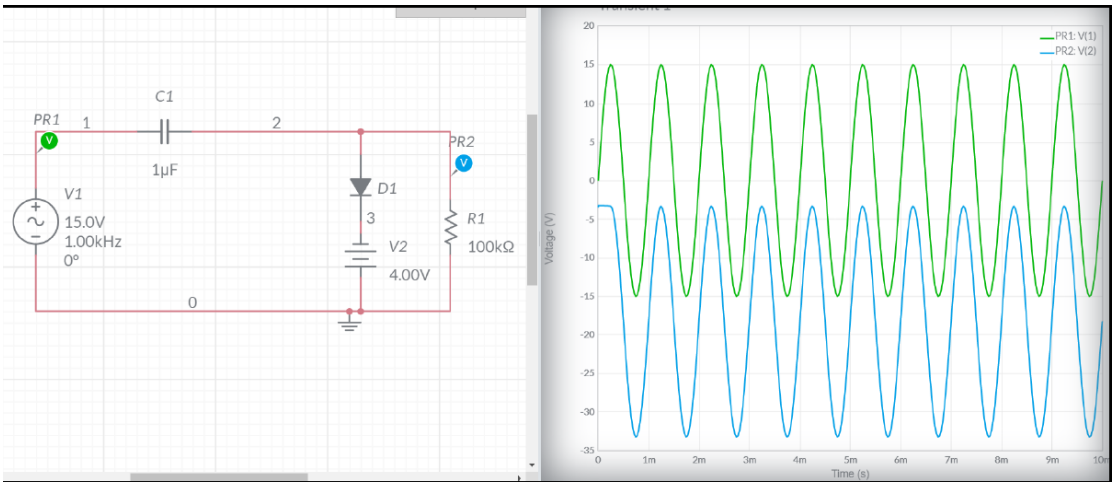
Applying KVL: Vi – V_c – V_o = 0

V_o = -V_c – Vi

Vo = -11V -15V = -26V

6) NEGATIVE CLAMPER CIRCUIT WITH NEGATIVE REFERENCE

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



CALCULATIONS:

Case-1) For interval 0<t<T/2

Diode is forward bias. Assume that capacitor will charge p instantaneously to a voltage level determined by the surrounding network

As diode is short circuited Vo = Vr = -4V

Voltage across capacitor Vc :

Applying KVL: Vi - Vc - Vo = 0

Vc = 19V

Case-2) For interval T/2<t<T:

Diode is reverse bias.

As diode is open circuited

Applying KVL : -Vi - Vc - Vo = 0

Vo = -Vc – Vi

Vo = -19V - 15V = -34V

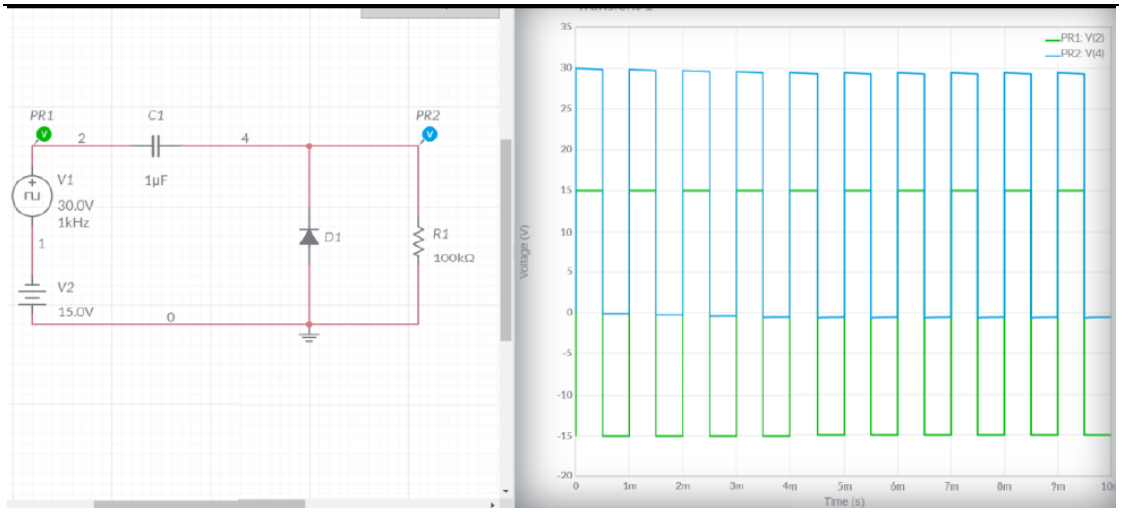
CONCLUSIONS

Here, the practical and theoretical characteristics of various negative and positive clamper (with and without bias) are same. Hence verified.

ASSIGNMENT

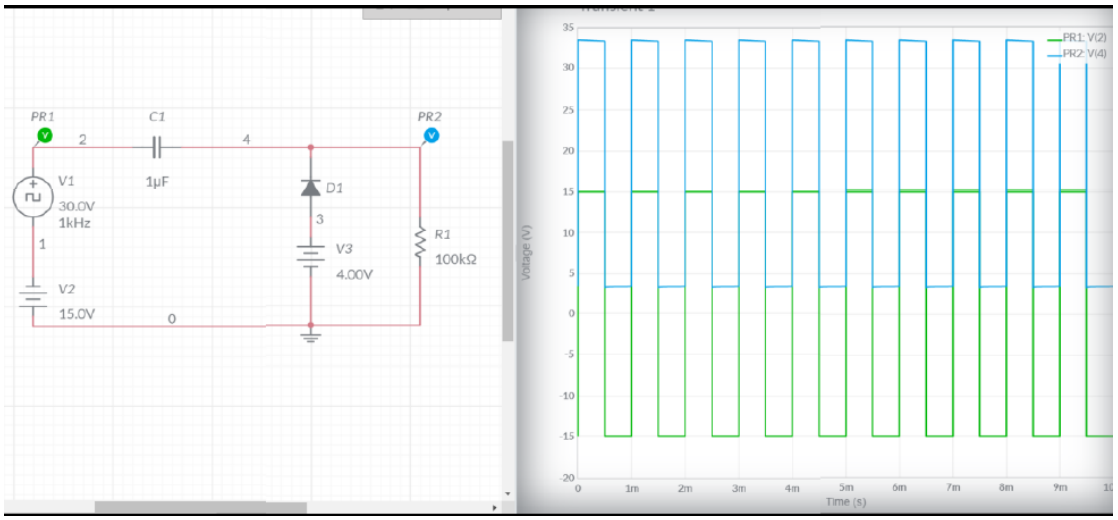
QUESTION 1:

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



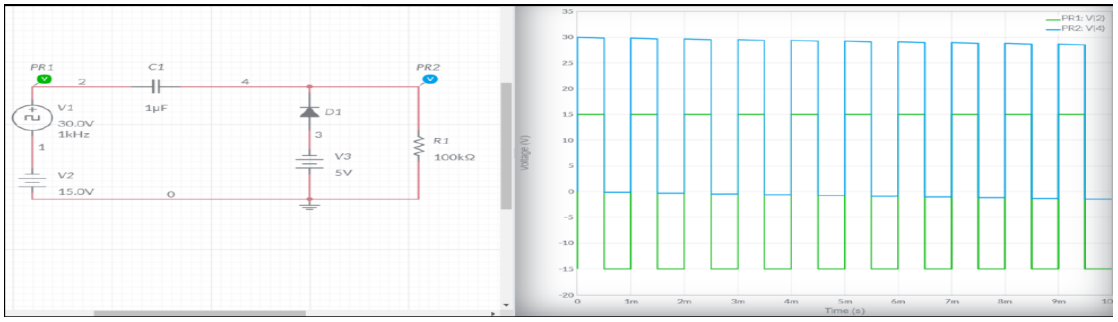
QUESTION 2:

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



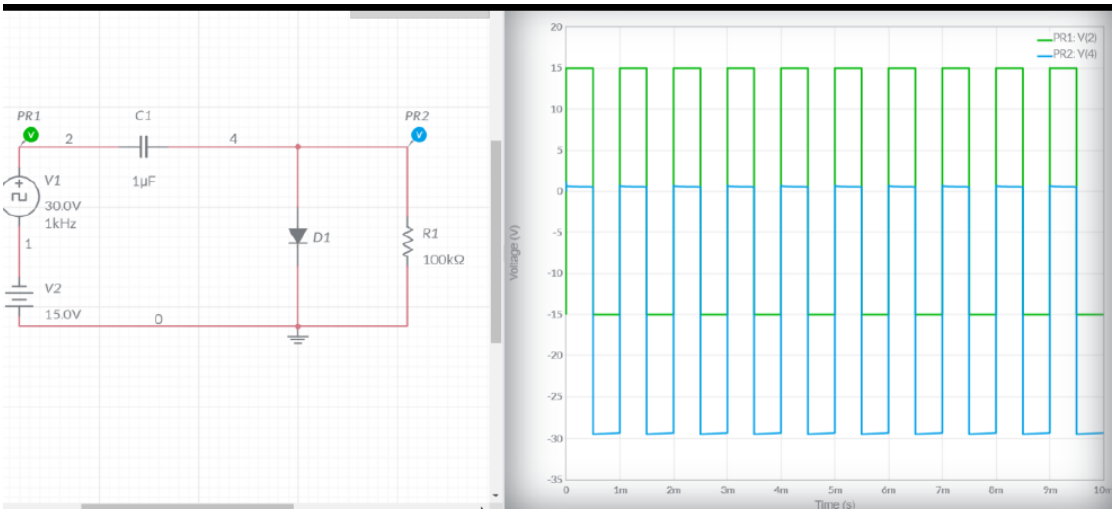
QUESTION 3:

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



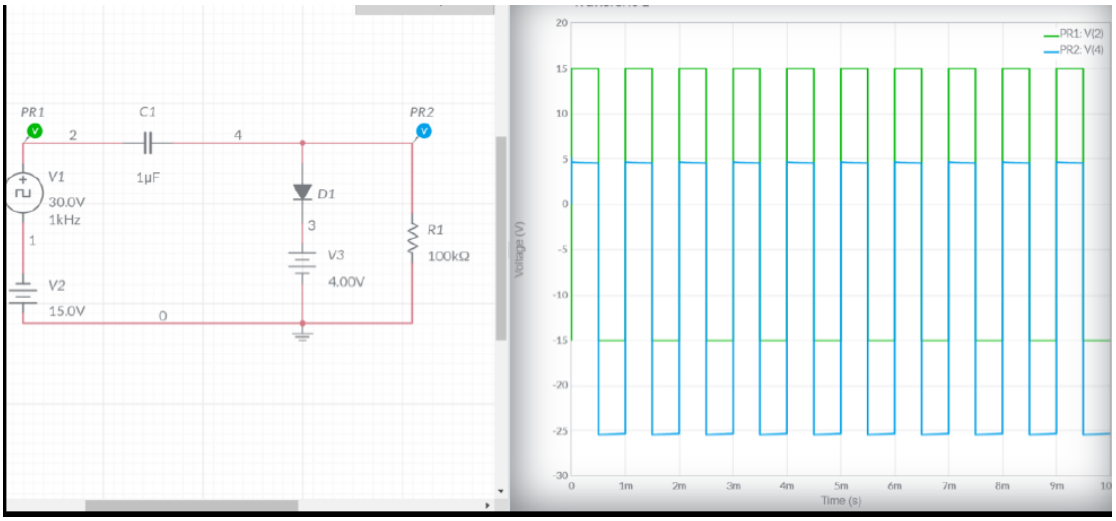
QUESTION 4:

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



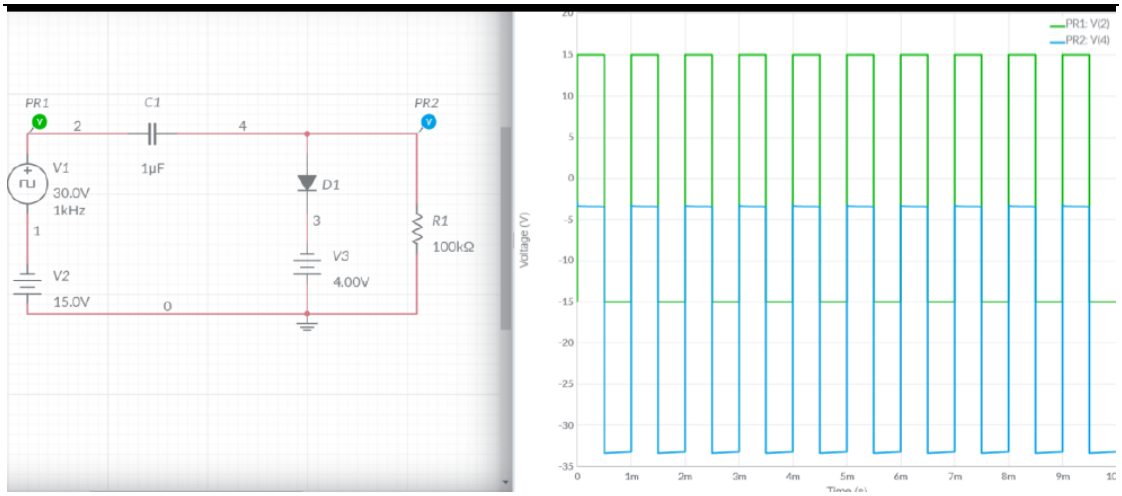
QUESTION 5:

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



QUESTION 6:

CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)


PR1
C1
PR2
2
4
V1
30.0V
1kHz
1µF
D1
3
R1
100kΩ
V3
4.00V
1
V2
15.0V
0
PR1: V(2)
PR2: V(4)
Voltage (V)
15
10
5
0
-5
-10
-15
-20
-25
-30
-35
0
1m
2m
3m
4m
5m
6m
7m
8m
9m