ADITYA MILIND SANGAMNERKAR

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EDUCATION

North Carolina State University | Raleigh, NC, USA **Aug 2022 – May 2024**
Master of Science, Computer Engineering ***GPA: 3.78/4.0***
Coursework: , Advanced Microarchitecture, ASIC Verification, Advanced Computer Architecture: Data Parallel Processors, Microprocessor Architecture, ASIC and FPGA Design, Embedded Systems Architecture

Shri Ramdeobaba College of Engineering and Management | Nagpur, India **Aug 2016 – Oct 2020**
Bachelor of Engineering, Electronics and Communication ***GPA: 9.17/10.0***

TECHNICAL SKILLS

- **Languages:** System Verilog, Verilog, C++, Python
- **Tools:** Git, Modelsim, Questasim, Design Vision, Keil uVision5, GDB, Bash

ACADEMIC PROJECTS (GitHub : https://github.com/Aditya-Sangamnerkar)

Functional Verification of I2C Bus Controller | System Verilog
- Created a test plan with diverse verification methods: testing, functional coverage, code coverage, and assertions.
- Developed a class-based layered testbench architecture with agent, river, monitor, generator, and coverage components.
- Designed an I2C slave Bus Functional Model (BFM) for interaction with I2C master DUT, supporting the full test plan.

Checkpoint Processing and Recovery Implementation | C++
- Incorporated CRP in 721sim featuring coarse-grain retirement, exact checkpoint placement & aggressive register freeing.
- Conducted IPC analysis of traditional Active List based machine against CPR.

Register Read and Renaming Mechanism Simulator for Modern Superscalar | C++.
- Developed a Register renaming machinery for a modern superscalar pipeline simulator using Free List (FL).
- Implemented misprediction recovery using branch checkpoints and an Architectural Map Table (AMT).

Synthesizable Convolution Neural Network | Verilog
- RTL implementation of standalone ASIC for CNN architecture.
- Designed convolution, max pooling, and fully connected layers of NN.
- Optimized hardware for one-input-per-clock-cycle processing, enhancing performance with minimal chip area.

Superscalar Pipeline Simulator | C++, Python
- Created a trace-driven simulator to model dynamic instruction execution in an out-of-order superscalar processor.
- Implemented components such as Reorder Buffer (ROB), Rename Map Table (RMT), and Issue Queues for efficient out-of-order execution.
- Executed automation scripts in Python to run traces and compare IPC for varying out-of-order execution windows.

Dynamic Branch Predictor | C++, Python
- Engineered a trace-driven simulator in C++ to accurately model Bimodal, G-Share, and Hybrid Branch Predictors.
- Implemented branch history table and 2-bit smith counters for dynamic prediction.
- Conducted analysis of misprediction rate trends across different benchmarks by varying branch predictor configurations.

Cache and Memory Hierarchy Simulator | C++, Python
- Modelled a flexible and generic Cache simulator that utilized LRU eviction policy along with WBWA write policies.
- Analyzed the impact of cache size, associativity, block size, stream buffers, & cache hierarchies on cache miss rate.

Quantum Circuit Simulation System on GPU | C++, CUDA
- GPU Simulation of a multiple qubit gate on an N bit quantum state on a GPU using CUDA.
- Optimized kernel function to utilize data locality of shared memory to improve IPC.

GPGPU Sim Cache Profiling Analysis | C++, CUDA
- Modified the GPGPU sim simulator to profile L1 cache accesses for loads and implemented a load bypass mechanism.

PROFESSIONAL EXPERIENCE

Accenture - Bengaluru, India | ***Senior Software Engineer*** **Dec 2020 – Jul 2022**
- Developed Database APIs for *DataOps* tool to accelerate automated data migration.
- Designed object-oriented *API Management Tool* for automated generation of flask-based APIs for MonogoDB.