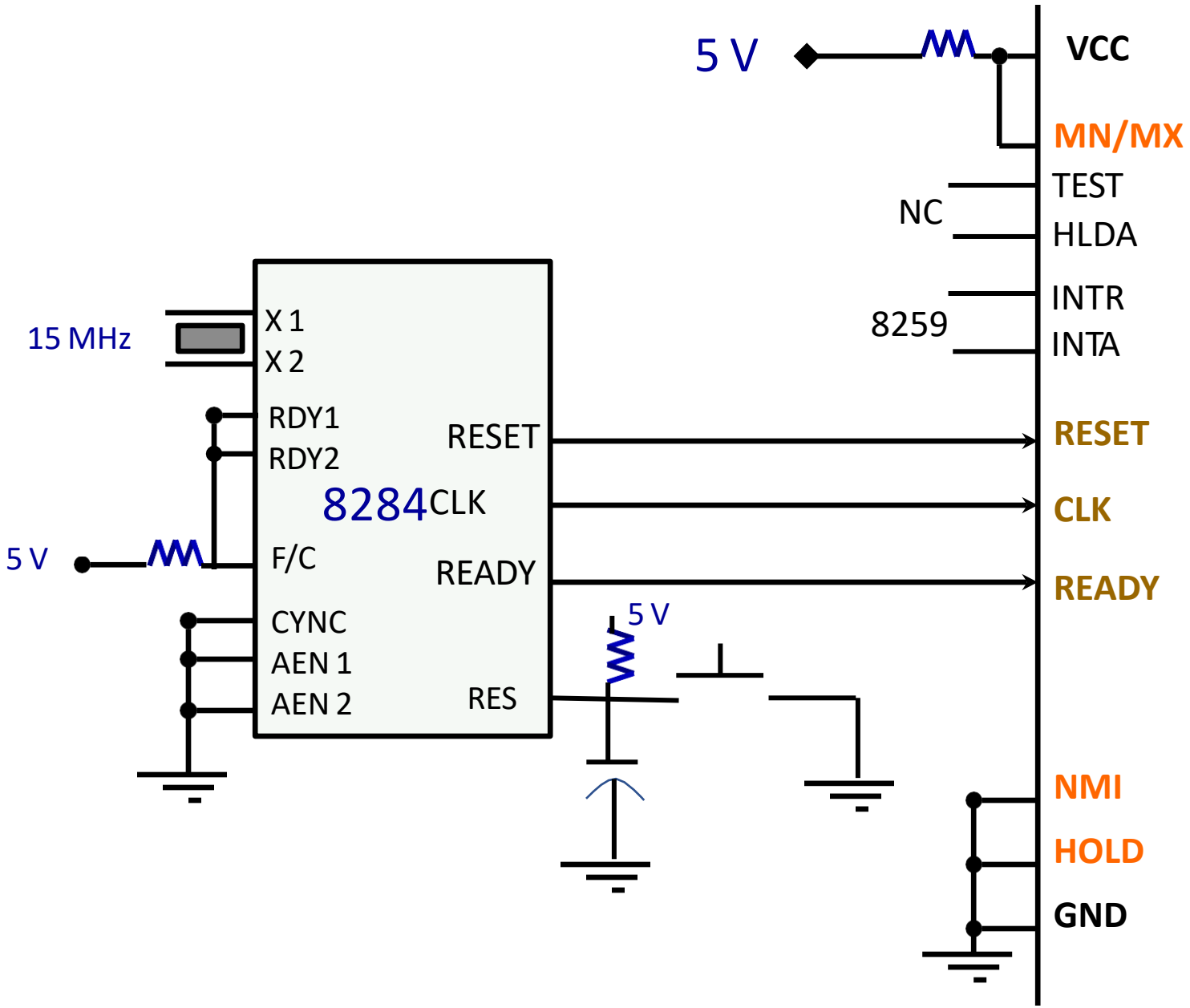
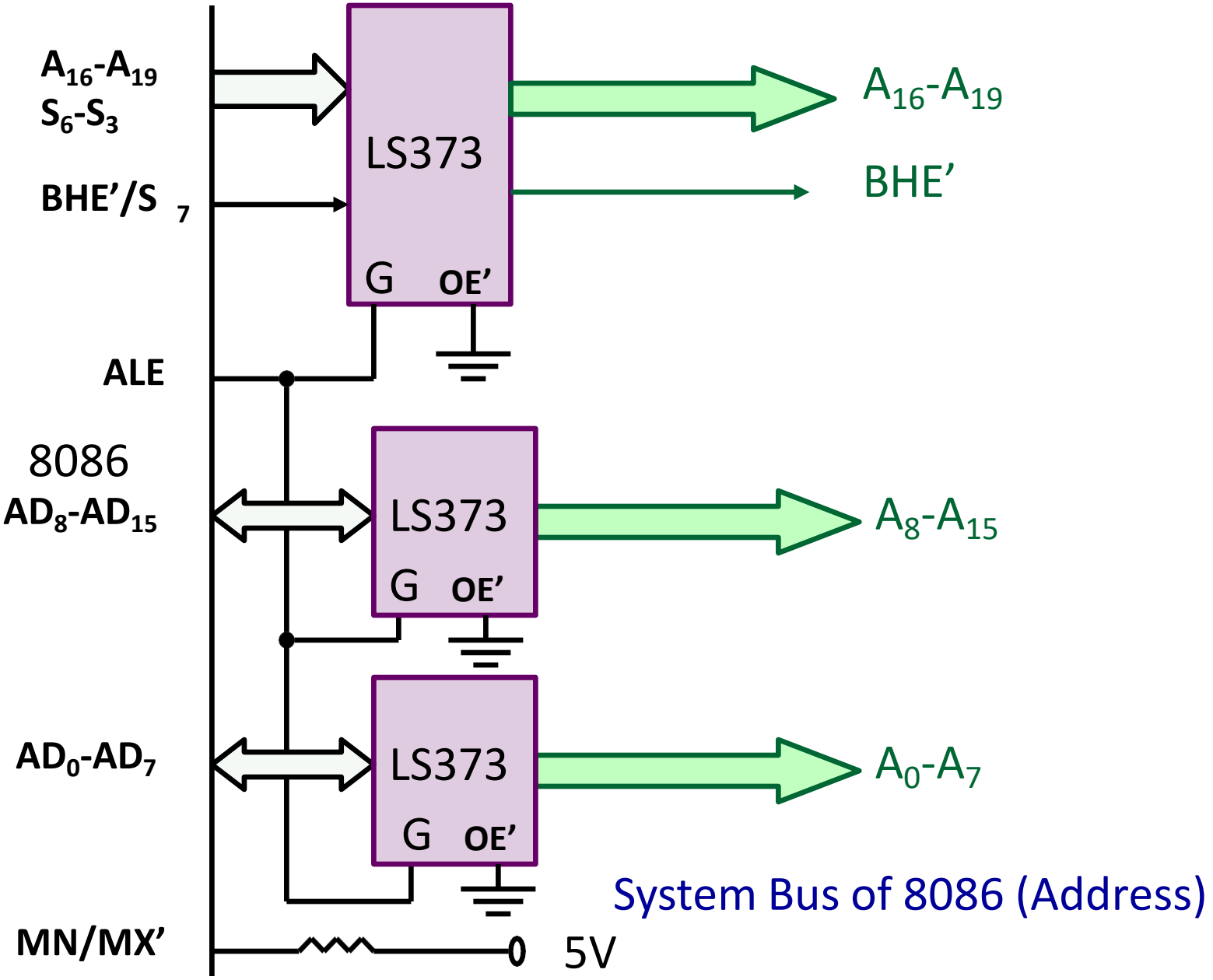
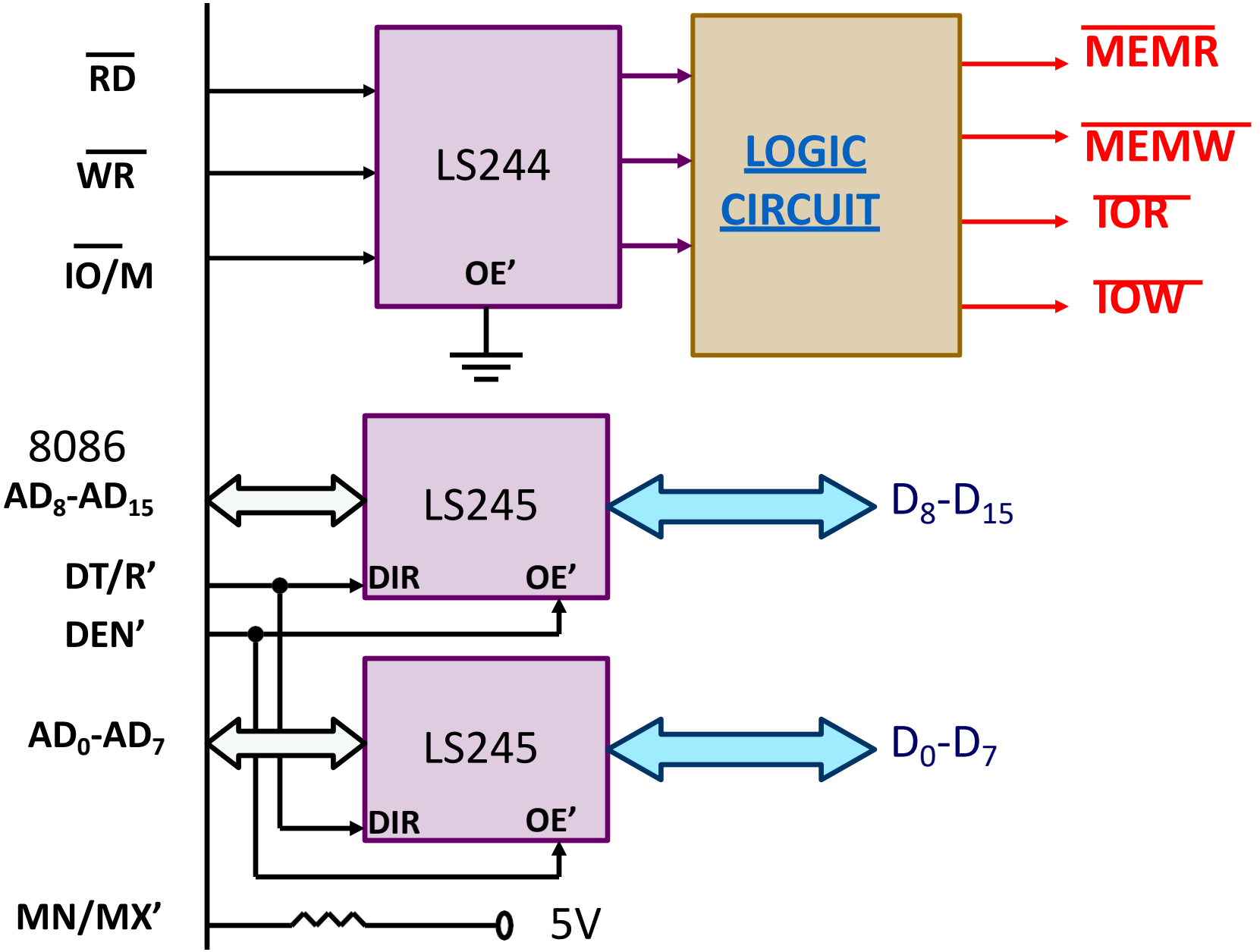
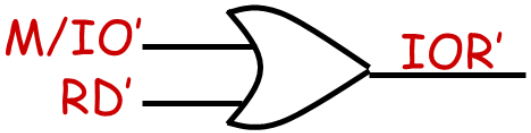

5 V
VCC
MN/MX
TEST
NC
HLDA
INTR
8259
INTA
15 MHz
X 1
X 2
RDY1
RDY2
RESET
8284
CLK
5 V
F/C
READY
CYNC
AEN 1
AEN 2
RES
5 V
RESET
CLK
READY
NMI
HOLD
GND

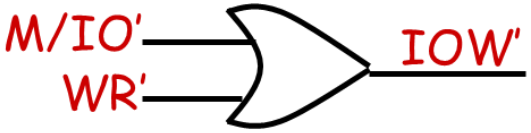
8086 Inputs


A16-A19
S6-S3
BHE'/S7
LS373
G
OE'
A16-A19
BHE'
ALE
8086
AD8-AD15
LS373
G
OE'
A8-A15
AD0-AD7
LS373
G
OE'
A0-A7
MN/MX'
5V
System Bus of 8086 (Address)

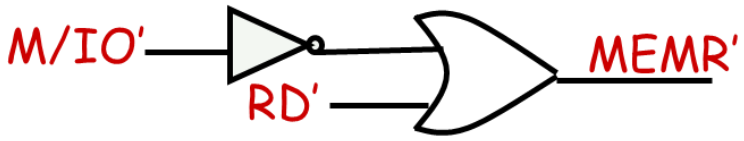


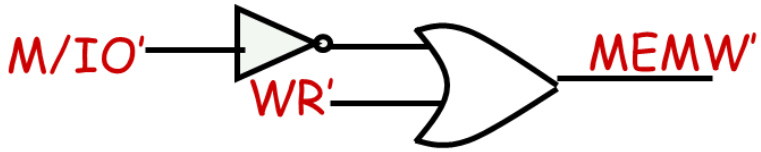
System Bus of 8086(Data + Control)



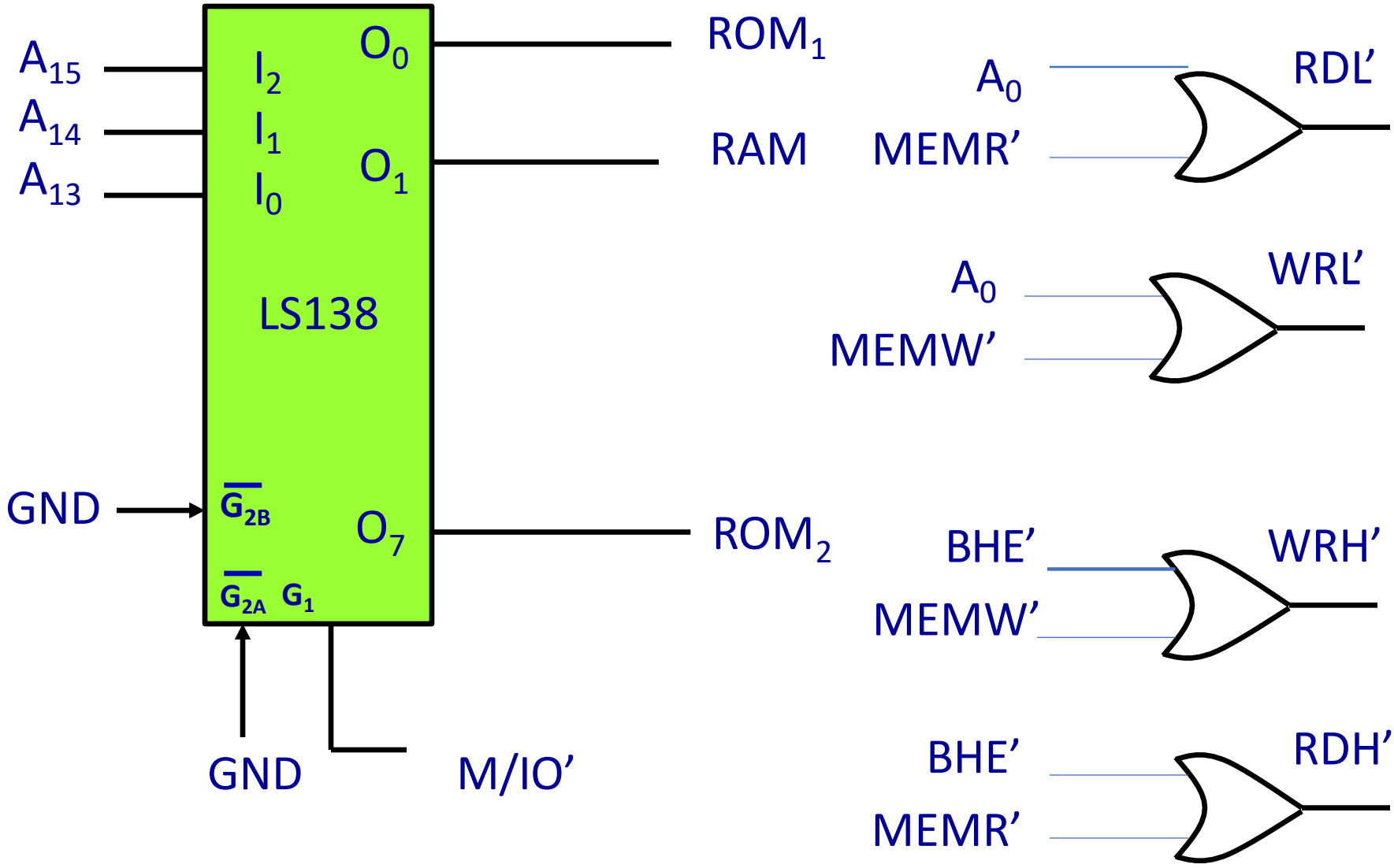


M/IO'	RD'	WR'	Bus cycle
1	0	1	MEMR'
1	1	0	MEMW'
0	0	1	IOR'
0	1	0	IOW'

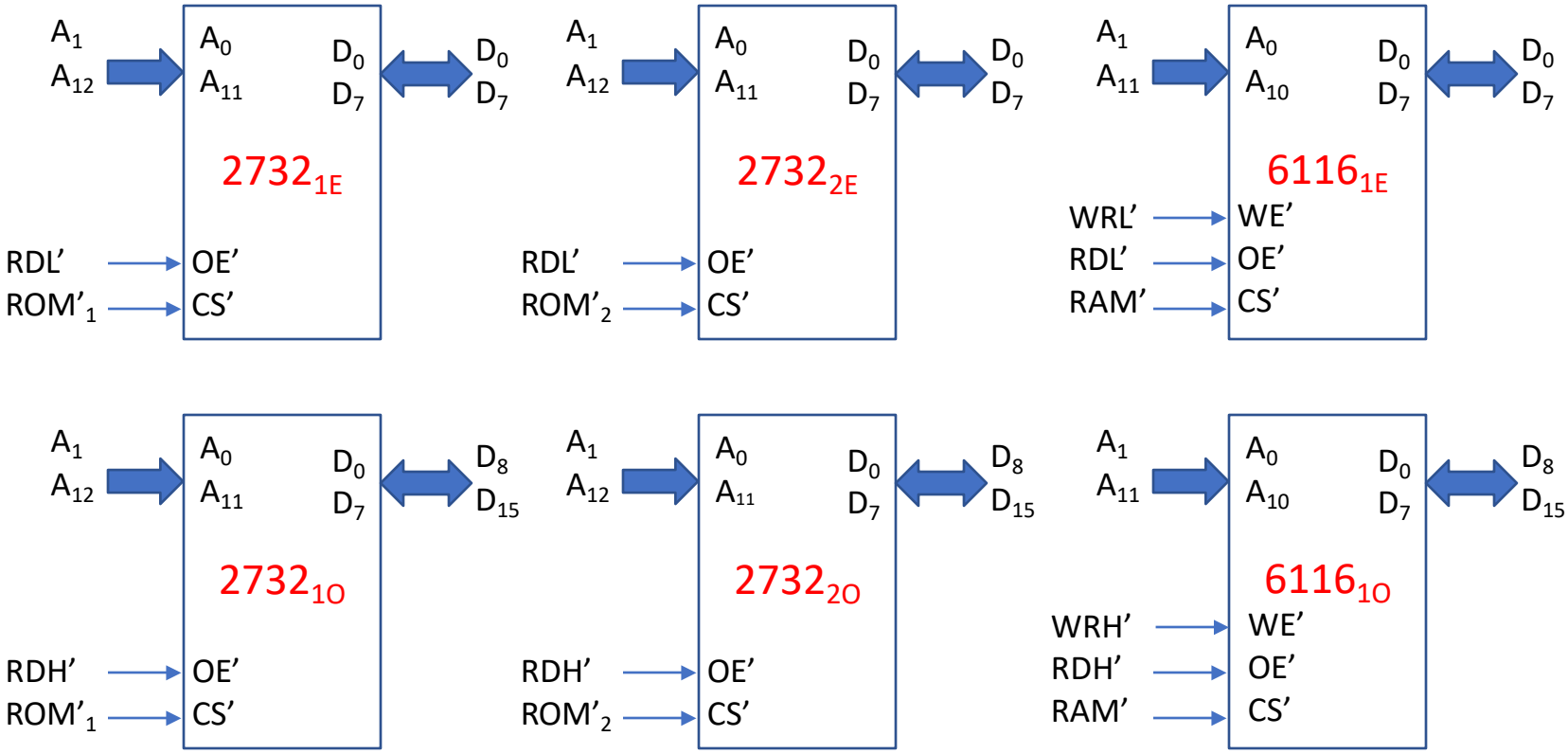




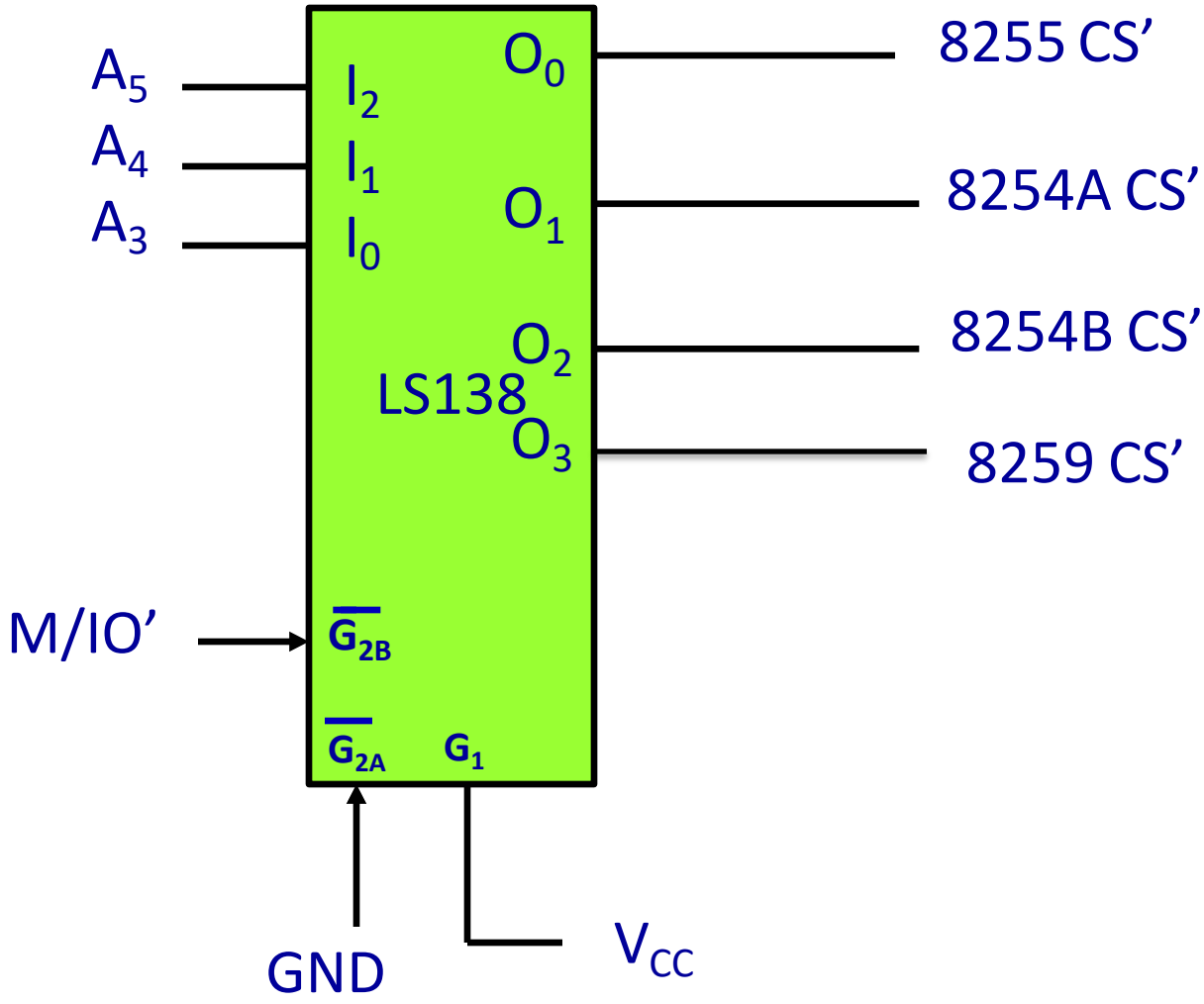
back



Memory Decoder

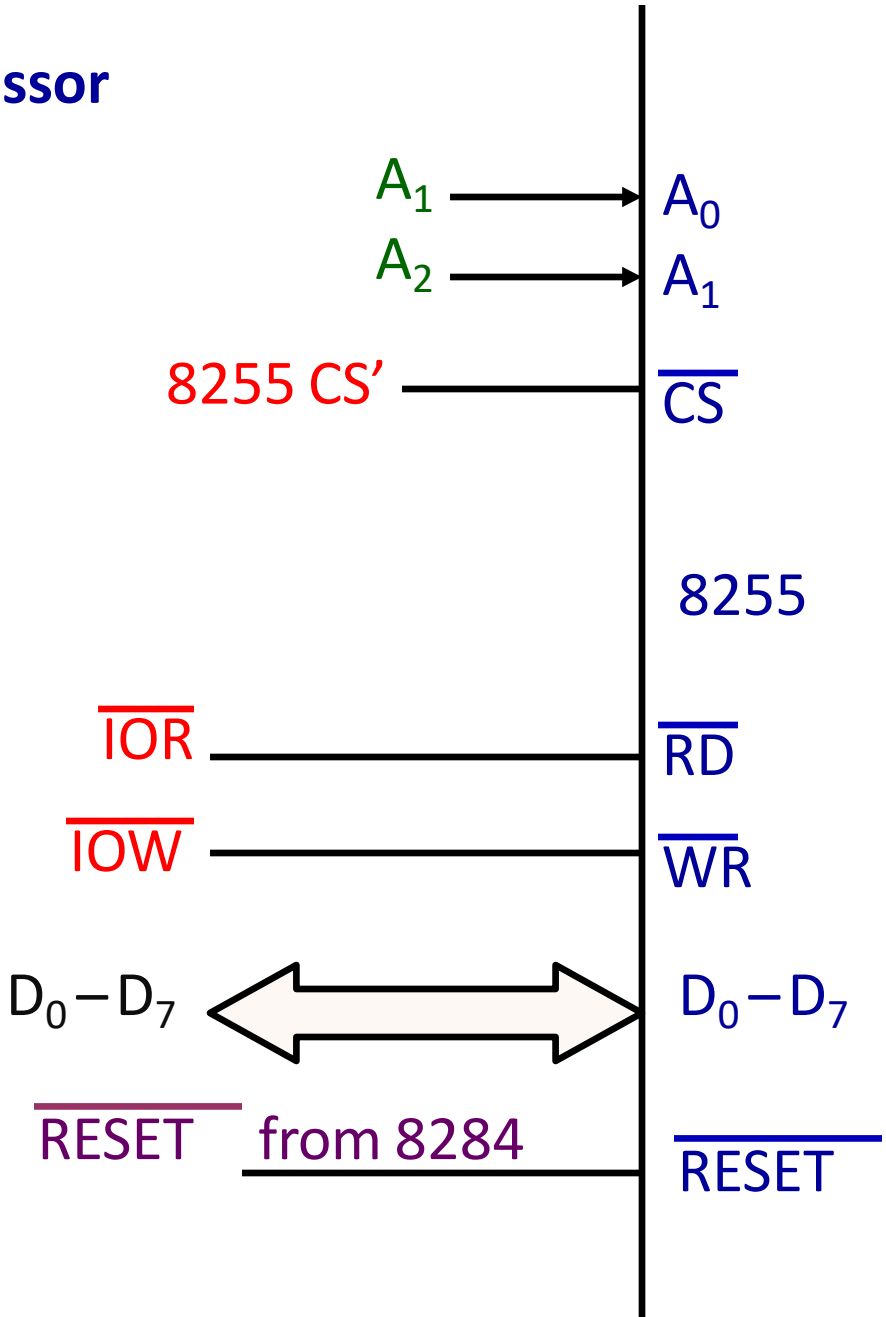


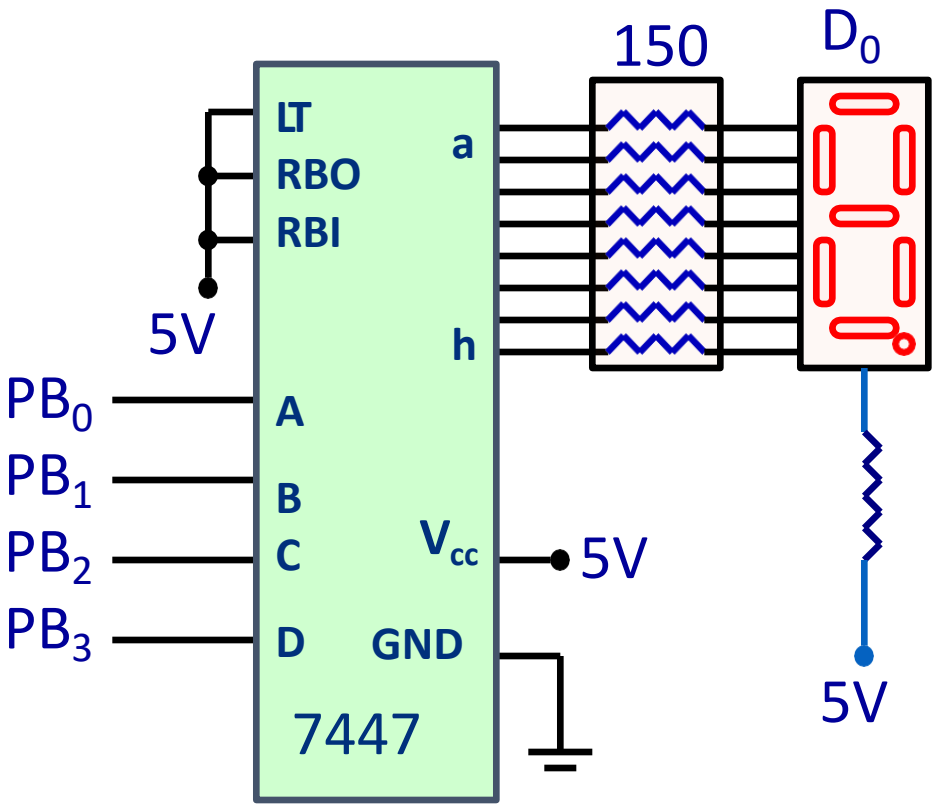
Memory Interfacing

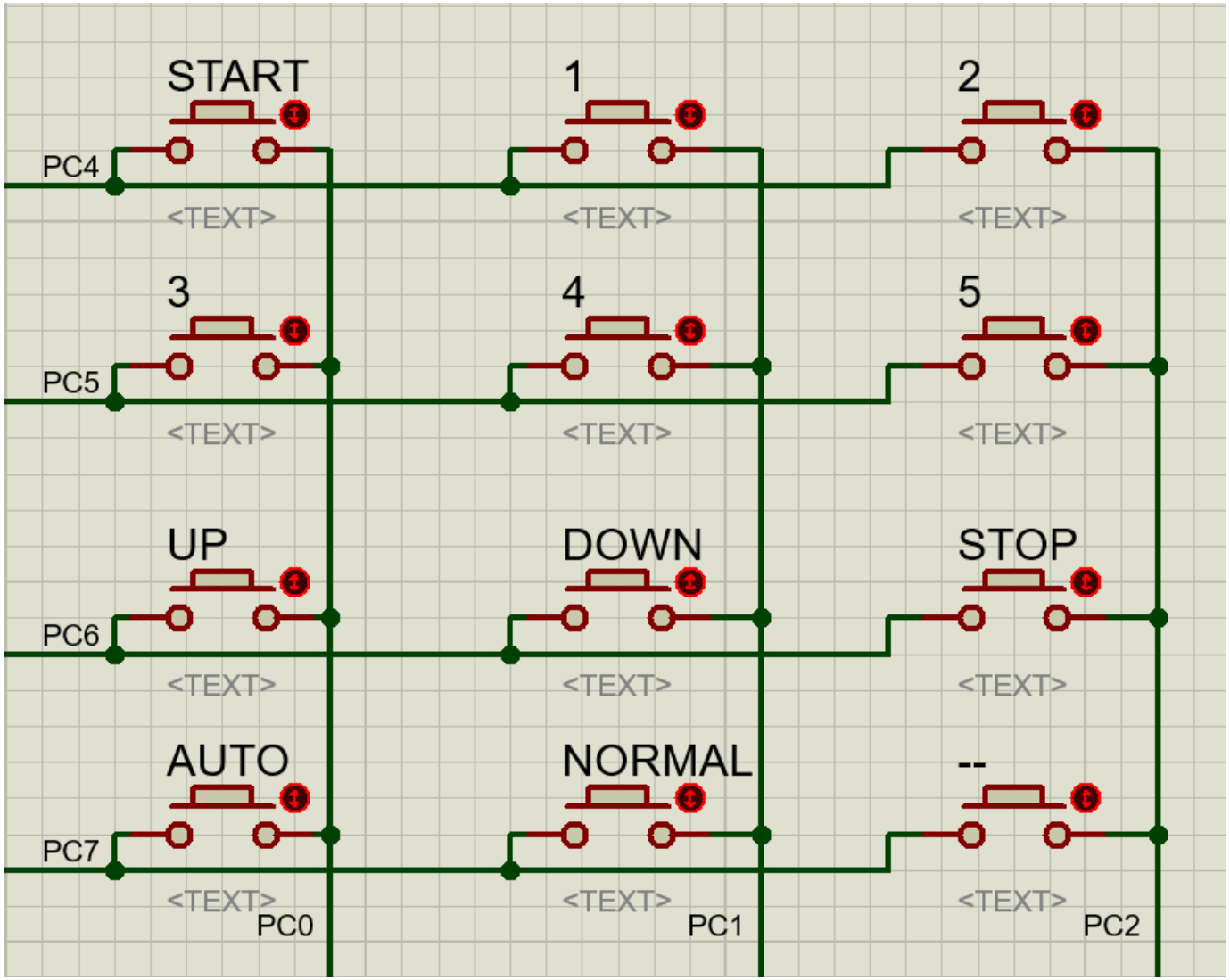

A5
A4
A3
I2
I1
I0
O0
O1
O2
O3
LS138
8255 CS'
8254A CS'
8254B CS'
8259 CS'
M/IO'
G2B
G2A
G1
GND
VCC

I/O Decoder

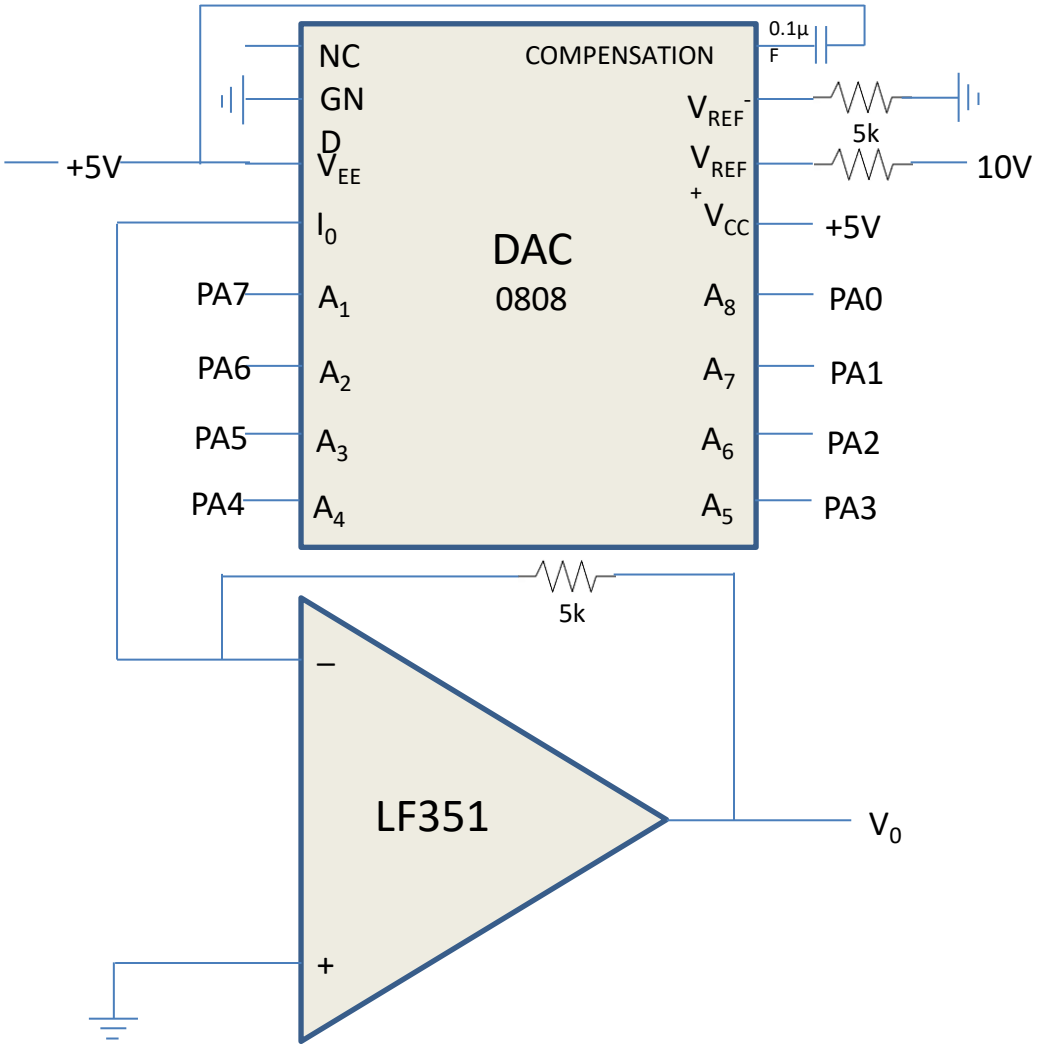
8255 Interface to the processor




150
D_0
LT
RBO
RBI
5V
a
h
PB_0
A
PB_1
B
PB_2
C
V_{cc}
5V
PB_3
D
GND
7447
5V

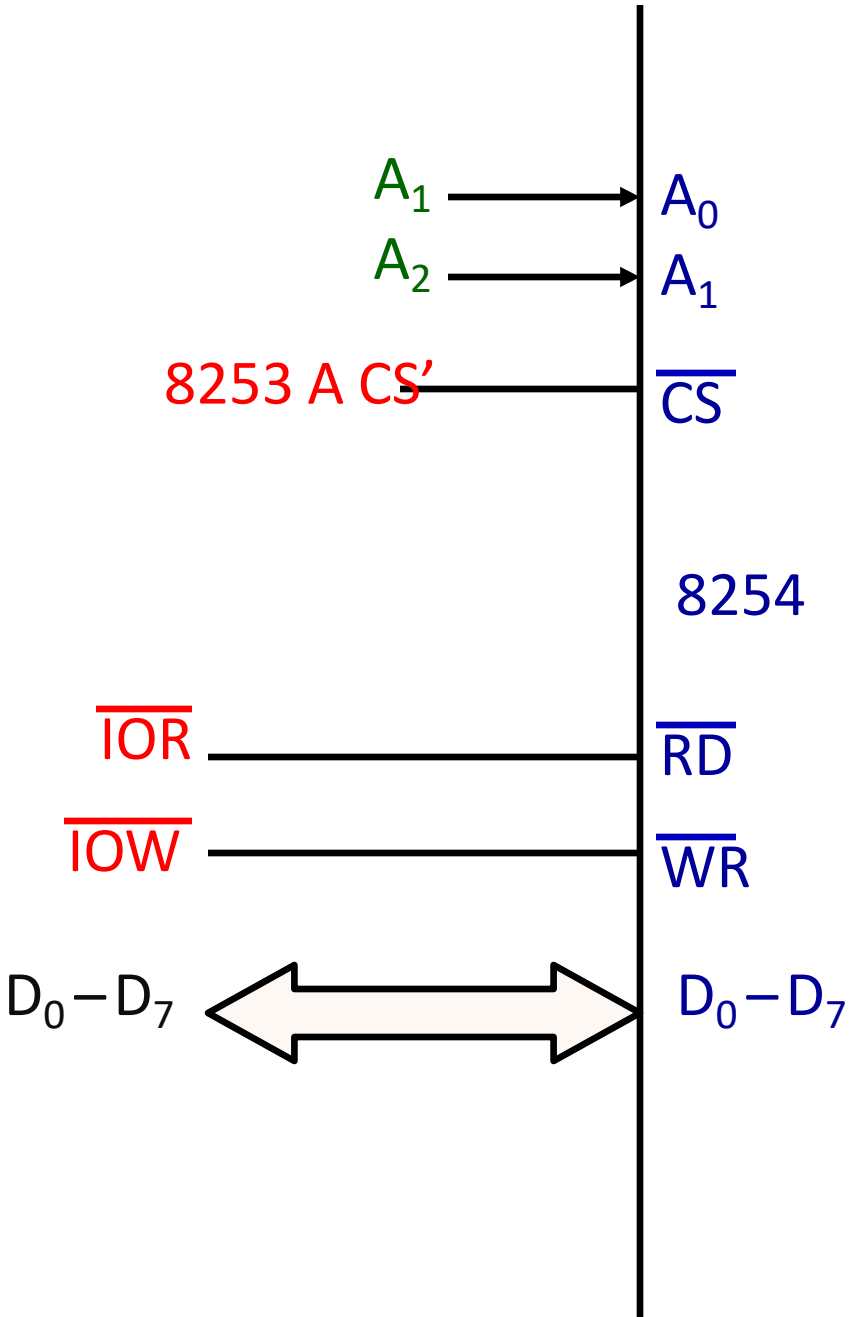

START
1
2
3
4
5
UP
DOWN
STOP
AUTO
NORMAL
--
PC4
PC5
PC6
PC7
PC0
PC1
PC2
<TEXT>

KEYPAD

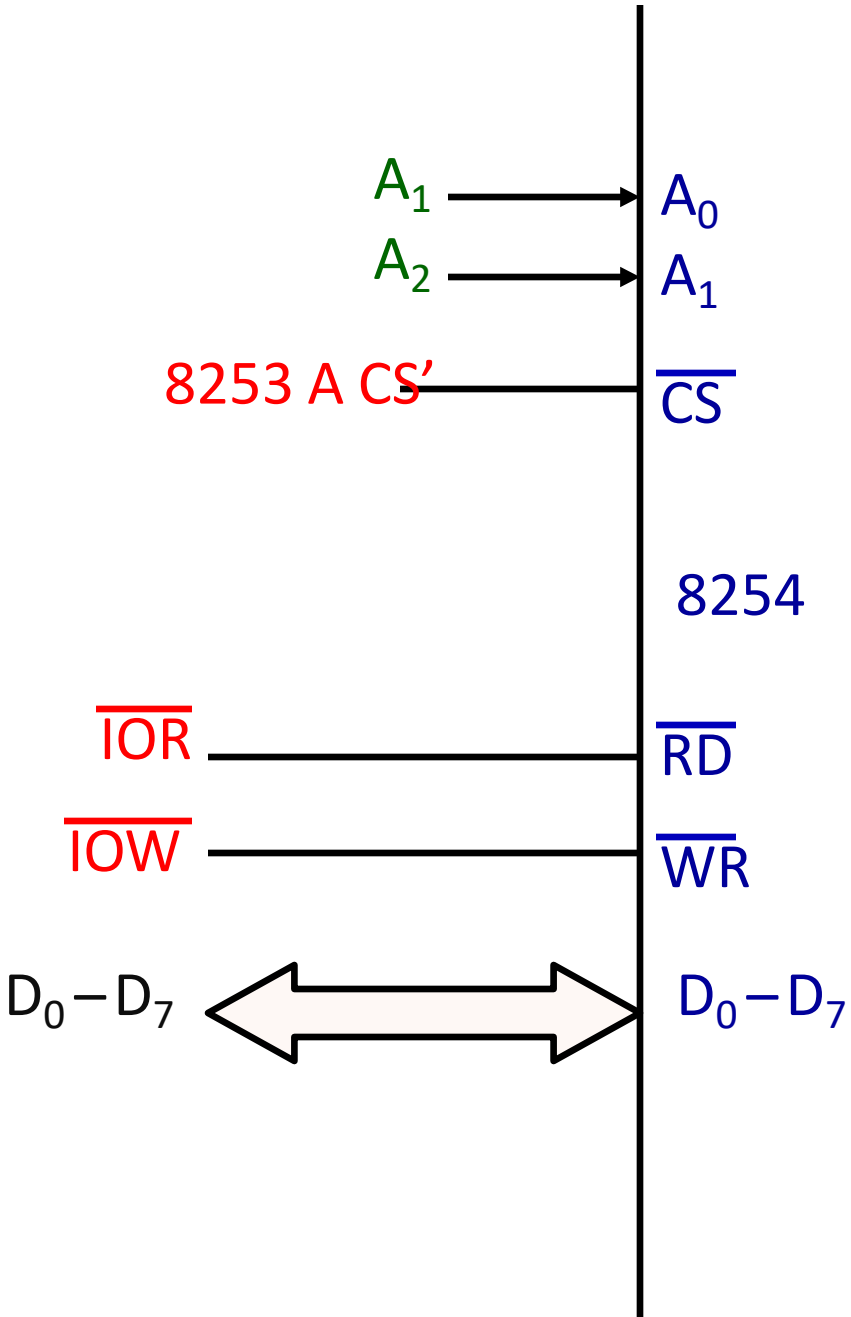

NC
COMPENSATION
0.1µ
F
GN
V_{REF}^-
5k
D
V_{EE}
V_{REF}^+
10V
+5V
I_0
V_{CC}
+5V
DAC
0808
PA7
A_1
A_8
PA0
PA6
A_2
A_7
PA1
PA5
A_3
A_6
PA2
PA4
A_4
A_5
PA3
5k
–
LF351
V_0
+

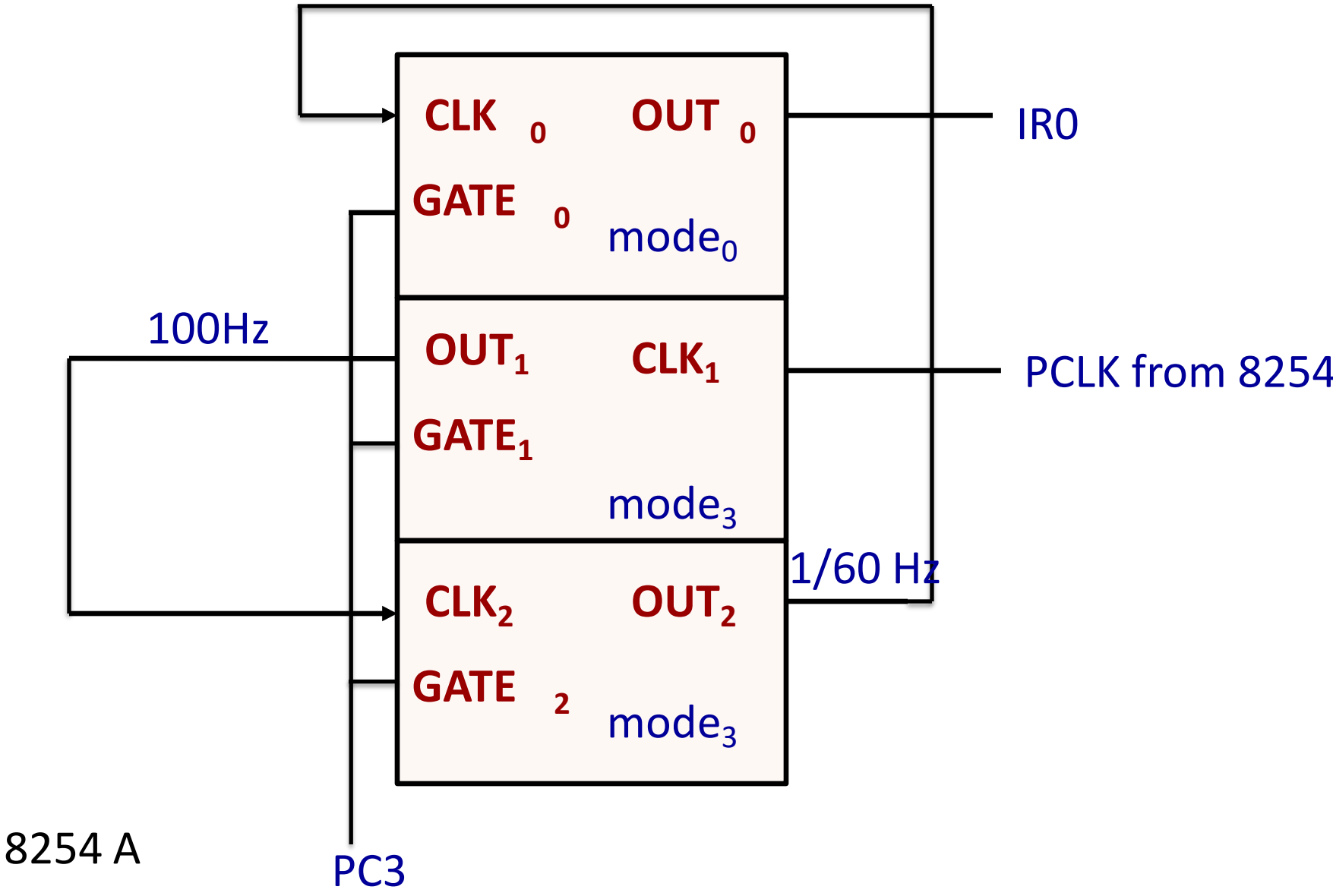
DAC 0808

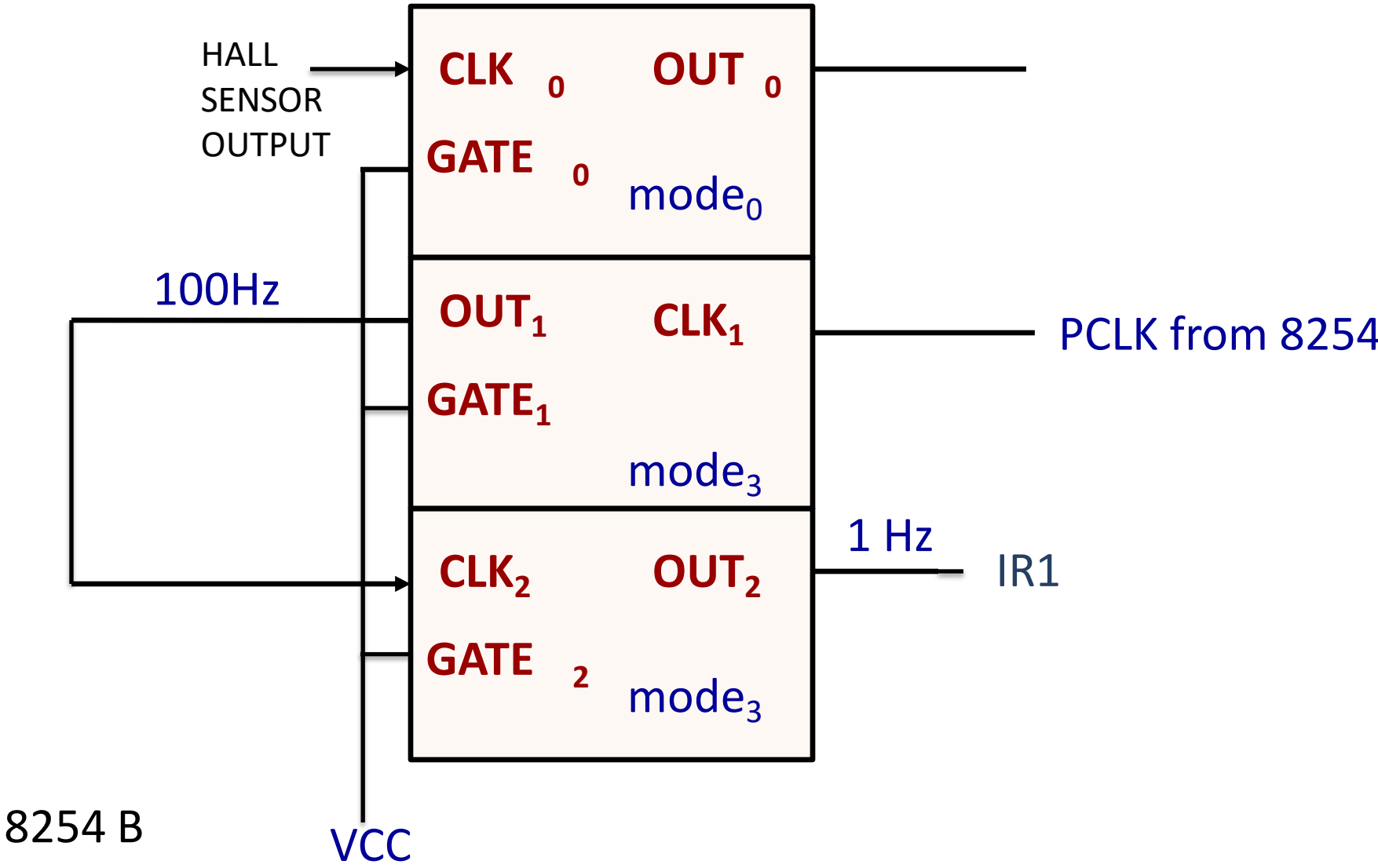
8254 (A) Interface to the processor

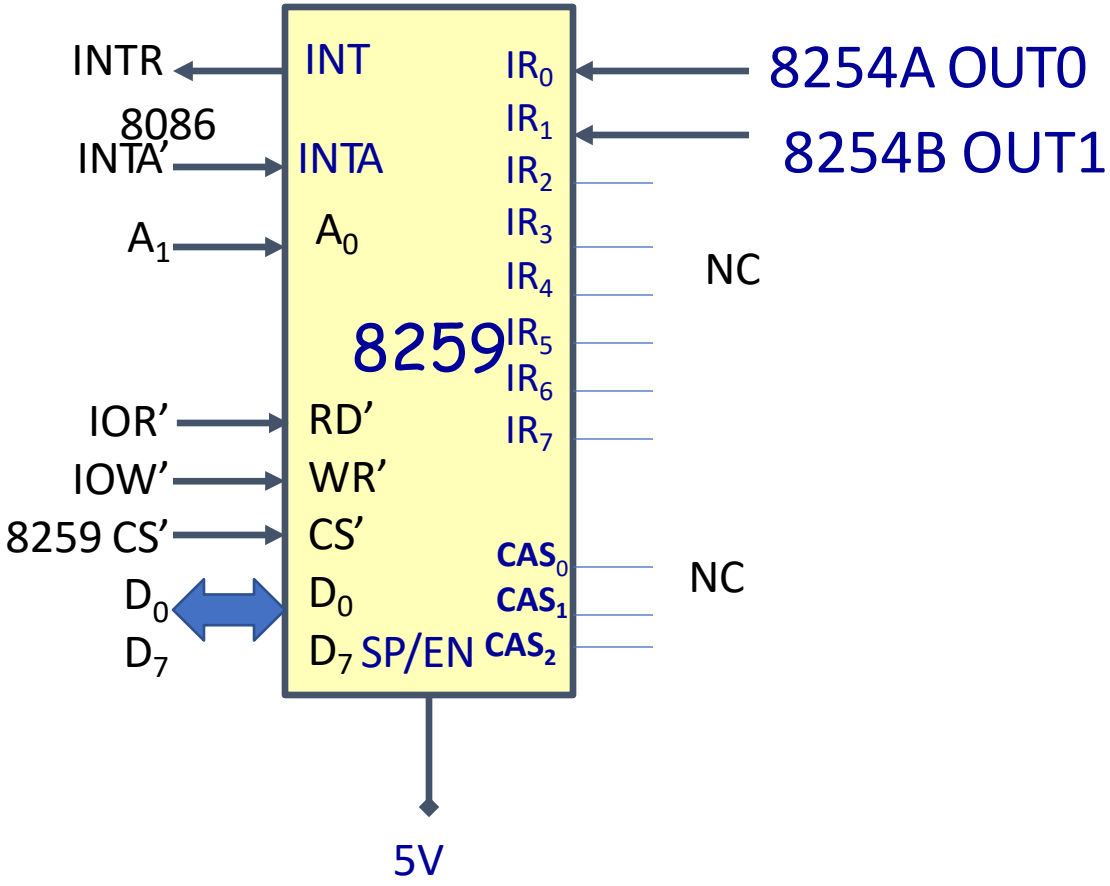


8254 (B) Interface to the processor



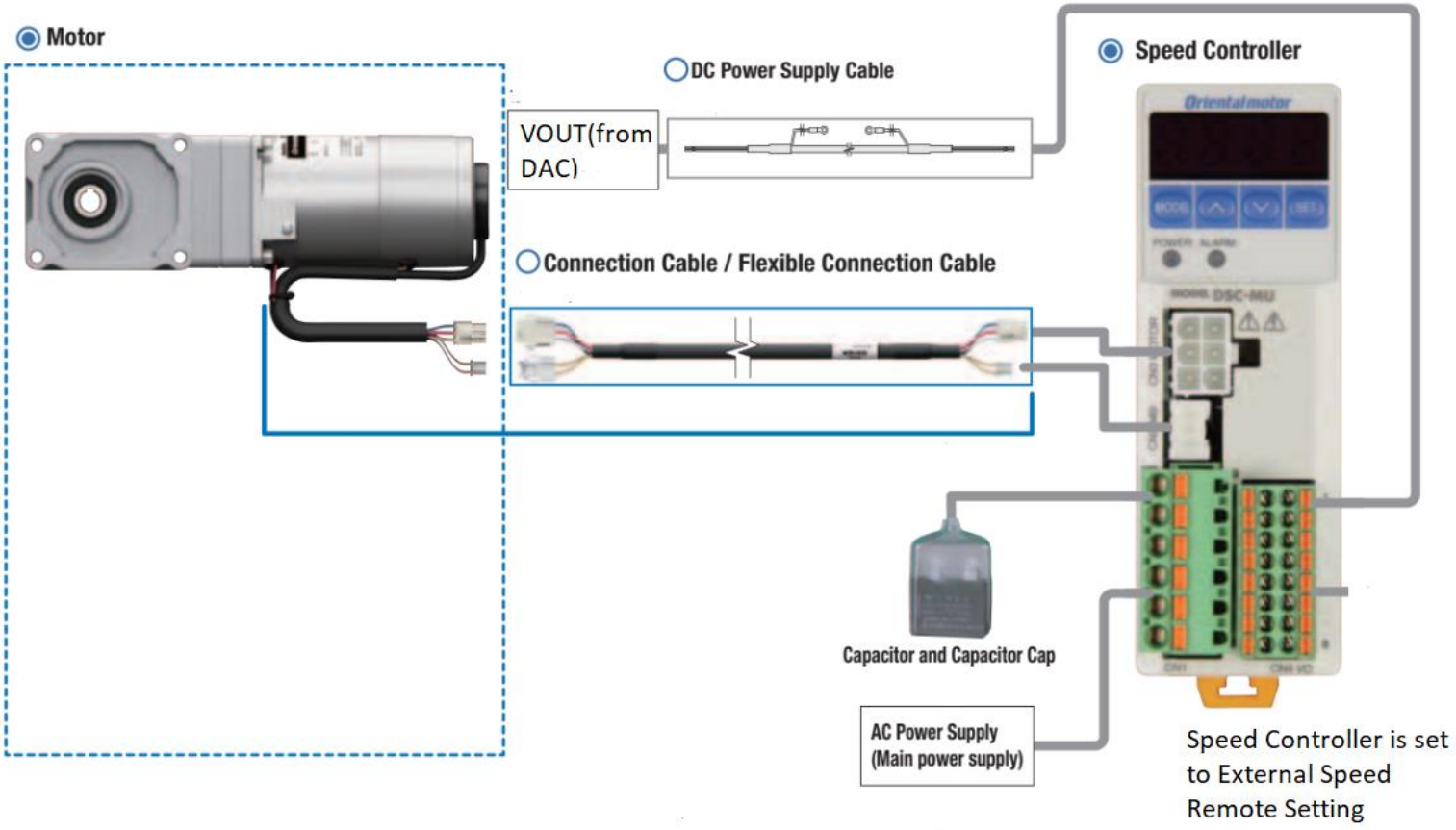

CLK 0
OUT 0
GATE 0
mode0
IR0
100Hz
OUT1
CLK1
GATE1
mode3
PCLK from 8254
1/60 Hz
CLK2
OUT2
GATE 2
mode3
8254 A
PC3

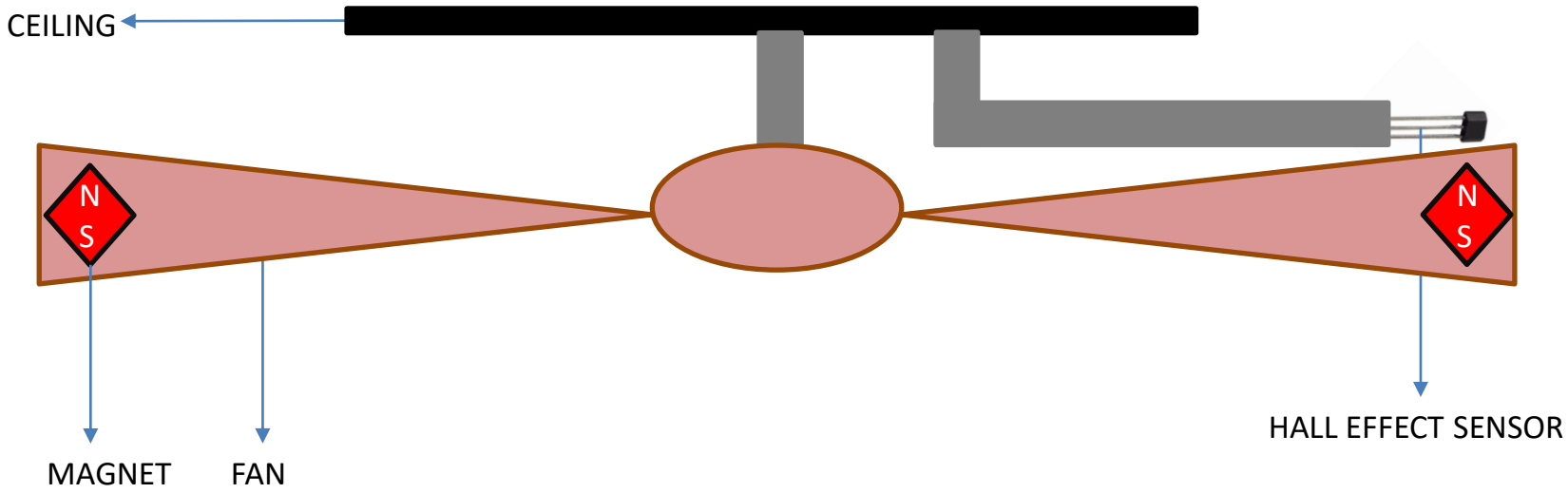

HALL
SENSOR
OUTPUT
CLK 0
OUT 0
GATE 0
mode0
100Hz
OUT1
CLK1
GATE1
mode3
PCLK from 8254
1 Hz
IR1
CLK2
OUT2
GATE 2
mode3
8254 B
VCC


INTR
INT
8086
INTA'
INTA
A1
A0
8259
IOR'
RD'
IOW'
WR'
8259 CS'
CS'
D0
D0
D7
D7 SP/EN
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
CAS0
CAS1
CAS2
8254A OUT0
8254B OUT1
NC
NC
5V

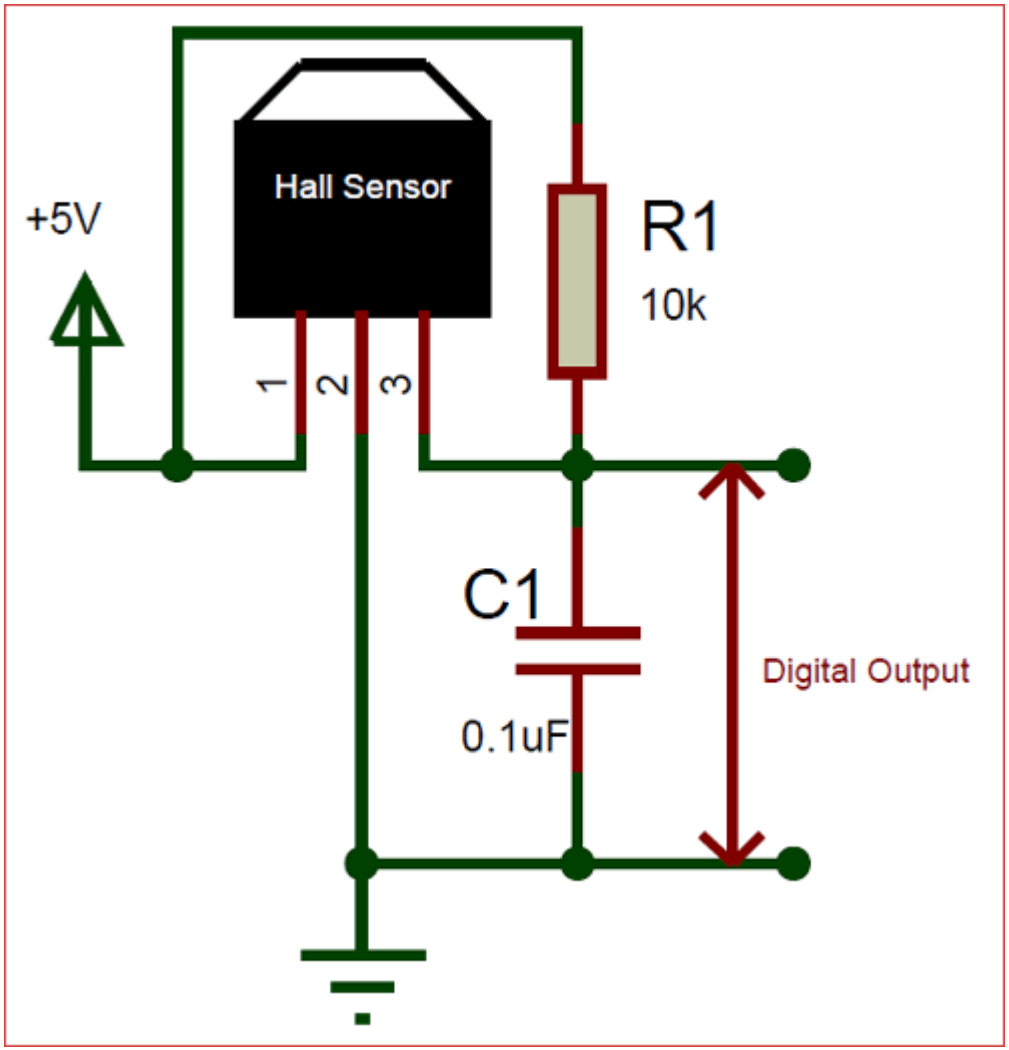
8259

Motor and Speed Controller





SYSTEM SETUP



HALL EFFECT SENSOR CIRCUIT