

**ECE 531**  
**Microelectronics**  
**Assignment 3**

**Aditya Sankaramanchi**  
**101266059**

## **Problem 1:**

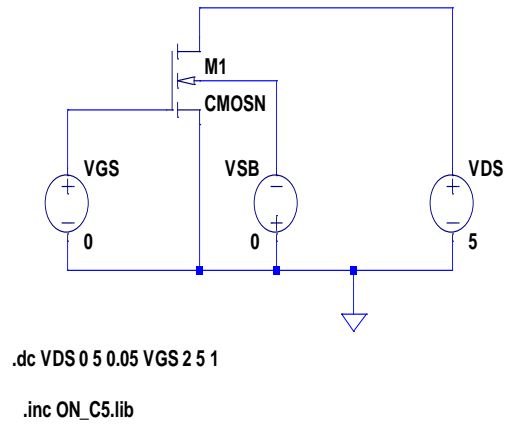


Figure 1 : LTSpice circuit diagram of NMOS transistor using CMOSN model.

Here  $W/L = 7.2 \mu\text{m} / 0.6 \mu\text{m}$

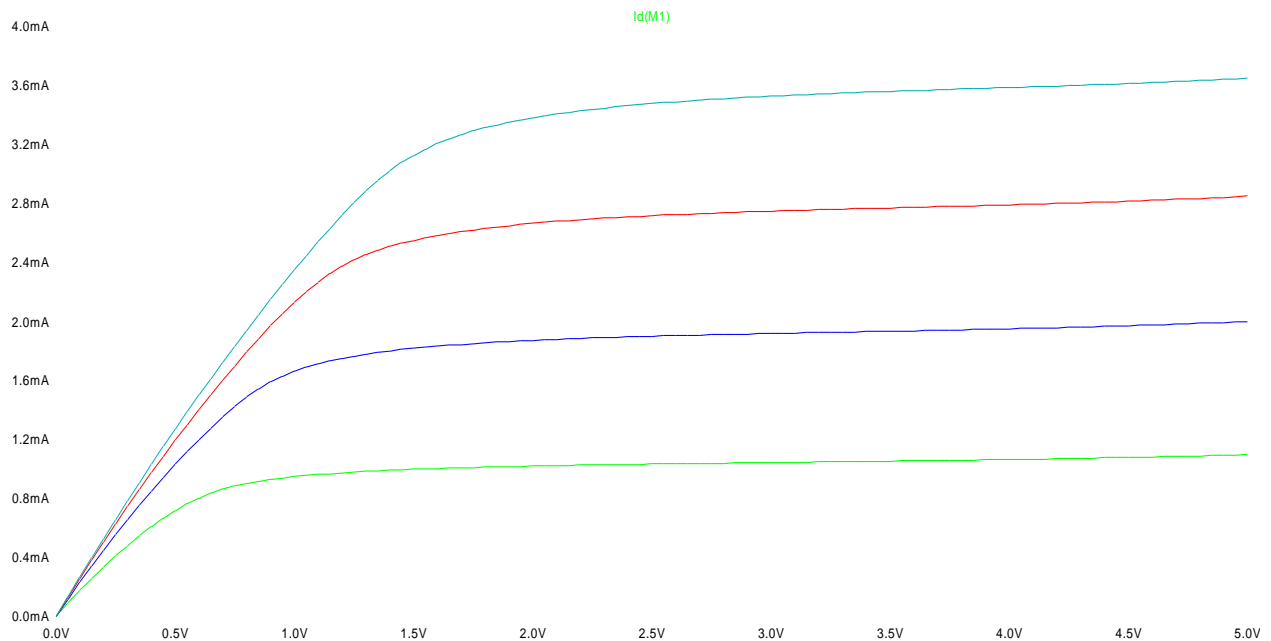
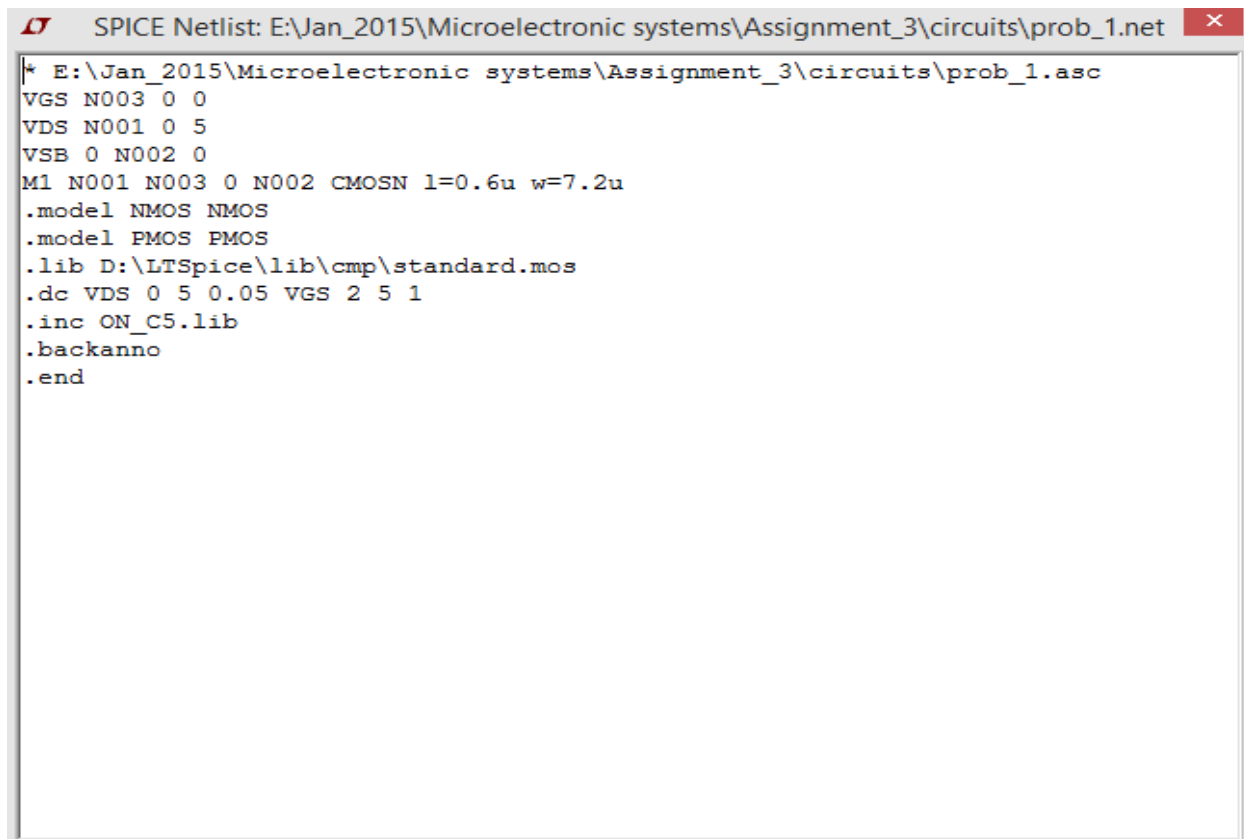


Figure 2: I-V curves for an NMOS transistor



The image shows a window titled "SPICE Netlist: E:\Jan\_2015\Microelectronic systems\Assignment\_3\circuits\prob\_1.net". The window contains a text editor with the following SPICE netlist code:

```
* E:\Jan_2015\Microelectronic systems\Assignment_3\circuits\prob_1.asc
VGS N003 0 0
VDS N001 0 5
VSB 0 N002 0
M1 N001 N003 0 N002 CMOSN l=0.6u w=7.2u
.model NMOS NMOS
.model PMOS PMOS
.lib D:\LTSpice\lib\cmp\standard.mos
.dc VDS 0 5 0.05 VGS 2 5 1
.inc ON_C5.lib
.backanno
.end
```

Figure 3: Spice Netlist

## **Problem 2:**

NMOS transistor in series:

Here width  $W = 3\text{ }\mu\text{m}$  ;  $L = 0.6\text{ }\mu\text{m}$

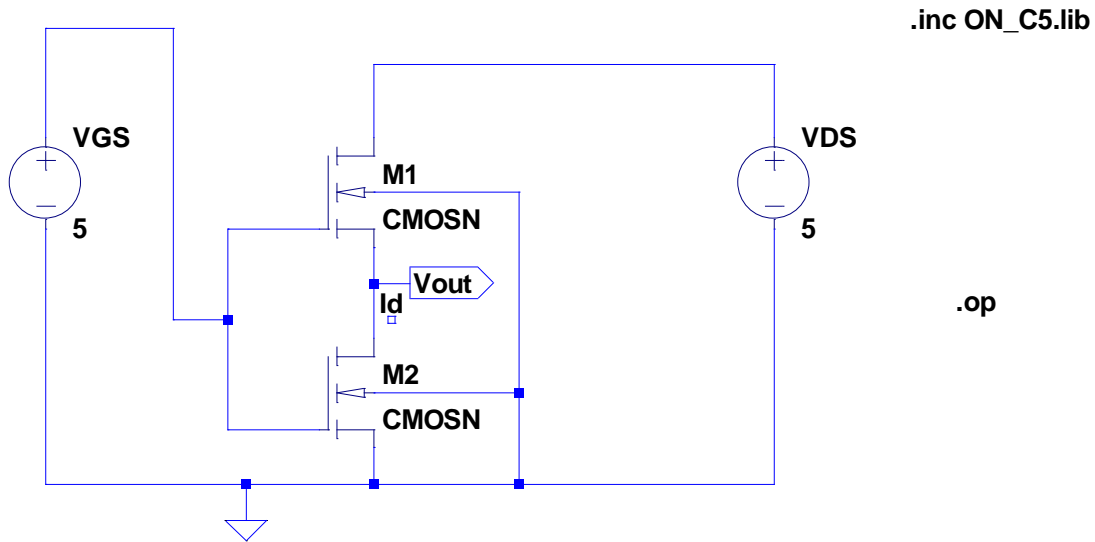


Figure 4: NMOS transistors in series

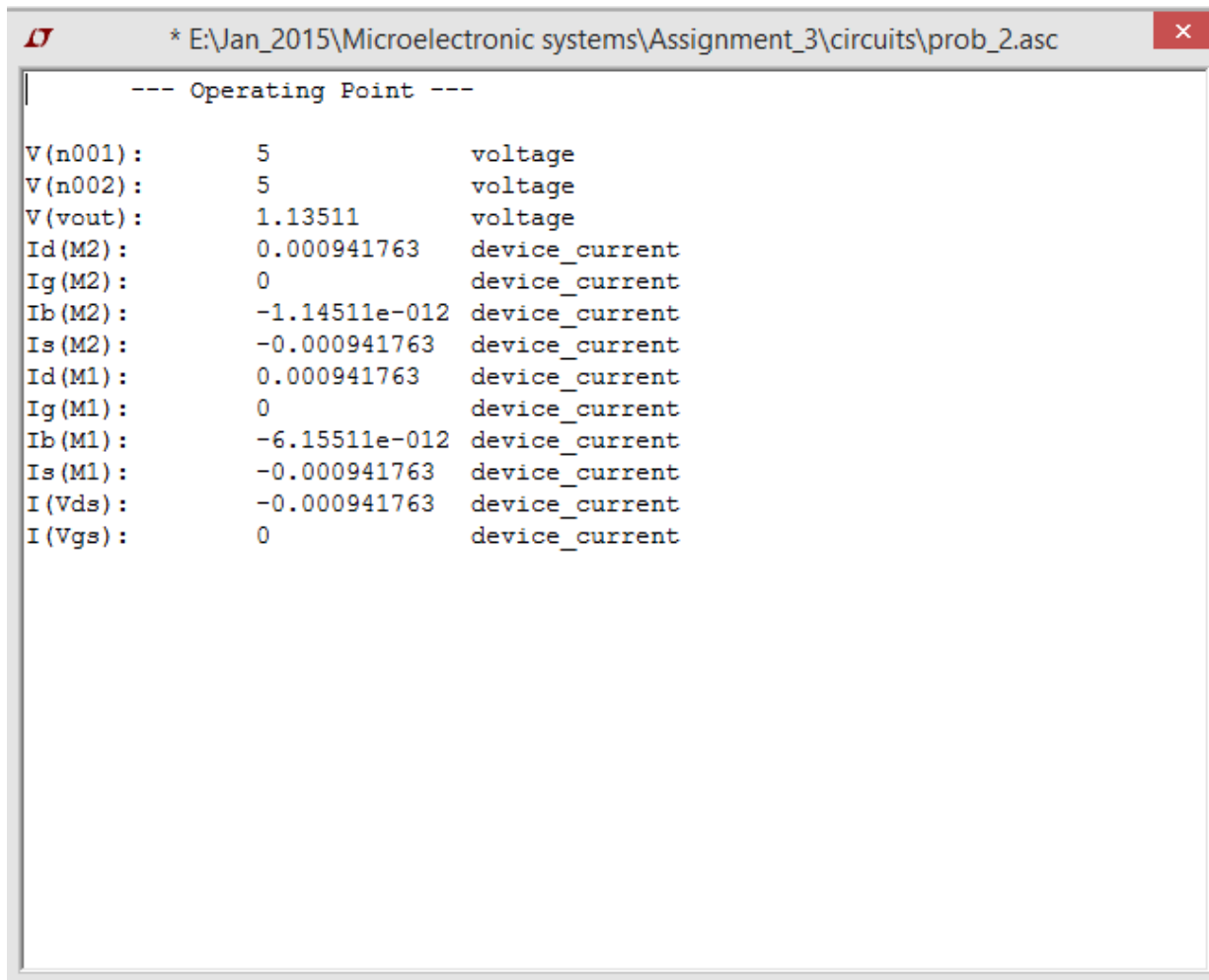


Figure 5: Operating point for NMOS transistors in series

Voltage  $V(\text{out}) = 1.135$  Volts. Current  $I_d = 0.000941$  amps =  $941 \mu\text{A}$

### **Problem 3:**

Given  $W = 8 \lambda = 8 \cdot 0.3 \mu\text{m} = 2.4 \mu\text{m}$

$L = 2 \lambda = 2 \cdot 0.3 \mu\text{m} = 0.6 \mu\text{m}$

$V_{DD} = 5 \text{ V}$

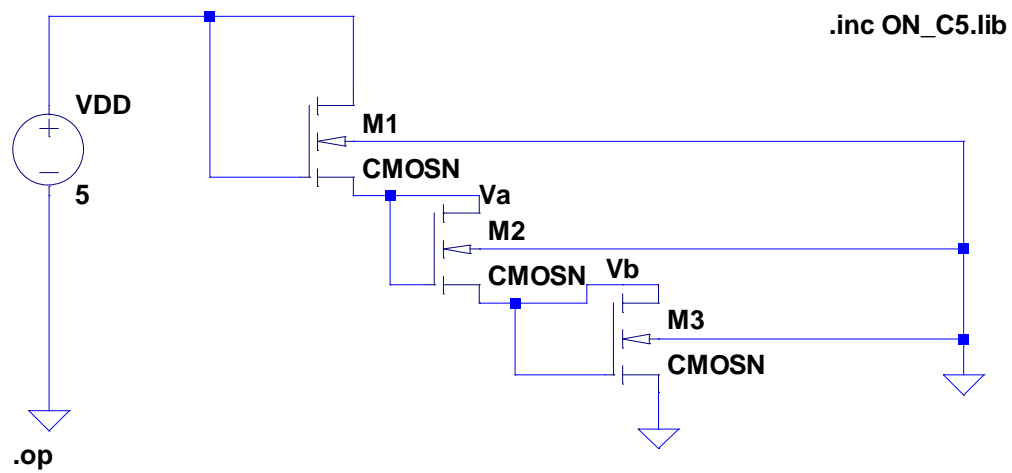


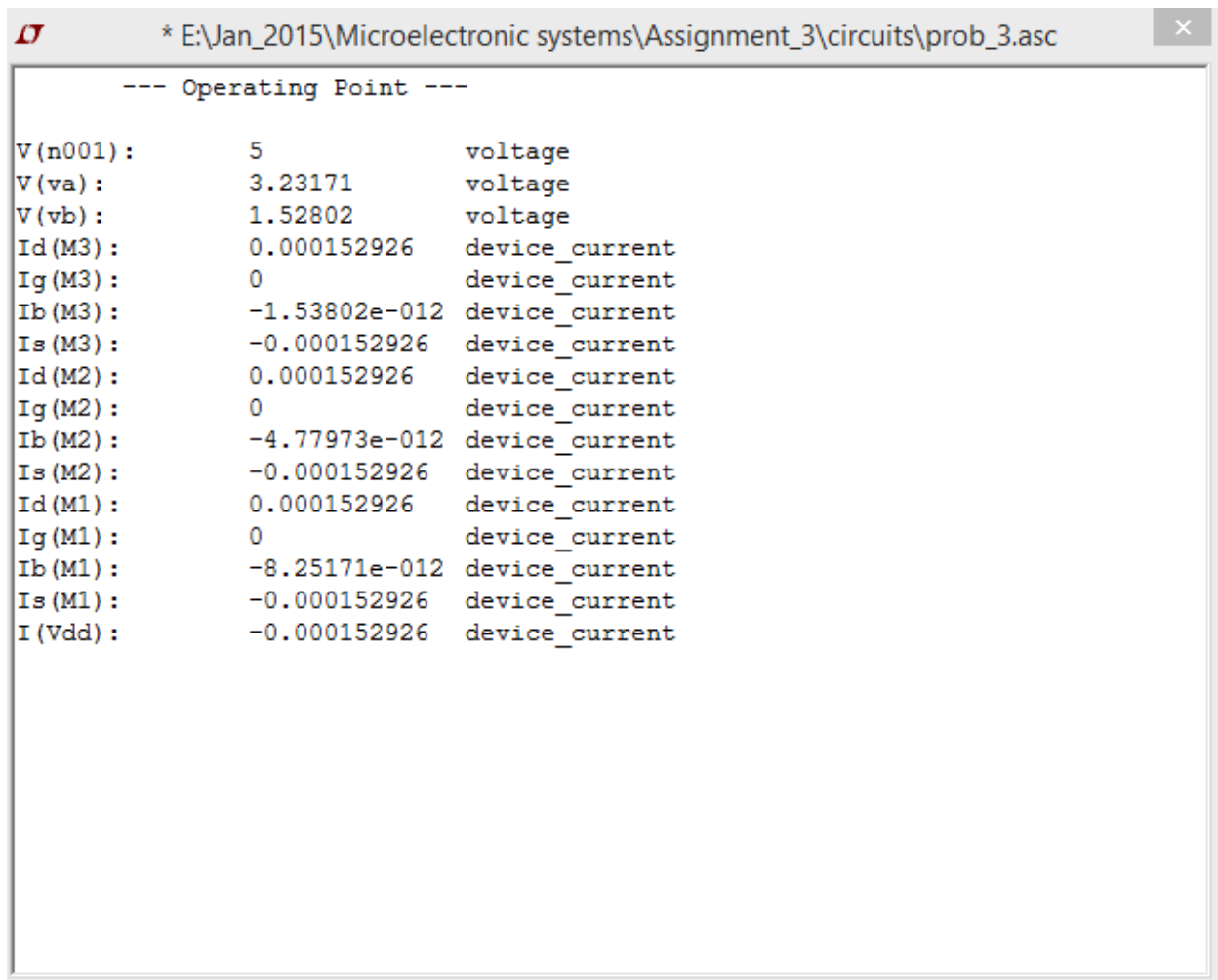
Figure 6: LTSpice figure of the required transistor circuit

```

SPICE Netlist: E:\Jan_2015\Microelectronic systems\Assignment_3\circuits\prob_3.net
* E:\Jan_2015\Microelectronic systems\Assignment_3\circuits\prob_3.asc
M1 N001 N001 Va 0 CMOSN l=0.6u w=2.4u
M2 Va Va Vb 0 CMOSN l=0.6u w=2.4u
M3 Vb Vb 0 0 CMOSN l=0.6u w=2.4u
VDD N001 0 5
.model NMOS NMOS
.model PMOS PMOS
.lib D:\LTSpice\lib\cmp\standard.mos
.op
.inc ON_C5.lib
.backanno
.end

```

Figure 7: Spcie Netlist of the required transistor circuit



```

* E:\Jan_2015\Microelectronic systems\Assignment_3\circuits\prob_3.asc

--- Operating Point ---

V(n001):      5          voltage
V(va):        3.23171    voltage
V(vb):        1.52802    voltage
Id(M3):       0.000152926 device_current
Ig(M3):       0          device_current
Ib(M3):       -1.53802e-012 device_current
Is(M3):       -0.000152926 device_current
Id(M2):       0.000152926 device_current
Ig(M2):       0          device_current
Ib(M2):       -4.77973e-012 device_current
Is(M2):       -0.000152926 device_current
Id(M1):       0.000152926 device_current
Ig(M1):       0          device_current
Ib(M1):       -8.25171e-012 device_current
Is(M1):       -0.000152926 device_current
I(Vdd):       -0.000152926 device_current
  
```

From the spcie operating point figure

$$V_a = 3.23 \text{ V} ; V_b = 1.52 \text{ V} ;$$

And the currents Id, Is, Ig and Ib are obtained.

#### **Problem 4:**

- a. To find the threshold voltage if  $V_{sb} = 3V$

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

From the given values

$$\begin{aligned}
 V_T &= 0.8 + 0.6(\sqrt{2.4} - \sqrt{0.6}) \\
 &= 0.8 + 0.6 * 0.775
 \end{aligned}$$

$$V_T = 1.265 \text{ V}$$

b. To convert  $C_{j0}$  to units  $\text{fF}/\mu\text{m}^2$

Here  $f = 10^{-15}$   $\mu = 10^{-6}$

$$= 4 * 10^{-4} * \frac{10^{-15}}{10^{-15}} * \frac{10^{-6}}{10^{-6}} \frac{F}{m^2}$$

$$= 4 * 10^5 \frac{fF}{\mu m^2}$$

c. To find bottom capacitance. Given  $V_{sb} = 3V$ ;  $AS = 50p$

We have  $C_j = \frac{C_{j0}}{(1 - \frac{V_D}{\phi_0})^m}$

$$C_j = \frac{4 * 10^{-4}}{(1 - (\frac{-3}{0.74})^{0.43}}$$

$$C_j = 1.992 * 10^{-4} \frac{F}{m^2}$$

Bottom capacitance  $C_{bottom} = C_j * Area$

$$= 1.992 * 10^{-4} * 50 * 10^{-12}$$

$$= 99.6 * 10^{-16}$$

Bottom capacitance=9.96 fF



## Problem 5:

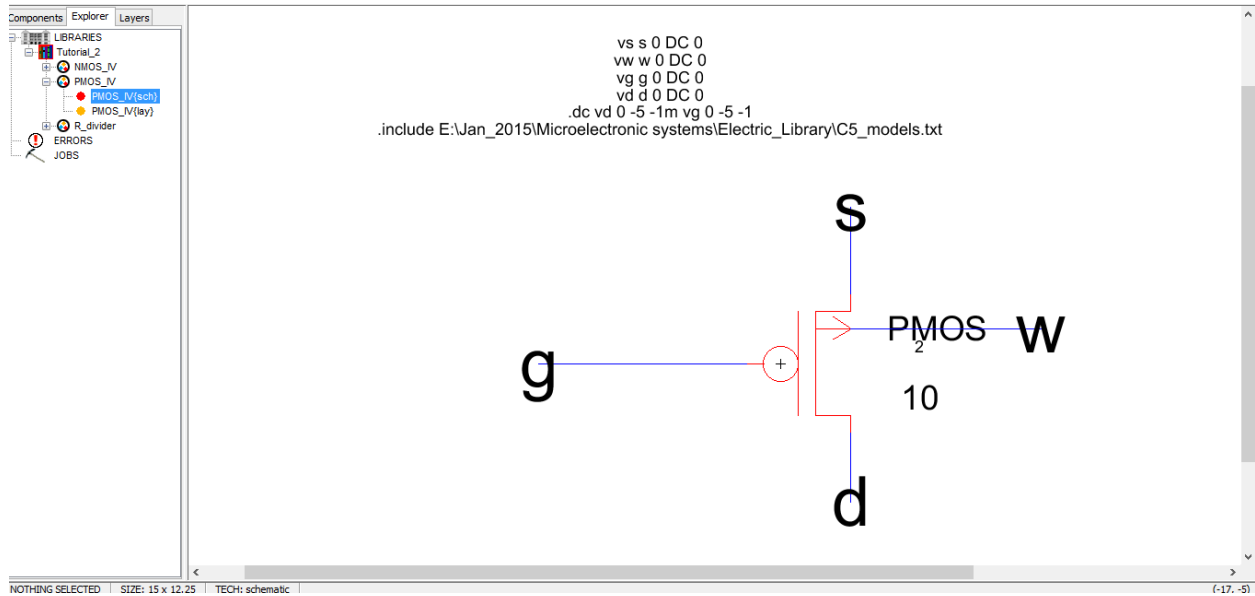


Figure 8 : Schematic view of PMOS Transistor

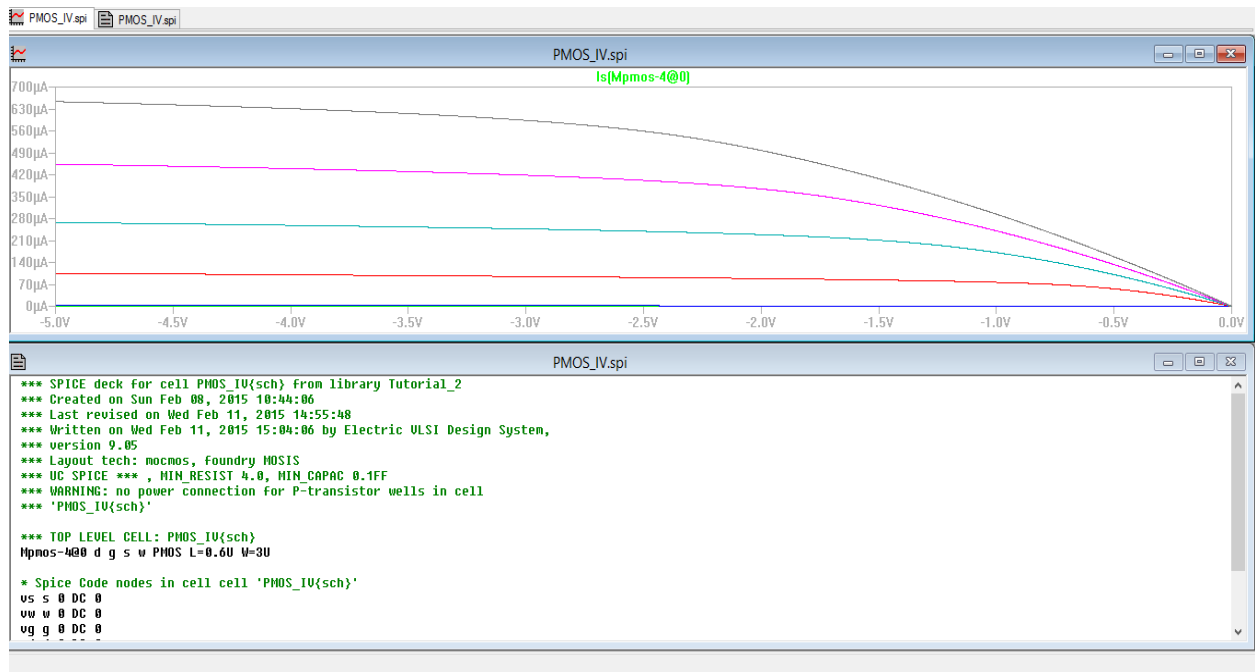


Figure 9 : Spice simulation view of PMOS transistor

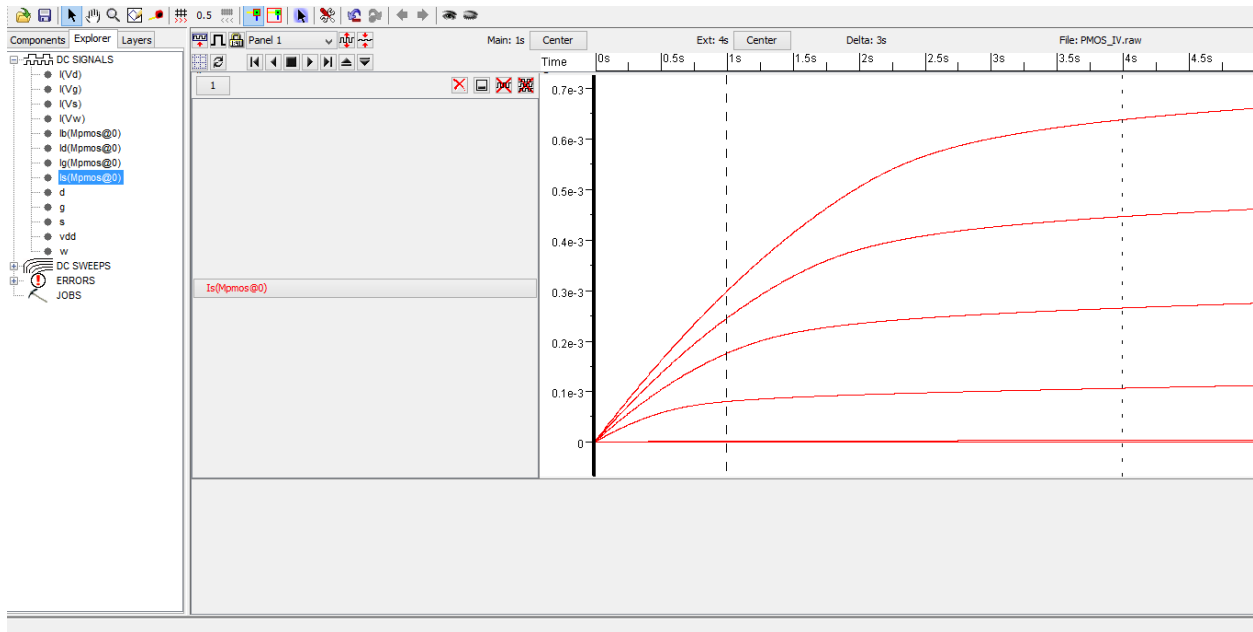


Figure 10: Electric simulation of PMOS transistor

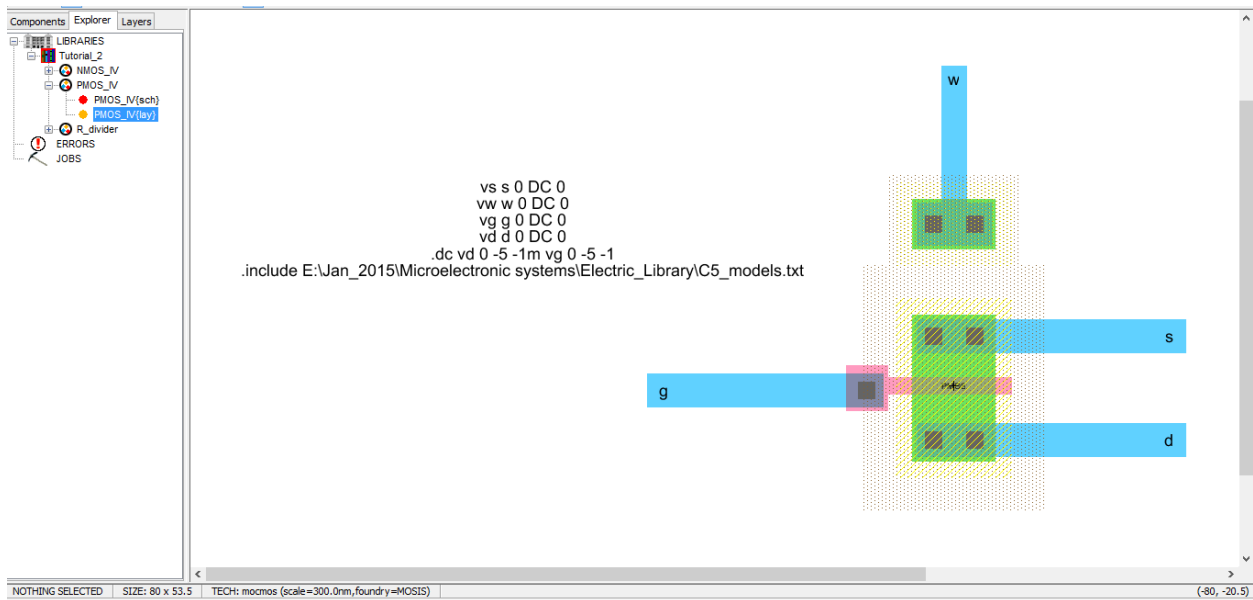


Figure 11: Layout view of PMOS transistor

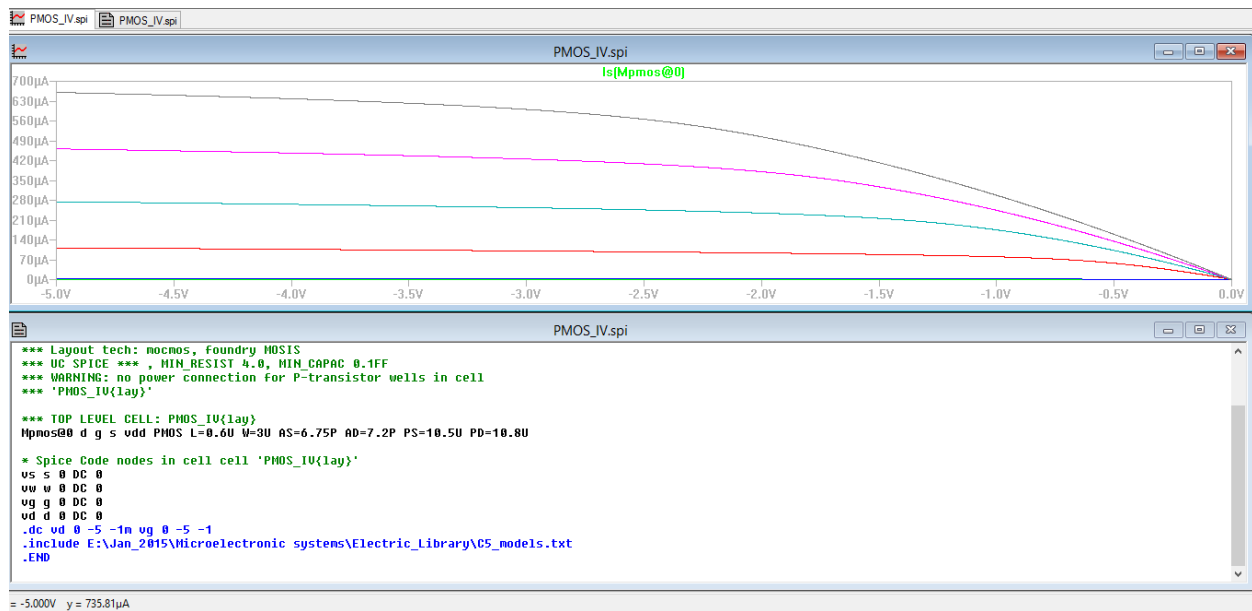


Figure 12: Spice simulation output of PMOS transistor

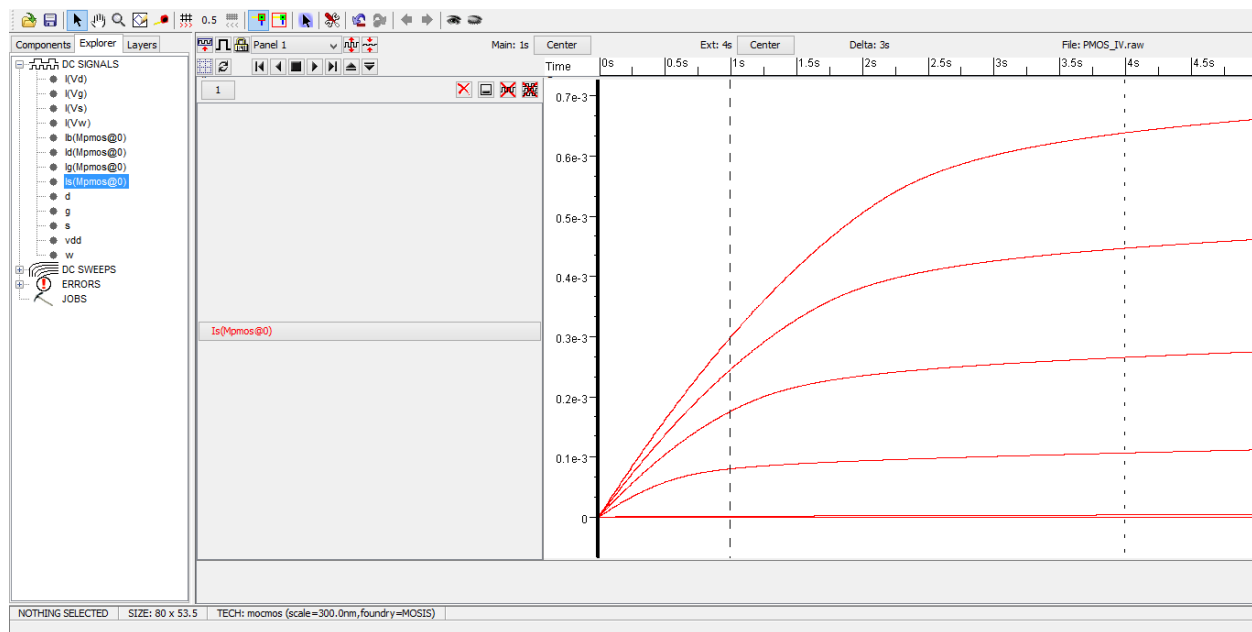


Figure 13: Electric simulation output of PMOS transistor

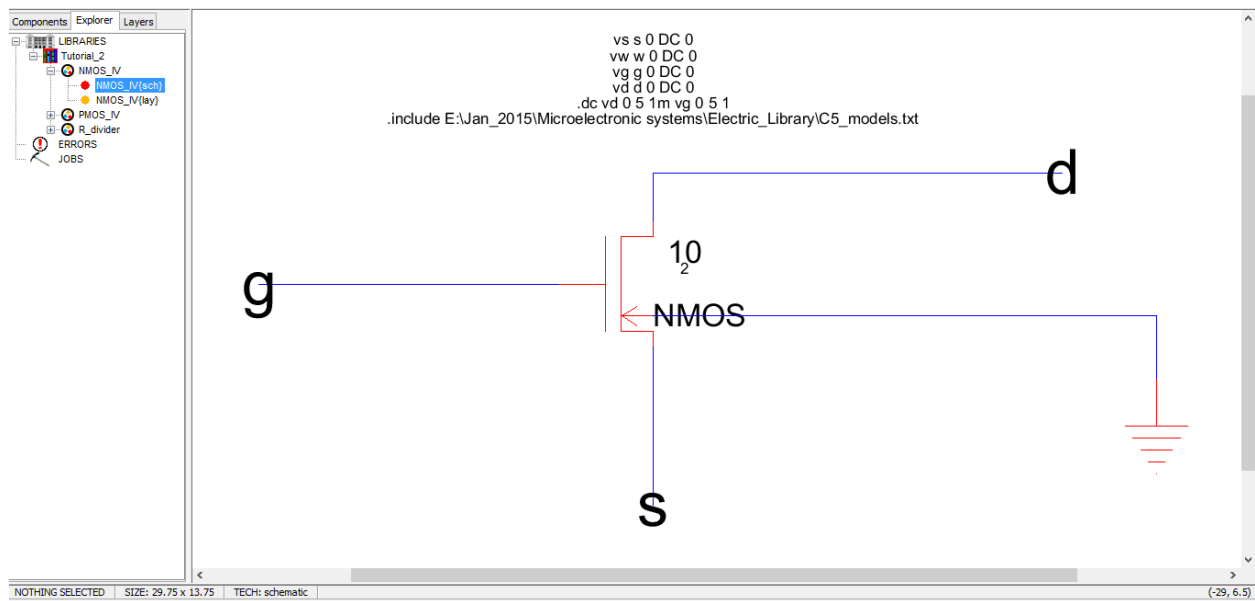


Figure 14: Schematic view of NMOS transistor

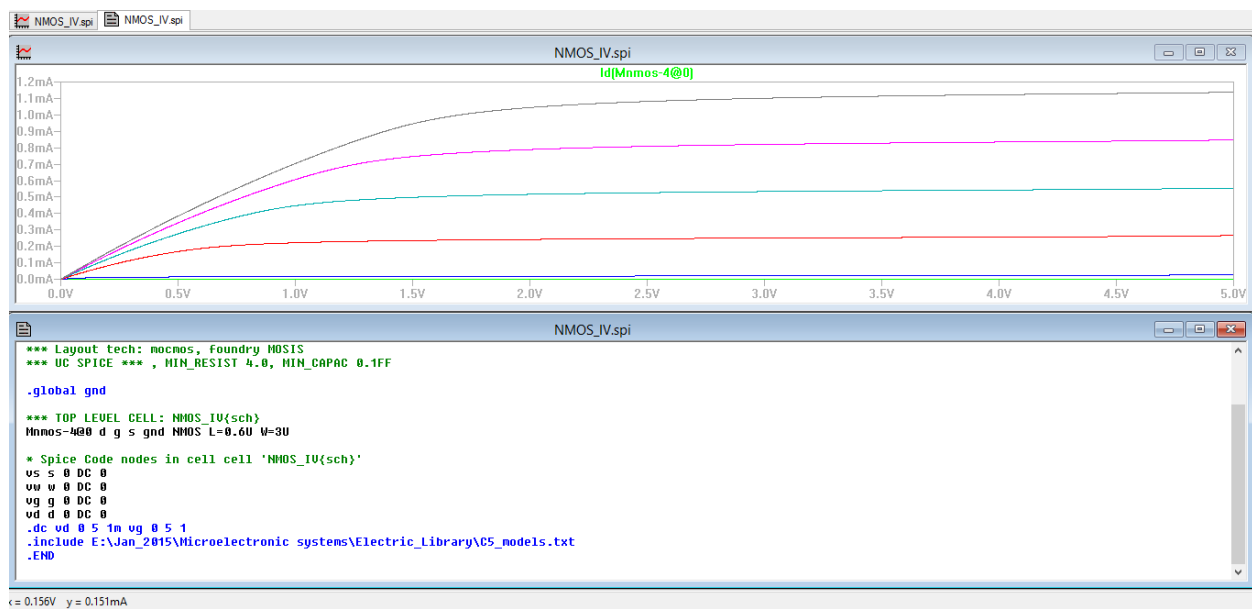


Figure 15: Spice simulation result of NMOS transistor

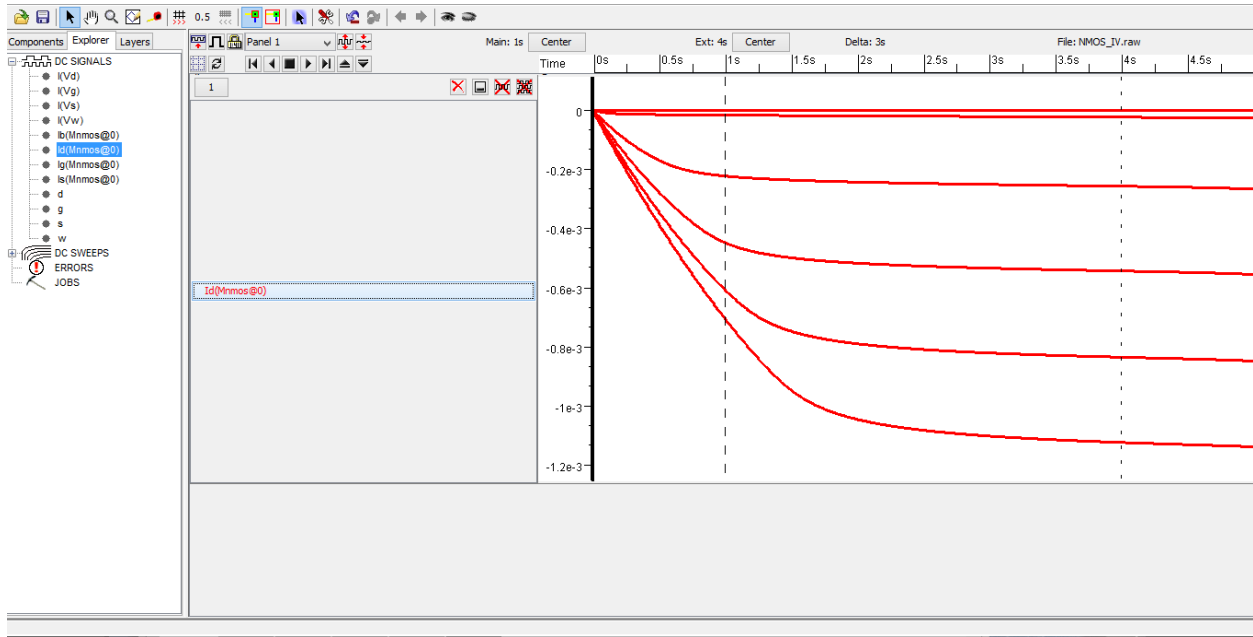


Figure 16: Electric simulation of NMOS transistor

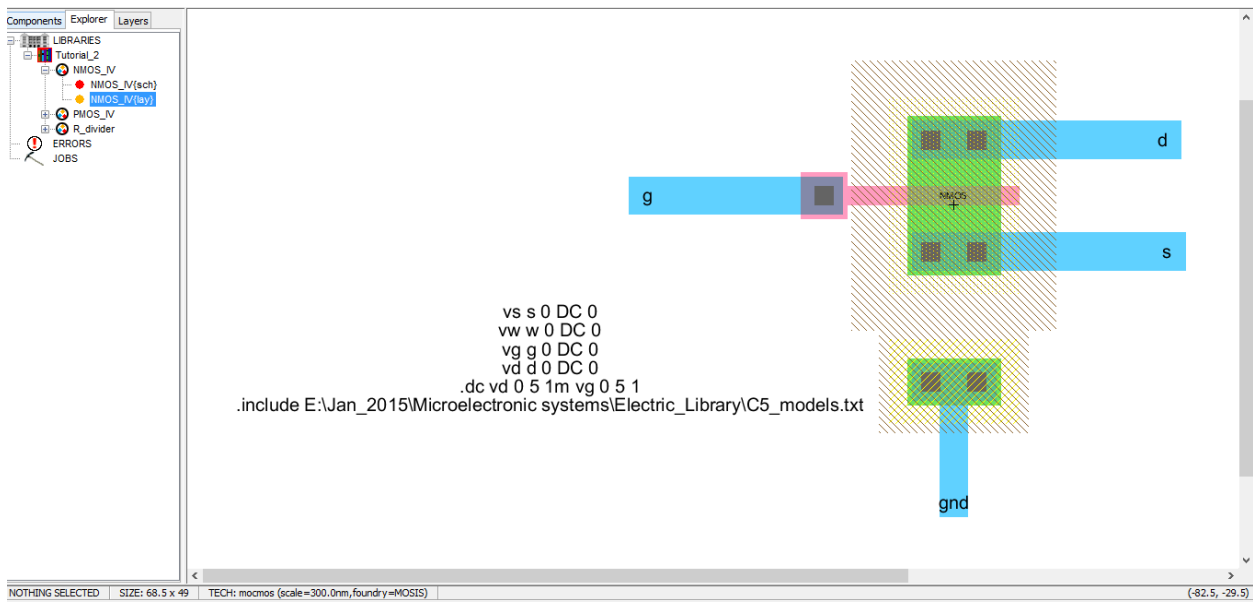


Figure 17: Layout view of NMOS transistor

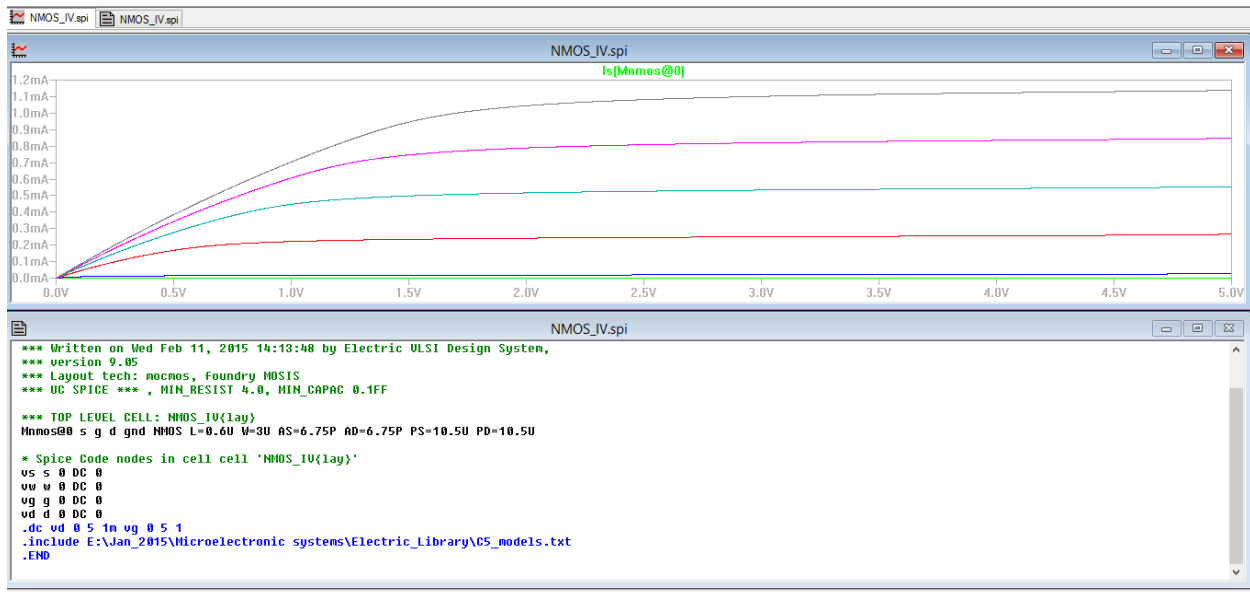


Figure 18: Spice simulation output of NMOS transistor

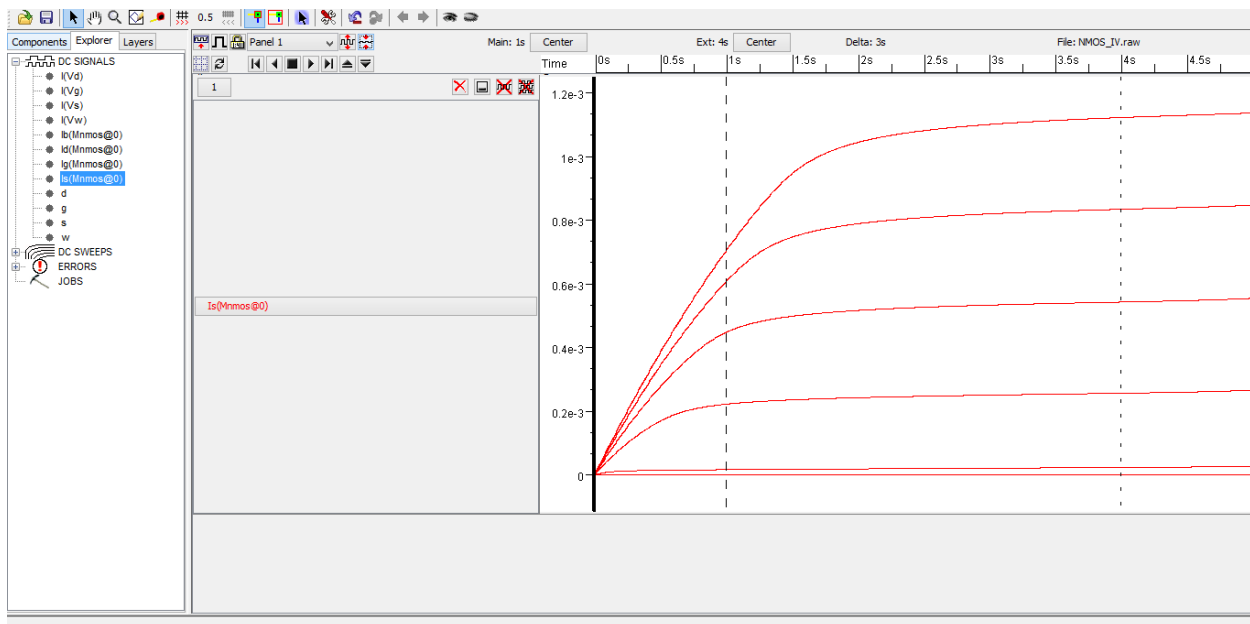


Figure 19: Electric simulation of NMOS transistor

