ECE 531

Microelectronics

Assignment 7

Aditya Sankaramanchi

101266059

Problem 1:

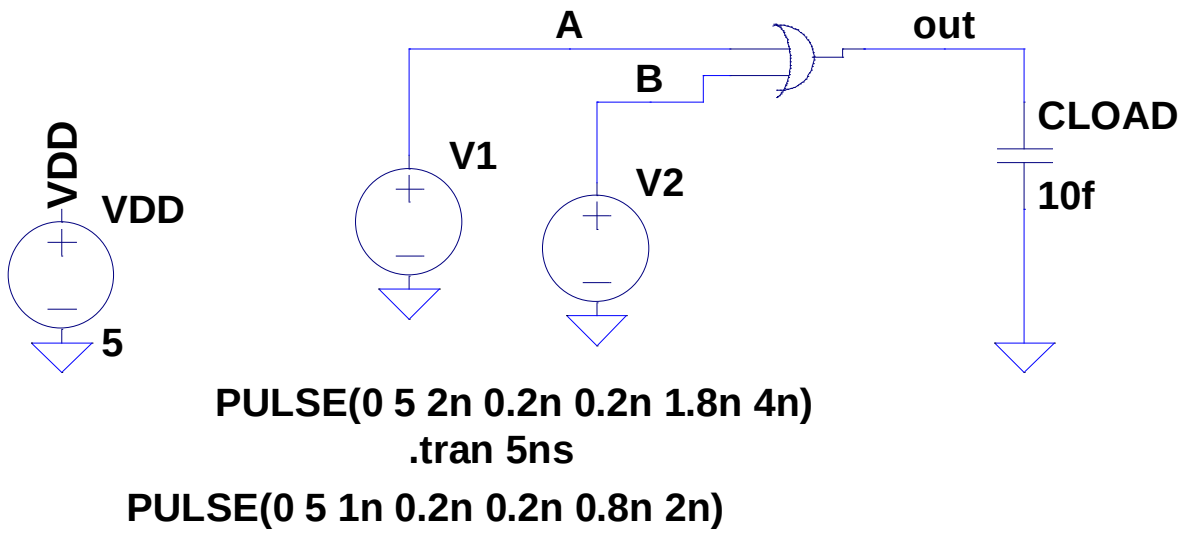

Figure 1: Test circuit to verify the operation of OR gate

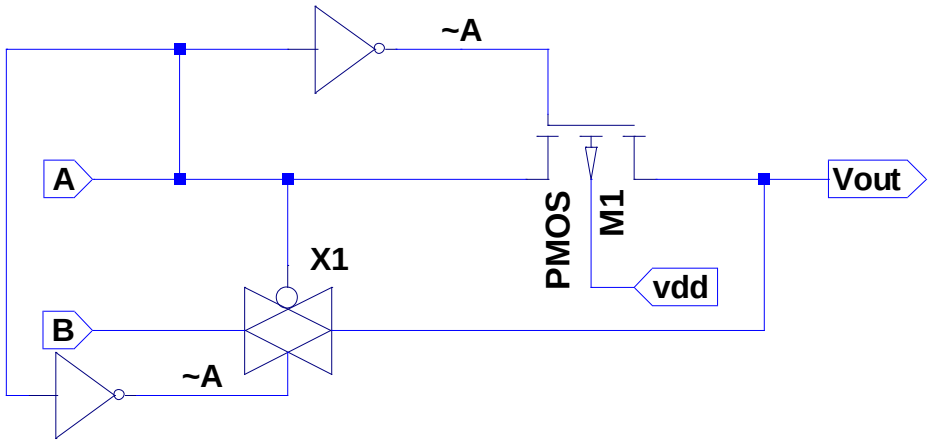

Figure 2: TG-based OR gate in LTSpice

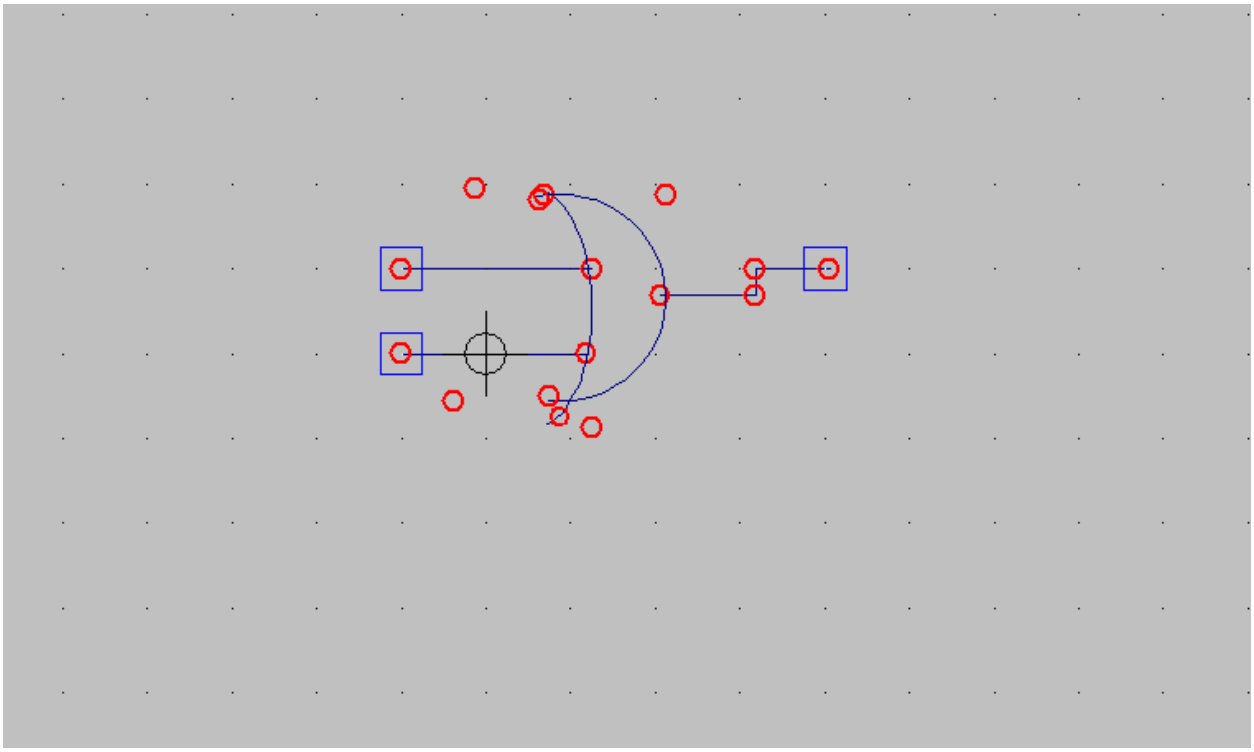

Figure 3: OR gate symbol in LTSpice

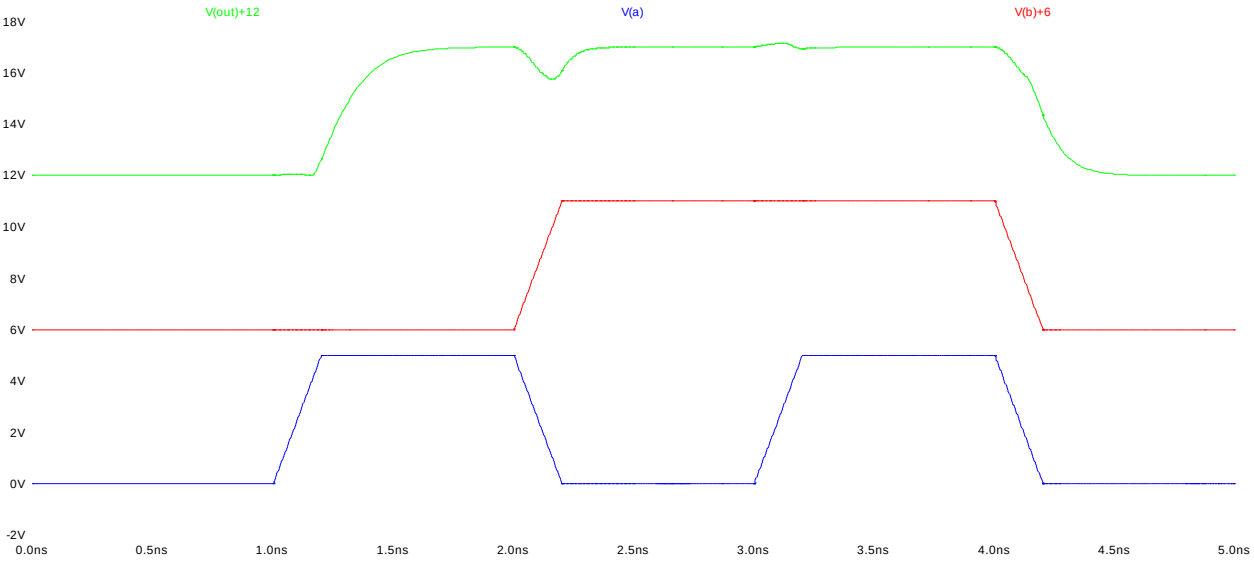

Figure 4: Output waveform of the test circuit

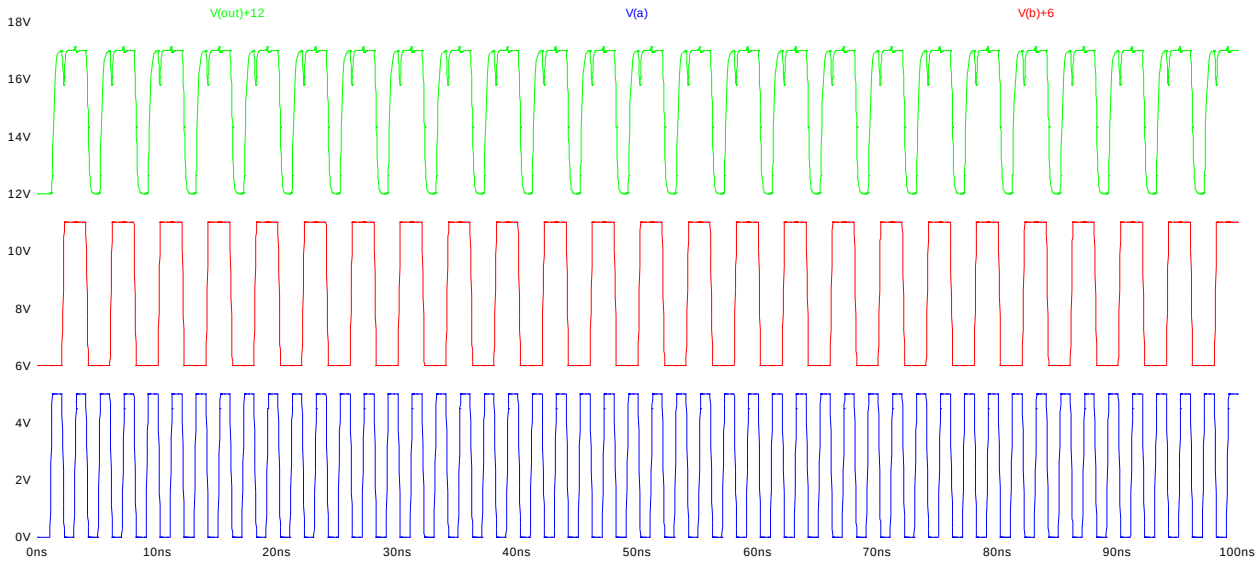

Figure 5: Output waveform for increased time period

From the above waveform, the green waveform represents the output of the OR gate. It is clear that when either of the inputs is high, the output is also high.

Hence verified.

Problem 2:

Cmos_nor

```
module cmos_nor(out,a,b);

parameter dly = 0;

input a,b;

output out;

wire w;

supply1 vdd;

supply0 vss;

nmos #dly m4(out,vss,b);   // nmos 2

nmos #dly m3(out,vss,a);        // nmos 1


pmos #dly m2(out,w,b);          // pmos 2
```

```
pmos #dly m1(w,vdd,a);          // pmos 1

endmodule
```

nor_test

```
module nor_test;
reg a, b;
wire out,test;


cmos_nor g1(out,a,b);
assign test = ~(a|b);

initial
begin
        a = 1'b0; b = 1'b0;
#10
        a = 1'b0; b = 1'b1;
#10
        a = 1'b1; b = 1'b0;
#10
        a = 1'b1; b = 1'b1;
```

```
#10
        a = 1'b0; b = 1'b0;
end
initial
        $monitor("time %d a %b b %b out %b test %b %s",
                $time,a,b,out,test,out==test? "valid":"invalid");
endmodule
```

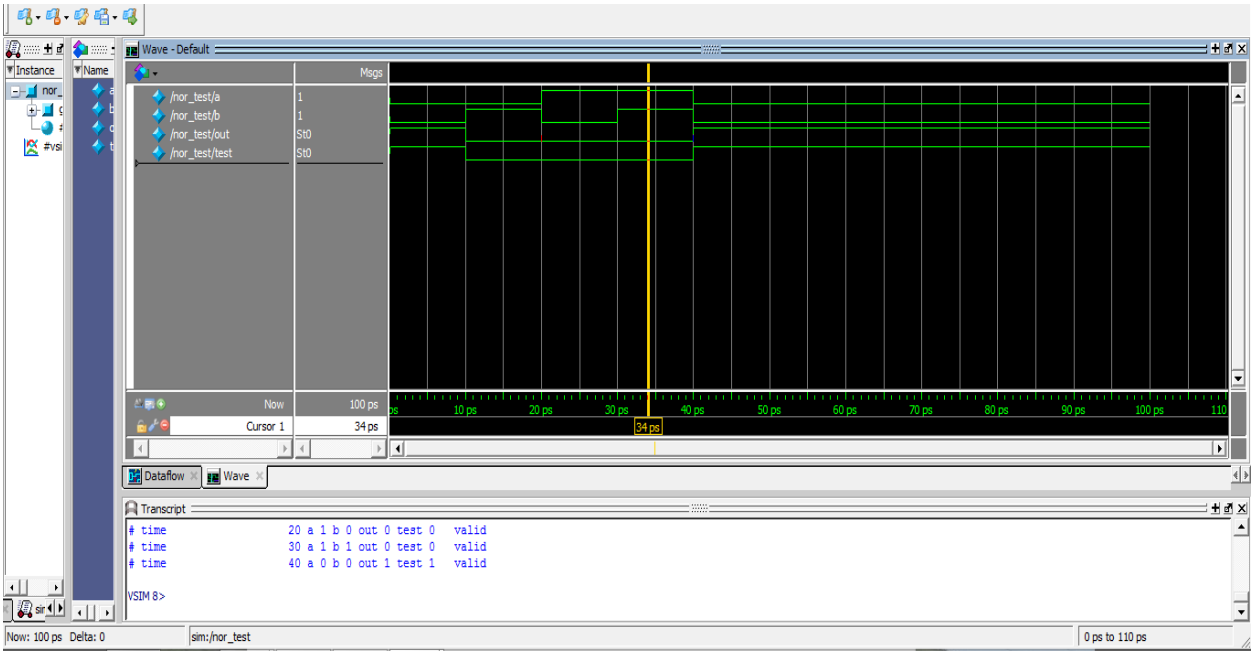

Figure 6: ModelSim output waveform of the NOR gate

ModelSim transcript window

```
add wave sim:/nor_test/*
VSIM 7> run
# time                      0 a 0 b 0 out 1 test 1   valid
# time                     10 a 0 b 1 out 0 test 0   valid
# time                     20 a 1 b 0 out 0 test 0   valid
# time                     30 a 1 b 1 out 0 test 0   valid
# time                     40 a 0 b 0 out 1 test 1   valid

VSIM 8>
```

Figure 7: ModelSim transcript window

Problem 3:

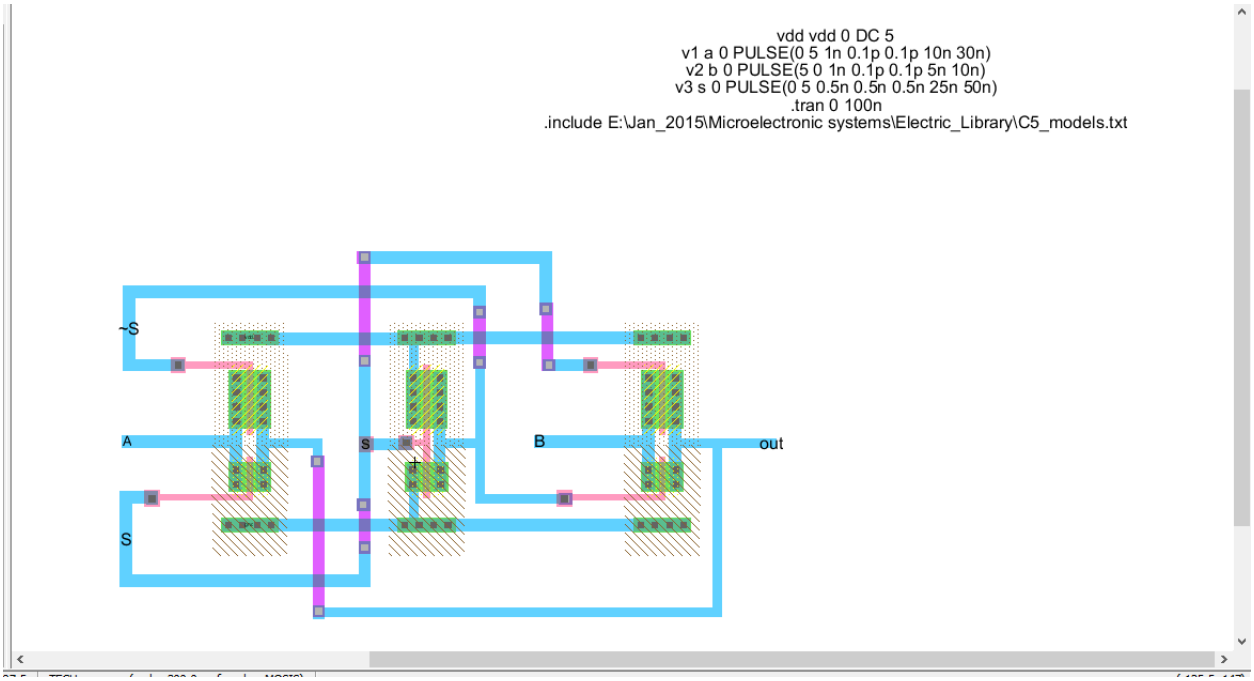

Figure 8: Layout of a multiplexer in Electric

mux_1.spi | mux_1.spi

```
*** SPICE deck for cell mux_1{lay} from library tutorial_5
*** Created on Thu Jan 07, 2010 20:19:07
*** Last revised on Fri Apr 03, 2015 15:38:03
*** Written on Fri Apr 03, 2015 19:51:52 by Electric VLSI Design System,
*** version 9.05
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

*** SUBCIRCUIT tutorial_5__inv_20_10 FROM CELL inv_20_10{lay}
.SUBCKT tutorial_5__inv_20_10 gnd in out vdd
Mnmos@0 out in gnd gnd NMOS L=0.6U W=3U AS=14.67P AD=8.415P PS=24.78U
+PD=12.75U
Mpmos@0 vdd in out vdd PMOS L=0.6U W=6U AS=8.415P AD=20.16P PS=12.75U
+PD=30.72U
.ENDS tutorial_5__inv_20_10

*** SUBCIRCUIT tutorial_5__transmission_gate FROM CELL transmission_gate{lay}
.SUBCKT tutorial_5__transmission_gate A gnd in out vdd _A
Mnmos@0 out A in gnd NMOS L=0.6U W=3U AS=8.415P AD=8.415P PS=12.75U PD=12.75U
Mpmos@0 in _A out vdd PMOS L=0.6U W=6U AS=8.415P AD=8.415P PS=12.75U
+PD=12.75U
.ENDS tutorial_5__transmission_gate

*** TOP LEVEL CELL: mux_1{lay}
Xinv_20_10@1 gnd S _S vdd tutorial_5__inv_20_10
Xtransmis@0 S gnd A out vdd _S tutorial_5__transmission_gate
Xtransmis@1 _S gnd B out vdd S tutorial_5__transmission_gate

* Spice Code nodes in cell cell 'mux_1{lay}'
vdd vdd 0 DC 5
v1 a 0 PULSE(0 5 1n 0.1p 0.1p 10n 30n)
v2 b 0 PULSE(5 0 1n 0.1p 0.1p 5n 10n)
v3 s 0 PULSE(0 5 0.5n 0.5n 0.5n 25n 50n)
.tran 0 100n
.include E:\Jan_2015\Microelectronic systems\Electric_Library\C5_models.txt
.END
```

Figure 9: Spice netlist of the multiplexer layout

Output waveform

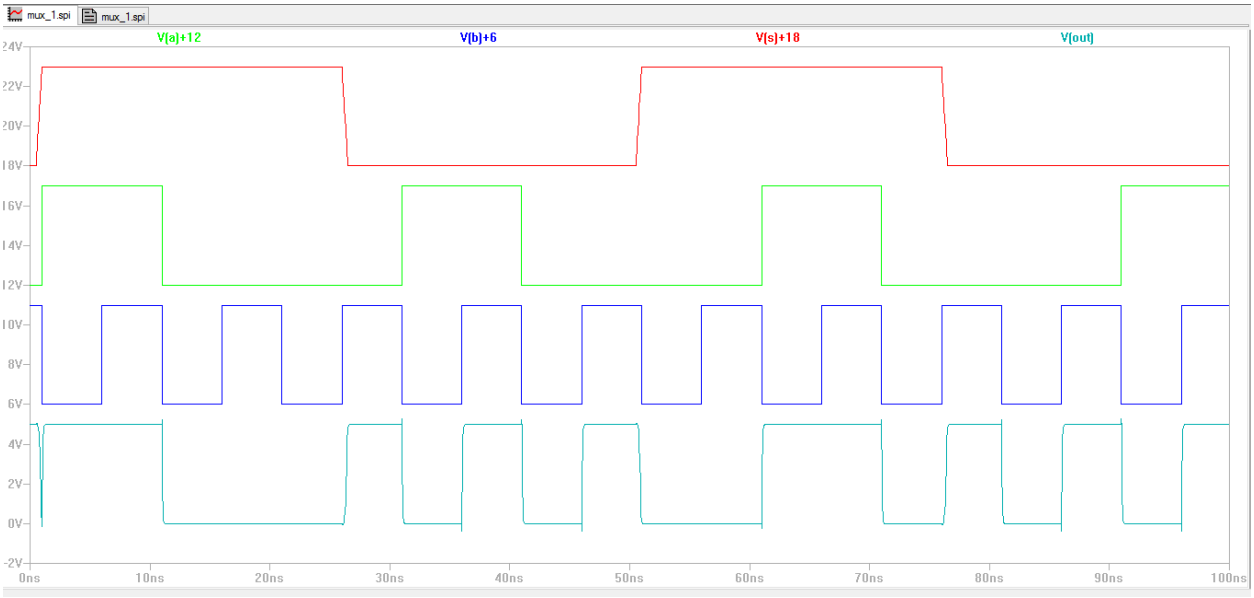

Figure 10: LTSpice output waveform

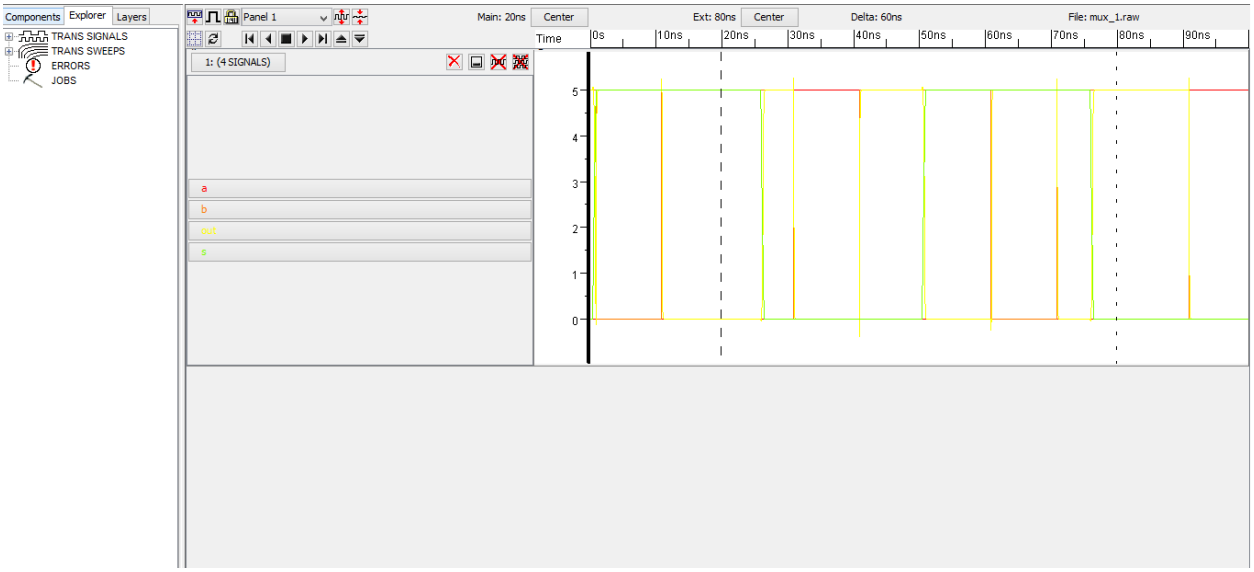

Figure 11: Multiplexer electric output

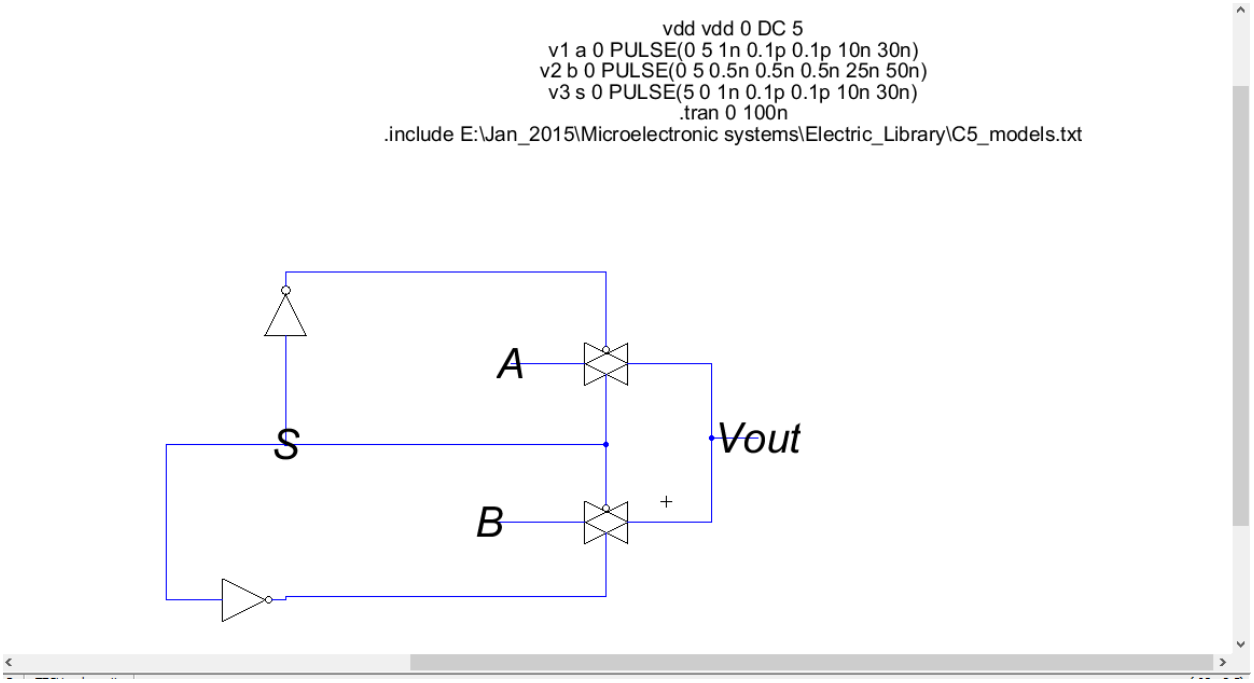

Figure 12: Schematic figure of multiplexer

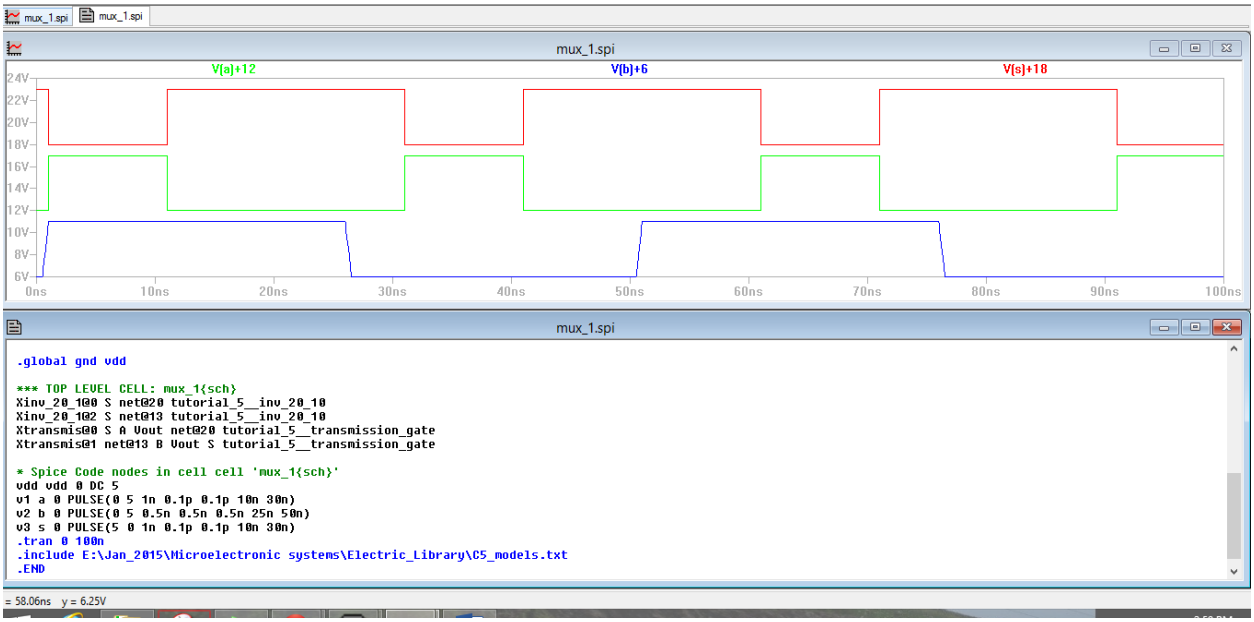

Figure 13: LTSpice simulation of the multiplier schematic

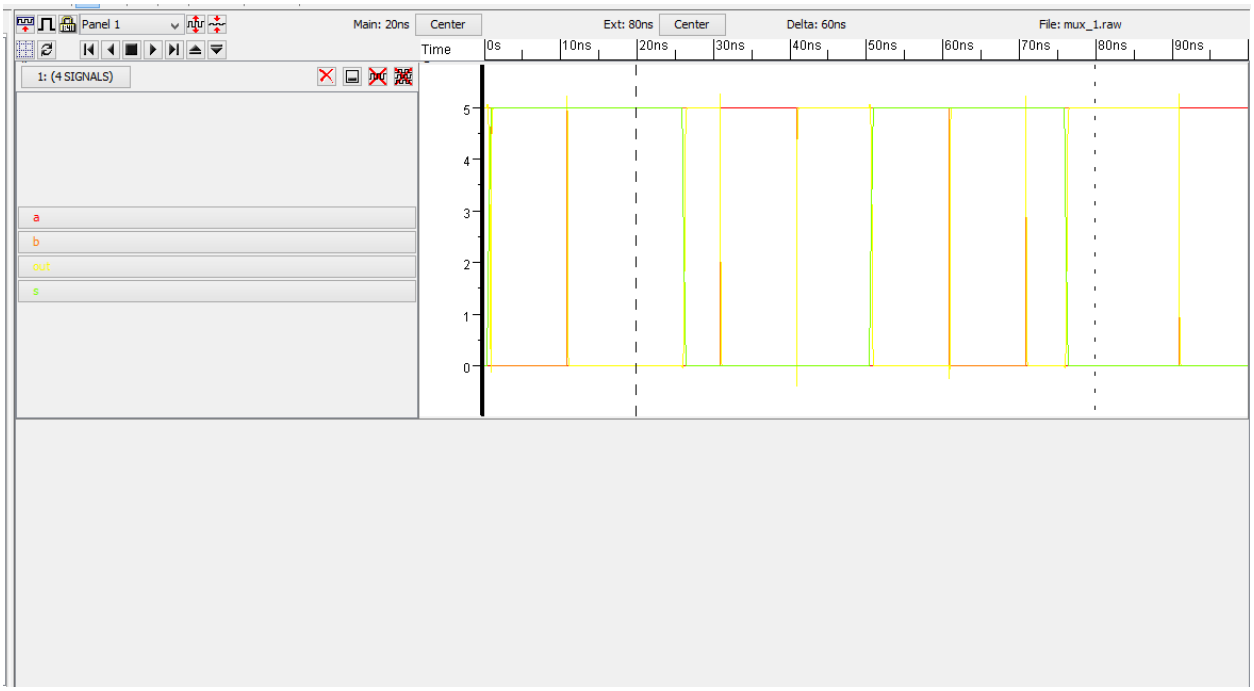

Figure 14: Electric simulation of the multiplexer

Test circuit in LTSpice

LTSPice test ciruit:

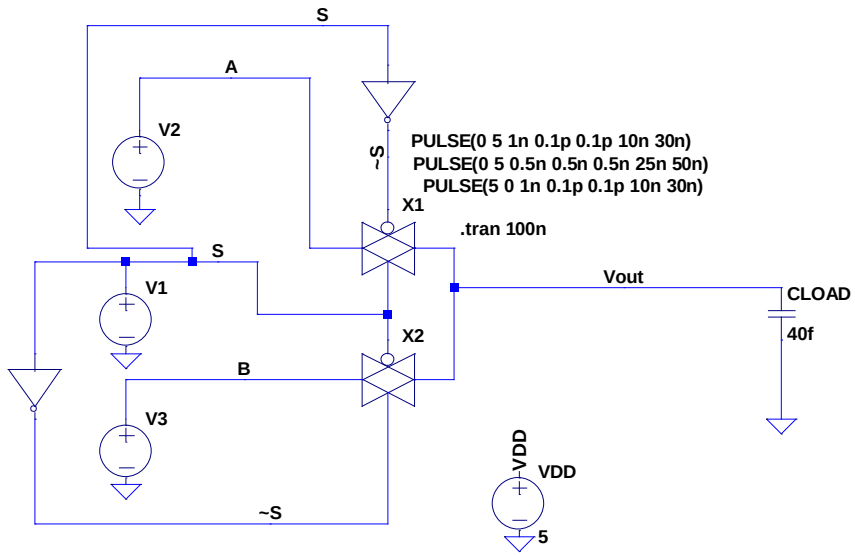

Figure 15: LTSPice circuit diagram of the multiplexer

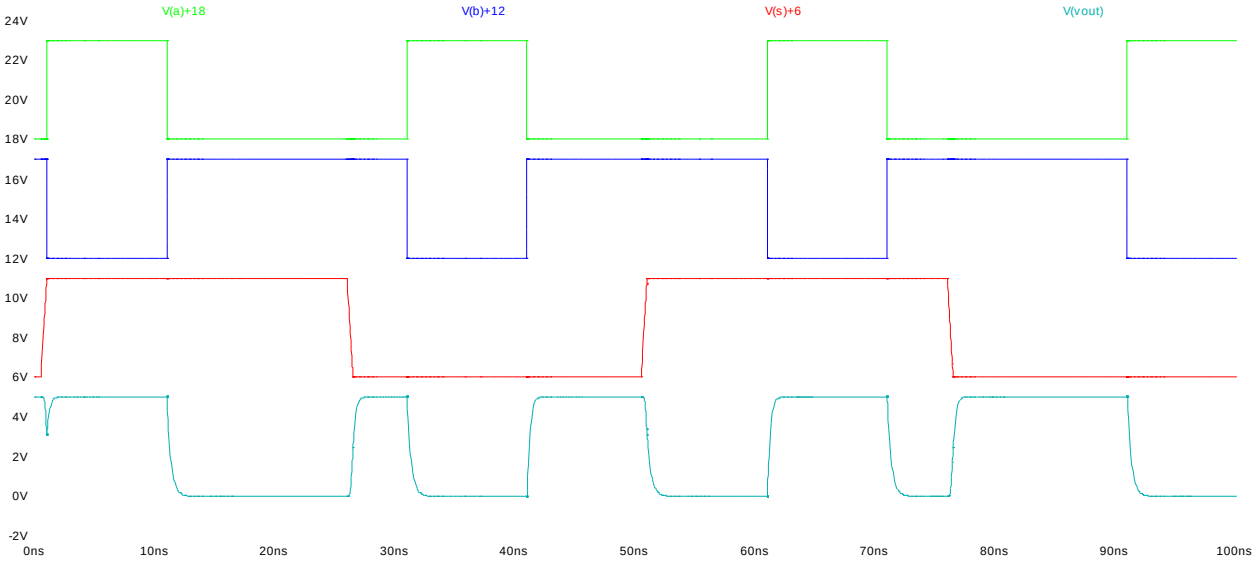

Figure 16: LTSpice test circuit simulation of the multiplexer

Hence proved

Problem 4:

Layout of the transmission gate

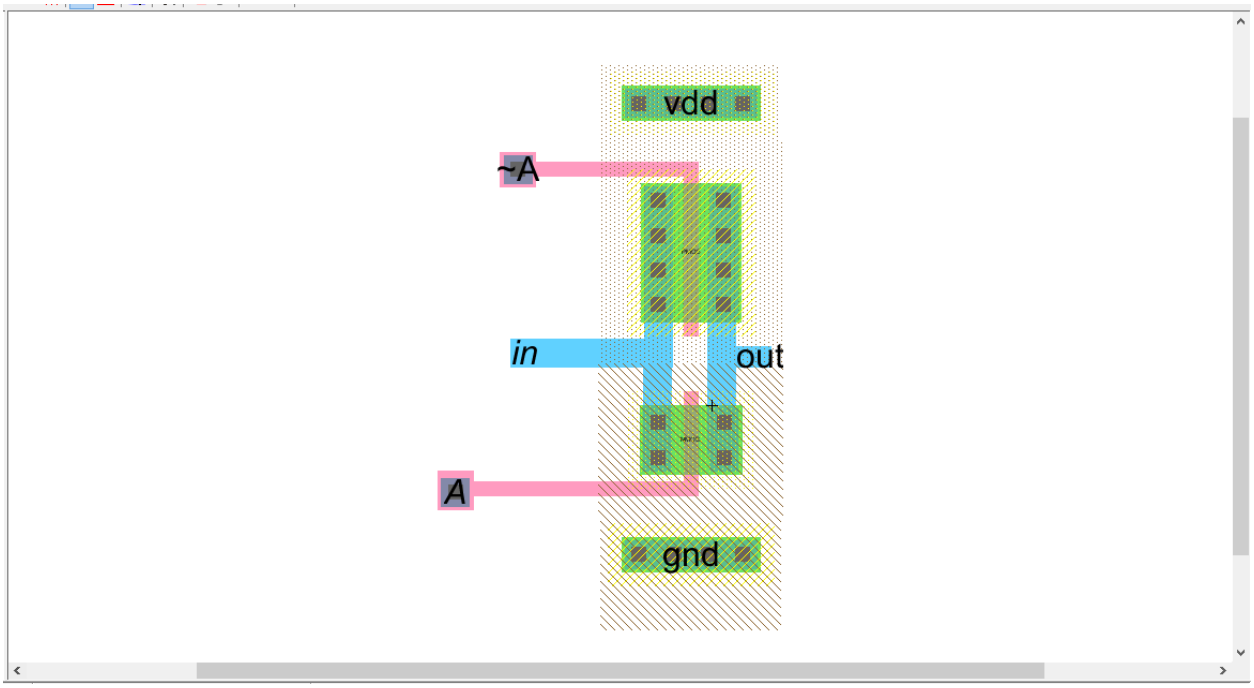

Figure 17: Layout of the transmission gate

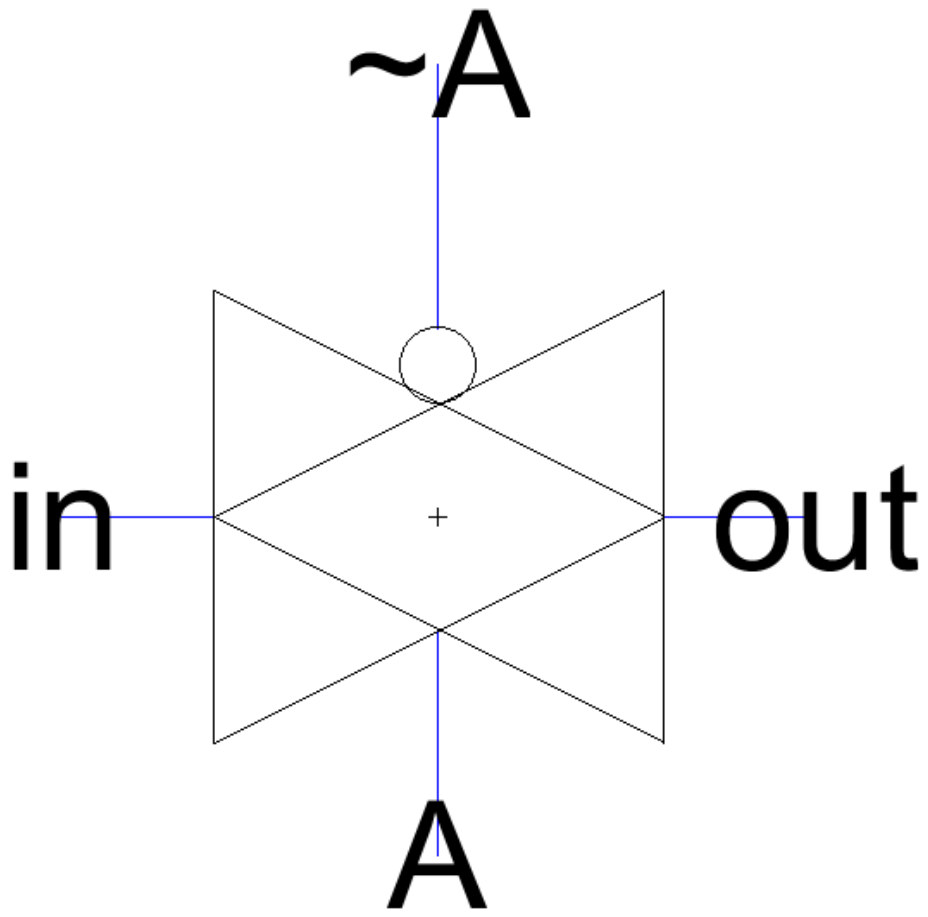

Figure 18: Transmission gate icon

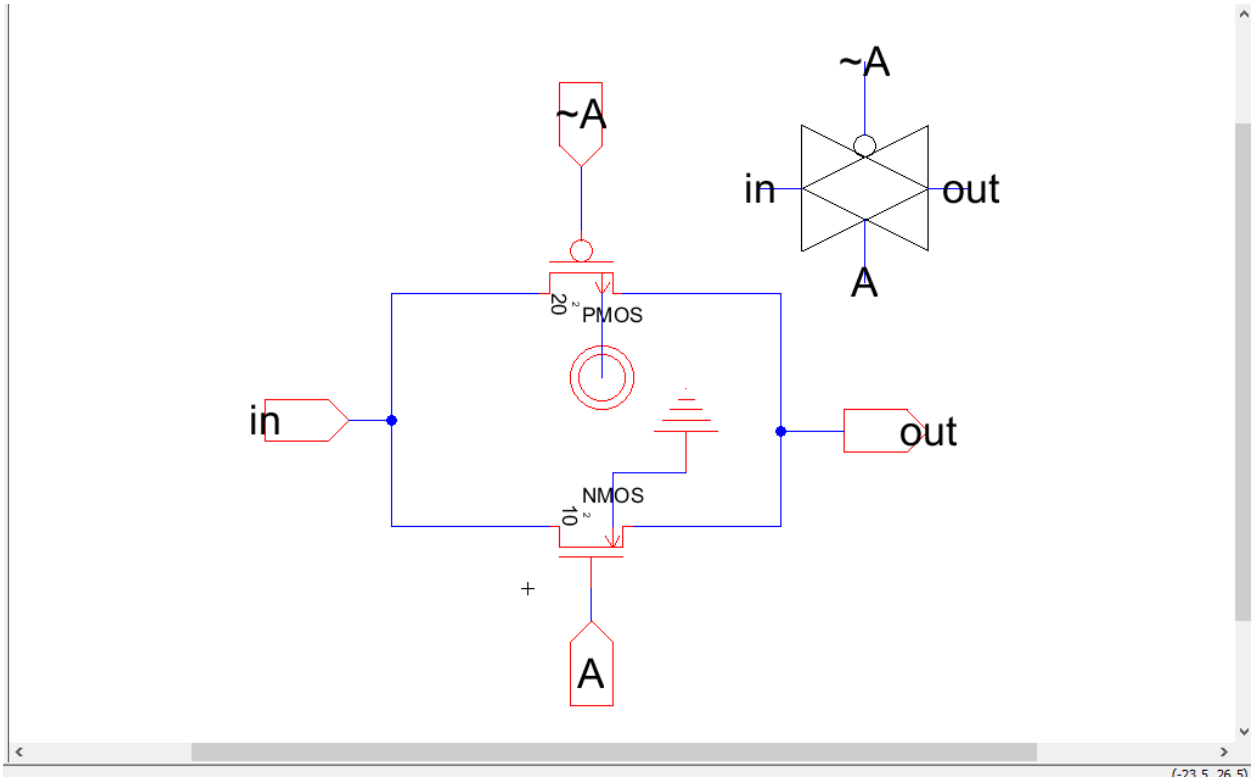

Figure 19: Transmission gate schematic

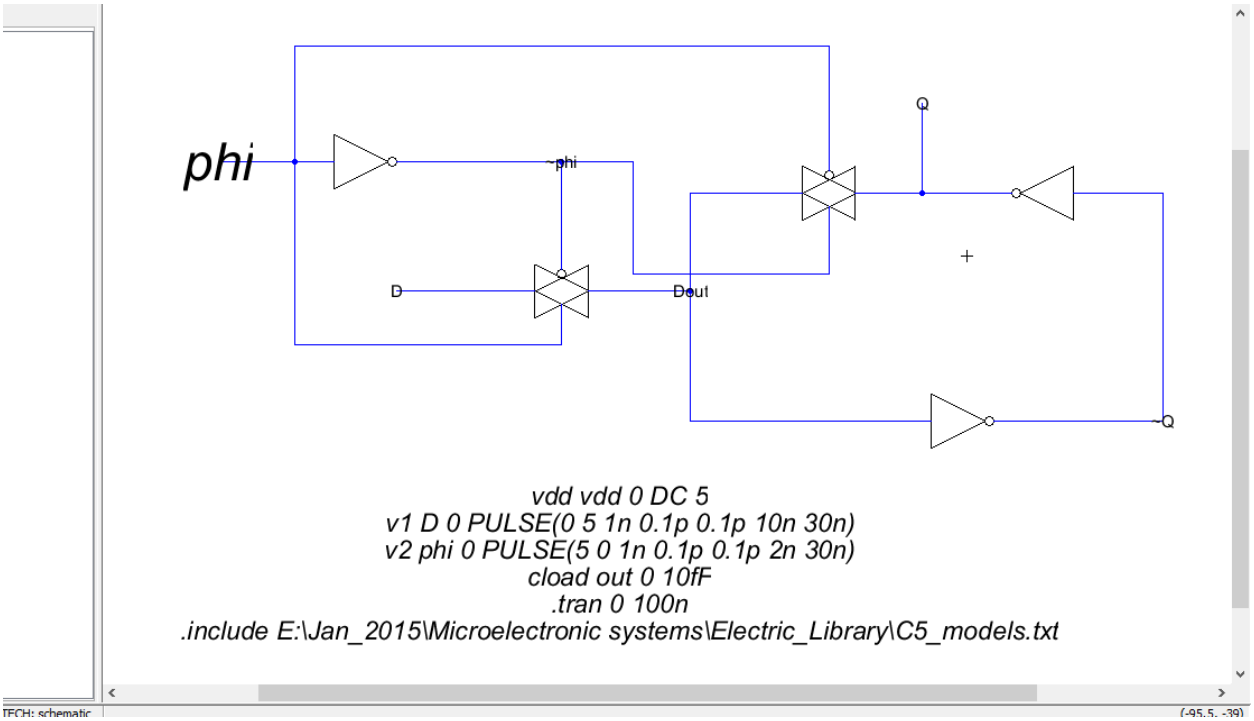

Figure 17: Schematic circuit of the Latch in electric vlsi

```
*** Last revised on Fri Apr 03, 2015 15:34:39
*** Written on Fri Apr 03, 2015 19:59:18 by Electric VLSI Design System,
*** version 9.05
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

*** SUBCIRCUIT tutorial_5__inv_20_10 FROM CELL inv_20_10{sch}
.SUBCKT tutorial_5__inv_20_10 in out
** GLOBAL gnd
** GLOBAL vdd
Mnmos@0 out in gnd gnd NMOS L=0.6U W=3U
Mnmos@1 out in vdd vdd PMOS L=0.6U W=6U
.ENDS tutorial_5__inv_20_10

*** SUBCIRCUIT tutorial_5__transmission_gate FROM CELL transmission_gate{sch}
.SUBCKT tutorial_5__transmission_gate A in out _A
** GLOBAL gnd
** GLOBAL vdd
Mnmos-4@0 in A out gnd NMOS L=0.6U W=3U
Mpmos-4@0 in _A out vdd PMOS L=0.6U W=6U
.ENDS tutorial_5__transmission_gate

.global gnd vdd

*** TOP LEVEL CELL: latch_1{sch}
Xinv_20_1@0 _Q Q tutorial_5__inv_20_10
Xinv_20_1@1 Dout _Q tutorial_5__inv_20_10
Xinv_20_1@2 phi _phi tutorial_5__inv_20_10
Xtransmis@2 _phi Dout Q phi tutorial_5__transmission_gate
Xtransmis@3 phi D Dout _phi tutorial_5__transmission_gate

* Spice Code nodes in cell cell 'latch_1{sch}'
vdd vdd 0 DC 5
v1 D 0 PULSE(0 5 1n 0.1p 0.1p 10n 30n)
v2 phi 0 PULSE(5 0 1n 0.1p 0.1p 2n 30n)
cload out 0 10fF
.tran 0 100n
.include E:\Jan_2015\Microelectronic systems\Electric_Library\C5_models.txt
.END
```

Figure 18: LTSpice netlist of the latch circuit

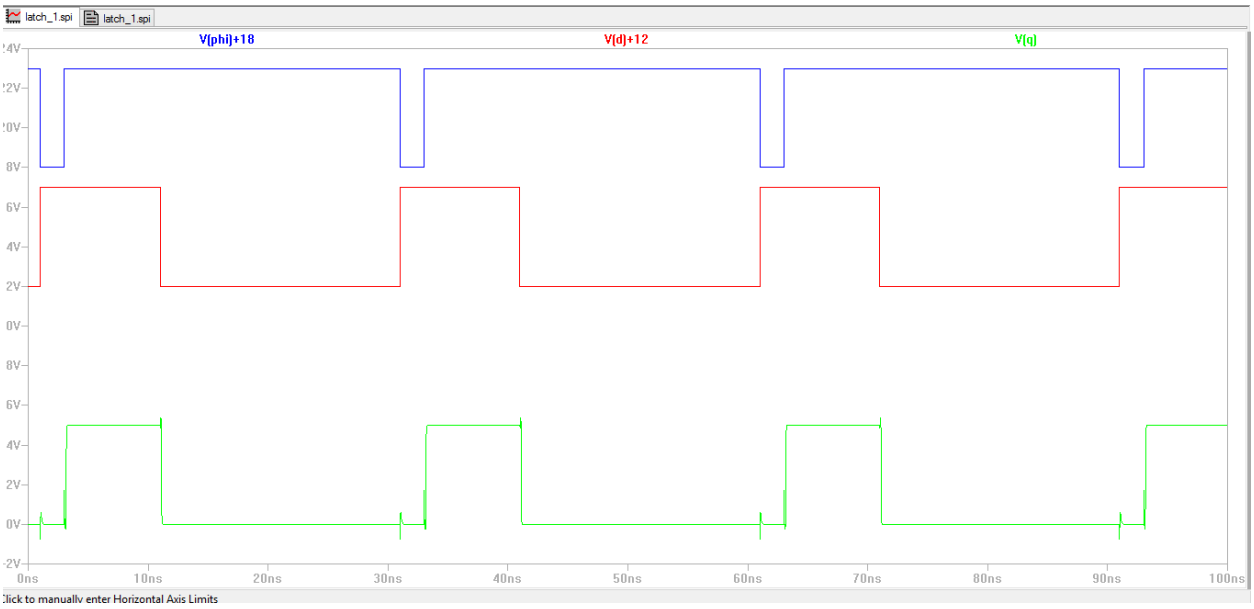

Figure 19: LTSpice simulation of the latch

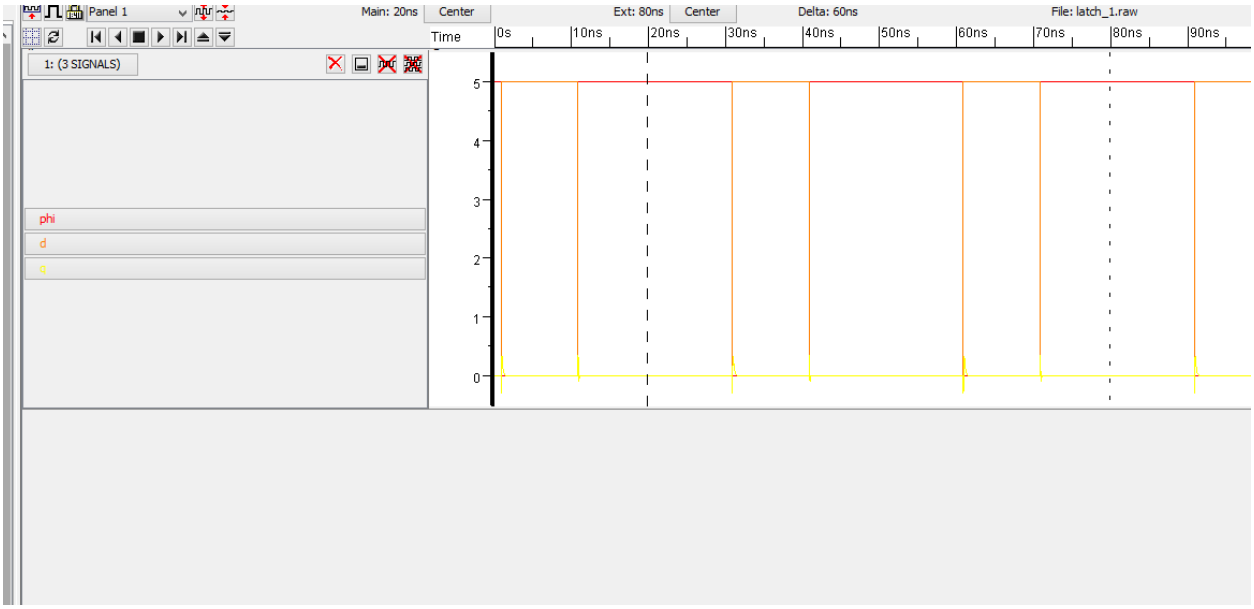

Figure 20: Electric simulation of the Latch

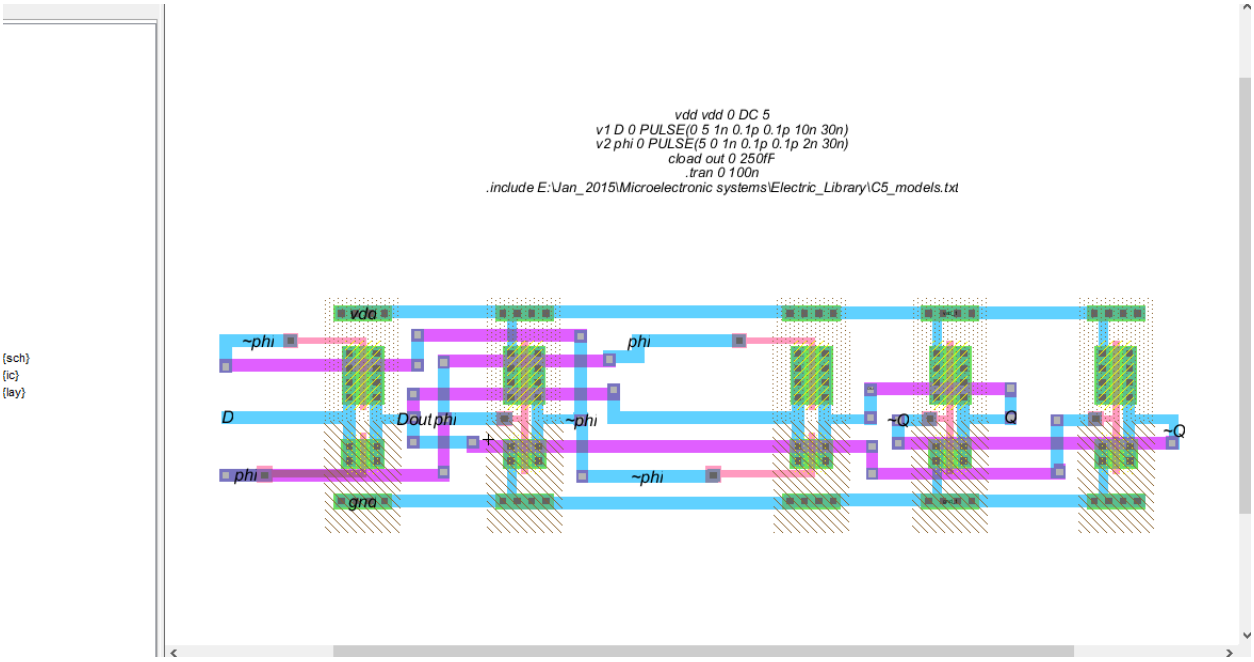

Figure 21: Layout of the Latch circuit

latch_1.spi latch_1.spi

```
*** SPICE deck for cell latch_1{lay} from library tutorial_5
*** Created on Thu Jan 07, 2010 20:19:07
*** Last revised on Fri Apr 03, 2015 15:34:27
*** Written on Fri Apr 03, 2015 20:01:58 by Electric VLSI Design System,
*** version 9.05
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

*** SUBCIRCUIT tutorial_5__inv_20_10 FROM CELL inv_20_10{lay}
.SUBCKT tutorial_5__inv_20_10 gnd in out vdd
Mnmos@0 out in gnd gnd NMOS L=0.6U W=3U AS=14.67P AD=8.415P PS=24.78U
+PD=12.75U
Mpmos@0 vdd in out vdd PMOS L=0.6U W=6U AS=8.415P AD=20.16P PS=12.75U
+PD=30.72U
.ENDS tutorial_5__inv_20_10

*** SUBCIRCUIT tutorial_5__transmission_gate FROM CELL transmission_gate{lay}
.SUBCKT tutorial_5__transmission_gate A gnd in out vdd _A
Mnmos@0 out A in gnd NMOS L=0.6U W=3U AS=8.415P AD=8.415P PS=12.75U PD=12.75U
Mpmos@0 in _A out vdd PMOS L=0.6U W=6U AS=8.415P AD=8.415P PS=12.75U
+PD=12.75U
.ENDS tutorial_5__transmission_gate

*** TOP LEVEL CELL: latch_1{lay}
Xinv_20_1@1 gnd phi _phi vdd tutorial_5__inv_20_10
Xinv_20_1@2 gnd _Q Q vdd tutorial_5__inv_20_10
Xinv_20_1@3 gnd Dout _Q vdd tutorial_5__inv_20_10
Xtransmis@0 phi gnd D Dout vdd _phi tutorial_5__transmission_gate
Xtransmis@1 _phi gnd Dout Q vdd phi tutorial_5__transmission_gate

* Spice Code nodes in cell cell 'latch_1{lay}'
vdd vdd 0 DC 5
v1 D 0 PULSE(0 5 1n 0.1p 0.1p 10n 30n)
v2 phi 0 PULSE(5 0 1n 0.1p 0.1p 2n 30n)
cload out 0 250fF
.tran 0 100n
.include E:\Jan_2015\Microelectronic systems\Electric_Library\C5_models.txt
.END
```

Figure 22: LTSpice netlist of the latch circuit

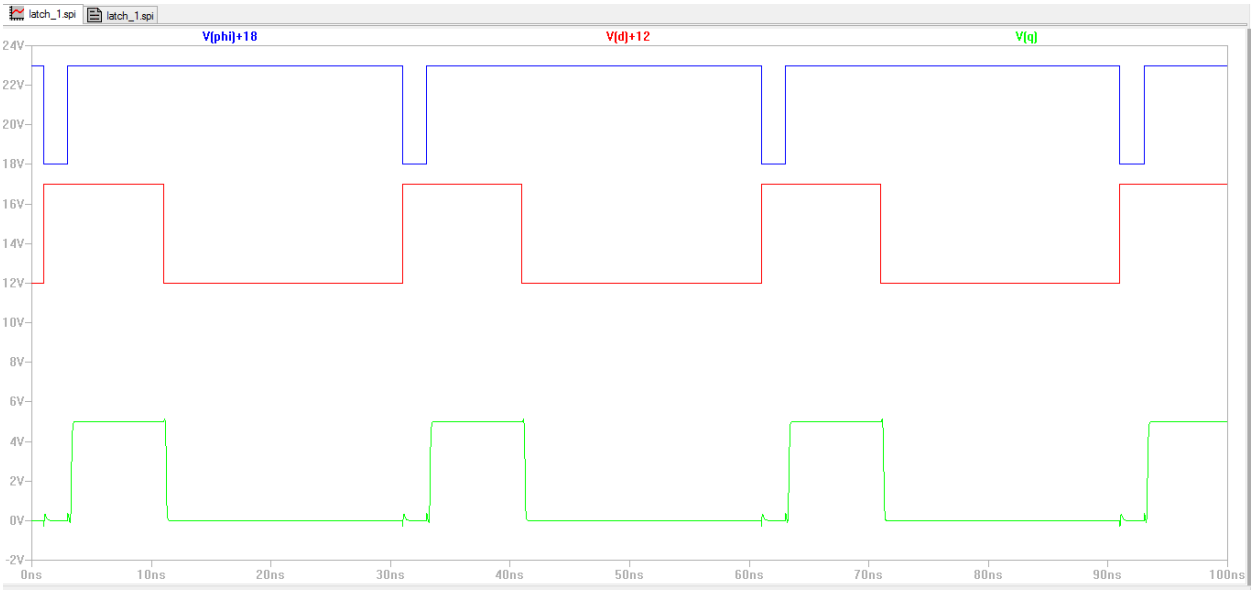

Figure 23: LTSpice simulation of the latch

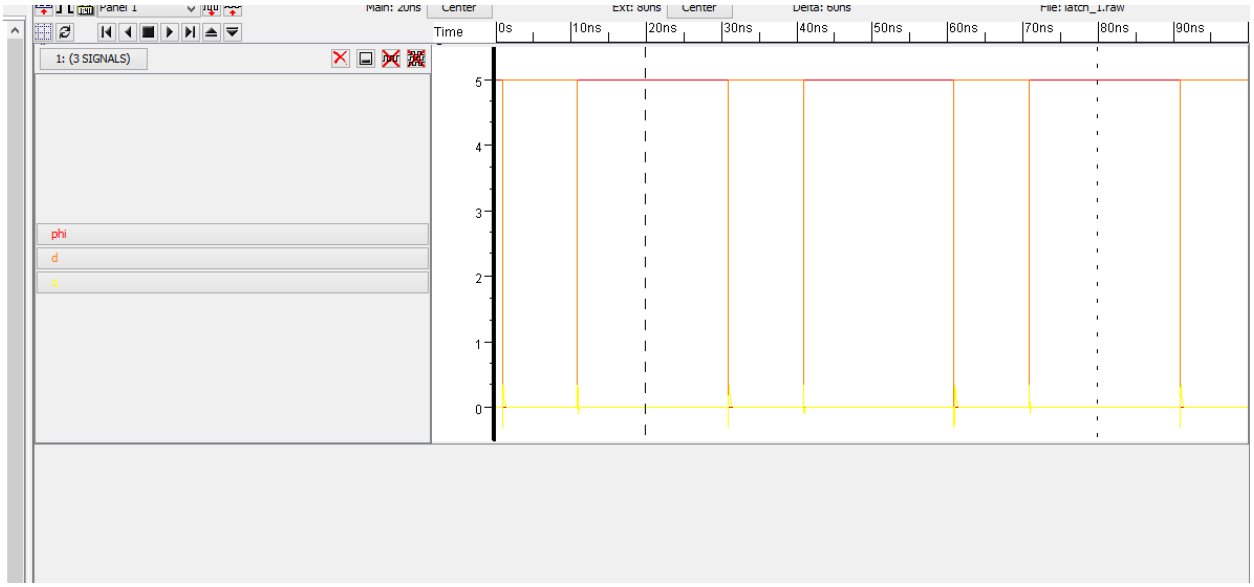

Figure 24: Electric simulation of the latch layout circuit

Test circuit of the Latch in LTSpice

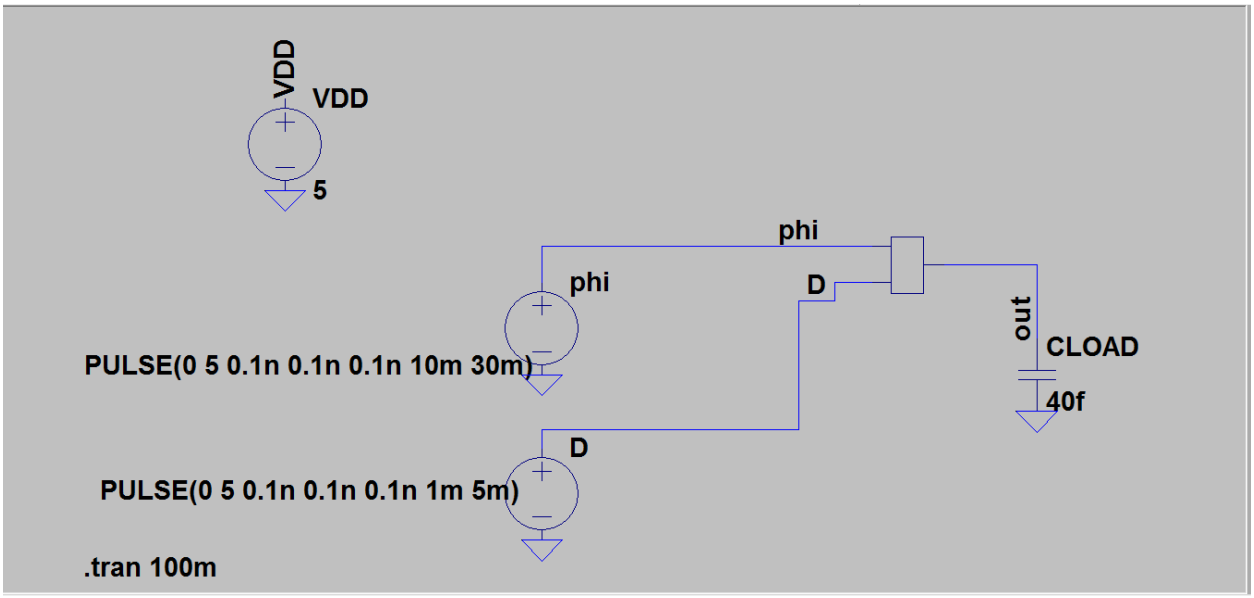

Figure 25: LTSPice test circuit of the latch

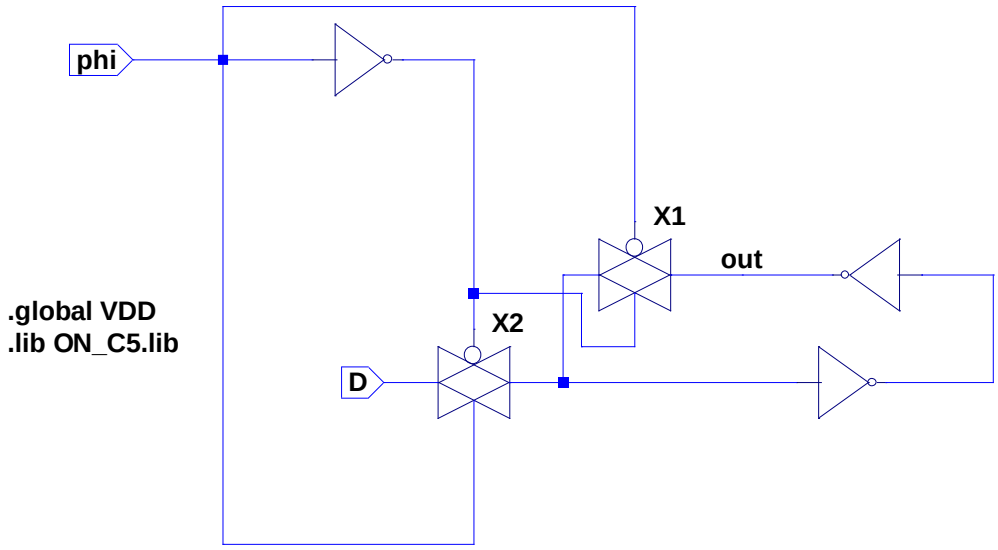

Figure 26: Latch circuit in LTSpice

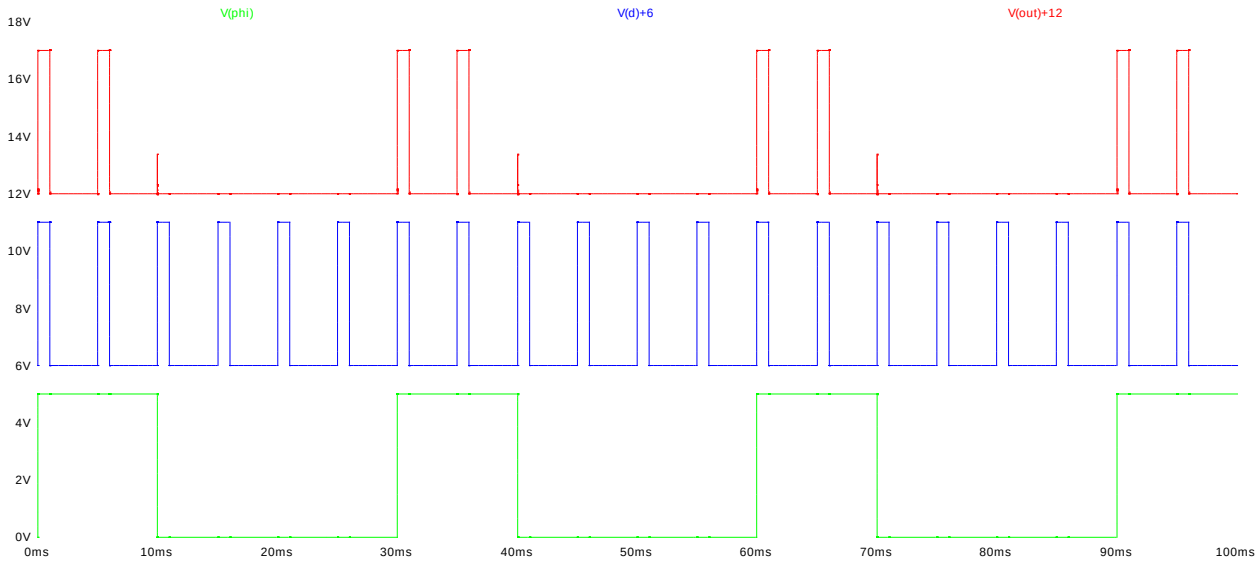

Figure 27: LTSPice simulation of the Latch test circuit