ECE 531

Microelectronics

Assignment 6

Aditya Sankaramanchi

101266059

Question 1:

Here the power rails are at the same relative location and the gates are arranged side by side.

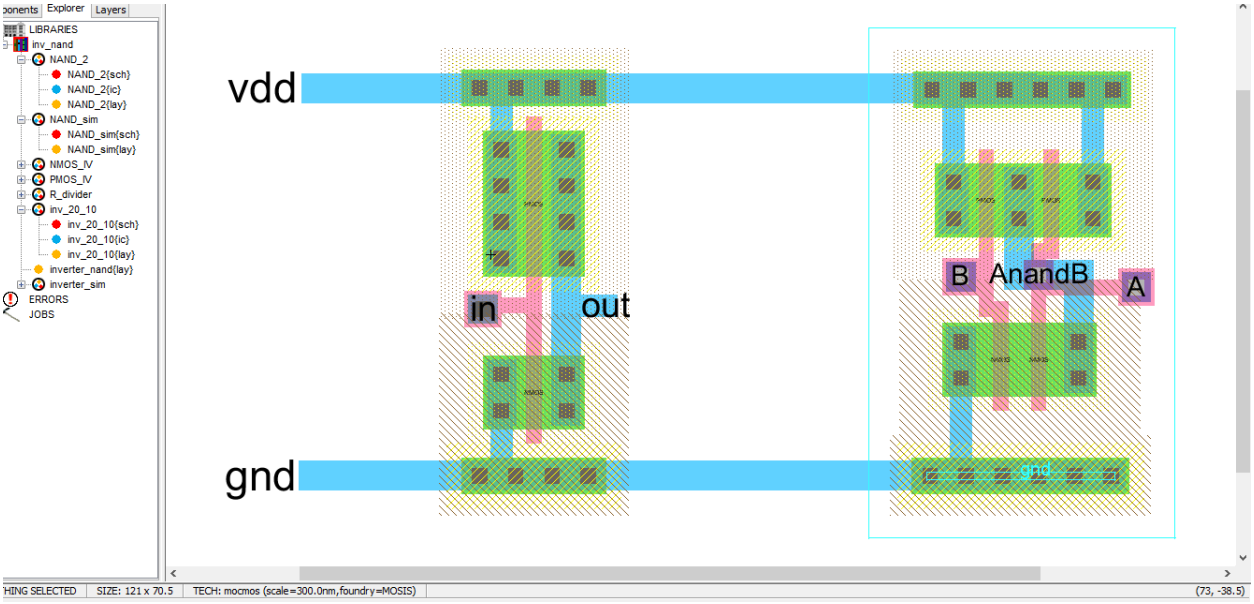

Figure 1: Electric Layout of the inverter and the nand gate.

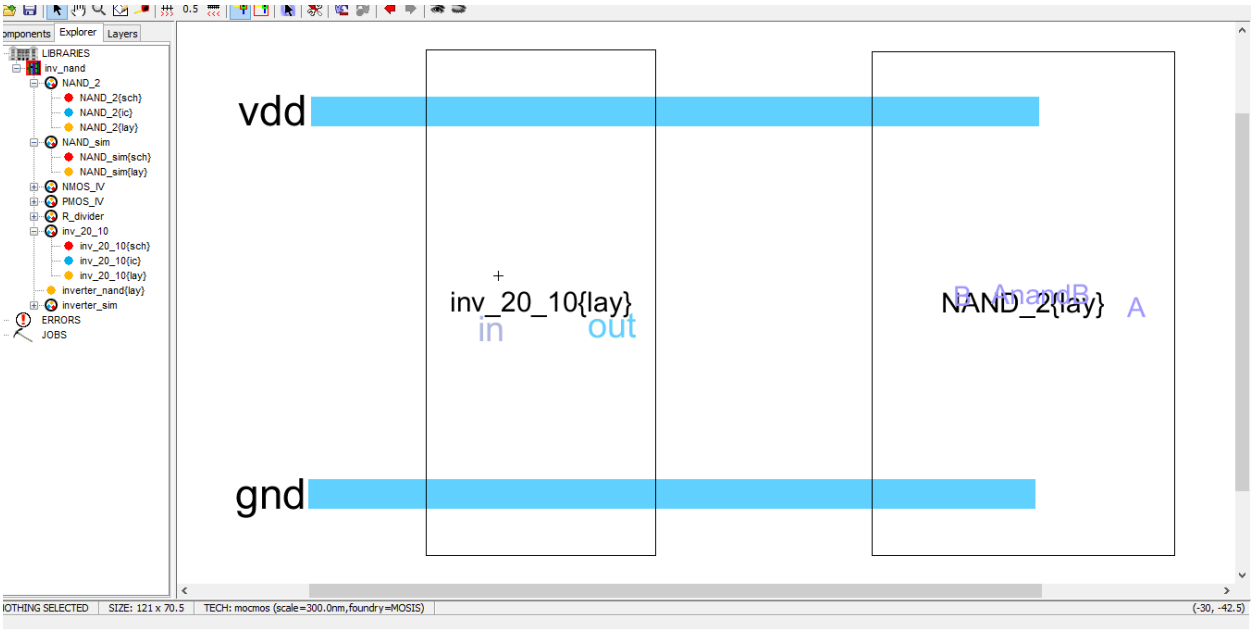

Figure 2: Electric Layout of the inverter and the nand gate.

Question 2:

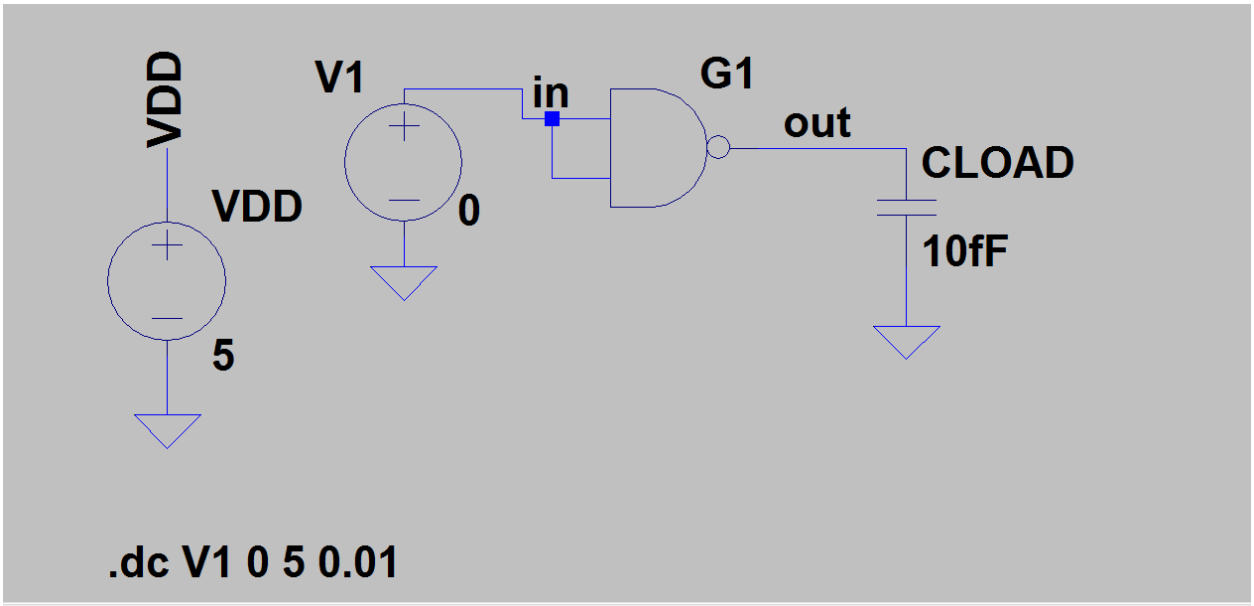

Figure 3: Equivalent circuit of the nand gate

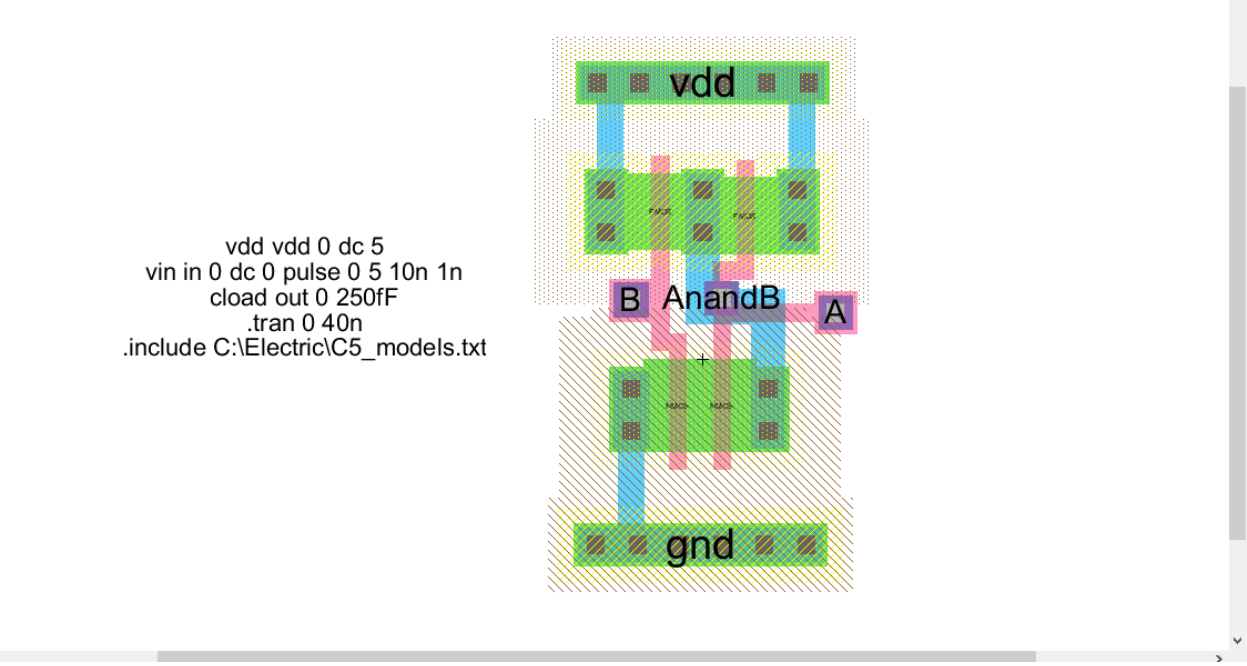

Figure 4: NAND gate in Electric Layout

The nand gate is designed in the Electric to get the parasitic parameters. Now these parameters kept in the LTSpice PMOS and NMOS.

```
*** SPICE deck for cell NAND_2{lay} from library tutorial_4
*** Created on Thu Jan 07, 2010 18:59:18
*** Last revised on Thu Mar 19, 2015 17:29:15
*** Written on Thu Mar 19, 2015 17:29:22 by Electric VLSI Design System,
*** version 9.05
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

*** TOP LEVEL CELL: NAND_2{lay}
Mnmos@0 net@7 B gnd gnd NMOS L=0.6U W=3.3U AS=20.07P AD=1.912P PS=31.8U
+PD=4.95U
Mnmos@1 AnandB A net@7 gnd NMOS L=0.6U W=3.3U AS=1.912P AD=4.5P PS=4.95U
+PD=7.2U
Mpmos@0 vdd B AnandB vdd PMOS L=0.6U W=2.7U AS=4.5P AD=13.579P PS=7.2U
+PD=21.225U
Mpmos@1 AnandB A vdd vdd PMOS L=0.6U W=2.7U AS=13.579P AD=4.5P PS=21.225U
+PD=7.2U

* Spice Code nodes in cell cell 'NAND_2{lay}'
vdd vdd 0 dc 5
vin in 0 dc 0 pulse 0 5 10n 1n
cload out 0 250fF
.tran 0 40n
.include C:\Electric\C5_models.txt
.END
```

Figure 5: Electric output

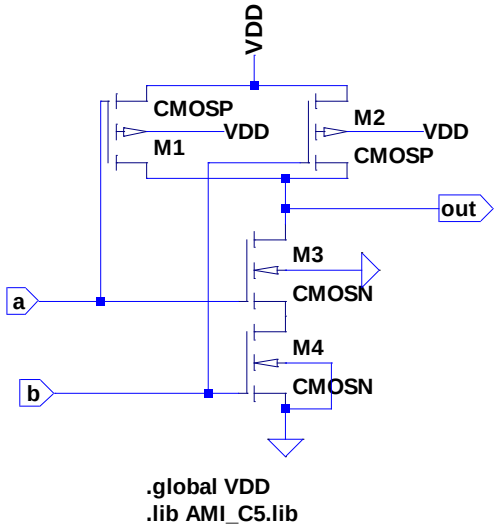

Figure 6: NAND gate LTSpice circuit

SPICE Netlist: E:\Jan_2015\Microelectronic systems\Assignment_6\problem_2\spice_na...

```
* E:\Jan_2015\Microelectronic systems\Assignment_6\problem_2\spice_nand\nand.as
M1 out a VDD VDD CMOSP l=0.6u w=2.7u ad=4.5P as=13.579P pd=7.2U ps=21.225U
M2 VDD b out VDD CMOSP l=0.6u w=2.7u ad=13.579P as=4.5P pd=21.225U ps=21.225U
M3 out a P001 0 CMOSN l=0.6u w=3.3u ad=4.5P as=1.912P pd=7.2U ps=4.95U
M4 P001 b 0 0 CMOSN l=0.6u w=3.3u ad=1.912P as=20.07P pd=4.95U ps=31.8U
.model NMOS NMOS
.model PMOS PMOS
.lib D:\LTSpice\lib\cmp\standard.mos
.global VDD
.lib AMI_C5.lib
.backanno
.end
```

Figure 7: Spcie Netlist of the Nand gate

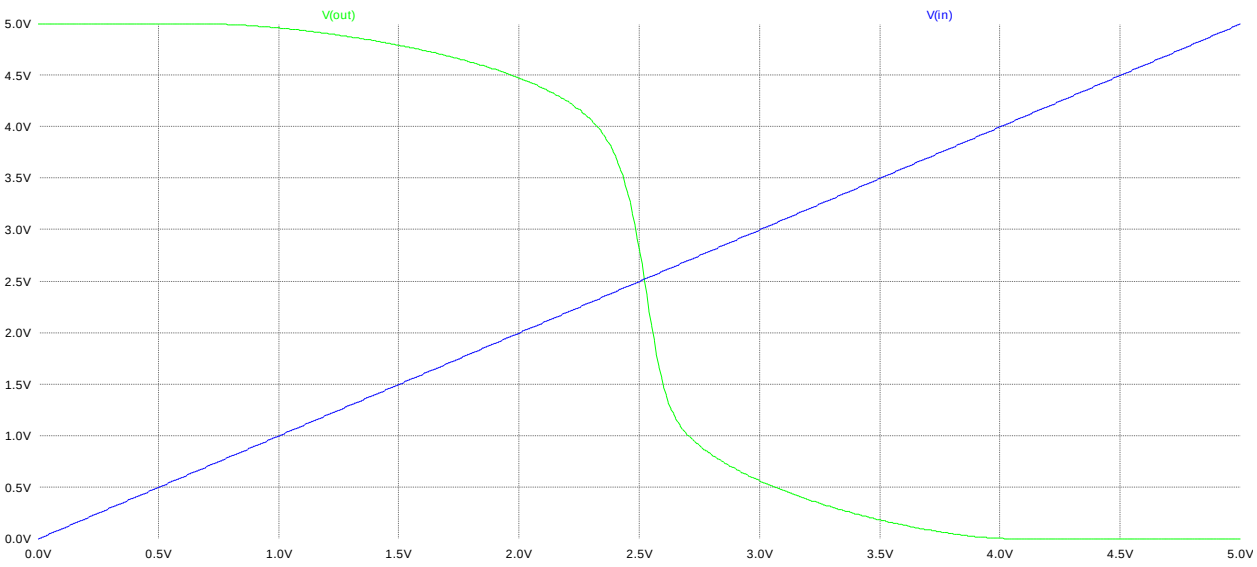

Figure 8: Spice output for the modified nand gate

Switch point = 2.5191131V.

Hence point

Question 3:

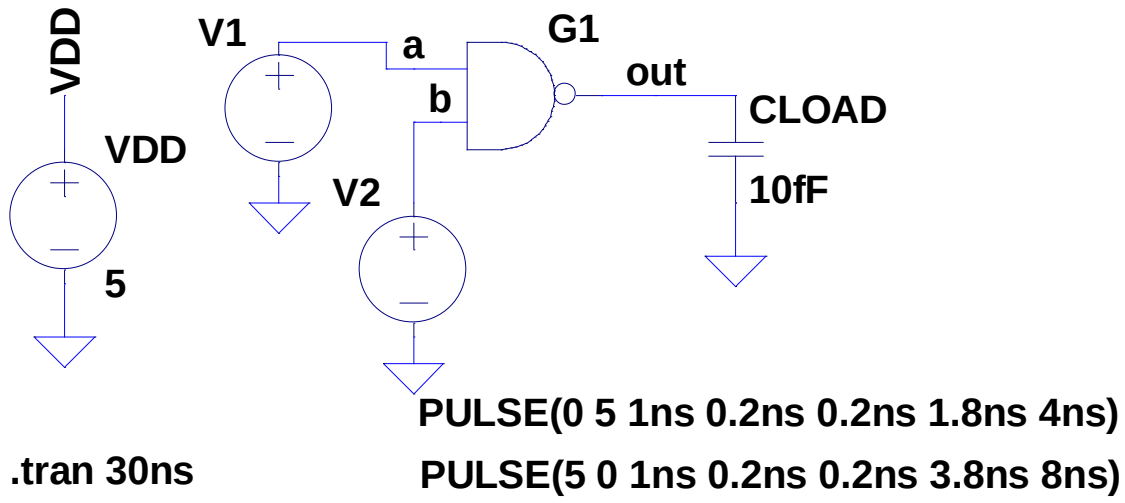

Figure 9: Equivalent circuit of the nand gate

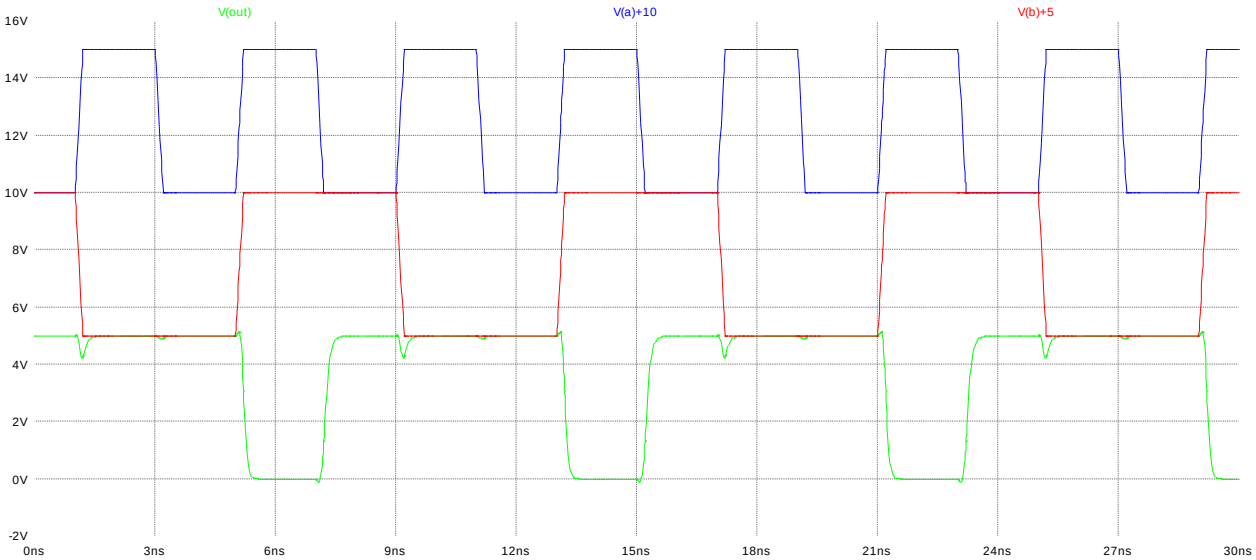

Figure 10: LTSpice simulation of the above circuit

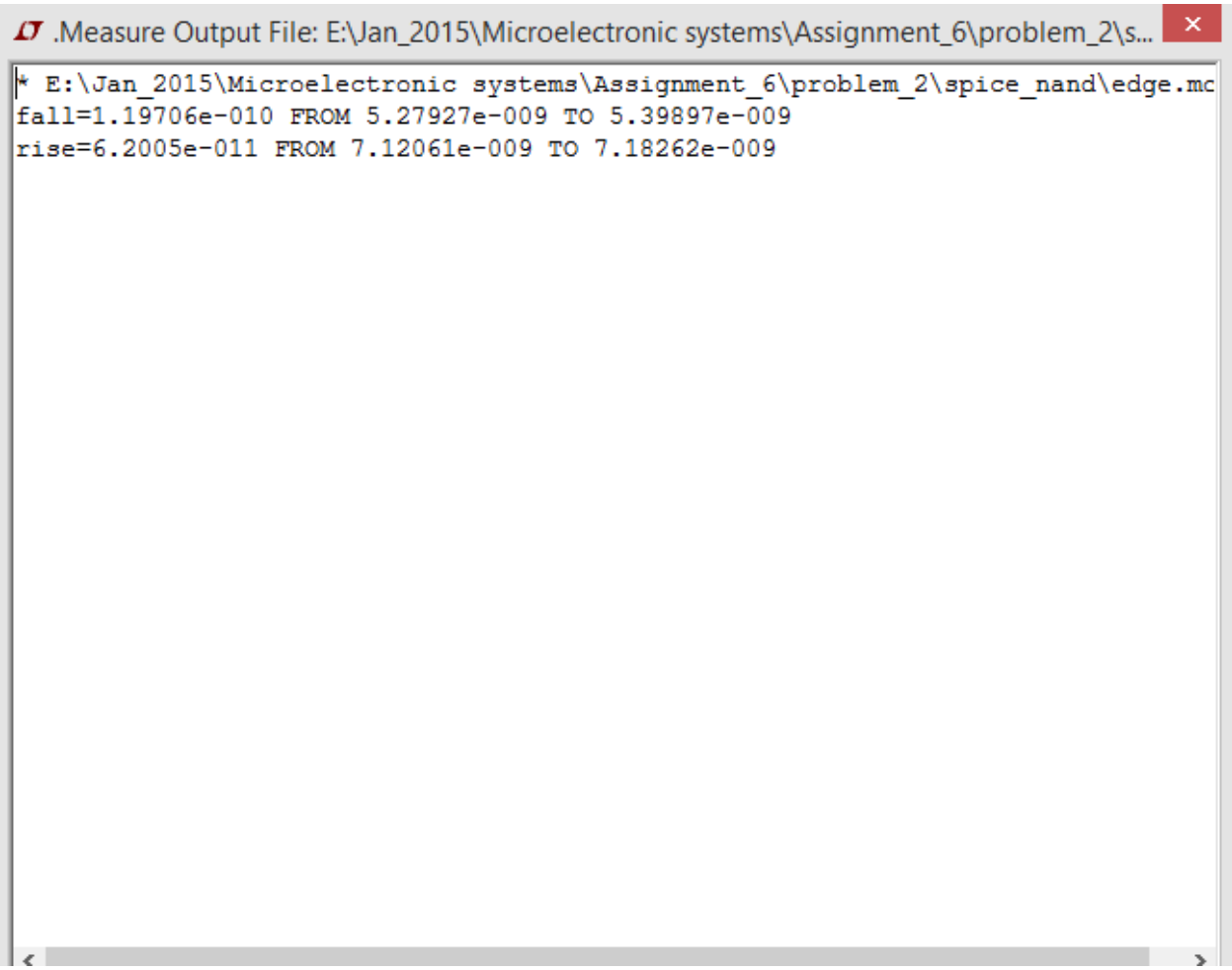

Figure 11: Rise and fall time of the above circuit

Parasitic parameters

```
*** SPICE deck for cell NAND_2{lay} from library tutorial_4
*** Created on Thu Jan 07, 2010 18:59:18
*** Last revised on Thu Mar 19, 2015 17:29:15
*** Written on Thu Mar 19, 2015 17:29:22 by Electric VLSI Design System,
*** version 9.05
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

*** TOP LEVEL CELL: NAND_2{lay}
Mnmos@0 net@7 B gnd gnd NMOS L=0.6U W=3.3U AS=20.07P AD=1.912P PS=31.8U
+PD=4.95U
Mnmos@1 AnandB A net@7 gnd NMOS L=0.6U W=3.3U AS=1.912P AD=4.5P PS=4.95U
+PD=7.2U
Mpmos@0 vdd B AnandB vdd PMOS L=0.6U W=2.7U AS=4.5P AD=13.579P PS=7.2U
+PD=21.225U
Mpmos@1 AnandB A vdd vdd PMOS L=0.6U W=2.7U AS=13.579P AD=4.5P PS=21.225U
+PD=7.2U

* Spice Code nodes in cell cell 'NAND_2{lay}'
vdd vdd 0 dc 5
vin in 0 dc 0 pulse 0 5 10n 1n
cload out 0 250fF
.tran 0 40n
.include C:\Electric\C5_models.txt
.END
```

Figure 12: Parasitic parameters of the nand gate

Question 4:

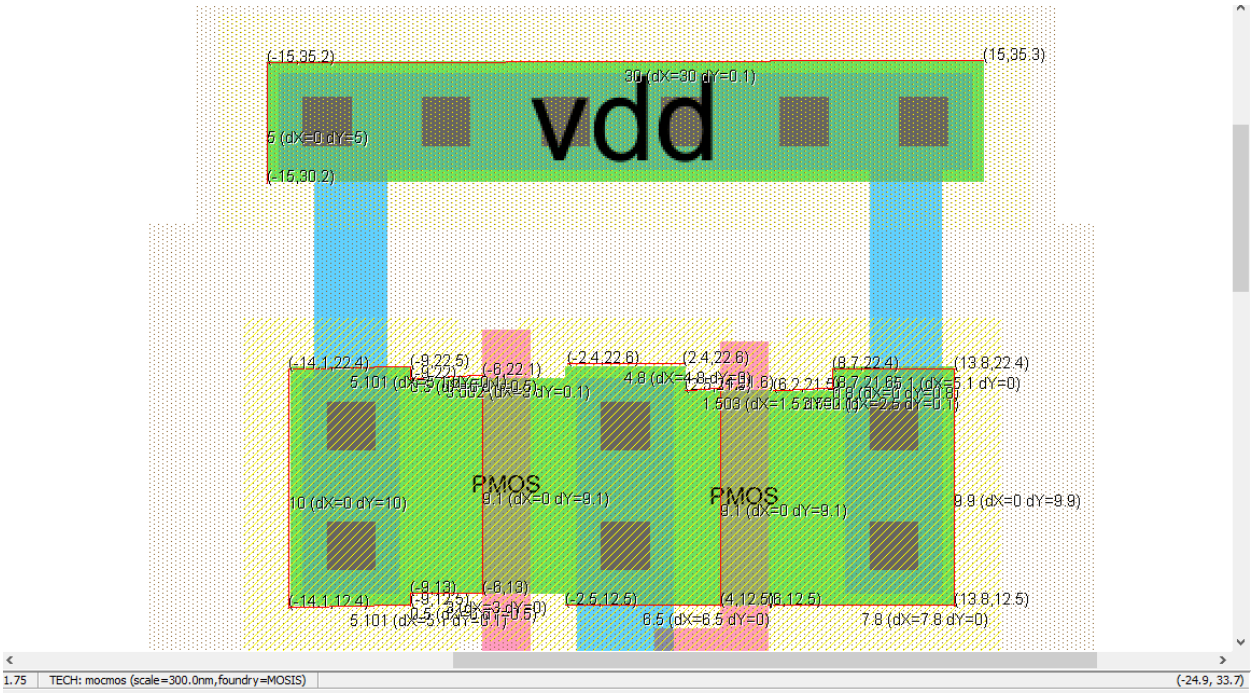

Figure 13: PMOS electric layout of NAND gate

Here λ = 0.3

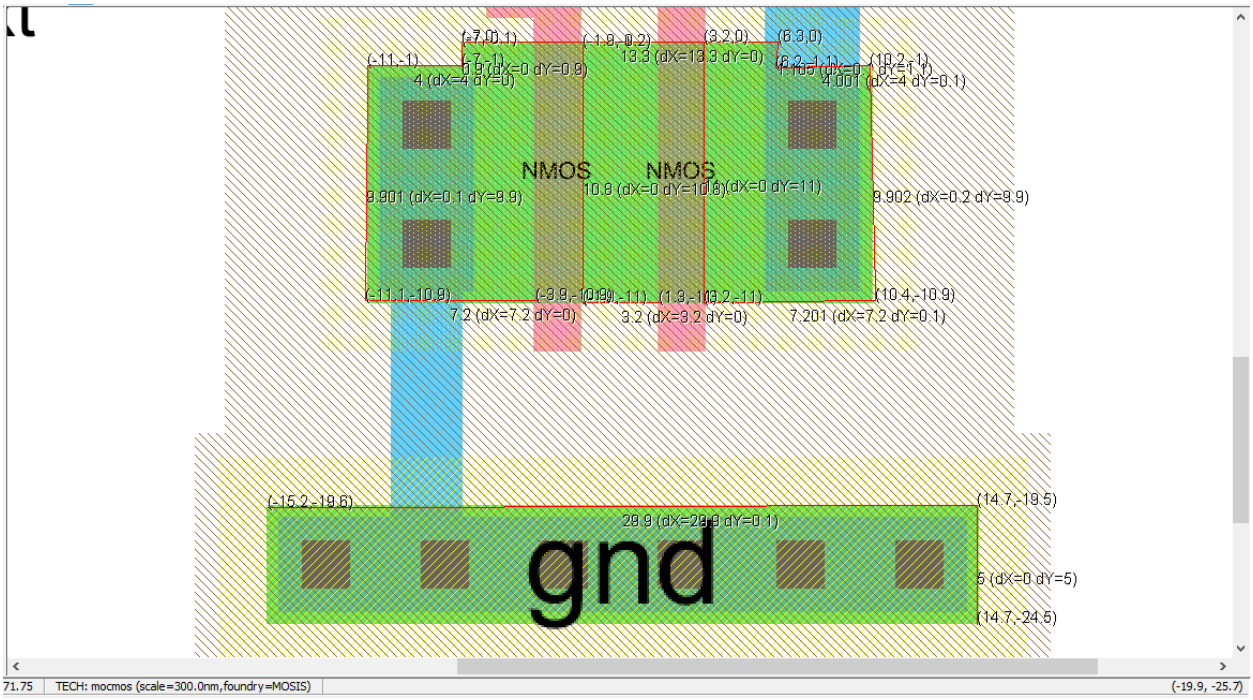

Figure 14: PMOS and NMOS Electic layout of NAND gate

<u>PMOS 1:</u>

Area of Vdd = 5*30*λ^2 = 13.5 p

Source Area = 10*5*λ^2 + 3*9*λ^2 = 4.5 + 2.45 = 6.93 p

Drain of PMOS 2 = 9*2.7*λ^2 + 5*10*λ^2 = 6.687 p

Area of source **AS** = 13.5 p

Area of drain= 9*1*λ^2+ 5*10*λ^2+1.5*9*λ^2+11*3*λ^2+10*4*λ^2 = 4.5 p

Area of Drain = **AD** = 4.5 p.

Perimeter of drain **PD** = (1.6 + 0.6 + 5+ 1+1.3+6.6+0.5+1.5+3+1+3.9+10+7+11)*λ/3 = 24.3 * λ = 7.2 u

Perimeter of source = **PS** = (9+3+0.5+5+10+5+0.5+3+70+9+1+5+10+7.5)*λ/2 = 21.2 u

<u>PMOS 0:</u>

Perimeter of drain **PD** = (9+3+0.5+5+10+5+0.5+3+70+9+1+5+10+7.5)*λ/2 = 21.2 u

Perimeter of source = **PS** = (1.6 + 0.6 + 5+ 1+1.3+6.6+0.5+1.5+3+1+3.9+10+7+11)*λ/3 = 24.3 * λ = 7.2 u

Area of source **AS** = 4.5 p

Area of Drain = **AD** = 13.5 p

NMOS 1:

Perimeter of source **PS** = (3+1+4+10+7+11+70)* λ/2 = 31.6 u

Area of Drain **AD** = (3.5*11) * λ * λ/2 = 1.74 p

Area of Source **AS** = $3*11*\lambda^2 + 4*10*\lambda^2 + 30*5*\lambda^2$ = 20.07 p

Perimeter of drain **PD** = (3.5+11)*2/2*λ = 4.4 u

Which is nearly equal to 4.9 u

NMOS 2:

Area of source **AS** = (3.5*11) * λ * λ/2 = 1.74 p

Area of Drain **AD**= $9*1*\lambda^2 + 5*10*\lambda^2 + 1.5*9*\lambda^2 + 11*3*\lambda^2 + 10*4*\lambda^2$ = 4.5 p

Perimeter of source **PS** = (3.5+11)*2/2*λ = 4.4 u

Perimeter of drain = **PD** = (1.6 + 0.6 + 5+ 1+1.3+6.6+0.5+1.5+3+1+3.9+10+7+11)*λ/3 = 24.3 * λ = 7.2 u

Question 5:

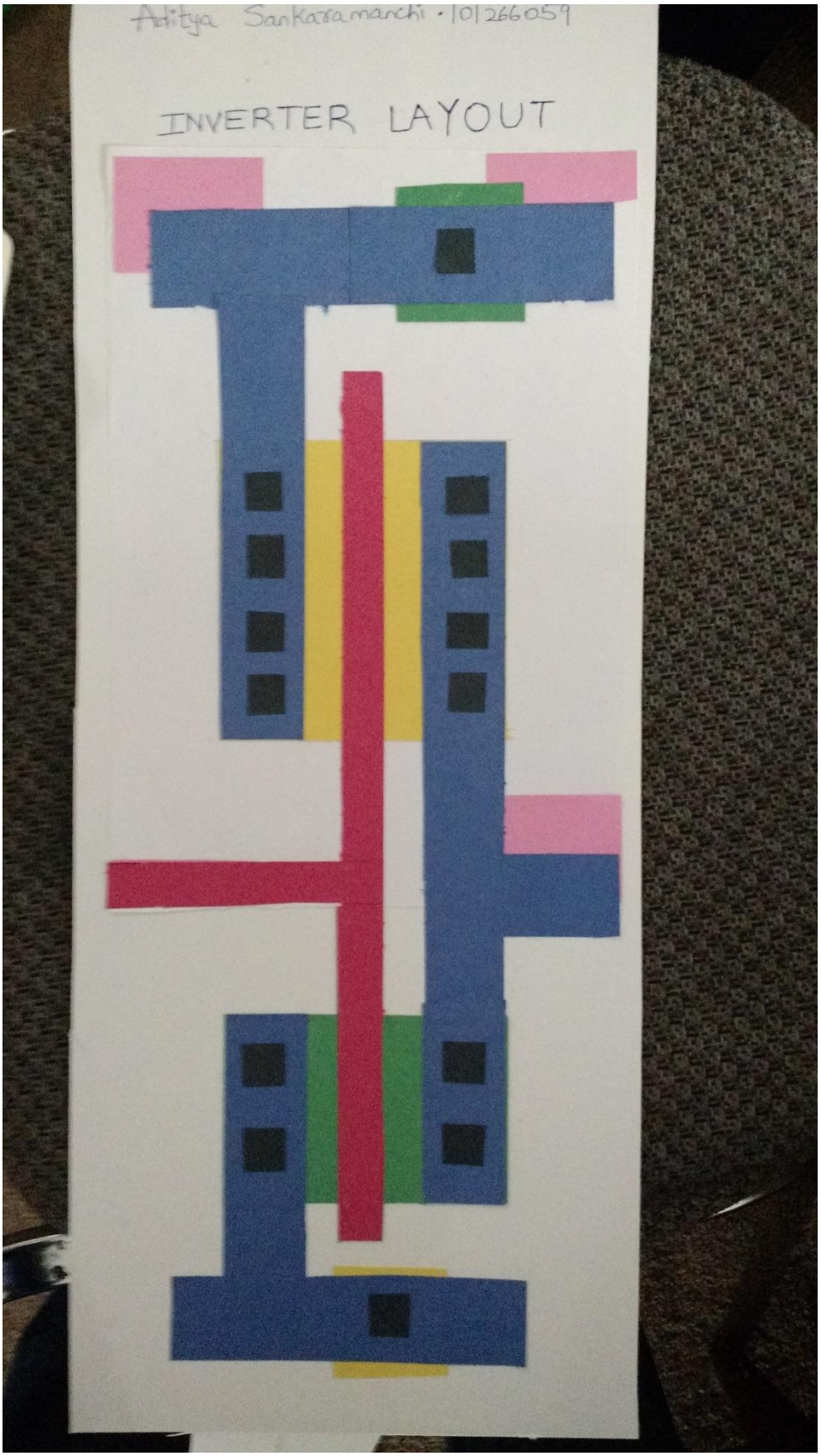
Aditya Sankaramanchi · 10126059
INVERTER LAYOUT

Figure 15: Layout of the inverter

For the above layout, I did not get the pink paper.

Question 6

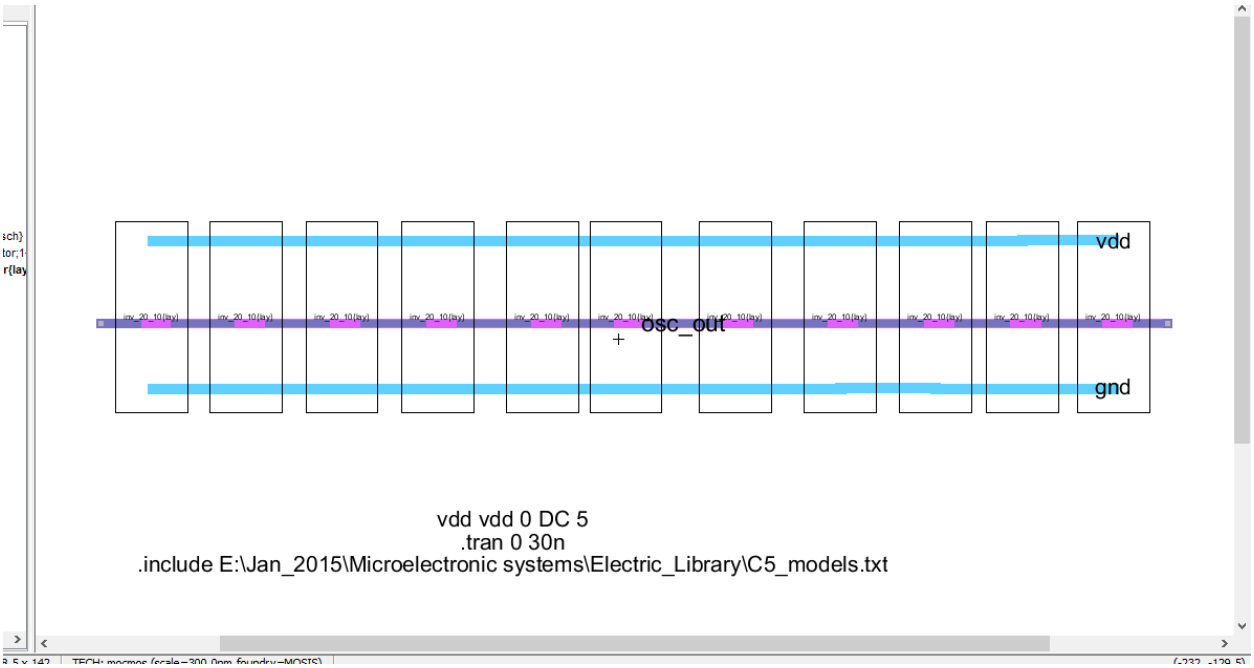

Figure 16: Layout of the ring oscillator

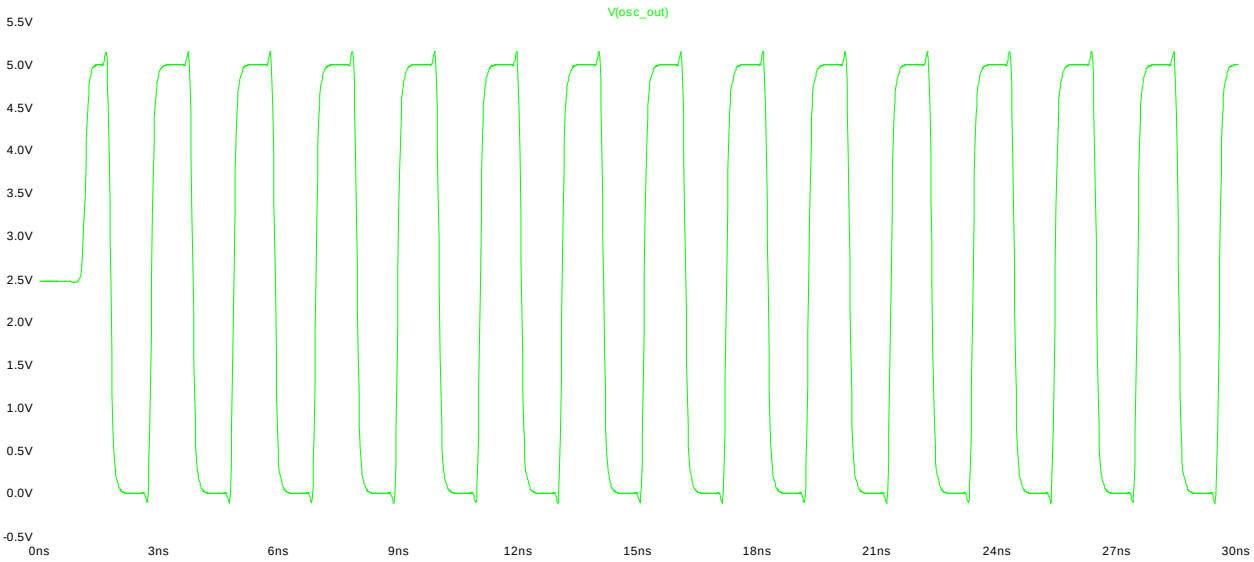

Figure 17: LTSpice output of the ring oscillator

```
*** SPICE deck for cell ring_oscillator{lay} from library tutorial_5
*** Created on Wed Mar 18, 2015 23:54:04
*** Last revised on Sat Mar 21, 2015 16:16:39
*** Written on Sat Mar 21, 2015 16:19:34 by Electric VLSI Design System,
*** version 9.05
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

*** SUBCIRCUIT tutorial_5__inv_20_10 FROM CELL inv_20_10{lay}
.SUBCKT tutorial_5__inv_20_10 gnd in out vdd
Mnmos@0 out in gnd gnd NMOS L=0.6U W=3U AS=14.67P AD=8.415P PS=24.78U
+PD=12.75U
Mpmos@0 vdd in out vdd PMOS L=0.6U W=6U AS=8.415P AD=20.16P PS=12.75U
+PD=30.72U
.ENDS tutorial_5__inv_20_10

*** TOP LEVEL CELL: ring_oscillator{lay}
Xinv_20_1@125 gnd net@23 net@24 vdd tutorial_5__inv_20_10
Xinv_20_1@126 gnd net@24 osc_out vdd tutorial_5__inv_20_10
Xinv_20_1@127 gnd osc_out net@26 vdd tutorial_5__inv_20_10
Xinv_20_1@128 gnd net@22 net@23 vdd tutorial_5__inv_20_10
Xinv_20_1@129 gnd net@21 net@22 vdd tutorial_5__inv_20_10
Xinv_20_1@130 gnd net@20 net@21 vdd tutorial_5__inv_20_10
Xinv_20_1@131 gnd net@26 net@27 vdd tutorial_5__inv_20_10
Xinv_20_1@132 gnd net@27 net@28 vdd tutorial_5__inv_20_10
Xinv_20_1@133 gnd net@28 net@29 vdd tutorial_5__inv_20_10
Xinv_20_1@134 gnd net@30 net@20 vdd tutorial_5__inv_20_10
Xinv_20_1@135 gnd net@29 net@30 vdd tutorial_5__inv_20_10

* Spice Code nodes in cell cell 'ring_oscillator{lay}'
vdd vdd 0 DC 5
.tran 0 30n
.include E:\Jan_2015\Microelectronic systems\Electric_Library\C5_models.txt
.END
```

Figure 18: Spice netlist of the ring oscillator

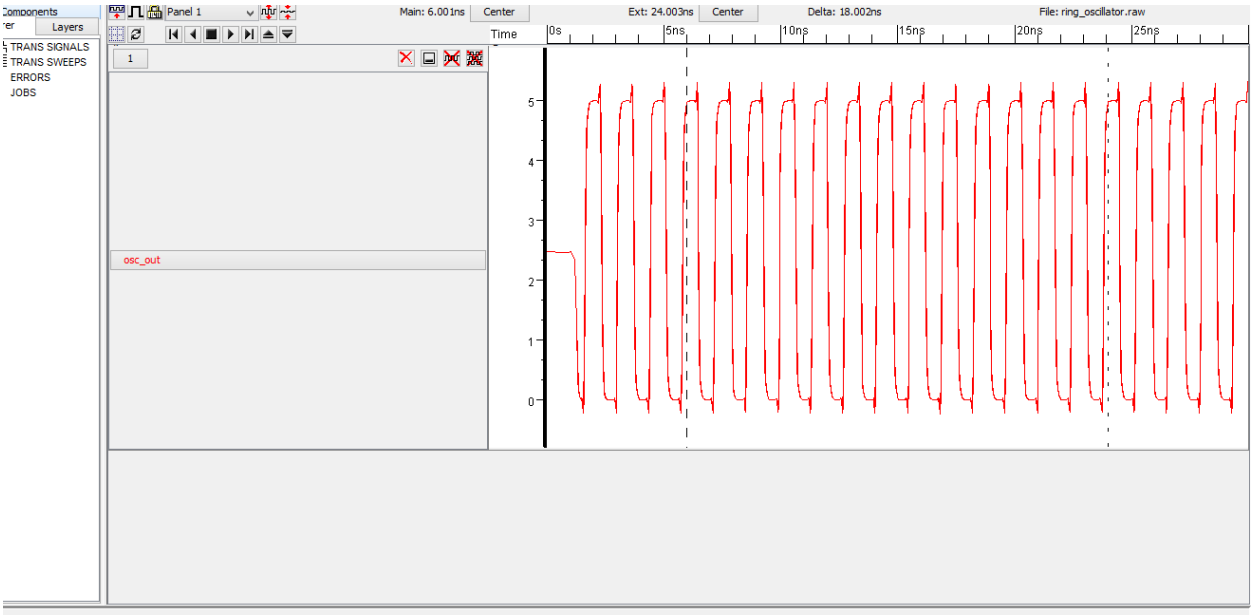

Figure 19: Electric output of the ring oscillator

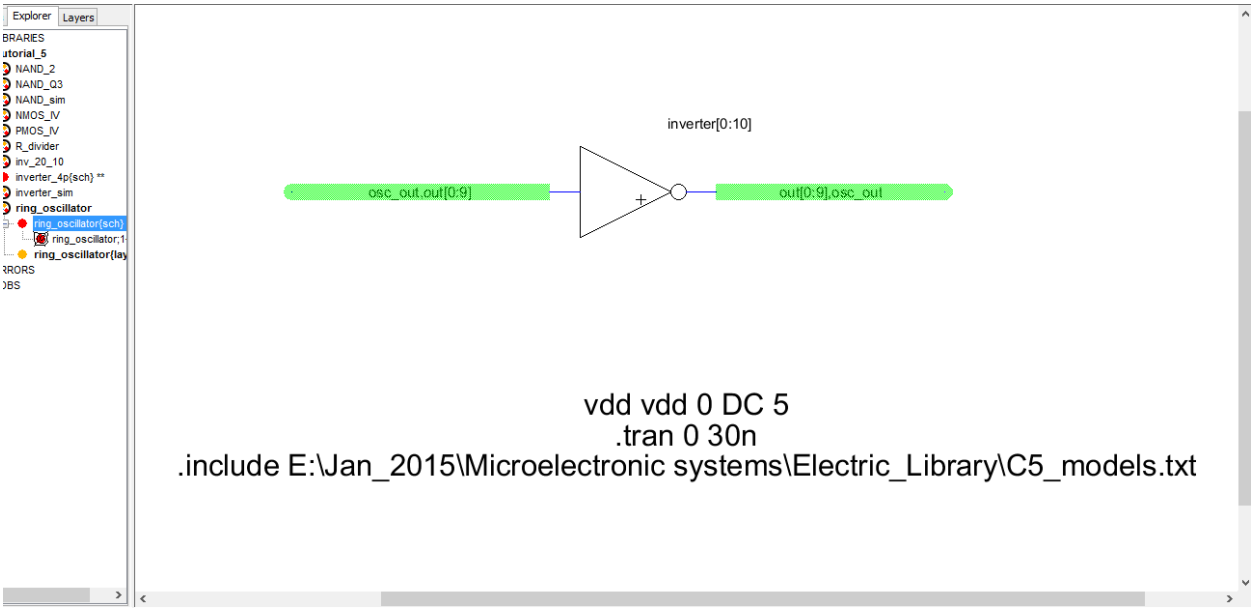

Figure 20: Ring oscillator schematic

ring_oscillator.spi ring_oscillator.spi

```
*** SPICE deck for cell ring_oscillator{sch} from library tutorial_5
*** Created on Wed Mar 18, 2015 23:22:27
*** Last revised on Wed Mar 18, 2015 23:50:49
*** Written on Sat Mar 21, 2015 16:33:25 by Electric VLSI Design System,
*** version 9.05
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF

*** SUBCIRCUIT tutorial_5__inv_20_10 FROM CELL inv_20_10{sch}
.SUBCKT tutorial_5__inv_20_10 in out
** GLOBAL gnd
** GLOBAL vdd
Mnmos@0 out in gnd gnd NMOS L=0.6U W=3U
Mnmos@1 out in vdd vdd PMOS L=0.6U W=6U
.ENDS tutorial_5__inv_20_10

.global gnd vdd

*** TOP LEVEL CELL: ring_oscillator{sch}
Xinverter[0] osc_out out[0] tutorial_5__inv_20_10
Xinverter[1] out[0] out[1] tutorial_5__inv_20_10
Xinverter[2] out[1] out[2] tutorial_5__inv_20_10
Xinverter[3] out[2] out[3] tutorial_5__inv_20_10
Xinverter[4] out[3] out[4] tutorial_5__inv_20_10
Xinverter[5] out[4] out[5] tutorial_5__inv_20_10
Xinverter[6] out[5] out[6] tutorial_5__inv_20_10
Xinverter[7] out[6] out[7] tutorial_5__inv_20_10
Xinverter[8] out[7] out[8] tutorial_5__inv_20_10
Xinverter[9] out[8] out[9] tutorial_5__inv_20_10
Xinverter[10] out[9] osc_out tutorial_5__inv_20_10

* Spice Code nodes in cell cell 'ring_oscillator{sch}'
vdd vdd 0 DC 5
.tran 0 30n
.include E:\Jan_2015\Microelectronic systems\Electric_Library\C5_models.txt
.END
```

Figure 21: Spice netlist of schematic

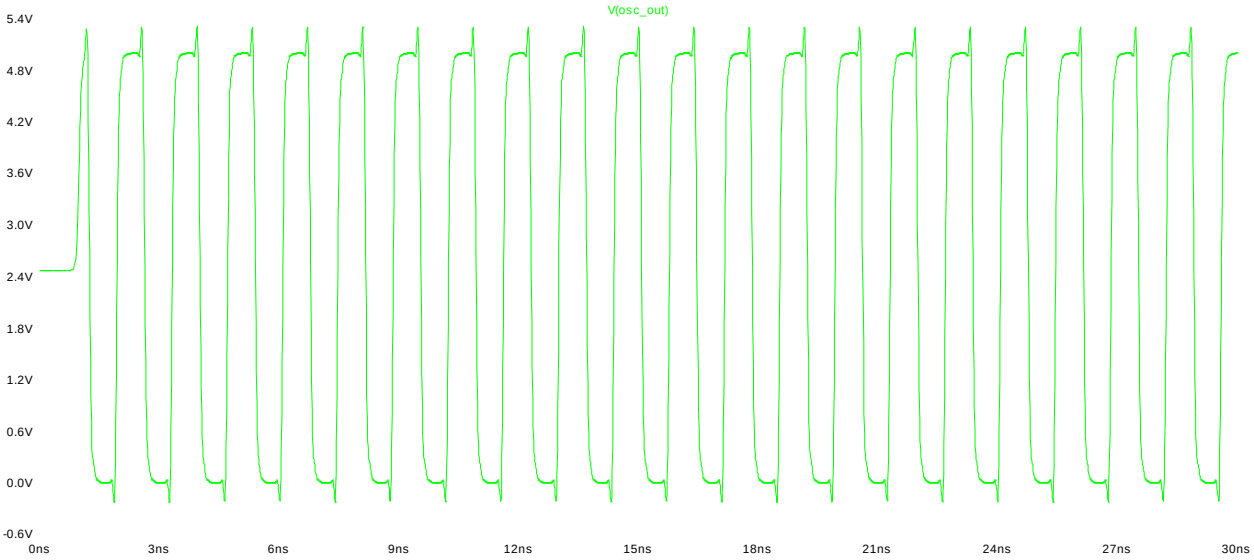

Figure 22: Spice output of the ring oscillator

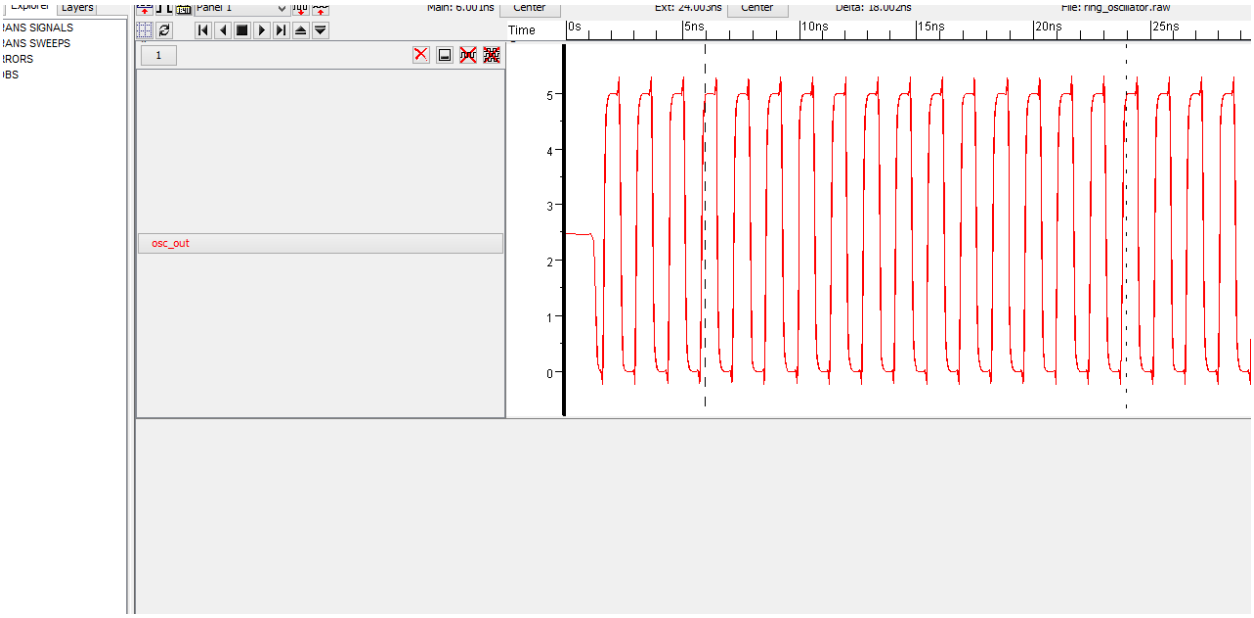

Figure 23: Electric output of the ring oscillator

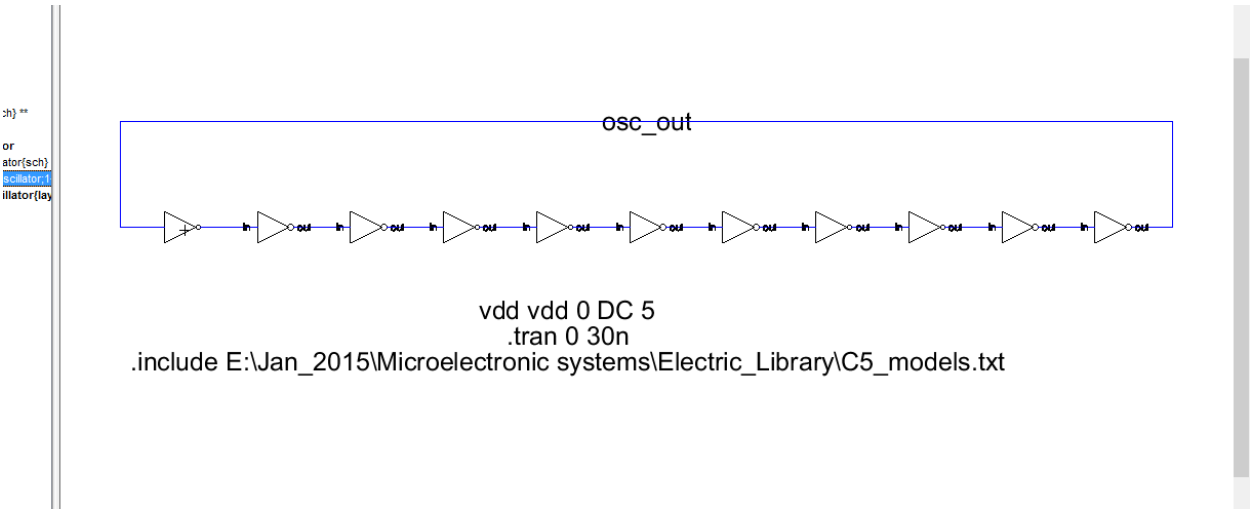

Figure 24: Ring oscillator

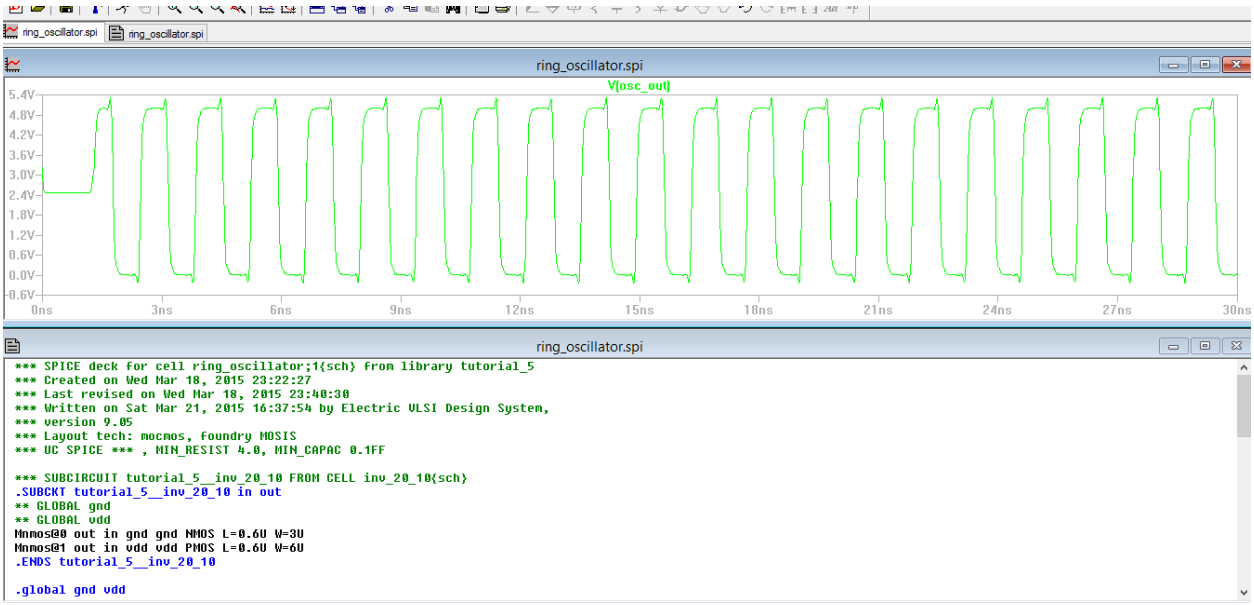

Figure 25: LTSpice output of the ring oscillator

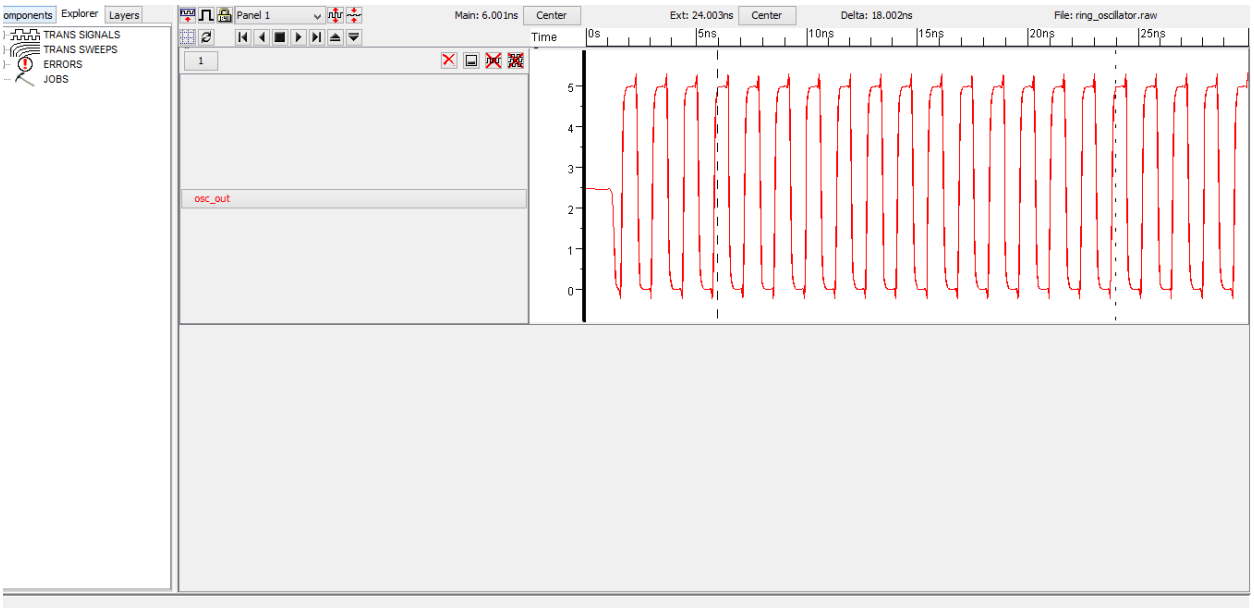

Figure 26: Electric output of the ring oscillator