ECE 531

Microelectronics

Assignment 3

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Problem 1:

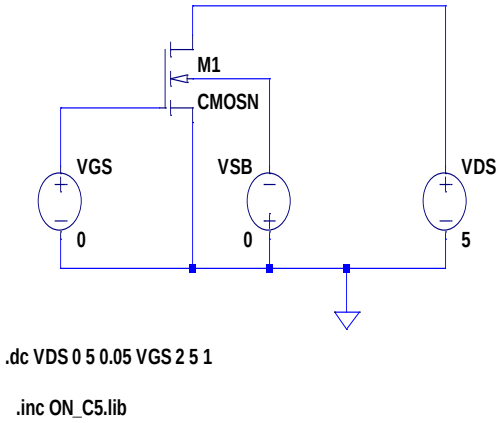


Figure 1 : LTSpice circuit diagram of NMOS transistor using CMOSN model.

Here W/L = 7.2 µm/ 0.6 µm

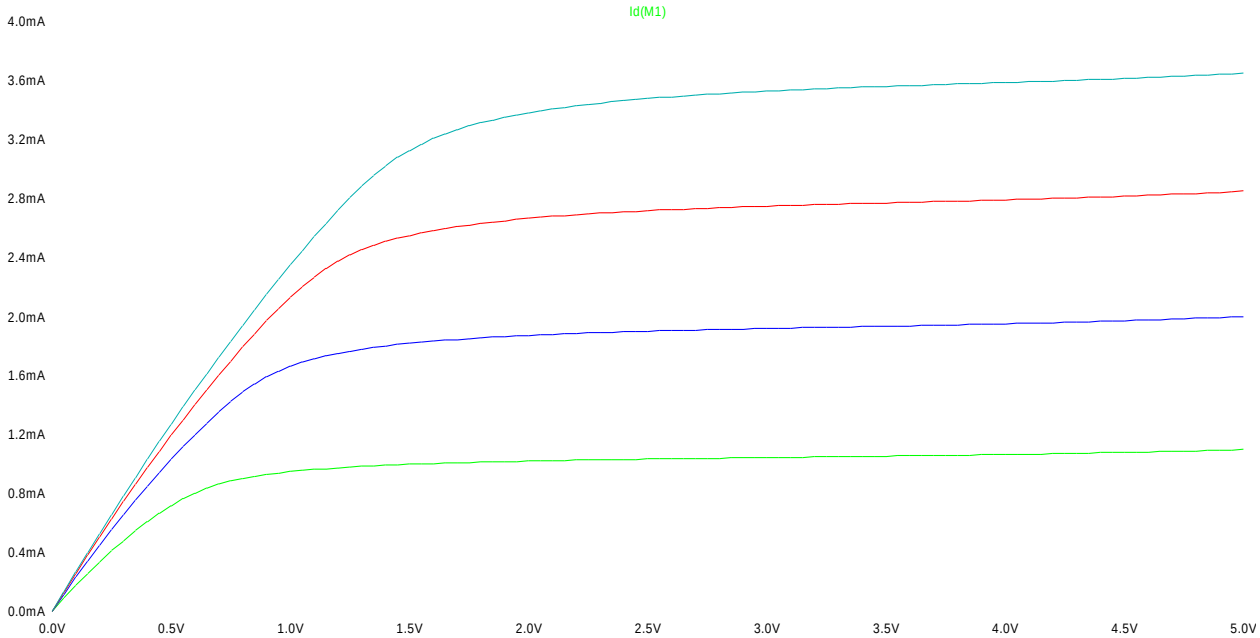


Figure 2: I-V curves for an NMOS transistor

SPICE Netlist: E:\Jan_2015\Microelectronic systems\Assignment_3\circuits\prob_1.net

```
* E:\Jan_2015\Microelectronic systems\Assignment_3\circuits\prob_1.asc
VGS N003 0 0
VDS N001 0 5
VSB 0 N002 0
M1 N001 N003 0 N002 CMOSN l=0.6u w=7.2u
.model NMOS NMOS
.model PMOS PMOS
.lib D:\LTSpice\lib\cmp\standard.mos
.dc VDS 0 5 0.05 VGS 2 5 1
.inc ON_C5.lib
.backanno
.end
```

Figure 3: Spice Netlist

Problem 2:

NMOS transistor in series:

Here width W= 3 µm ; L = 0.6 µm

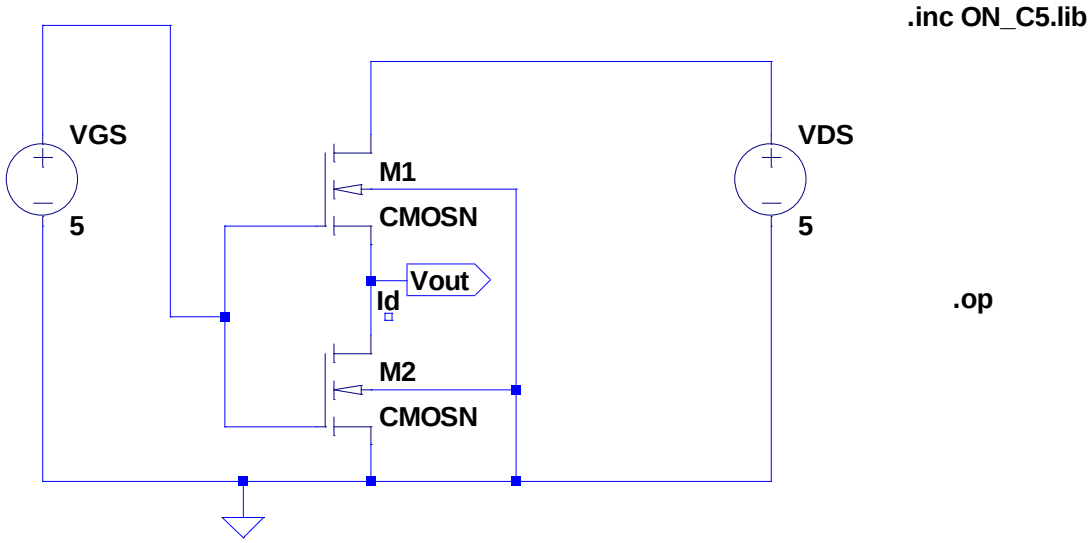


Figure 4: NMOS transistors in series

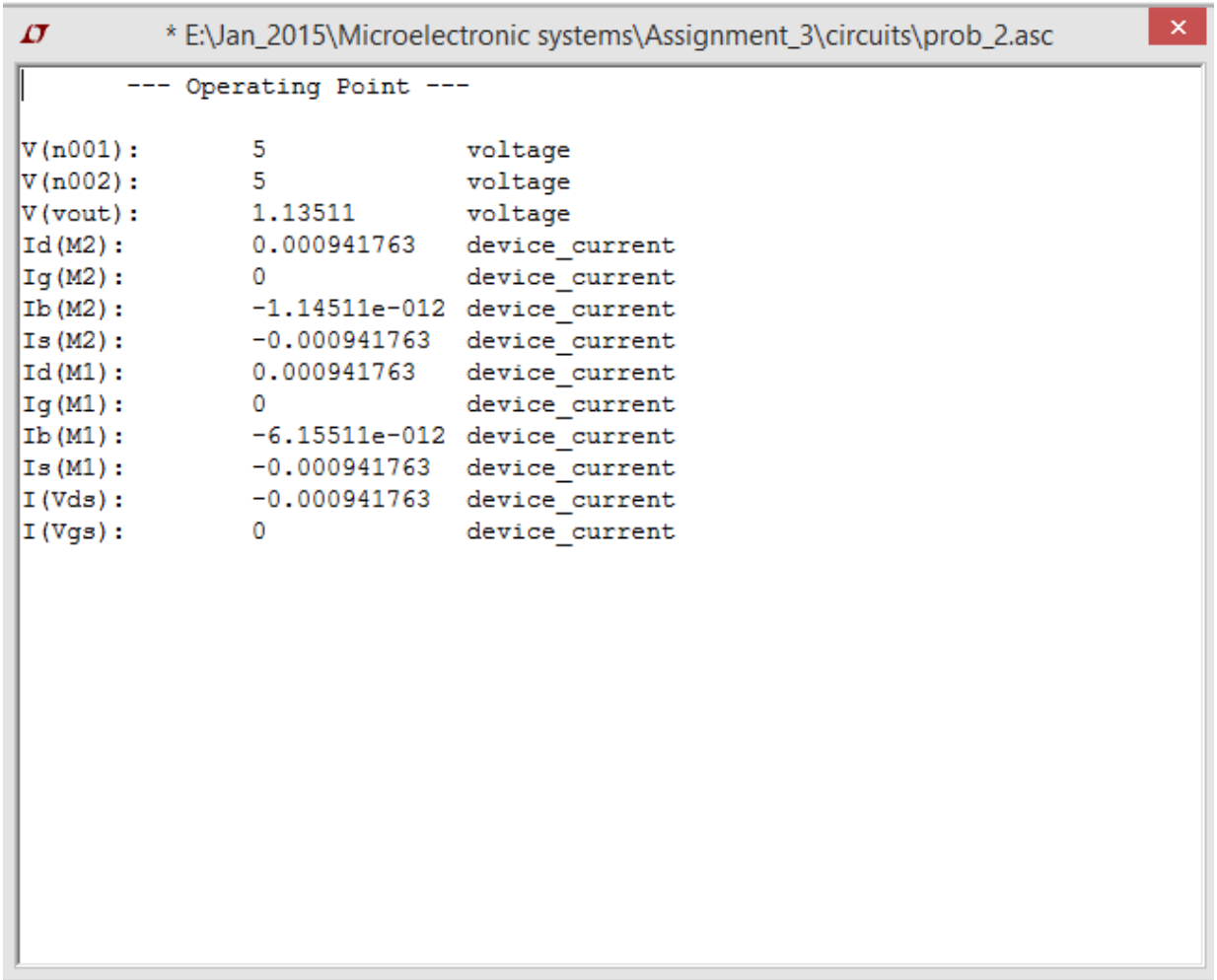


Figure 5: Operating point for NMOS transistors in series

Voltage V(out) = 1.135 Volts. Current I_d = 0.000941 amps = 941 µA

Problem 3:

Given W = 8 λ = 8*0.3 µm = 2.4 µm

L = 2 λ = 2*0.3 µm = 0.6 µm

VDD = 5 V

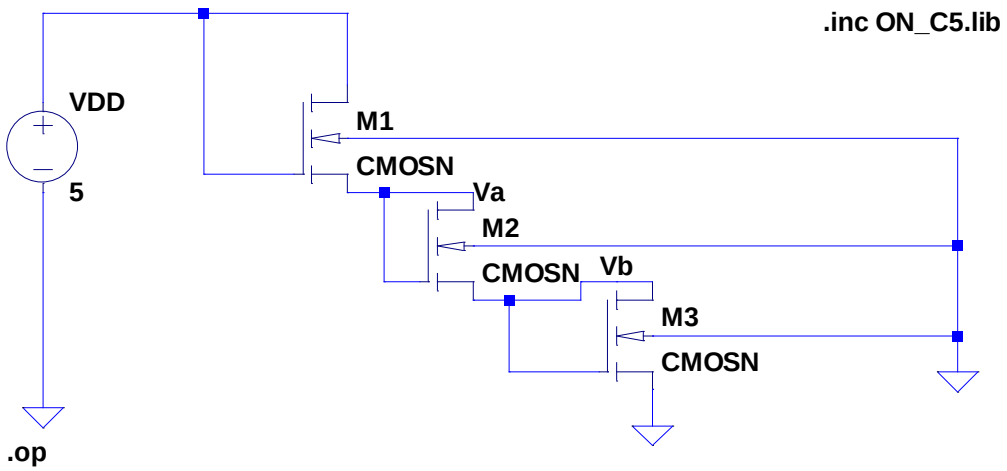
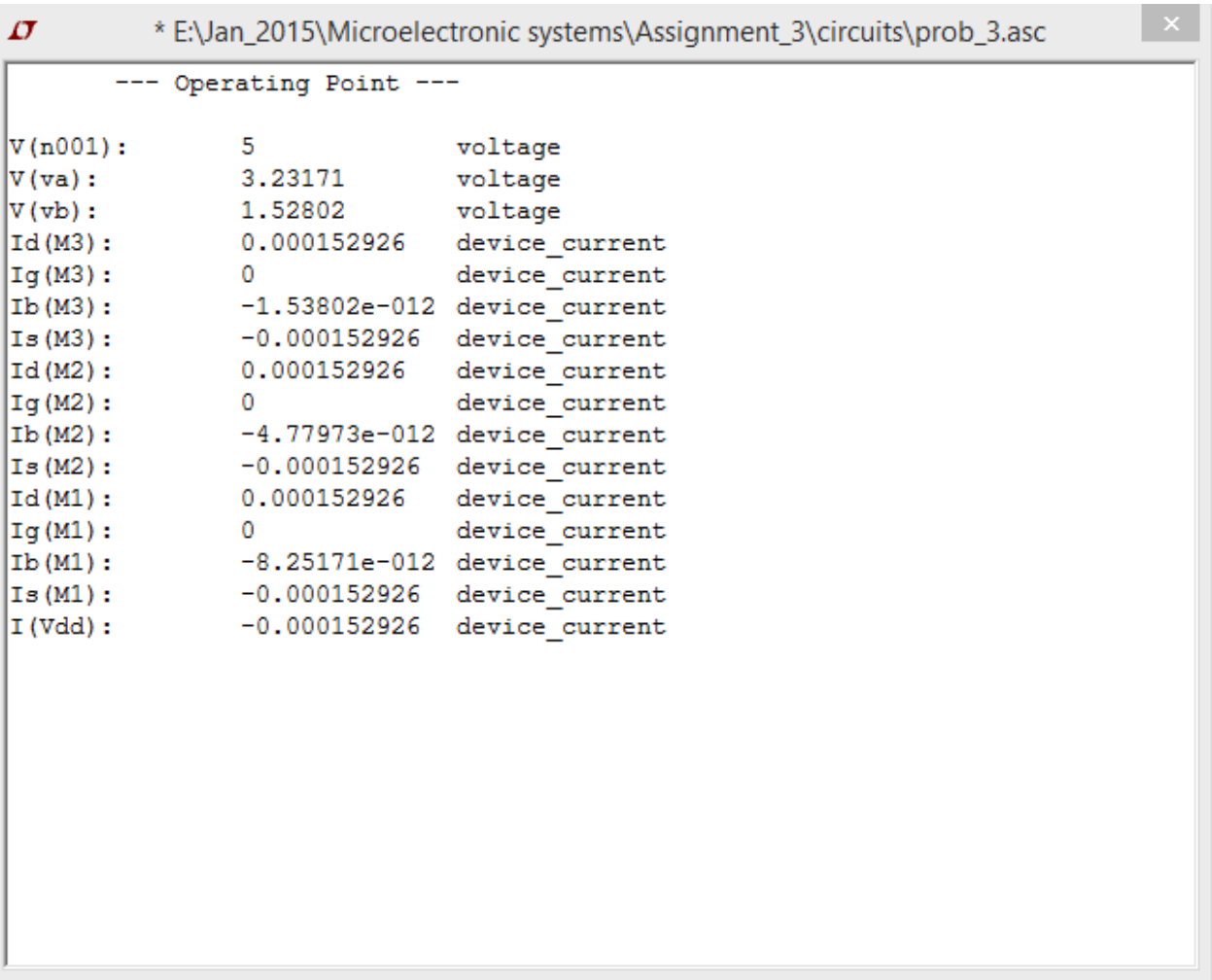


Figure 6: LTSpice figure of the required transistor circuit

SPICE Netlist: E:\Jan_2015\Microelectronic systems\Assignment_3\circuits\prob_3.net

```
* E:\Jan_2015\Microelectronic systems\Assignment_3\circuits\prob_3.asc
M1 N001 N001 Va 0 CMOSN l=0.6u w=2.4u
M2 Va Va Vb 0 CMOSN l=0.6u w=2.4u
M3 Vb Vb 0 0 CMOSN l=0.6u w=2.4u
VDD N001 0 5
.model NMOS NMOS
.model PMOS PMOS
.lib D:\LTSpice\lib\cmp\standard.mos
.op
.inc ON_C5.lib
.backanno
.end
```

Figure 7: Spcie Netlist of the required transistor circuit



From the spcie operating point figure

$$V_a = 3.23\,V\ ;\ V_b = 1.52\,V;$$

And the currents Id, Is, Ig and Ib are obtained.

Problem 4:

a. To find the threshold voltage if $V_{sb} = 3V$

$$V_T = V_{T0} + \boldsymbol{\gamma}(\sqrt{|-2\emptyset_F + V_{SB}|} - \sqrt{|-2\emptyset_F|})$$

From the given values

$$V_T = 0.8 + 0.6(\sqrt{2.4} - \sqrt{0.6})$$

$$= 0.8 + 0.6* 0.775$$

$$V_T = 1.265\ V$$

b. To convert C_{j0} to units fF/μm^2

Here f = 10^{-15} μ = 10^{-6}

$$= 4 * 10^{-4} * \frac{10^{-15}}{10^{-15}} * \frac{10^{-6}}{10^{-6}} \quad \frac{F}{m^2}$$

$$= 4 * 10^{5} \frac{fF}{\mu m^2}$$

c. To find bottom capacitance. Given $V_{sb} = 3V; AS = 50p$

We have $C_j = \frac{C_{j0}}{(1-\frac{V_D}{\emptyset_0})^m}$

$$C_j = \frac{4 * 10^{-4}}{(1 - (\frac{-3}{0.74})^{0.43}}$$

$$C_j = 1.992 * 10^{-4} \frac{F}{m^2}$$

Bottom capacitance $C_{bottom} = C_J * Area$

$$= 1.992 * 10^{-4} * 50 * 10^{-12}$$

$$= 99.6 * 10^{-16}$$

Bottom capacitance=9.96 fF

Problem 5:

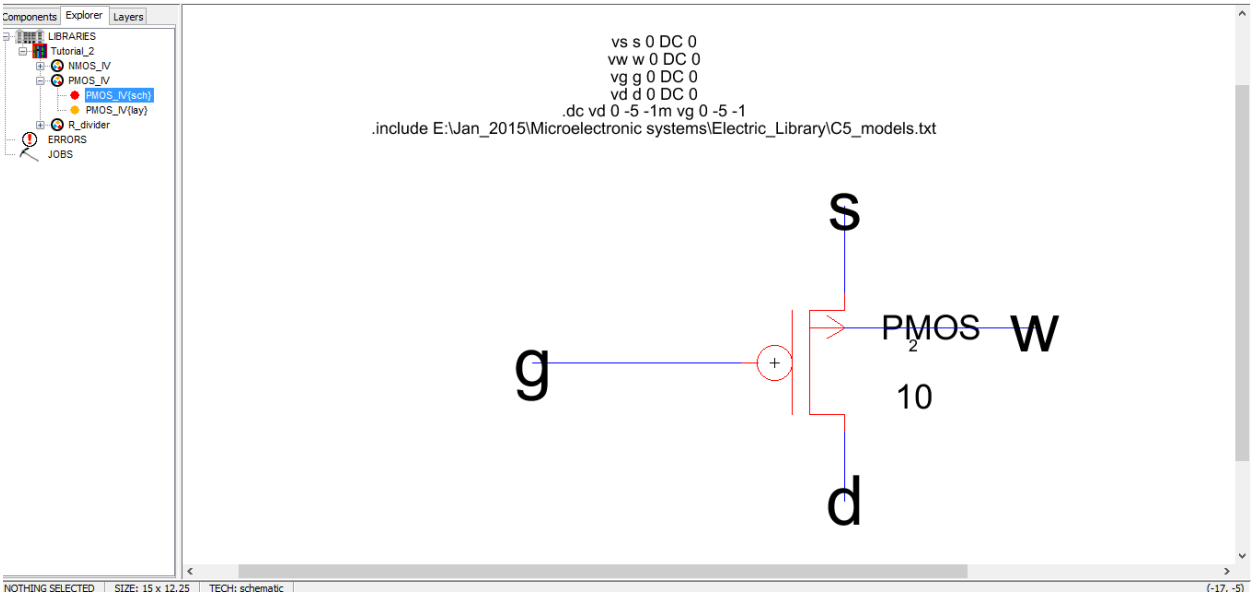


Figure 8 : Schematic view of PMOS Transistor

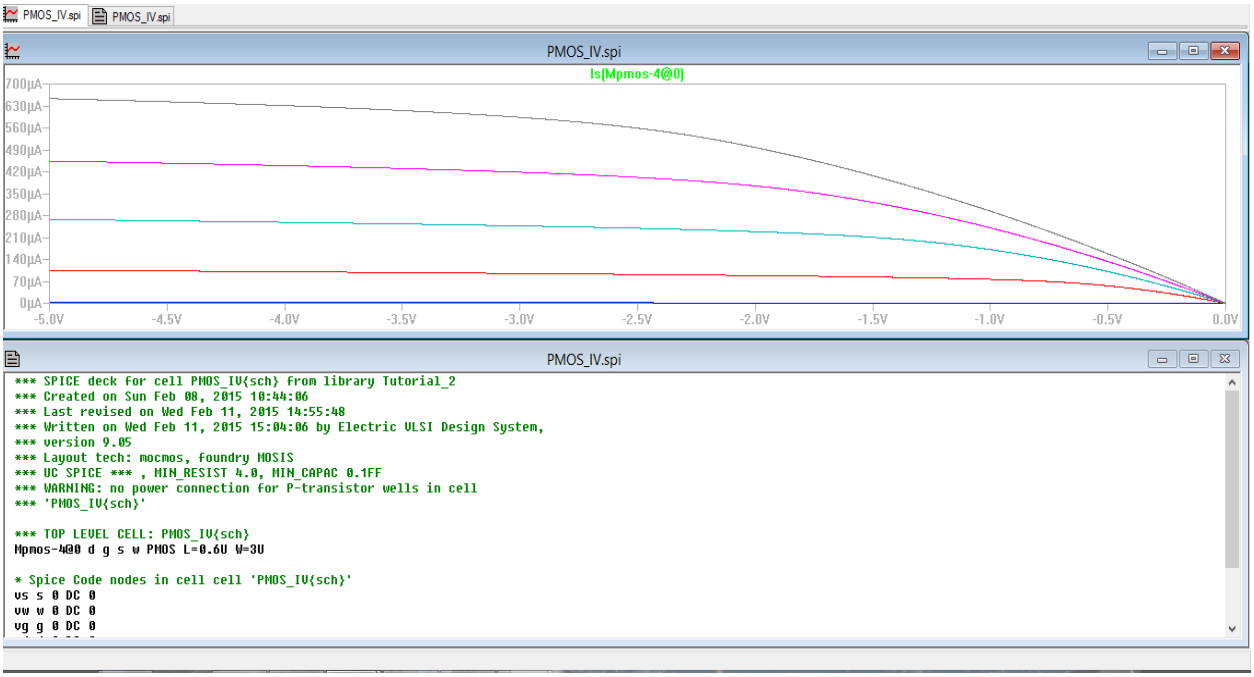


Figure 9 : Spice simulation view of PMOS transistor

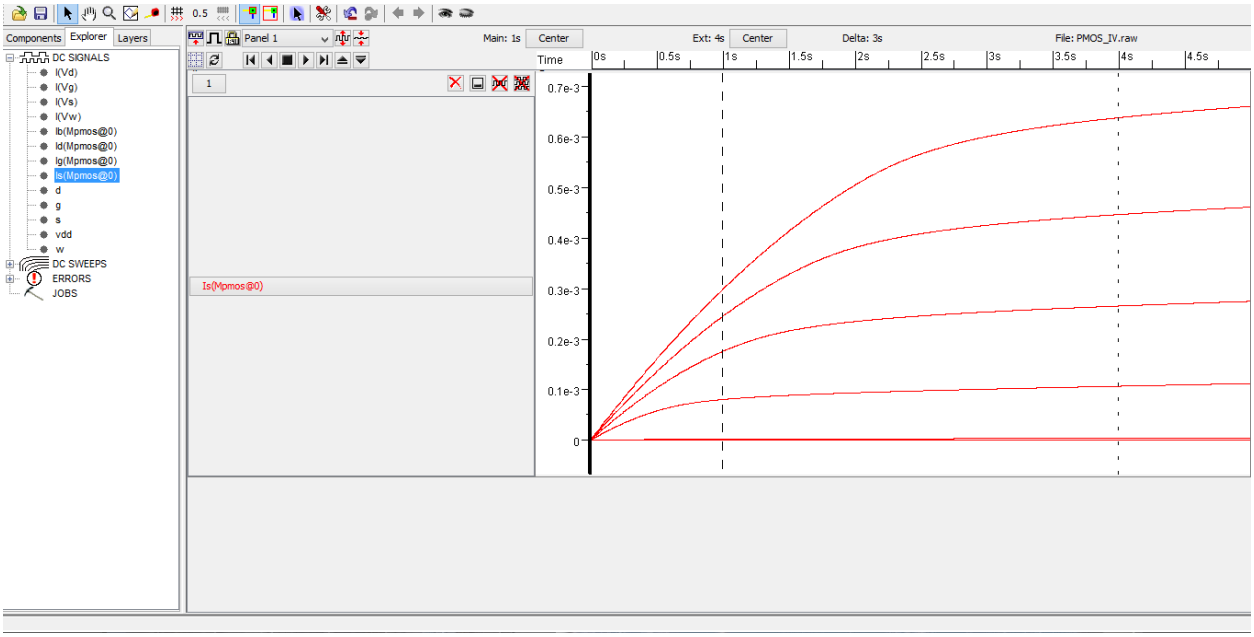


Figure 10: Electric simulation of PMOS transistor

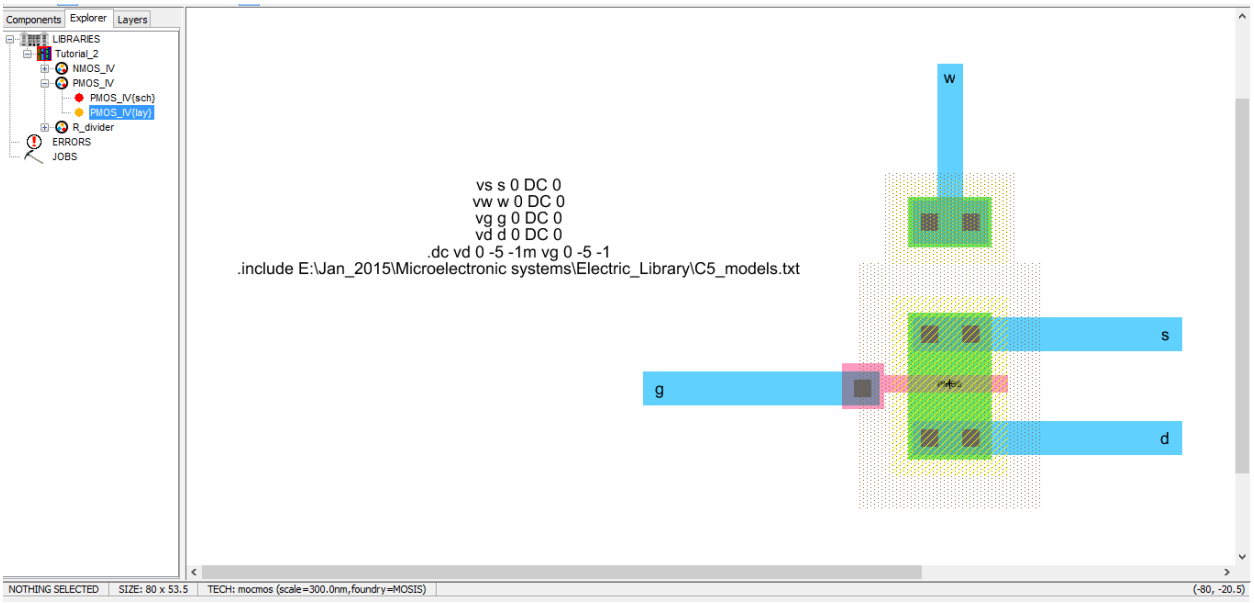


Figure 11: Layout view of PMOS transistor

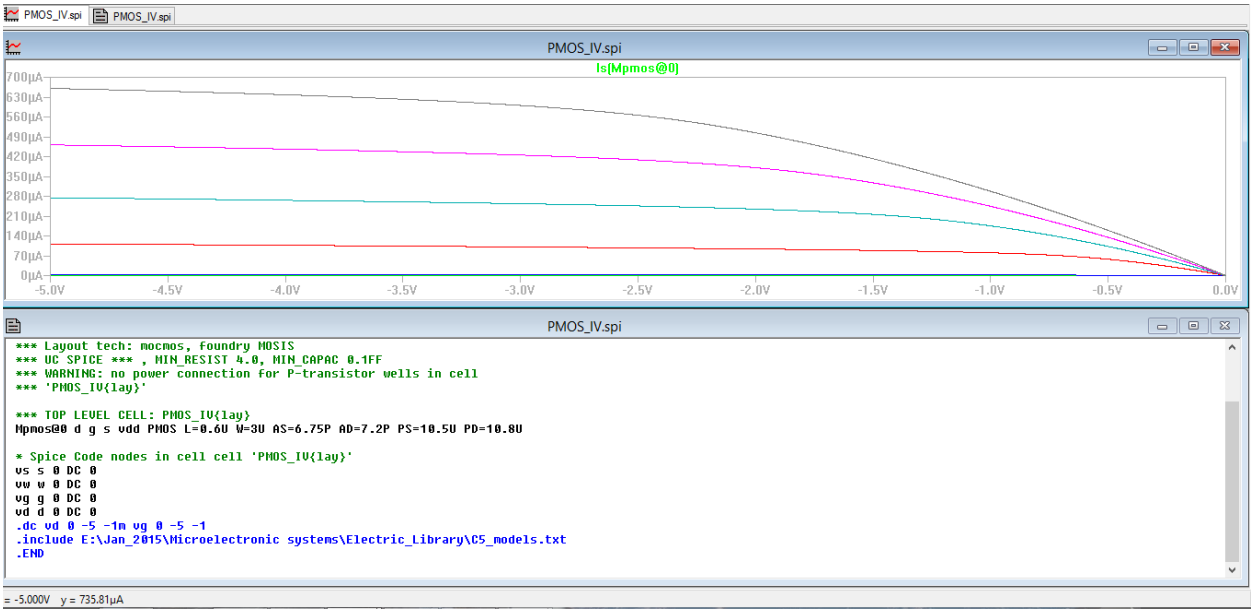


Figure 12: Spice simulation output of PMOS transistor

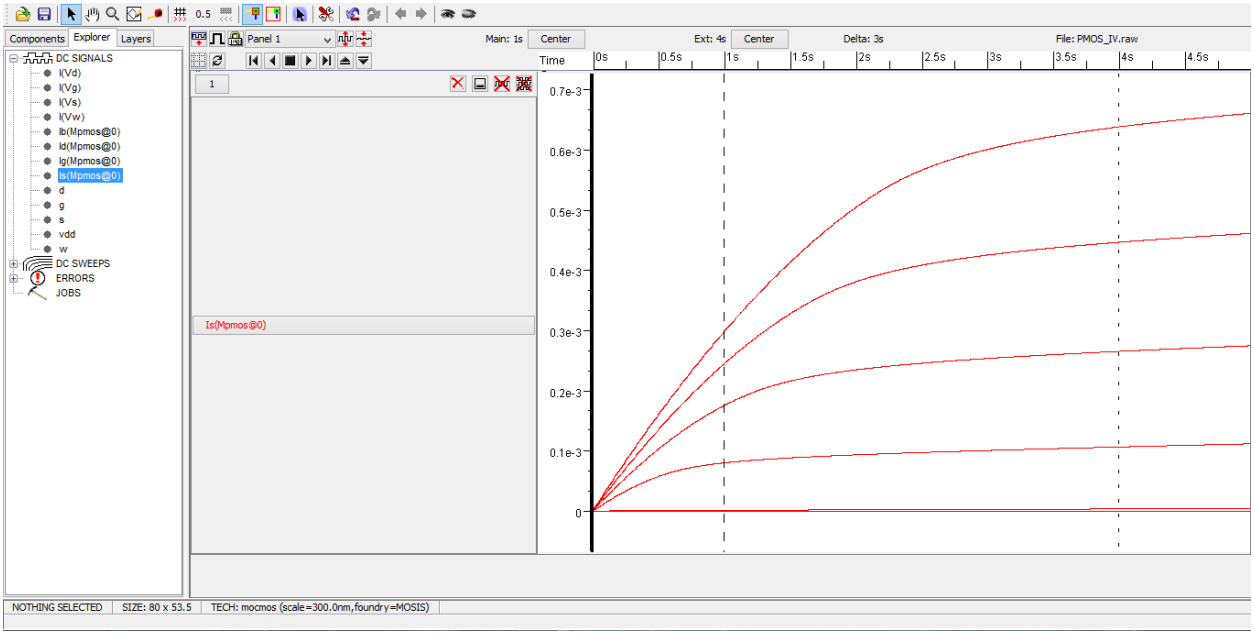


Figure 13: Electric simulation output of PMOS transistor

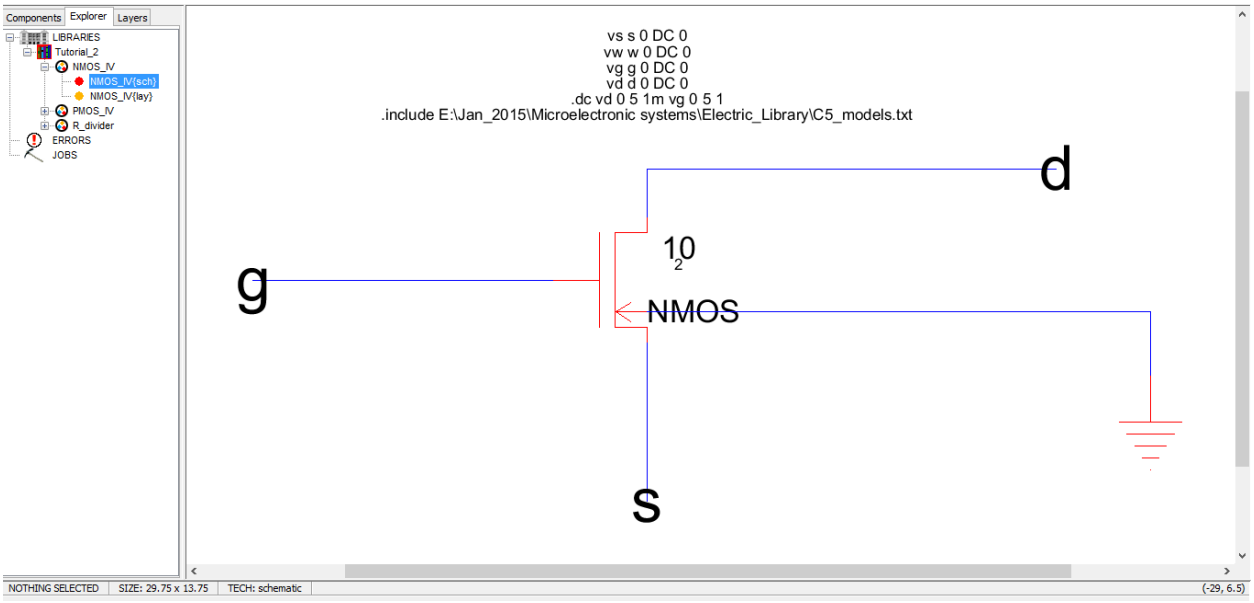


Figure 14: Schematic view of NMOS transistor

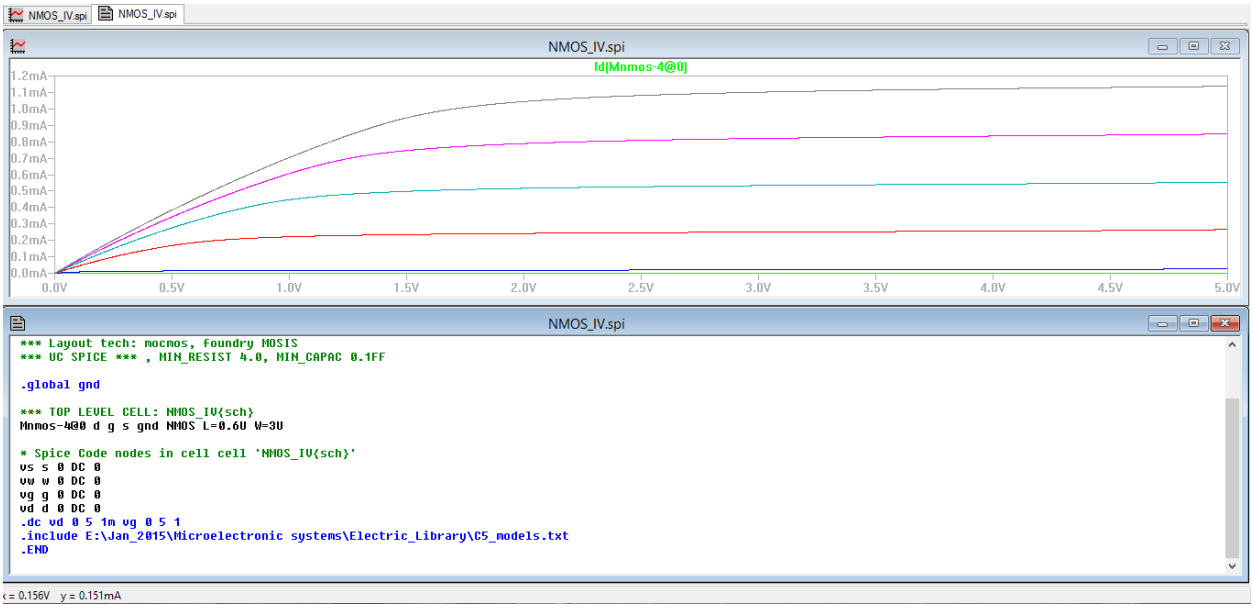


Figure 15: Spice simulation result of NMOS transistor

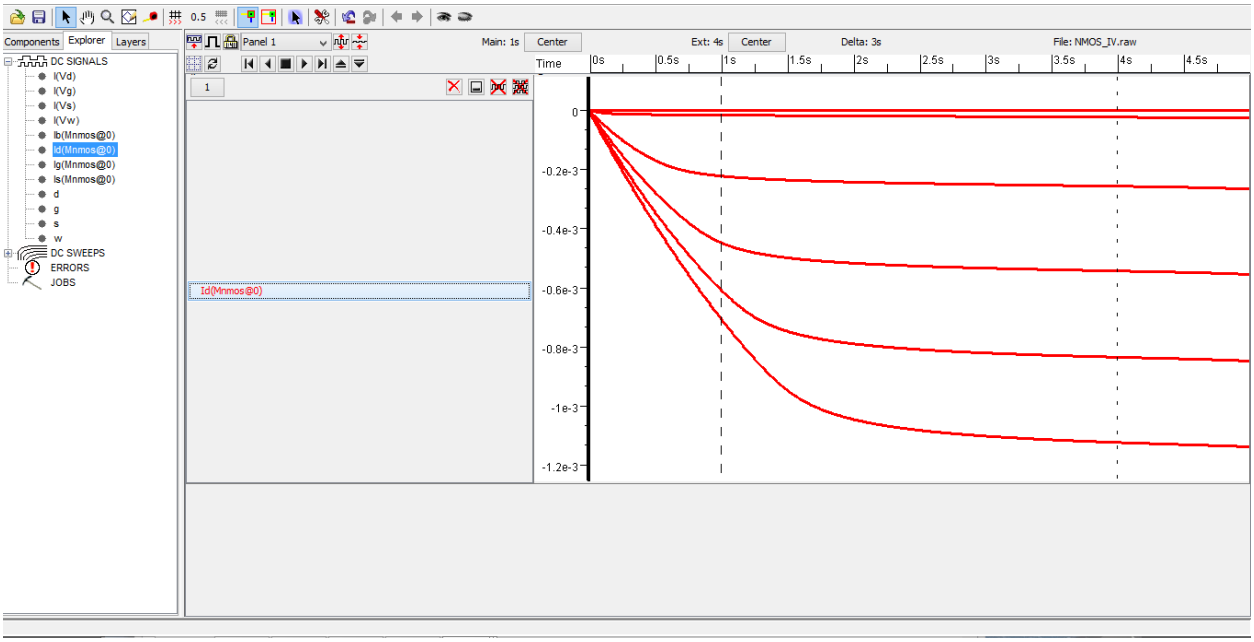


Figure 16: Electric simulation of NMOS transistor

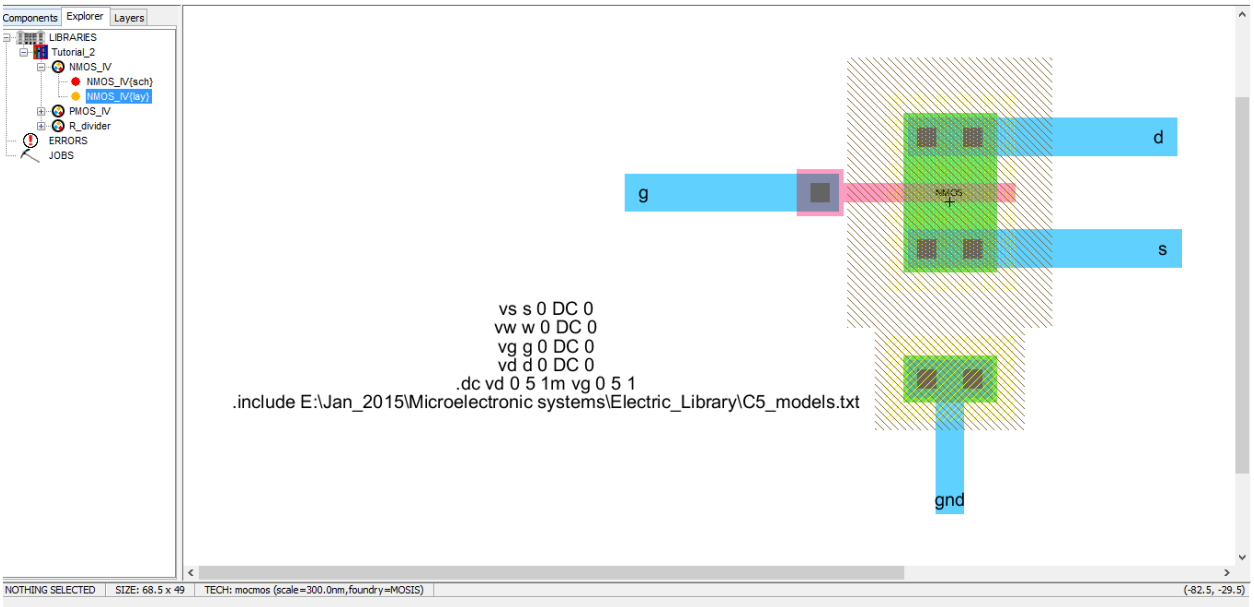


Figure 17: Layout view of NMOS transistor

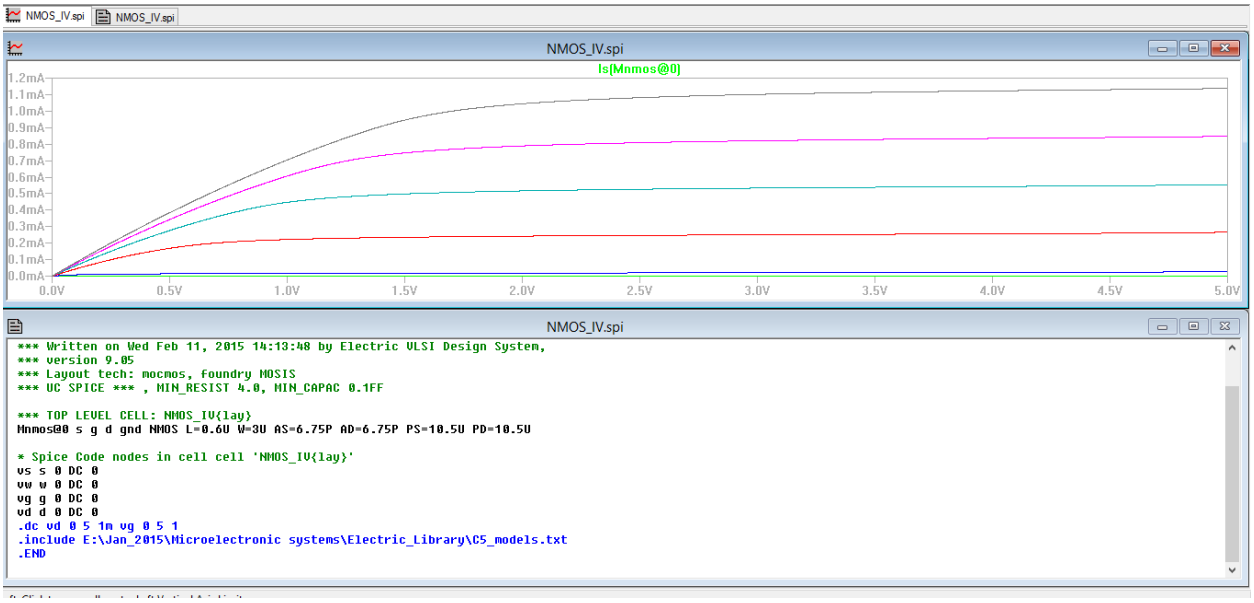


Figure 18: Spice simulation output of NMOS transistor

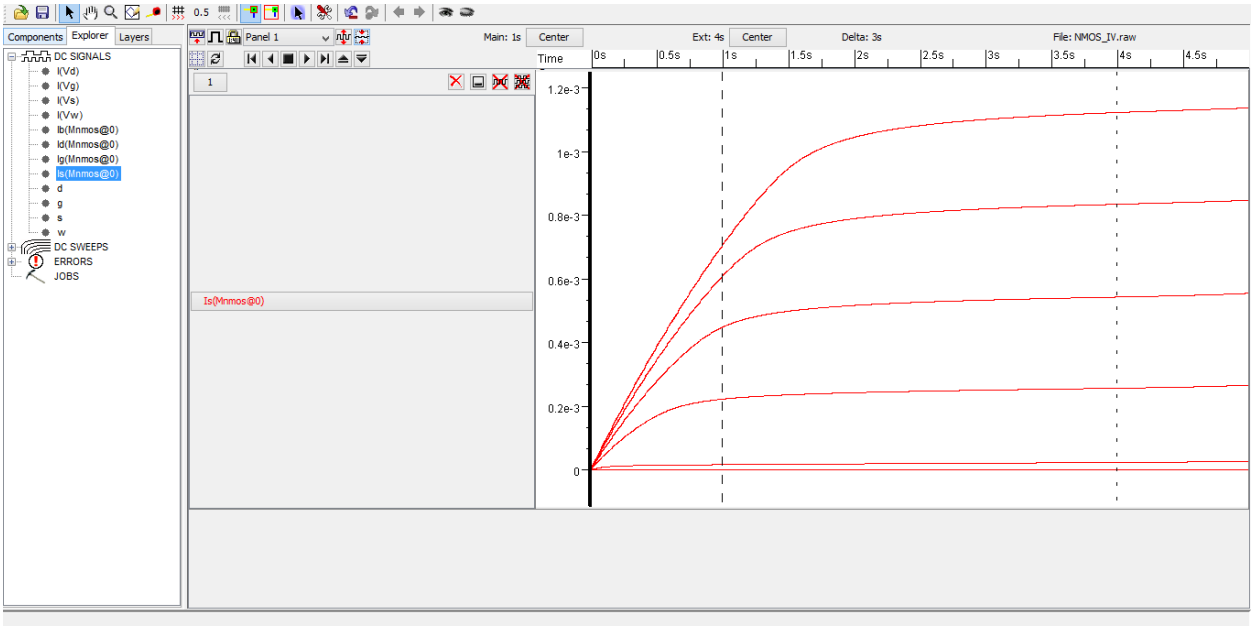


Figure 19: Electric simulation of NMOS transistor