

Hardware Report

AI1110: Probability and Random Variables
Indian Institute of Technology Hyderabad

Kudupudi D.V.Sai Aditya
AI22BTECH11013

- 1) **Components:** The following components are necessary to construct the random number generator circuit:

Component's name	Count
Breadboard	1
Seven-Segment Display	1 (Common Anode)
Decoder (7447 IC)	1
D Flip-Flop (7474 IC)	2
XOR Gate (7486 IC)	1
555 Timer IC	1
Resistors	1K Ω (20)
Resistor	1M Ω (1)
Capacitor	100nF (1)
Capacitor	10nF (1)
Jumper Wires	20

TABLE I: Components for the circuit

2) **Description of the Random Number Generator Circuit using Shift Registers::**

- Importing Required Modules: The random number generator circuit is designed to generate random numbers using shift registers, providing a versatile and reliable solution for applications that require randomness. The circuit incorporates various components, including a breadboard, seven-segment display, decoder, flip-flops, XOR gate, 555 timer IC, resistors, capacitors, and jumper wires.
- At the core of the circuit is the shift register, constructed using two D flip-flops (7474 ICs) and an XOR gate (7486 IC). The shift register operates based on the clock signal generated by the 555 timer IC. The clock signal serves as the synchronization mechanism, ensuring the precise shifting of data within the shift register.
- The clock signal generated by the 555 timer circuit is connected to the CLOCK input of the D flip-flops, enabling the sequential shifting of data through the flip-flops. This shifting action creates a cascading effect, allowing the circuit to generate a sequence of random bits.
- The output of each D flip-flop is connected to the Decoder IC (7447 IC), which converts the binary input into a corresponding output that can be displayed on the seven-segment display. The connections between the flip-flops and the decoder are carefully established to ensure the proper mapping of binary values to the display segments.

- e) The output of each D flip-flop is connected to the Decoder IC (7447 IC), which converts the binary input into a corresponding output that can be displayed on the seven-segment display. The connections between the flip-flops and the decoder are carefully established to ensure the proper mapping of binary values to the display segments.
- f) Power and ground connections are established for all components to ensure proper operation and signal integrity. The circuit requires a stable power supply, and the voltage specifications of each component should be respected to prevent damage and ensure accurate performance.
- g) The random number generator circuit offers various applications, such as simulations, gaming, cryptography, testing, art, research, and decision-making. By following the circuit diagram and carefully assembling the components, users can create a functional and reliable random number generator capable of providing high-quality random numbers for their specific needs.

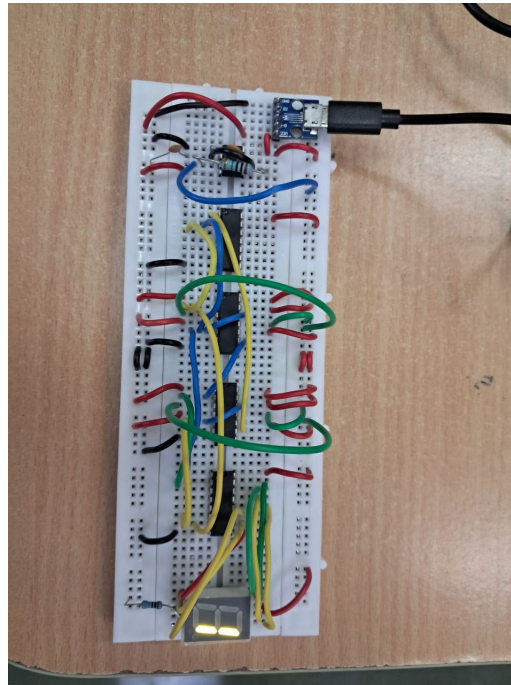


Image of hardware circuit showing random number as 1.

3) **Block Diagram:**

- a) In this block diagram, each block represents a key component of the circuit. The 555 Timer Circuit generates the CLOCK signal, which is then connected to the D Flip-Flops. The XOR Gate and the D Flip-Flops together form the Shift Registers, responsible for shifting the data through the circuit.
- b) The output of the Shift Registers is then connected to the Decoder IC, which converts the binary input into the corresponding output signals. These output signals are then sent to the Seven-Segment Display, which visually represents the generated random numbers.
- c) The Power Supply block provides the necessary power to the entire circuit, and the Ground block ensures proper grounding and signal referencing throughout the circuit.
- d) This block diagram provides an overview of the different components and their interconnections, offering a visual representation of the random number generator circuit using shift registers.

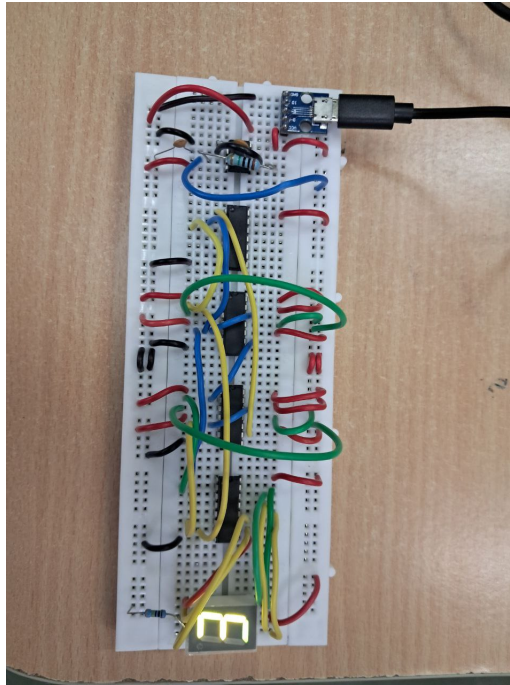
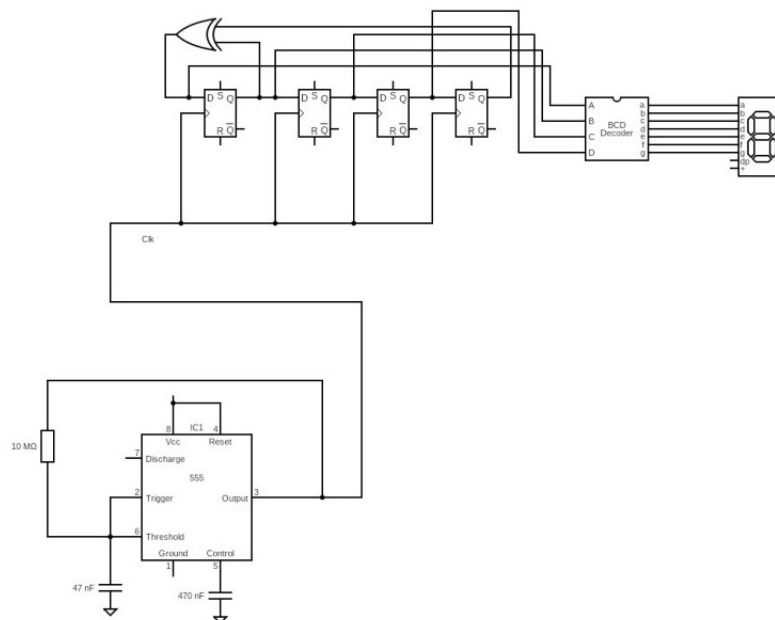


Image of hardware circuit showing random number as 3.



Block Diagram for the Circuit.