CS/BCA/SEM-2/BCA-201/09

1. .....
Signature of Invigilator

2. .....
Signature of the Officer-in-Charge

Reg. No. | | | | | | | | | | | | | | |

Roll No. of the Candidate | | | | | | | | | | | | | | |

– –

CS/BCA/SEM-2/BCA-201/09

ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE – 2009

COMPUTER ARCHITECTURE AND SYSTEM SOFTWARE (SEMESTER - 2)

Time : 3 Hours] [Full Marks : 70

INSTRUCTIONS TO THE CANDIDATES :

1. This Booklet is a Question-cum-Answer Booklet The Booklet consists of **32 pages**. The questions of this concerned subject commence from Page No. 3.
2. a) In **Group – A**, Questions are of Mul ple Choice type. You have to write the correct choice in the box provided **against each question**.
   b) For **Groups – B** & **C** you ha e to answer the questions in the space provided marked 'Answer Sheet'. Questions of **Group B** are Short answer type. Questions of **Group – C** are Long answer type. Write on both sides of the paper.
3. **Fill in your Roll No. in the box** provided as in your Admit Card before answering the questions.
4. Read the instructions given inside carefully before answering.
5. You should not forget to write the corresponding question numbers while answering.
6. Do not write your nam or put any special mark in the booklet that may disclose your identity, which will render you liable to disqualification. Any candidate found copying will be subject to Disciplinary Action under the relevant rules.
7. **Use of Mobile Phone and Programmable Calculator is totally prohibited in the examination hall.**
8. You should return the booklet to the invigilator at the end of the examination and should not take any page of this booklet with you outside the examination hall, **which will lead to disqualification**.
9. Rough work, if necessary is to be done in this booklet only and cross it through.

No additional sheets are to be used and no loose paper will be provided

FOR OFFICE USE / EVALUATION ONLY

Marks Obtained

	Group – A										Group – B			Group – C				
Question Number																	***Total Marks***	***Examiner's Signature***
Marks Obtained																		

.....
Head-Examiner/Co-Ordinator/Scrutineer

2205 (03/06)

ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE – 2009

COMPUTER ARCHITECTURE AND SYSTEM SOFTWARE

SEMESTER - 2

Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : 10 × 1 = 10

i) The instruction LOAD A is a

a) zero address instruction b) one address instruction

c) two address instruction d) three address instruction. ☐

ii) The purpose of cache memory in a computer is to

a) ensure fast booting b) reduce load on CPU registers

c) replace stati memory d) speed up memory access. ☐

iii) Object code is

a) input to assembler b) output of assembler

c) intermediate code d) none of these. ☐

iv) Which of the following is not an advantage of Dynamic RAMs ?

a) High density b) Low cost

c) High speed d) No need of memory refresh. ☐

v) DMA module can communicate with CPU through

a) interrupt b) cycle stealing

c) branch instruction d) none of these. ☐

vi) The number of fetch operation(s) to execute instruction in immediate mode is

a) 0 b) 1

c) 2 d) none of these. ☐

vii) A CPU has 16 bit program counter(PC). This means CPU can address

a) 16K b) 32K

c) 64K d) 256K memory locations. ☐

viii) The major objective in choosing page replacement policy is to

a) minimize hit ratio b) reduce size of page

c) maximize hit ratio d) none of these. ☐

ix) The sum of $(24D)_{16}$ and $(9AA)_{16}$ is

a) $(BE7)_{16}$ b) $(BE6)_{16}$

c) $(AF7)_{16}$ d) $(BE7)_{16}$. ☐

x) In a stack computer, there is support for

a) PUSH and POP instruction only

b) zero address instruction only

c) zero address instructions, PUSH and POP

d) none of these. ☐

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Distinguish between Fixed point and Floating point representations. 5

3. Distinguish between vectored and non-vectored interrupt. What is subroutine ? 4 + 1

4. What are the 16-bit registers available in 8085 Microprocessor ? Write about them. 2 + 3

5. Why is 'bootstrap loader' program stored in ROM and not in RAM ? 5

6. a) What would be happen if a computer does not have any OS installed in it ?

   b) What are the differences between static memory and dynamic memory ?

   c) What is flash memory ? 2 + 2 + 1

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Explain memory interleaving with diagram.

   b) Write short note about content addressable memory (CAM) with diagram.

   c) Discuss direct mode and indirect mode of addressing of instruction with examples. 5 + 6 + 4

8. a) What is parallel processing ?

   b) What is arithmetic pipelining ?

   c) What is vector processing ? Explain how matrix multiplication is performed using vector processing. 6 + 4 + (1 + 4)

9. Draw and explain a 4-bit arithmetic circuit which can perform the following : 15

a) Add

b) Add with carry

c) Subtract with borrow

d) Subtract

e) Transfer of *A*

f) Transfer *A*

g) Increment

h) Decrement.

10 a) What is virtual memory ? What could be th maximum size of virtual memory ? Justify.

b) Briefly explain an instruction execu ion cycle with proper timing diagram.

c) Explain the Booth algorithm Illustrate with an example.

d) Briefly discuss different types of ROM.

e) Differentiate between static RAM and dynamic RAM. 3 + 3 + 3 + 3 + 3

11. Write short notes on any *three* of the following : 3 × 5 = 15

a) Single-pass assembler

b) DMA controller

c) Interrupt handling

d) Cache memory

e) Shift micro-operations.

END

Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/BCA/SEM-2/BCA-201/2010

2010

COMPUTER ARCHITECTURE AND SYSTEM SOFTWARE

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

   i) 8085 is a ..... bit microprocessor.

   a) 8 b) 16

   c) 32 d) 64

   ii) The sum of $(10110)_2$ and $(1100)_2$ is

   a) 011011 b) 100011

   c) 001100 d) 100010.

   iii) The instruction LOAD is a

   a) zero-address instruction

   b) one-address instruction

   c) two-address instruction

   d) three-address instruction.

iv) 2's complement of 1010100 is

a) 0110011 b) 0101100

c) 1010101 d) 0010010.

v) DMA stands for

a) Data Memory Access

b) Distributed Memory Access

c) Detect Memory Access

d) none of these.

vi) ..... is an implementation technique whereby multiple instructions are overlapped during an execution.

a) Pipelining b) Hazard

c) Interrupt d) Strobe.

vii) MAR stands for

a) Memory Address Register

b) Memory Abstract Register

c) Memory Activity Register

d) none of these.

viii) The ..... register is used to store result of an instruction.

a) Program counter b) Base register

c) Flag register d) None of these.

ix) The Race condition is appeared in a clock S-R flip-flop when the values of R & S are

a) 1, 1 b) 1, 0

c) 0, 0 d) 0, 1.

x) ..... is a memory which transmits data from main memory to CPU and vice versa.

a) RAM b) Cache

c) Auxiliary d) Virtual.

GROUP – B
(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. What do you mean by memory read and write operation ? Describe using register transfer language.

3. Explain direct and indirect addressing with the help of neat sketch.

4. What is virtual memory ?

5. Write down the register transfer language for execution of
LDAX B
STAX D

6. Comment on Direct mapping function of 2048 word cache memory onto 65,536 word main memory.

GROUP – C
(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. What is virtual memory ? What could be maximum size of virtual memory ? Justify. Briefly describe an instruction execution cycle with proper timing diagram. Explain the Booth's algorithm. Illustrate with example. Briefly discuss different types of ROM. Differentiate between Static RAM and Dynamic RAM. 3 + 3 + 3 + 3 + 3

8. What are the differences between RISC and CISC processors ? Explain the concepts of sequential processing, pipelining and parallel processing with examples. What are the elements of a machine instruction ? What is meant by memory access time ?

4 + 6 + 3 + 2

9. What are 16-bit registers available in 8085 Microprocessor ? Write about them. What is 'bootstrap loader' program stored in ROM and not in RAM ? What are the elements of machine instruction ?

2 + 3 + 5 + 5

10. What is interrupt ? What is the difference between primary and secondary storage devices ? What is stack ? What is flag ? What is the disadvantage of microprocessor ? What is the difference between microprocessor and microcontroller ?

2 + 4 + 2 + 2 + 2 + 3

11. Write short notes on any *three* of the following : 3 × 5

a) Vector processing

b) Paging

c) DMA controller

d) Cache memory

e) 4 in 1 multiplexer.

Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/BCA/SEM-2/BCA-201/2011

2011

COMPUTER ARCHITECTURE AND SYSTEM SOFTWARE

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks

Candidates are required to give their answers in their own words as far as practicable.

GROUP A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : 10 × 1 = 10

   i) The program ha translates a high-level language program to binary is called

      a) compiler b) byte code

      c) operating system d) none of these.

   ii) There are two major types of control organization. They are

      a) Hardwared control and micro-programmed control

      b) Hardware and software

      c) Operating system and hardware

      d) System software and application software.

iii) The full form of MRI is

a) Memory reference instruction

b) Memory reference interpreter

c) Memory reference interrupt

d) None of these.

iv) The input symbolic program is called

a) Source program b) Object-program

c) Byte code d) None of these.

v) The data register is sometimes called

a) Pipeline register b) Buffer

c) Compiler d) Sequencer.

vi) The full form of PSW is

a) Program status word

b) Password sta us word

c) Program sta us work

d) Password status work.

vii) The full form of RISC is

a Reduced Instruction Set Computer

b) Register Instruction Set Computer

c) Reduced Instruction Set Component

d) None of these.

viii) 9's complement of 546700 is

a) 453299 b) 483270

c) 32955 d) 669290.

ix) The 2's complement of 1101100 is

a) 0010100 b) 11001100

c) 11111111 d) 11110000.

x) The full form of MAR is

a) Memory Address Register

b) Memory Address Routine

c) Memory Adder Register

d) Multiplexer Adder R gister.

GROUP – B
(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Establish the concept of three state lens buffer

3. Describe the working principle of binary incrementer.

4. What is OP code ? What is instruction code ? What is Assembler ? 1 + 2 + 2

5. What is locality of reference ? What is biased exponent ? 2 + 3

6. Discuss the memory read and memory write operations.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. Describe the rules of the language ? What do you mean by subroutine ? What is binary adder ? 9 + 3 + 3

8. What is parallel processing ? Describe the working principle of pipelining. Explain the major characteristics of an RISC processor. 2 + 10 + 3

9. Write the applications of vector processing. Explain memory interleaving. 5 + 10

10. a) Perform the subtraction with following unsigned decimal number by taking the 10's c mplement of the subtrahend.

    5250 – 1 21

    b) Perform the subtraction with the following unsigned binary number by taking the 2's complement of the subtrahend.

    11010 – 1101

    c) Explain asynchronous mode of data transfer. 5 + 5 + 5

11. Write short note on any *three* of the following : 3 × 5

    a) Memory stack

    b) Addressing modes

    c) Program interrupt

    d) Data dependency

    e) Content Addressable Memory (CAM).

Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/BCA/SEM-2/BCA-201/2012

2012

COMPUTER ARCHITECTURE AND SYSTEM SOFTWARE

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks

Candidates are required to give their answers in their own words as far as practicable.

GROUP A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

   i) Gray code for decimal 12 is

   a) 1100 b) 1011

   c 1010 d) 0100.

   ii) 9's complement of 46 is

   a) 54 b) 64

   c) 63 d) 53 .

   iii) BCD numbers express each decimal digit as

   a) Byte b) Nibble

   c) Bit d) ASCII .

iv) A microprocessor has memory locations from 0000 to 7FFF. Each location stores 1 byte. The memory capacity is

a) 8 k byte b) 16 k byte

c) 24 k byte d) 32 k byte.

v) The transfer operation P : $R_2 \leftarrow R_1$ will be executed only when

a) P = 0 b) P = 1

c) P > 0 d) P < 1

vi) The number of multiplexers required to construct a common bus for 8 registers with 4 bits each is

a) 16 b) 8

c) 4 d) 2 .

vii) A logical shift is one that t ansfers ..... through the serial input.

a) 0 b) 1

c) either 0 or 1 d) both (a) and (b).

viii) A computer instruction is a ..... code.

a) Hexadecimal b) Decimal

c) Binary d) Octal .

ix) DMA stands for

a) Digital Memory Address

b) Direct Memory Access

c) Digital Memory Array

d) Dual Memory Arithmetic.

x) The basic computer consists of ..... types of registers.

a) 6 b) 8

c) 9 d) 18 .

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Describe the working principle of binary incrementer.
3. What is meant by random access and sequential access of memory devices ? Explain.
4. Briefly describe an instruction execution cycle with proper timing diagram.
5. What is locality of ref renc ? What is biased exponent ? 2 + 3
6. What are the uses of a System Bus and Data Bus ? How do they differ from an Address Bus ? 3 + 2

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. What is virtual memory ? What could be the maximum size of virtual memory ? Justify. Briefly describe an instruction execution cycle with proper timing diagram. Explain the Booth's algorithm. Illustrate with example. Briefly discuss different types of ROM. Differentiate between Static RAM and Dynamic RAM. 3 + 3 + 3 + 3 + 3

8. What are the differences between RISC and CISC processors ? Explain the concepts of sequential processing pipelining and parallel processing with example. What are the elements of a machine instruction ? What is meant by memory access time ? 4 + 6 + 3 + 2

9. What are 16-bit registers available in 8085 microprocessor ? Write about them. What is 'bootstrap loader' program stored in ROM and not in RAM ? What are the elements of machine instruction ? 2 + 3 + 5 + 5

10. What is interrupt ? What is the difference etween primary and secondary storage devices ? What is stack ? What is flag ? What is the disadvantag of microprocessor ? What is the difference between microprocessor and the microcontroller ? 2 + 4 + 2 + 2 + 2 + 3

11. Write short notes on any *three* of the following : 3 × 5

    a) Vector Processing

    b) Pag ng

    c) DMA controller

    d) Cache memory

    e) 4 in 1 multiplexer.

Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/BCA/SEM-2/BCA-201/2013

2013

COMPUTER ARCHITECTURE AND SYSTEM SOFTWARE

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct altern tives for any *ten* of the following : $10 \times 1 = 10$

i) Gray code for decimal 12 is
   a) 1100 b) 1011
   c) 1010 d) 0100.

ii) 9's complement of 46 is
   a) 54 b) 64
   c) 63 d) 53.

iii) BCD numbers express each decimal digit as
   a) Byte b) Nibble
   c) Bit d) ASCII.

iv) A microprocessor has memory locations from 0000 to 7FFF. Each location stores 1 byte. The memory capacity is
   a) 8 k byte b) 16 k byte
   c) 24 k byte d) 32 k byte.

v) Computer registers are designated by

a) capital letters

b) both capital and small letters

c) numerals

d) small letters.

vi) The transfer operation $P : R_2 \leftarrow R_1$ will be executed only when

a) $P = 0$ b) $P = 1$

c) $P > 0$ d) $P < 1$.

vii) The number of multiplexers required to construct a common bus for 8 registers with 4 bits each is

a) 16 b) 8

c) 4 d) 2.

viii) Both Selective – complement and Clear operations are achieved by .... micro-operation.

a) OR b) AND

c) NOT d) XOR.

ix) A logical shift is one that transfers ..... through the serial input

a) 0 b) 1

c) either 0 or 1 d) both 0 and 1.

x) A computer instruction is a ..... code.

a) hexadecimal b) decimal

c) binary d) octal.

xi) DMA stands for

a) Digital Memory Address

b) Direct Memory Access

c) Digital Memory Array

d) Dual Memory Arithmetic.

xii) The basic computer consists of ..... types of registers.

a) 6 b) 8

c) 9 d) 18.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Describe the working principle of binary incrementer.
3. What is virtual memory ? What is locality of reference ? 3 + 2
4. What are the uses of a System Bus and Data Bus ? How do they differ from an Address Bus ? 3 + 2
5. Explain direct and indirect addressing with the help of neat sketch.
6. Why is 'bootstrap loader' program stored in ROM and not in RAM ?

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) What is parallel processing ?
   b) What is arithmetic pipelining ?
   c) What is vect r processing ? Explain how matrix multiplic t on is performed using vector processing.
   d) Discuss Booth's algorithm for binary multiplication using the example of multiplication of two signed numbers +13 and –11. 3 + 3 + (1 + 3) + 5
8. a) What is interrupt ?
   b) Discuss different major types of interrupts.
   c) Point out the differences and similarities between external and internal interrupts. 3 + 8 + 4
9. What are the 16-bit registers available in 8085 microprocessor ? What are the types of CPU organization ? Discuss in brief with example. 5 + 10

10. Explain asynchronous mode of data transfer. Discuss priority interrupt. 10 + 5

11. Write short notes on any *three* of the following : 3 × 5

    a) Stack organization

    b) Memory stack

    c) Addressing mode

    d) Cache memory

    e) First and Second Pass Assembler.

==========

CS/BCA(H)/Even/2nd Sem/BCA-201/2014

2014

Computer Architecture and System Software

Time Alloted : 3 Hours *Full Marks : 70*

The figure in the margin indicate full marks. Candidates are required to give their answers in their own words as far as practicable

GROUP - A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following: 10x1=10

i) The contents of a Base Register may be changed in _____ mode.

a) User b) Privileged
c) Safe d) None of the above

ii) An arithmetic left shift

a) Multiplies a signed number by 2
b) Divides a signed number by 2
c) Multiplies a signed number by 4
d) Divides a signed number by 4

iii) Number of address lines required for access of 1MB memory is

a) 17 b) 18 c) 19 d) 20

iv) A _____ is a complete CPU on a single chip.

a) Microprocessor b) Micro-controller
c) Control Unit d) ALU

v) 8086 has a total of _____ registers.

a) 10 b) 11 c) 12 d) 13

vi) ADD is a _____ address instruction.

a) Zero b)One c)Two d) Three

vii) The 8086 instruction to transfer a data to a register in immediate mode is _____.

a) MOV b) MVI
c) LOAD d) None of these

viii) _____ calculates the address of the next microinstruction to be executed.

a) Program Counter
b) Address computation circuit
c) Instruction register
d) None of these

ix) The minimum time elapsed between two read requests is called

a) Access time b) Cycle time
c) Turnaround time d) Waiting time

x) Division by zero causes an error of class

a) Trap b) Timer interrupt
c) I/O interrupt d) Hardware failure

GROUP - B

(Short Answer Type Questions)

Answer any *three* of the following. 3x5=15

2. Draw a 4 - bit Adder - subtractor circuit and explain its function. 5

3. Draw and explain the common bus system for 4 registers using 4 x 1 MUX. 5

4. What are Direct and Indirect address? Explain with example.

5

5. Make a list of registers for the basic computer, indicating the function of each register.

5

6. What is instruction cycle? What are the different phases of this cycle.

2+3

7. Write an Assembly language program to add two numbers.

5

GROUP - C

(Long Answer Type Questions)

Answer any *three* of the following. 3x15=45

8. a) What will be the content of the Program Counter after fetching 8bit/ 16bit data from a memory location 3065H. The instruction to fetch the data resides at 5132H. Assume the instruction length to be 3 bytes.

   b) Why are interrupts considered to be a useful mechanism in the context of improving the efficiency of processing?

   c) What are the steps for a simple instruction cycle? Explain Fetch Cycle and Indirect Cycle using Register Transfer Language.

2+3+(2+8)

9. Draw and explain one stage of an ALU with shift capability along with the micro-operations performed.

[15]

10. a) What do you mean by packing? Given two decimal digits 5 and 9, show the packing procedure through proper steps.

    b) What is an Instruction Set?

    c) Convert the following expression into Reverse Polish Notation

and show the evaluation procedure in the stack organized CPU:

A x B + C x (D+ E)

(2+5)+2+6

11. a) Explain the Programmed Input/Output with a flow chart. 8

b) Draw the logic diagram of a binary cell and explain its working. 8+7

12. Write short notes on any three of the following: 5x3 = 15

a) Cache Memory

b) Arithmetic Pipelining

c) Program Counter

d) RIM and SIM instructions

e) Flag Register in 8085

WEST BENGAL UNIVERSITY OF TECHNOLOGY

BCA-201

COMPUTER ARCHITECTURE AND SYSTEMS SOFTWARE

Time Allotted: 3 Hours | Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.
All symbols are of usual significance.

GROUP A
(Multiple Choice Type Questions)

1. Answer *all* questions. $10 \times 1 = 10$

(i) Gray code for decimal 12 is

(A) 1100 (B) 1011 (C) 1010 (D) 0100

(ii) 9's complement of 46 is

(A) 54 (B) 64 (C) 63 (D) 53

(iii) BCD number express each decimal digit as

(A) Byte (B) Nibble (C) Bit (D) ASCII

(iv) A microprocessor has memory locations from 0000 to 7FFF. Each location stores 1 byte. The memory capacity is

(A) 8k byte (B) 16k byte (C) 24k byte (D) 32k byte

(v) Computer registers are designated by

(A) capital letters (B) both capital and small letters
(C) numerals (D) small letters

(vi) The number of multiplexers required to construct a common bus for 8 registers with 4 bits each is

(A) 16 (B) 8 (C) 4 (D) 2

(vii) Both *Selective – complement* and *Clear* operations are achieved by _____ microoperation

(A) OR (B) AND (C) NOT (D) XOR

(viii) A logical shift is one that transfers _____ through the serial input.

(A) 0 (B) 1
(C) either 0 or 1 (D) both 0 and 1

(ix) A computer instruction is a _____ code.

(A) Hexadecimal (B) Decimal (C) Binary (D) Octal

(x) DMA stands for

(A) Digital Memory Address (B) Direct Memory Access
(C) Digital Memory array (D) Dual Memory Arithmetic

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. 3×5 = 15

2. Distinguish between vectored and non-vectored interrupt. What is subroutine? 3+2

3. Convert the hexadecimal number A0B9 into decimal, binary and octal. 5

4. What is OP code? What is instruction code? What is assembler? 2+2+1

5. What is Instruction cycle? What are the different phases of this cycle. 2+3

6. Write an Assembly language program to add two numbers. 5

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

7. (a) What is DMA? Briefly explain with suitable diagram, the DMA operation in association with CPU. (2+6)+3+4

   (b) What is speed up, throughput of a pipelined architecture?
   A hierarchical cache – main memory subsystem has the following speculations (i) cache access time of 60nsec. (ii) Main memory Access time of 600nsec. (iii) 80% of memory request are for read. (iv) Hit ratio of 0.9 for read access and the write – through scheme is used.
   Calculate average access time of the memory system considering only read cycle.

8. (a) Perform the subtraction of the following unsigned decimal number by taking the 10's complement of the subtrahend: 7452 – 1243 5

   (b) Perform the subtraction of the following unsigned binary number by taking the 2's complement of the subtrahend 11010 – 1101 5

   (c) Explain asynchronous mode of data transfer. 5

9. (a) What do you mean by "addressing mode"? 2

   (b) How many addressing modes are found in 8085 microprocessor? What are those modes? 5

   (c) Briefly describe with example the "memory – direct – addressing mode". 2

   (d) What is a stack? What are the operations that can be performed on a stack? 2

(e) Write an Assembly – Language – Program to add n numbers where the numbers are stored in n consecutive locations (NUM, NUM + 1 ..... NUM + n – 1) and to store the result in memory location SUM. The number 'n' is stored in memory location N. 4

10.(a) Draw the basic organization of a Hardwired Control Unit. 3

(b) Write the Register Transfer Language of the execution of ADD M instruction. 6

(c) Draw the basic organization of a micro programmed Control Unit. 3

(d) What is a microinstruction and a micro program? 3

11.(a) Design a Half-Adder Circuit. 3

(b) Design a 1-bit Full Adder using two Half-Adders. 2

(c) Draw the Circuit diagram of an 8-bit normal Full Adder. If the delay to produce C_{i+1} from C_i is 10ns and S_i from A_i, B_i and C_i is 15 ns, what is the addition time? 5

(d) How Carry Look Ahead technique improves the delay? 5

MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : BCA-201

COMPUTER ARCHITECTURE & SYSTEMS SOFTWARE

Time Allotted : 3 Hours | *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

   i) The 8085 instruction to transfer a data to a register in immediate mode is

   a) MOV b) MVI

   c) LOAD d) none of these.

   ii) Memory address which refers to the successive memory words and the machine is called as

   a) Word addressable

   b) Bit addressable

   c) Byte addressable

   d) Terra byte addressable.

iii) What is true for a typical RISC architecture ?

a) Micro-programmed control unit

b) Instruction takes multiple clock cycles

c) Have few registers in CPU

d) Emphasis on optimizing instruction pipelines.

iv) The full form of PSW is

a) program status word

b) password status word

c) program status work

d) password status work.

v) In a virtual system, the addresses used by the programmer belong to

a) Memory space

b) Physical addresses

c) Address space

d) Main memory address.

vi) DMA stands for

a) Digital Memory Address

b) Direct Memory Access

c) Digital memory Array

d) Dual Memory Arithmetic.

vii) The transfer operation $P : R_2 \leftarrow R_1$ will be executed only when

a) $P = 1$ b) $P = 0$

c) P is 0 or 1 d) None of these.

viii) The method updating the main memory as soon as a word is removed from the cache is called

a) write-through b) write-back

c) protected write d) cache-write.

ix) Stack overflow causes

a) Hardware interrupt

b) External interrupt

c) Internal interrupt

d) Software interrupt.

x) Data hazards occur when

a) Greater performance loss

b) Pipeline changes the order of read/write access to operands

c) Some functional unit is not fully pipelined

d) Machine size a limited.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. What is instruction cycle ? Compare and contrast hardwired *vs* micro-programmed control unit. 2 + 3

3. What do you mean by memory read and write operation ? Describe using register reference language. 3 + 2

4. Calculate the speed-up of a *k*-stage pipeline system processing *n* tasks.

5. a) What do you mean by "Micro-operation" ?
   b) What are the different types of micro-operations ? 2 + 3

6. Write an Assembly level program to add two single byte numbers.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) With the help of a neat diagram show the structure of a typical arithmetic pipeline performing $(A^*B + C)$. 7
   b) What do you mean by Hazard ? State various types of hazards in brief. 1 + 7

8. a) What are cache misses ? Write down the techniques to minimize the cache misses. 2 + 6

b) A hierarchical main memory sub-system has the following specifications :

Cache access time : 50 ns

Main memory access time : 500 ns

80% of memory required for read

Hit ratio : 0·9 for read access and write through scheme is used.

(i) Calculate the average access time of the memory system considering only memory read cycle. 3

(ii) Calculate the average access time of memory system both for read and write cycle. 4

9. a) A computer has 512 kB cache memory and 2MB main memory. If the block size is 64 bytes then find subfield for

   (i) associative memory

   (ii) direct mapping

   (iii) set-associative mapping. 10

   b) How does cache memory increase the speed of processing ? Explain. 5

10. a) Explain different types of addressing modes. 5

   b) What are the advantages of Relative addressing mode over Direct addressing mode ? 5

   c) Differentiate between Vectored and Non-vectored interrupts. 5

11. a) Write a program to evaluate the arithmetic statement : 4×2

   $X = (A + B)/(C + D)$

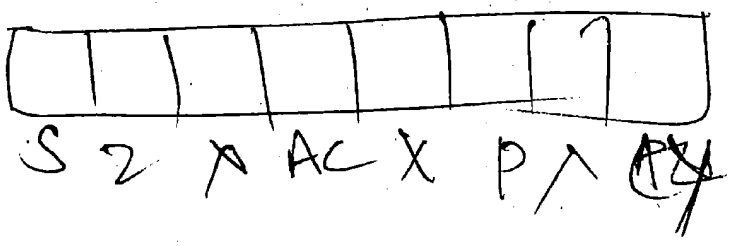
   i) Using a stack organized computer with zero address operation instruction.

ii) Using an accumulator type computer with one address instruction.

iii) Using general register computer with two address instruction.

iv) Using general register computer with three address instruction.

b) Write the features of 8085 micro-processor. Discuss Flag Register in 8085. 4 + 3



MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : BCA-201

COMPUTER ARCHITECTURE & SYSTEM SOFTWARE

Time Allotted: 3 Hours | *Full Marks*: 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following: 1×10=10

(i) An exception condition in a computer system caused by an event external to the CPU is known as
- (a) Halt
- (b) Process
- (c) Interrupt
- (d) None of these

(ii) Cache memory is implemented using
- (a) Dynamic RAM
- (b) EEPROM
- (c) EPROM
- (d) ROM

(iii) The major objective in choosing page replacement policy is to
- (a) minimize hit ratio
- (b) reduce page size
- (c) maximize hit ratio
- (d) None of these

(iv) Whenever CPU detects an interrupt, what it do with current state?
- (a) Save it
- (b) Discard it
- (c) Depends system to system
- (d) First finish it

(v) The purpose of cache memory in a computer is to
- (a) ensure fast booting
- (b) reduce load on CPU registers
- (c) replace static memory
- (d) speed-up memory access

(vi) Where the result of an arithmetic and logical operation are stored?
(a) In Accumulator (b) In Cache Memory
(c) In ROM (d) In Instruction Registry

(vii) 8085 has a total of _____ registers.
(a) 10 (b) 11
(c) 12 (d) None of these

(viii) The minimum time elapsed, between two read requests is
(a) Access time (b) Cycle time
(c) Turnaround time (d) Waiting time

(ix) The CPU activates the _____ output to inform the external DMA that the buses are in the high-impedance state.
(a) bus request (b) bus grant
(c) cycle stealing (d) None of these

(x) Which of the following bus is bi-directional?
(a) Address bus (b) Data bus
(c) Control bus (d) Address-Data bus

Group – B

(Short Answer Type Questions)

Answer *any three* questions. 5×3=15

2. Explain the Von-Neumann architecture with diagram.
3. How the bus signal $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$ and $\overline{IOW}$ are generated from 8085 microprocessor?
4. What are the uses of a System bus and Data bus? How do they differ from an Address bus?
5. Explain the role of program counter, stack pointer and address register.
6. Differentiate between direct addressing and indirect addressing with the help of a diagram.

Group – C

(Long Answer Type Questions)

Answer *any three* questions. 15×3=45

7. (a) What are Hit ratio and Miss ratio in a memory system? 2
(b) What do you mean by speed up ratio of a pipelining system? Explain with an example for 'k' segment pipeline. 3+5=8
(c) Write a program to add two 8 bit number in assembly language. 5

8. What are the differences between RISC and CISC processors? Explain the concepts of sequential processing pipelining and parallel processing with example. What are the elements of a machine instruction? What is meant by memory access time? 4+6+3+2=15

9. (a) What is an instruction cycle? Draw the flowchart of an instruction cycle and explain with the help of timing diagram. 2+5=7

   (b) Change the following expression into Reverse Polish notation using stack implementation: 4

   $Y = A * [B + (C * D)]/(E * F)$ Ans. $CD * B + A * EF */$

   (c) Explain briefly the different types of Addressing mode. 4

10. Draw and explain a 4 bit arithmetic circuit which can perform the following: 15

   (a) Add

   (b) Add with carry

   (c) Subtract with borrow

   (d) Subtract

   (e) Transfer of A (Accumulator)

   (f) Transfer A (Accumulator)

   (g) Increment

   (h) Decrement

11. Write short notes of the following (*any three*): 5×3=15

   (a) DMA controller

   (b) Vector Processing

   (c) RISC and CISC

   (d) Virtual memory

   (e) Common bus system

MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : BCAN-201(N)

COMPUTER ARCHITECTURE

Time Allotted : 3 Hours | *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) The 8085 instruction to transfer a data to a register in immediate mode is

   a) MOV b) MVI

   c) LOAD d) None of these.

   ii) A multiplexer is also known as a/an

   a) Encoder b) Data selector

   c) Decoder d) Register.

   iii) 9's complement of 546700 is

   a) 483270 b) 453299

   c) 32955 d) 669290.

iv) The number of multiplexer required to construct a common bus for 8 registers with 16 bits each is

a) 8 b) 16

c) 4 d) 2.

v) The components that form a multiprocessor system is/are

a) CPU's b) Memory Unit

c) IOps d) All of these.

vi) CISC stands for

a) Clock Instruction Set Computer

b) Complex Instruction Set Computer

c) Control Instruction Set Computer

d) None of these.

vii) PC points to the

a) Address of present instruction

b) Address of next instruction

c) Address of previous instruction

d) Topmost element of stack.

viii) ROR is a

a) Program control instruction

b) Shift instruction

c) Logical instruction

d) Data transfer instruction.

ix) DMA stands for

a) Digital Memory Address

b) Direct Memory Access

c) Digital Memory Array

d) Dual Memory Arithmetic.

x) A processor performing fetching and decoding of different instruction during the execution of another instruction is
   a) Cache
   b) Parallel Processing
   c) Pipelining
   d) All of these.

xi) In case of, Zero-address instruction method the operands are stored in
   a) Register
   b) Stack
   c) Both (a) and (b)
   d) Push down and stack.

xii) Physical memory is divided into set of finite size
   a) Frame
   b) Pages
   c) Block
   d) Vector.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Write an assembly language program to add two numbers.

3. Briefly describe an instruction execution cycle with proper timing diagram.

4. What are the different hazards ? Explain How do we avoid them ?

5. What is locality of reference in cache memory ? What are the differences between L1 cache and L2 cache ? 2 + 3

6. What is bootstrap loader ? Explain its functionality. 2 + 3

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. How many addressing modes are found in 8085 microprocessor ? What are they ? What do you know about SIM and RIM instructions ? How many types of data transfer schemes are there ? Describe any one among them. 5 + 5 + 2 + 3

8. What is parallel processing ? What is arithmetic pipelining ? What is vector processing ? Explain how matrix multiplication is performed using vector processing. Discuss Booth's algorithm for multiplication using the example of multiplication of two signed numbers + 13 and – 11. 3 + 3 + 1 + 3 + 5

9. a) Perform $X = (A + B / C) \times (D \times E - F)$
   Using the following addressing mode :
   i) Two Address
   ii) One Address
   iii) Zero Address.
   b) Explain Sub routine call with example.
   c) Compare direct and set associative mapping technique. 6 + 4 + 5

10. Write short notes on any *three* of the following : 3 × 5
    a) CAM
    b) Virtual Memory
    c) Register stack and memory stack
    d) Asynchronous data transfer.
    e) Memory Interleaving.

11. a) Draw the flowchart of Booth's multiplication algorithm.
    b) Explain your algorithm for – 7*3.
    c) Differentiate between paging and segmentation. 5 + 5 + 5