WEST BENGAL UNIVERSITY OF TECHNOLOGY

BCA-201

COMPUTER ARCHITECTURE AND SYSTEMS SOFTWARE

Time Allotted: 3 Hours | Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.
All symbols are of usual significance.

GROUP A
(Multiple Choice Type Questions)

1. Answer *all* questions. 10×1 = 10

(i) Gray code for decimal 12 is

(A) 1100 (B) 1011 (C) 1010 (D) 0100

(ii) 9's complement of 46 is

(A) 54 (B) 64 (C) 63 (D) 53

(iii) BCD number express each decimal digit as

(A) Byte (B) Nibble (C) Bit (D) ASCII

(iv) A microprocessor has memory locations from 0000 to 7FFF. Each location stores 1 byte. The memory capacity is

(A) 8k byte (B) 16k byte (C) 24k byte (D) 32k byte

(v) Computer registers are designated by

(A) capital letters (B) both capital and small letters
(C) numerals (D) small letters

(vi) The number of multiplexers required to construct a common bus for 8 registers with 4 bits each is

(A) 16 (B) 8 (C) 4 (D) 2

(vii) Both *Selective – complement* and *Clear* operations are achieved by _____ microoperation

(A) OR (B) AND (C) NOT (D) XOR

(viii) A logical shift is one that transfers _____ through the serial input.

(A) 0 (B) 1
(C) either 0 or 1 (D) both 0 and 1

(ix) A computer instruction is a _____ code.

(A) Hexadecimal (B) Decimal (C) Binary (D) Octal

(x) DMA stands for

(A) Digital Memory Address (B) Direct Memory Access
(C) Digital Memory array (D) Dual Memory Arithmetic

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. 3×5 = 15

2. Distinguish between vectored and non-vectored interrupt. What is subroutine? 3+2

3. Convert the hexadecimal number A0B9 into decimal, binary and octal. 5

4. What is OP code? What is instruction code? What is assembler? 2+2+1

5. What is Instruction cycle? What are the different phases of this cycle. 2+3

6. Write an Assembly language program to add two numbers. 5

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

7. (a) What is DMA? Briefly explain with suitable diagram, the DMA operation in association with CPU. (2+6)+3+4

   (b) What is speed up, throughput of a pipelined architecture?
   A hierarchical cache – main memory subsystem has the following speculations (i) cache access time of 60nsec. (ii) Main memory Access time of 600nsec. (iii) 80% of memory request are for read. (iv) Hit ratio of 0.9 for read access and the write – through scheme is used.
   Calculate average access time of the memory system considering only read cycle.

8. (a) Perform the subtraction of the following unsigned decimal number by taking the 10's complement of the subtrahend: 7452 – 1243 5

   (b) Perform the subtraction of the following unsigned binary number by taking the 2's complement of the subtrahend 11010 – 1101 5

   (c) Explain asynchronous mode of data transfer. 5

9. (a) What do you mean by "addressing mode"? 2

   (b) How many addressing modes are found in 8085 microprocessor? What are those modes? 5

   (c) Briefly describe with example the "memory – direct – addressing mode". 2

   (d) What is a stack? What are the operations that can be performed on a stack? 2

(e) Write an Assembly – Language – Program to add n numbers where the numbers are stored in n consecutive locations (NUM, NUM + 1 ..... NUM + n – 1) and to store the result in memory location SUM. The number 'n' is stored in memory location N. 4

10.(a) Draw the basic organization of a Hardwired Control Unit. 3

(b) Write the Register Transfer Language of the execution of ADD M instruction. 6

(c) Draw the basic organization of a micro programmed Control Unit. 3

(d) What is a microinstruction and a micro program? 3

11.(a) Design a Half-Adder Circuit. 3

(b) Design a 1-bit Full Adder using two Half-Adders. 2

(c) Draw the Circuit diagram of an 8-bit normal Full Adder. If the delay to produce C_{i+1} from C_i is 10ns and S_i from A_i, B_i and C_i is 15 ns, what is the addition time? 5

(d) How Carry Look Ahead technique improves the delay? 5