ENGINEERING & MANAGEMENT EXAMINATIONS, DECEMBER – 2008
DIGITAL ELECTRONICS
SEMESTER – 1

Time : 3 Hours]   [Full Marks : 70

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) $(1100 \cdot 1011)_2 = (?)_{10}$

        a) $10 \cdot 6785$ b) $11 \cdot 6578$

        c) $12 \cdot 6875$ d) $13 \cdot 6785$.

   ii)   2's complement of 10101100 is

        a)   11001010   b)   01010011

        c)   01010100   d)   01011001.

   iii) $(247 \cdot 36)_8 = (?)_{16}$

        a) $A7 \cdot 78$ b) $1A7 \cdot 36$

        c) $B7 \cdot 87$ d) $1B7 \cdot 36$.

   iv)   MBR, in reference to memory management is

        a)   Memory Broad Register   b)   Memory Buffer Relay

        c)   Memory Buffer Register   d)   None of these.

   v)   Output of NAND gate is 1, if and only if

        a)   all inputs are 1   b)   any input is 1

        c)   all inputs are 0   d)   any input is 0.

vi) $A + \overline{A} = ?$

a)   1   b)   0

c)   A   d) $\overline{A}$.

vii) If the no. of states of a counter is 8, then the no. of flip-flops is

a)   8   b)   3

c)   4   d)   6.

viii) $(A.B + \overline{A}.B + \overline{A}.\overline{B})$ is equal to

a) $A + \overline{B}$ b) $\overline{A} + B$

c) $A + B$ d)   1.

ix)   Karnaugh Map is used to

a)   simplify Boolean function

b)   design Boolean function

c)   evaluate Boolean function

d)   none of these.

x)   A multiplexer has

a)   single input   b)   multiple output

c)   no output   d)   single output.

xi)   Output of R-S (NAND) flip-flop, for R = 1 & S = 1 is

a)   set   b)   reset

c)   race   d)   no change.

xii) Subtracting 1111 from 11000 will result to

a)   1000   b)   1100

c)   1001   d)   1011.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Apply K-map to obtain the minimal form for the function :

   $F (A, B, C, D) = \Sigma (0, 4, 5, 7, 8, 9, 13, 15)$

   $d (A, B, C, D) = \Sigma (1, 2, 6, 10)$

3. Draw a half-adder circuit and describe its operations.

4. Design a 4-bit up-down counter.

5. Prove the following logical equation using Boolean algebra :

   $(A+BC) . (B+ A \overline{C}) = BC + A \overline{C}$

6. i)   Subtract $(7489)_{10} - (2485)_{10}$ using 10's complement method.

   ii) What is a Multiplexer ? Why is it called "Data selector" ?

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following questions. $3 \times 15 = 45$

7. a)   Represent the decimal number "27" in

   i)   BCD code

   ii)   Octal code

   iii) Gray code.

   b)   Draw the block diagram of a digital multiplexer and explain its function.

   c)   Give the functional truth table of a 4 : 1 multiplexer and realize it using basic gates AND, OR and NOT.

   d)   Implement the expression using a multiplexer :

   $f (A, B, C, D) = \Sigma m (0, 2, 3, 6, 8, 9, 12, 14)$ $3 + 4 + 4 + 4$

8. a) What do you mean by a sequential circuit ?

    b) What are synchronous & asynchronous sequential circuits ?

    c) Explain the functionality of D-flip-flop. Give the truth table, State diagram.

    d) What do you mean by Edge-triggering & Level-triggering in flip-flops ?

                                                        2 + 3 + 5 + 5

9. a) What is a flip-flop ?

    b) What are the uses of flip-flops ?

    c) Give the circuit diagram of a J-K flip-flop.

    d) Give the truth tables of S-R & J-K flip-flops.   2 + 3 + 4 + 6

10. a) Given the following truth table :

Inputs			Outputs	
x	y	z	F1	F2
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

    i)   Obtain the simplified functions in sum of products.

    ii) Obtain the simplified functions in product of sums.

    b) Design a BCD to Exess-3 Code converter.   8 + 7

11. a) Explain different types of RAM and ROM.

    b) Write short notes on any *two* of the following :
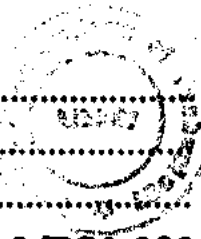
        i)   Parity checker

        ii)   Ring counter

        iii) Magnitude comparator.   7 + (2 × 4)

END

CS/BCA/SEM-1/BCA-101/2009-10

2009

DIGITAL ELECTRONICS

Time Allotted : 3 Hours   Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following :

$$10 \times 1 = 10$$

i) A 3-bit synchronous counter uses flip-flops with propagation delay time of 20 ns each. The maximum possible time required for change of state will be

   a)   60 ns   b)   40 ns

   c)   20 ns   d)   none of these.

ii) BCD sutraction is performed by using which complement representation ?

   a)   1's   b)   2's

   c)   10's   d)   9's.

iii) The SOP form of logical expression is most suitable for designing logic circuits using only

   a)   XOR gates   b)   NOR gates

   c)   NAND gates   d)   OR gates.

11006   **[Turn over**

iv) The dual of a Boolean function is obtained by

   a) interchanging all 0s and 1s only

   b) changing 0s to 1s only

   c) changing 1s to 0s only

   d) interchanging all 0s and 1s and '+' and ',' signs.

v) When representing in the following code the consecutive decimal numbers differ only in one bit

   a) Excess-3   b) Gray

   c) BCD   d) Hexadecimal.

vi) In a $J - K$ flip-flop when $J = 1$ and $K = 1$ and clock = 1 the output will be

   a) toggle

   b) 1

   c) 0

   d) recalls previous output.

vii) $(AB + A'B + A'B)$ is equal to

   a) $A + B'$ b) $A' + B$

   c) $A + B$ d) 1.

viii) 2's complement of 1010101 is

   a) 0101011   b) 10101010

   c) 1100000   d) 1000001.

ix) The basic fuse technologies used in PROM are

   a) metal links   b) silicon links

   c) p-n junctions   d) all of these.

x) In general, a boolean expression of $(n + 1)$ variable can be implemented using a multiplexer with

   a) 2^{n+1} inputs   b) 2^{n-1} inputs

   c) 2^n inputs   d) None of these.

GROUP – B
(Short Answer Type Questions)
Answer any *three* of the following. $3 \times 5 = 15$

2. Draw the neat diagram of 3-bits Bi-directional Shift Register using mode control (M). When M is logic zero then left shift and right shift for M is logic one.

3. Design 2-bit Gray-Binary converter using basic logic gates with proper truth table.

4. Draw the logic diagram and truth table of J - K f/f. Why is J - K F/F much more versatile that S - R F/F ?

5. What is a full subtractor ? Explain its basic structure with proper logic diagrams & truth tables. $1 + 4$

6. Realize the funciton $f (A, B, C) = \Sigma m (1, 3, 5, 6)$ by a multiplexer. Discuss the operation logic.

GROUP – C
(Long Answer Type Questions)
Answer any *three* of the following. $3 \times 15 = 45$

7. a) Using K-map method minimize the following expression :

   $F (w, x, y, z) = m \Sigma (1, 5, 6, 12, 13, 14) + d \Sigma (2, 4).$

   8

   b) Implement Ex-OR gate using NAND Gate and NAND gate using NOR gate. $3\frac{1}{2} + 3\frac{1}{2}$

8. a) Design and implement Mod-6 synchronous counter considering lock out problem. Is the counter self-starting ? $8 + 1$

   b) Explain the difference between Ring and Johnson Counter with proper state diagram and circuit diagram.

   6

9. a) Explain the concept of parity checking.

   b) Discuss about the design of an odd parity generator.

   c) What is biased exponent in relation to Floating Point Representation (FPR) ?

   d) Represent (– 1101011) in Floating Point Representation (FPR) for a 32-bit CPU.   3 + 4 + 3 + 5

10. What do you mean by race condition in flip-flop ? Design a j - k flip-flop and discuss its operation. Design and explain the functioning of the 4-bit adder-subtractor circuit.

   3 + 5 + 7

11. Write short notes on any *three* of the following :   3 × 5

   a) Universal gates

   b) Decoder

   c) Shift Register

   d) Flip-flop excitation table

   e) Ripple counter.

CS/BCA/SEM-1/BCA-101/2010-11

2010-11

DIGITAL ELECTRONICS

Time Allotted : 3 Hours   *Full Marks :* 70

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Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :   10 × 1 = 10

   i) In which of the following base systems is 789 not a valid number ?

       a) Base 5

       b) Base 16

       c) Base 8

       d) Base 3.

   ii) Storage of 1 kB means the what number of bytes ?

       a) 1000   b) 964

       c) 1024   d) 1064.

1004   [Turn over

iii) Pick out the correct statement :

    a) In a positional number system, each symbol represents the same value irrespective of its position

    b) The highest symbol in a position number system is a value equal to the number of symbols in the system

    c) It is not always possible to find the exact binary

    d) Each hexadecimal digit can be represented as a sequence of three binary symbols.

iv) The binary code of $(21.125)_{10}$ is

    a) 10101.001   b) 10100.001

    c) 10101.010   d) 10100.111

v) Race condition is avoided by

    a) J-K flip-flop   b) S-R flip-flop

    c) master-slave flip-flop   d) none of these.

vi) Which one is sequential circuit ?

    a) multiplexer   b) decoder

    c) priority encoder   d) counter.

vii) Which is correct ?

    a) $A + \overline{A} B = A + B$ b) $A + 1 = A$

    c) $A + \overline{A} = A$ d) $\overline{A} / A = A$

viii) Decimal digits can be converted to binary code using

    a) Decoder   b) Encoder

    c) Mux   d) DeMux.

ix) Carry of a full adder is a

    a) dual function

    b) self dual function

    c) non-symmetric function

    d) none of these.

x) Every flip-flop is defined by

    a) characteristic equation

    b) excitation table

    c) both of these

    d) none of these.

xi) Immediate Access Storage Device is the name of

    a) primary memory   b) secondary memory

    c) hard disk   d) pen drive.

xii) Control unit does not process data.

    a) False   b) True

    c) Unpredictable   d) None of these.

xiii) If there are three inputs then the number of input combinations will be

    a) four   b) eight

    c) six   d) two.

xiv) Excess-3 Code representation of decimal 59 is

    a) 01100110   b) 10001100

    c) 01011001   d) 11000110.

xv) Hexadecimal equivalent of $(26.25)_{10}$ is

    a) A6.4   b) 1A.4

    c) FA.4   d) 1A.25

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Implement XOR operation using four 2-input NAND gates. Verify the output for different combinations of inputs.

3. Write down the BCD code of $(9612)_{10}$. Add two numbers $(6952)_{10}$ and $(1589)_{10}$ using BCD codes and obtain the result also in BCD.

4. a) Find out the dual and the complement of the following Boolean function :

   $$F = ABC + \overline{A}\,\overline{B}C + \overline{A}BC + AB\overline{C}$$

   b) Simplify the following Boolean expression
   $$(X + Y)\left(\overline{X} + Y + Z\right)\left(\overline{X} + Y + \overline{Z}\right)$$

   to minimum number of literals using algebraic method.

5. a) Prove that the multiplexer is a universal logic module.

   b) Use 4-to-1 MUX and other necessary logic gate to design a full-subtractor.

6. a) What is the advantage of JK flip-flop over SR flip-flop ?

   b) Write the Maxterm form of the following function :

   $$F = XY + \overline{X}Z$$

GROUP – C

### (Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7.   a)   Draw the truth table for a three input adder. Explain clearly the meaning of the input and the output symbols in the truth table. Write the Boolean expressions for the sum and carry.   5

   b)   Use a Karnaugh map to find the minimum sum of products for the expression $X = A'B'C + AB'C + A'BC + ABC'$ 5

   c)   Simplify the following expressions using Boolean algebra :   5

   i) $AB + A(B + C) + B(B + C)$

   ii) $A'BC + B'CD + AC + A'B'CD'$

8.   a)   State the main differences between sequential and combinational circuits.   2

   b)   Draw the truth table and logic circuit of a Full Subtractor. Using Karnaugh map find out the expression for difference (D) and borrow (B).   4 + 3

   c)   Implement the Boolean function $F = (A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15)$ using 8×1 multiplexer with A, B and D connected to select lines s_2, s_1, s_0 respectively.   6

9. a) Define flip-flop and its propagation delay. 4

 b) Using the logic diagram convert a J-K flip-flop to a *D* flip-flop and *T* flip-flop. 5

 c) Design a J-K master-slave flip-flop with circuit diagram and give the truth table. 6

10. a) What is the usefulness of excitation table of the flip-flop ? 3

 b) The 4-bit shift register is initialised to 001. After how many clock pulses is the register re-initialied to same value ? 6
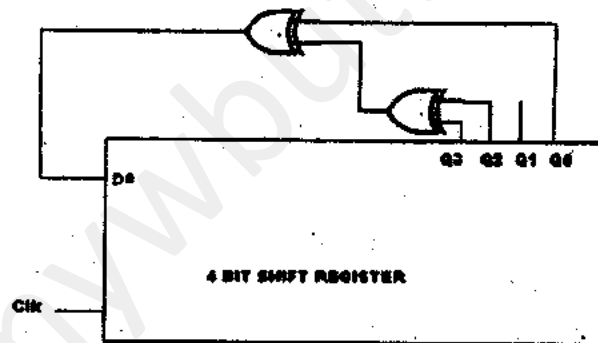
 c) Determine the modulus of the following counter. 6
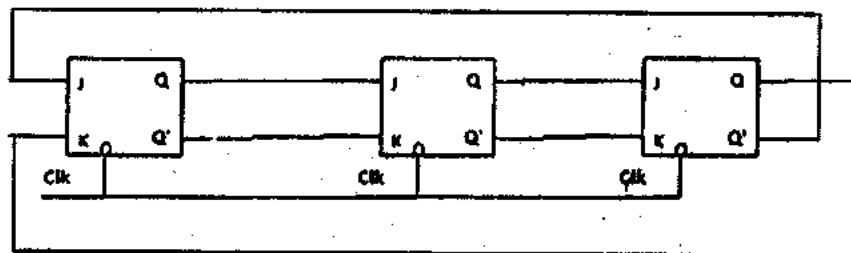
11. Write short notes on any *three* of the following :   3 × 5

   a)   Decoder

   b)   Shift register

   c)   PROM

   d)   Priority Checker

   e)   Ring counter.

Name : ……………………………………………………………

Roll No. : …………………………………………………………

Invigilator's Signature : ………………………………………

CS/BCA/SEM-1/BCA-101/2011-12

2011

DIGITAL ELECTRONICS

Time Allotted : 3 Hours   Full Marks : 70

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Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1.   Choose the correct alternatives for any *ten* of the following :

$10 \times 1 = 10$

i)   ($A + A' B + B'$) is equal to

   a)   A   b) B'

   c)   1   d)   0.

ii)   (10110) is equivalent to

   a)   20   b)   22

   c)   24   d)   18.

iii)   A BCD counter is an example of

   a)   a decade counter

   b)   a full modules counter

   c)   both (a) and (b)

   d)   none of these.

iv) The output of a gate is LOW if and only if all its inputs are HIGH. It is true for

a) AND b) XNOR

c) NOR d) NAND.

v) De-Morgan's law states that

a) $(A + B)' = A' \cdot B'$ b) $(A + B)' = A' + B'$

c) $(A \cdot B)' = A' \cdot B'$ d) both (a) and (c).

vi) The complement of a variable is always

a) 0

b) 1

c) equal to the variable

d) the inverse of the variable.

vii) 2's complement of '101011' is

a) 010100 b) 010011

c) 101001 d) 010101.

viii) What is the ASCII code of 'A' ?

a) 98 b) 0100

c) 1100 d) none of these.

ix) 4-bit register can store

a) a bit at a time b) a byte at a time

c) a nibble at a time d) none of these.

x) In toggle state of JK Flip-Flop

a) present output is opposite of previous output

b) present output is same as previous output

c) both (a) and (b)

d) none of these.

xi) Full adder can add

    a)   two binary numbers   b)   three binary numbers

    c)   four binary numbers   d)   none of these.

xii) MOD - 10 counter can count up to

    a)   9   b)   10

    c)   8   d)   none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following.   3 × 5 = 15

2.   State and prove De-Morgan's theorems.

3.   Express the Boolean function $F = AB + \bar{A}C$ in a product of maxterm form.

4.   Define multiplexer. Why is it called "Data Selector" ?   3 + 2

5.   Use 4 : 1 MUX and other necessary logic gates to design a full adder.

6.   What is flip-flop ? What is meant by race condition ?   1 + 4

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following.   3 × 15 = 45

7.   a)   Using K-map method, simplify the following Boolean function and obtain minimal SOP expression :

    $Y = \sum m\ (\ 0,\ 2,\ 3,\ 6,\ 7\ ) + \sum d\ (\ 8,\ 10,\ 11,\ 15\ )$.

    b)   Implement the Boolean Function $F = (\ A,\ B,\ C,\ D\ ) = \sum m\ (\ 0,\ 1,\ 3,\ 8,\ 9,\ 15\ )$ using two 4 - to-1 multiplexer and one OR gate.

    c)   Design a gray code to binary converter circuit of 5 bits. What is nibble ?   5 + 5 + (4 + 1)

8. a) Design a half adder circuit using minimum number of 2-input NOR gates only. Write Down the truth table and Boolean functions also.

    b) Convert a *D* flip-flop to a J-K flip-flop. You can use additional circuiting if required.

    c) What is full subtractor ? Explain its basic structure with proper logic diagrams and truth tables.   5 + 5 + 5

9. a) Convert the following :
        i) $(AC15)_{16}$ $= (?)_{10}$
        ii) $(1011001)_2$ $= (?)_{10}$

    b) Discuss about the design of an odd parity generator.

    c) Explain the concept of parity checking.

    d) What is the advantage of J-K flip-flop over SR flip-flop.

    5 + 5 + 2 + 3

10. a) What is the difference between sequential and combinational circuit ?

    b) Describe the propagation delay of a flip-flop.

    c) Express the Boolean function
        $F = AB + A^{/} C$ in a product of maxterm form.   5 + 5 + 5

11. a) Draw a block diagram and write truth table of a *D* flip-flop.

    b) Compare asynchronous and synchronous counter.

    c) Use 4 to 1 MUX and other necessary logic gate to design a full adder.   5 + 5 + 5

12. Write short notes on any *three* of the following :   3 × 5

    a) EPROM

    b) *D* flip-flop

    c) Ripple counter

    d) Encoder

    e) 4-bit parallel Adder.

CS/BCA/SEM-1/BCA-101/2012-13

2012
DIGITAL ELECTRONICS

Time Allotted : 3 Hours   *Full Marks* : 70

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as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives of the following :

                                                        $10 \times 1 = 10$

i)   The Boolean equation of AND operation is

   a) $Y = \overline{A}$ b) $Y = AB$

   c) $Y = A + B$ d)   None of these.

ii) The logical expression $Y = A + \overline{A}B$ is equivalent to

   a) $Y = AB$ b) $Y = \overline{A}B$

   c) $Y = A + \overline{B}$ d) $Y = A + B$.

iii) The BCD equivalent of 57 is

   a)   111001   b)   01010111

   c)   101111   d)   10001010.

iv) In the BCD code, the decimal number 123 is written as

   a)   11011   b)   C3

   c)   001010011   d)   000100100011.

v) A carry look-ahead adder is frequently used for addition, because it

    a) is faster   b) is more accurate

    c) uses fewer gates   d) costs less.

vi) A combinational circuit is one in which the output depends on the

    a) input combination at a time

    b) previous output and input combination

    c) previous input and input combination at a time

    d) present output and previous output.

vii) Each individual term in standard SOP form is called as

    a) Maxterm   b) Minterm

    c) Midterm   d) None of these.

viii) A decoder with 64 output lines has _____ data inputs.

    a) 64   b) 1

    c) 6   d) None of these.

ix) The number of flip-flops required to build a Mod-15 counter is

    a) 4   b) 5

    c) 6   d) 7.

x) The full form of CCD is

    a) Charged-couple disk   b) Charge-coupled device

    c) Cache coupled device   d) None of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Draw a full adder circuit as combination of 2 half adders.

3. State Demorgan's law and prove it for 2 variables.

4. a) Evaluate $(7352)_{10} - (9456)_{10}$ using 9's compliment.

    b) State Duality principle.

5. Minimize the following Boolean expression using K-map.

   $F(A,B,C,D) = \sum(0,1,3,6,8,10,11,13,15)$

6. Design a 4 bit parallel-in parallel-out (PIPO) shift register.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Represent the decimal number 45 in

    i)   Hexadecimal code

    ii) Gray code

    iii) BCD code.

    b) Which gates are called universal gates and why ?

    c) Design a 2×4 decoder. Give truth table and draw circuit diagram using basic gates.

    d) Implement the expression using a Multiplexer.

    $F(A,B,C,D) = \sum (0,1,4,5,7,9,11,13,15)$ $3 + 5 + 4 + 3$

8. a) What is combinational circuit ?

    b) Differentiate between combinational and sequential circuit.

    c) Explain the functionality of clocked JK flip-flop. Give truth table and diagram.

    d) Convert SR to JK flip-flop.   2 + 3 + 5 + 5

9. a) What is register ?

    b) Design a decimal to binary encoder.

    c) What do you mean by Johnson counter ?   3 + 6 + 6

10. a) Given the following truth table.

X	Y	Z	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Obtain the SOP and POS form and draw the circuit diagram.

    b) Express the following Boolean expressions :

    i) $f = AB + A'C$ in POS form.

    ii) $f = (A + BC)(B + C'A)$ in SOP form.   8 + 7

11. a) What is the difference between synchronous and asynchronous counter ?

    b) Write short notes on the following :

    i)   EPROM

    ii) DRAM.

    c) What is the difference between SRAM and DRAM ?

                                                       4 + 6 + 5

CS/BCA/SEM-1/BCA-101/2013-14

2013
DIGITAL ELECTRONICS

Time Allotted : 3 Hours   *Full Marks* : 70

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GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

    i)   Excess-3 code representation of decimal 984 is

        a)   1011 1010 1101   b)   1100 1011 0111

        c)   1110 1001 1010   d)   1101 1111 0111

    ii)   Hexadecimal equivalent of $(1586)_{10}$ is

        a) $(362)_{16}$ b) $(623)_{16}$

        c) $(632)_{16}$ d) $(263)_{16}$.

    iii)   2's compliment of 1010111 is

        a)   0101001   b)   0110110

        c)   0101100   d)   0101101.

iv) A function of three variables

$F(A, B, C) = \Sigma(1, 3, 5, 6)$ is given by

   a) an 8-to-1 multiplexer

   b) two 4-to-1 multiplexer

   c) one 4-to-1 multipexer

   d) none of these.

v) Multiplexer is also known as

   a) Data selector   b) Data distributor

   c) Multiplexer   d) Encoder.

vi) Parallel Binary Adders are

   a) combinational logic circuit

   b) sequential logic circuit

   c) both (a) and (b)

   d) none of these.

vii) A Half Adder adds .... bits.

   a) 16   b) 10

   c) 8   d) 2.

viii) Control Unit does not process data.

   a) true   b) false

   c) unpredictable   d) none of these.

ix) $(ABC + A\overline{B}C + AB\overline{C})$ is equal to

   a) $A(B + C)$ b) $\overline{A}(B+C)$

   c) $A(B+\overline{C})$ d) $A(\overline{B}+C)$

x) Race Condition is avoided by

   a) J-K flip-flop   b) Master-Slave flip-flop

   c) D flip-flop   d) S-R flip-flop.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Draw the logic symbol, Boolean expression and truth table of NOR and NAND gates. $1 + 2 + 2$

3. State and prove De Morgan's theorem in Boolean algebra.

$2 + 3$

4. Represent the decimal number '27' in

   a) Binary code

   b) BCD code

   c) Octal code

   d) Hexadecimal code

   e) Gray code. $1 + 1 + 1 + 1 + 1$

5. Prove the following logical equation using Boolean algebra :
   $(A+BC).(B+A\overline{C}) = BC + A\overline{C}$

6. Realize the EX-OR logic operation using either NAND gate or NOR gate.

7. Discuss the function of *T*-type flip-flop with the help of graphic symbol and characteristic table. $3 + 2$

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

8. a) Write down the truth table and logic symbol of a 3-input OR gate.

   b) Using NOR gates, design Full Adder and describe with diagram.

   c) Explain Universal Gate.

   d) Express the function $Y = A + \overline{B}C$ in a canonical SOP form.

   $2 + 5 + 5 + 3$

9. a) Using *K*-map method simplify the following Boolean function and obtain minimal SOP expression :
$Y = \sum_m (0,2,3,6,7) + \sum_d (8,10,11,15)$.

b) Implement the Boolean function $F = (A, B, C, D) = \sum_m (0, 1, 3, 8, 9, 15)$ using two 4-to-1 multiplexer and one OR gate.

c) Describe the application of Data Distributor.

d) What is Decoder ?   6 + 6 + 2 + 1

10. a) Explain the concept of parity checking.

b) Write down the 4-bit gray code in the ascending order of its decimal value.

c) Design a synchronous Mod-12 down-counter using J-K flip-flops.   5 + 5 + 5

11. a) Design and implement Mod-6 synchronous counter considering lock-out problem. Is the counter self-starting ?

b) Using the logic diagram convert a J-K flip-flop to a *D* flip-flop and *T* flip-flop.

c) Explain the difference between Ring and Johnson counter with proper state and a circuit diagram.

       7 + 5 + 3

12. a) What do you mean by race condition in flip-flop ?

b) Design a Master-Slave flip-flop and discuss its operation.

c) Design and explain 4 bit Parallel Adder/Subtractor.

       3 + 5 + 7

BCA-101

DIGITAL ELECTRONICS

Time Allotted: 3 Hours   Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP A
(Multiple Choice Type Questions)

1. Answer any *ten* questions. $10 \times 1 = 10$

(i) The 10's complement of 03250 is

(A) 03251   (B) 96749
(C) 96750   (D) 32140

(ii) (AB+BC+CA+1) is equal to

(A) 0   (B) 1
(C) A+B+C   (D) ABC

(iii) The addition of 3 bits is done by

(A) half adder   (B) full adder
(C) half subtractor   (D) full subtractor

(iv) (A.A').(A+B+C+D) is

(A) 1   (B) 0
(C) A   (D) A+B+C+D

(v) A decoder is a combinational circuit that converts binary information from n input lines to a maximum of

(A) 2n   (B) 2+n
(C) 2^n (D) n output lines

1057   1   [Turn over]

(vi) In a J-K flip flop when J = 1 and K = 1 and clock = 1 the output will be

(A) toggle   (B) 1

(C) 0   (D) recalls previous output

(vii) $(AB + A'B + A'B')$ is equal to

(A) $A + B'$ (B) $A' + B$

(C) $A + B$ (D) 1

(viii) A BCD counter is a

(A) decade counter   (B) a full modules counter

(C) both (A) and (B)   (D) none of these

(ix) $X + XY = X$. The given expression follows

(A) De Morgan's Law   (B) Associative law

(C) Distributive law   (D) Absorption law

(x) The output of a sequential circuit depends on

(A) present input only   (B) past input only

(C) both present and past inputs   (D) present output only

(xi) Subtracting 1111 from 11000 will result to

(A) 1000   (B) 1100

(C) 1001   (D) 1011

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. $3\times5 = 15$

2. What is flip flop? Draw a block diagram and state the excitation and characteristics table of D flip flop   5

3. (a) $(AC15)_{16} = (?)_{10}$ 2.5

     (b) $(1011001)_2 = (?)_{10}$ 2.5

4. Draw the truth table and logic circuit of a full–Subtractor. Using Karnaugh map find out the expression for difference (d) and borrow (B).   5

5. (a) Design a J- K master slave Flip–Flop with circuit diagram and give the truth table.   3

     (b) Define Flip-Flop and its propagation delay.   2

6. (a) Prove that the multiplexer is a universal logic module.   2

     (b) Use 4–to–1 MUX and other necessary logic gate to design a Full–Subtractor.   3

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. $3\times15 = 45$

7. (a) Briefly discuss the function of a full adder.   3

     (b) Make a truth table for a full adder.   3

     (c) Simplify the outputs of a full adder using K–map.   5

     (d) Realize the simplified logic equations using NAND gate.   4

8. (a) What is Multiplexer? Why is it called " Data selector"?   3

     (b) Draw the block diagram of a digital multiplexer and explain the function.   4

(c) Draw the functional truth table of a 4:1 multiplexer and realize it using basic gates (AND, OR, and NOT).   4

(d) Implement the expression using a multiplexer
$f(A,B,C,D) = \sum m(0,2,3,6,8,9,12,14)$ 4

9. (a) Design a 4-bit up down counter.   5

(b) Design a Ring Counter   5

(c) Design a Mod 3 Counter   5

10.(a) What do you mean race condition in flip-flop?   3

(b). Design a Master-Slave Flip-flop and discuss its operation.   5

(c) Design and explain 4 bit Parallel Adder/Subtractor   7

11.   Write short notes on any *three* of the following: 3×5

(a) Ripple Counter
(b) Encoder
(c) Demultiplexer
(d) Flip-Flop excitation table
(e) Priority checker

MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : BCA-101

DIGITAL ELECTRONICS

Time Allotted : 3 Hours   *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1.   Choose the correct alternatives for the following :

$10 \times 1 = 10$

i)   The Boolean equation of AND operation is

a) $Y = \overline{A}$ b) $Y = AB$

c) $Y = A + B$ d)   None of these.

ii)   The logical expression $Y = A + AB$ is equivalent to

a) $Y = A$ b) $Y = AB$

c) $Y = \overline{AB}$ d) $Y = A + B$.

iii)   The BCD equivalent of 57 is

a)   111001   b)   01010111

c)   101111   d)   10001010.

10008   [Turn over

iv) In the BCD code, the decimal number 123 is written as

a) 11011   b) C3

c) 001010011   d) 000100100011.

v) A carry look-ahead adder is frequently used for addition, because it

a) is faster   b) is more accurate

c) uses fewer gates   d) costs less.

vi) A combinational circuit is one in which the output depends on the

a) input combination at a time

b) previous output and input combination

c) previous input and input combination at a time

d) present output and previous output.

vii) Each individual term in standard SOP form is called as

a) Max-term   b) Min-term

c) Mid-term   d) None of these.

viii) A decoder with 64 output lines has .... data inputs.

a) 64   b) 1

c) 6   d) none of these.

ix) The number of flip-flops required to build a Mod-15 counter is

a) 4   b) 5

c) 6   d) 7.

x) The race around condition will be avoided by

   a) J-K flip-flop

   b) S-R flip-flop

   c) Master-Slave flip-flop

   d) None of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following.   3 × 5 = 15

2. Draw a full adder circuit as combination of 2 half adders.

3. State De Morgan's law and prove it for 2 variables.

4. a) Evaluate $(7352)_{10} - (9456)_{10}$ using 9's complement.

   b) State Duality principle.

5. Minimize the following Boolean expression using K-map.

$F(A, B, C, D) = \sum(0, 1, 3, 6, 8, 10, 11, 13, 15)$.

6. Design a 4-bit parallel-in parallel-out (PIPO) shift register.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following.   3 × 15 = 45

7. a) Represent the decimal number 45 in

   (i) Hexadecimal code

   (ii) Gray code

   (iii) BCD code.

   b) Which gates are called universal gates and why ?

   c) Design a 2 × 4 decoder. Giver truth table and draw circuit diagram using basic gates.

    d) Implement the expression using a Multiplexer.

       $F(A, B, C, D) = \sum(0, 1, 4, 5, 7, 9, 11, 13, 15)$.

$$3 + 5 + 4 + 3$$

8. a) What is combinational circuit ?

   b) Differentiate between combinational and sequential circuits.

   c) Explain the functionality of clocked JK flip-flop. Give truth table and diagram.

   d) Convert SR to JK flip-flop.   2 + 3 + 5 + 5

9. a) What is register ?

   b) Design an decimal to binary encoder.

   c) What do you mean by Johnson counter ?

10. What do you mean by race around condition in flip-flop ? Design a J-K flip-flop and discuss its operation. Design and explain the functioning of BCD adder circuit.   5 + 5 + 5

11. Write short notes on any *three* of the following :   3 × 5

   a) Universal Gate

   b) Multiplexer

   c) PAL and PLA

   d) Excitation Table

   e) Full adder using Half-adder.

MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : BCAN-101

DIGITAL ELECTRONICS

Time Allotted: 3 Hours   *Full Marks*: 70

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as far as practicable.

Group – A

(Multiple Choice Type Questions)

1. Choose the correct alternative for *any ten* of the following: 1×10=10

    (i)   In a multiplexer, the output depends on its

        (a) Data inputs   ·   (b) Select inputs

        (c) Select outputs   (d) None of these

    (ii) Which of the following condition is not allowed in SR flip-flop?

        (a) $S=0\ R=0$ (b) $S=0\ R=1$

        (c) $S=1\ R=0$ (d) $S=1\ R=1$

    (iii) The logical expression $Y=A+AB+AB'C+A'\ BC'\ D+1$ is equivalent to

        (a) $A + C'$ (b) 1

        (c) A' (d) A

    (iv) A flip-flop has _____.

        (a) one stable state   (b) no stable states

        (c) two stable states   (d) None of these

8481   **Turn Over**

(v) The dual of a Boolean expression is obtained by

    (a) interchanging all 0s and 1s

    (b) interchanging all 0s and 1s, all + and '.' signs

    (c) interchanging all 0s and 1s, all + and '.' signs and complementing all the variables

    (d) interchanging all + and '.' signs and complementing all the variables

(vi) $A + A'B$ is equal to

    (a) $A + B$ (b) A

    (c) B   (d) $A' + B$

(vii) $11101 \div 1100$ is equal to

    (a) 10.1101   (b) 100.1101

    (c) 10.01101   (d) None of these

(viii) In general, a sequential logic circuit consists of

    (a) only flip-flops   (b) only gates

    (c) flip-flops and combinational logic circuits   (d) only combinational logic circuits

(ix) Race condition arises in

    (a) S-R Latch   (b) S-R F/F

    (c) J-K F/F   (d) T F/F

(x) When two n bit binary numbers are added, the sum will contain at most

    (a) n bits   (b) $n + 1$ bits

    (c) $n+2$ bits   (d) $n + n$ bits

(xi) While performing BCD addition, if the value of each 4-bit group becomes _____ we add 6 with that group.

    (a) greater than 9   (b) greater or equal to 9

    (c) greater than 6

Group – B
(Short Answer Type Questions)
Answer *any three* of the following.   5×3=15

2. Difference between Synchronous and Asynchronous counters.

3. Simplify the expressions:

    (i) $A = XYZ + XY'Z + X\square\,'$

    (ii) $B = P + P'Q + P'Q'R + P'Q'R'S$ 2+3=5

4. Subtract (–33) from (–57) using 2's complement method.

Convert $(4536)_{10}$ to

    (i) 2421 code

    (ii) 5421 code

    3+2=5

5. Draw the truth table and logic circuit of a full-subtractor. Using K-map find out the expression for difference (D) and borrow (B).
5

1+4=5

6. What is flip-flop? What is race condition?

Group – C
(Long Answer Type Questions)
Answer any three of the following.
15×3=45

7. (a) Using K-map method minimize the following expression:

$F(w, x, y, x) = m\Sigma(1,5,6,12,13,14) + d\Sigma(2,4)$.

Implement the logic circuit using NAND gates only.

    (b) Implement Ex-OR gate using NAND Gate and NAND gate using NOR gate.   (5+4)+(3+3)=15

8. (a) Define excitation table of flip-flop and propagation delay.

    (b) Using the logic diagram convert a J-K flip-flop D flip-flop and T flip-flop.

    (c) Design a J-K master-slave flip-flop with circuit diagram and give the truth table.   5+5+5=15

9. (a) Write down the simplified Boolean expression in

        (i) sum of product form and

        (ii) product of sum form for

    Y(A,B,C,D)=I1M(0,1,3,5,6,7,9,10,11,12,13,15)

    (b) Implement a full adder using 2 half adders.   (4+4)+7=15

10. (a) Design a carry look ahead adder.

    (b) Design a combinational logic circuit to implement 4-bit odd parity checker.   9+6=15

5×3=15

11. Write short notes on any three of the following:

    (i) PIPO

    (ii) Ripple Counter

    (iii) 4-bit parallel adder

    (iv) Gray Code

    (v) Master slave J-K flip-flop

3

CS/BCAN/Odd/SEM-1/BCAN-101(New)/2018-19

MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : BCAN-101

DIGITAL ELECTRONICS

Time Allotted: 3 Hours

Full Marks: 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words
as far as practicable.

Group – A

(Multiple Choice Type Questions)

1. Choose the correct alternative for *any ten* of the following: 1×10=10

   (i) In a multiplexer, the output depends on its

      (a) Data inputs   (b) Select inputs

      (c) Select outputs   (d) None of these

   (ii) Which of the following condition is not allowed in SR flip-flop?

      (a) $S=0\ R=0$ (b) $S=0\ R=1$

      (c) $S=1\ R=0$ (d) $S=1\ R=1$

   (iii) The logical expression $Y=A+AB+AB'C+A'BC'D+1$ is equivalent to

      (a) $A + C'$ (b) 1

      (c) A' (d) A

   (iv) A flip-flop has _____ .

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      (c) two stable states   (d) None of these

8481

Turn Over

(v) The dual of a Boolean expression is obtained by

    (a) interchanging all 0s and 1s

    (b) interchanging all 0s and 1s, all + and '.' signs

    (c) interchanging all 0s and 1s, all + and '.' signs and complementing all the variables

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(vi) $A + A'B$ is equal to

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    (a) 10.1101   (b) 100.1101

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    (a) n bits   (b) $n + 1$ bits

    (c) $n+2$ bits   (d) $n + n$ bits

(xi) While performing BCD addition, if the value of each 4-bit group becomes _____ we add 6 with that group.

    (a) greater than 9   (b) greater or equal to 9

    (c) greater than 6

Group – B

(Short Answer Type Questions)

Answer *any three* of the following.   5×3=15

2. Difference between Synchronous and Asynchronous counters.

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CS/BCAN/Odd/SEM-1/BCAN-101(New)/2018-19

4. Subtract (–33) from (–57) using 2's complement method.

Convert $(4536)_{10}$ to

   (i) 2421 code

   (ii) 5421 code   3+2=5

5. Draw the truth table and logic circuit of a full-subtractor. Using K-map find out the expression for difference (D) and borrow (B).   5

6. What is flip-flop? What is race condition?   1+4=5

Group – C
(Long Answer Type Questions)
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    Implement the logic circuit using NAND gates only.

  (b) Implement Ex-OR gate using NAND Gate and NAND gate using NOR gate.   (5+4)+(3+3)=15

8. (a) Define excitation table of flip-flop and propagation delay.

  (b) Using the logic diagram convert a J-K flip-flop D flip-flop and T flip-flop.

  (c) Design a J-K master-slave flip flop with circuit diagram and give the truth table.   5+5+5=15

9. (a) Write down the simplified Boolean expression in

    (i) sum of product form and

    (ii) product of sum form for

    $Y(A,B,C,D) = \Pi M(0,1,3,5,6,7,9,10,11,12,13,15)$

  (b) Implement a full adder using 2 half adders.   (4+4)+7=15

10. (a) Design a carry look ahead adder.   http://www.makaut.com

  (b) Design a combinational logic circuit to implement 4-bit odd parity checker.   9+6=15

11. Write short notes on *any three* of the following: 5×3=15

   (i) PIPO

   (ii) Ripple Counter

   (iii) 4-bit parallel adder

   (iv) Gray Code

   (v) Master slave J-K flip-flop