Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/BCA/SEM-1/BCA-101/2013-14

2013
DIGITAL ELECTRONICS

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

i) Excess-3 code representation of decimal 984 is

a) 1011 1010 1101 b) 1100 1011 0111

c) 1110 1001 1010 d) 1101 1111 0111

ii) Hexadecimal equivalent of $(1586)_{10}$ is

a) $(362)_{16}$ b) $(623)_{16}$

c) $(632)_{16}$ d) $(263)_{16}$.

iii) 2's compliment of 1010111 is

a) 0101001 b) 0110110

c) 0101100 d) 0101101.

iv) A function of three variables
$F(A, B, C) = \Sigma(1, 3, 5, 6)$ is given by
a) an 8-to-1 multiplexer
b) two 4-to-1 multiplexer
c) one 4-to-1 multipexer
d) none of these.

v) Multiplexer is also known as
a) Data selector b) Data distributor
c) Multiplexer d) Encoder.

vi) Parallel Binary Adders are
a) combinational logic circuit
b) sequential logic circuit
c) both (a) and (b)
d) none of these.

vii) A Half Adder adds ..... bits.
a) 16 b) 10
c) 8 d) 2.

viii) Control Unit does not process data.
a) true b) false
c) unpredictable d) none of these.

ix) $(ABC + A\overline{B}C + AB\overline{C})$ is equal to
a) $A(B + C)$ b) $\overline{A}(B+C)$
c) $A(B+\overline{C})$ d) $A(\overline{B}+C)$

x) Race Condition is avoided by
a) J-K flip-flop b) Master-Slave flip-flop
c) D flip-flop d) S-R flip-flop.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Draw the logic symbol, Boolean expression and truth table of NOR and NAND gates. 1 + 2 + 2
3. State and prove De Morgan's theorem in Boolean algebra. 2 + 3
4. Represent the decimal number '27' in
   a) Binary code
   b) BCD code
   c) Octal code
   d) Hexadecimal code
   e) Gray code. 1 + 1 + 1 + 1 + 1
5. Prove the following logical equation using Boolean algebra :
   $(A+BC).(B+A\overline{C}) = BC+A\overline{C}$
6. Realize the EX-OR logic operation using either NAND gate or NOR gate.
7. Discuss the function of *T*-type flip-flop with the help of graphic symbol and characteristic table. 3 + 2

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

8. a) Write down the truth table and logic symbol of a 3-input OR gate.
   b) Using NOR gates, design Full Adder and describe with diagram.
   c) Explain Universal Gate.
   d) Express the function $Y = A+\overline{B}C$ in a canonical SOP form. 2 + 5 + 5 + 3

9. a) Using *K*-map method simplify the following Boolean function and obtain minimal SOP expression : $Y = \sum_m (0,2,3,6,7) + \sum_d (8,10,11,15)$.

   b) Implement the Boolean function $F = (A,B,C,D) = \sum_m (0, 1, 3, 8, 9, 15)$ using two 4-to-1 multiplexer and one OR gate.

   c) Describe the application of Data Distributor.

   d) What is Decoder ? 6 + 6 + 2 + 1

10. a) Explain the concept of parity checking.

    b) Write down the 4-bit gray code in the ascending order of its decimal value.

    c) Design a synchronous Mod-12 down-counter using J-K flip-flops. 5 + 5 + 5

11. a) Design and implement Mod-6 synchronous counter considering lock-out problem. Is the counter self-starting ?

    b) Using the logic diagram convert a J-K flip-flop to a *D* flip-flop and *T* flip-flop.

    c) Explain the difference between Ring and Johnson counter with proper state and a circuit diagram. 7 + 5 + 3

12. a) What do you mean by race condition in flip-flop ?

    b) Design a Master-Slave flip-flop and discuss its operation.

    c) Design and explain 4 bit Parallel Adder/Subtractor. 3 + 5 + 7