//post lab

//RA2111004010177

```
Module postlab177 (input A,B,C,D,E, output Y);

Wire wl,w2,w3,winot, w2not, w3not;

Switchnor gl (wl,D,E);

Switchnot nl (wl,wlnot);

Switchnand g2 (w2,A,wlnot);

Switchnot n2 (w2,w2not);

Switchnand g3 (w3,B,C);

Switchnot n3 (w3,w3not);

Switchnor g4 (Y,w3not, w2not);

Endmodule
```

//Test bench

```
Module postlab_177_tb_v;

// Inputs

Reg A;

Reg B;

Reg C;

Reg D;

Reg E;

Wire Y;

// Instantiate the Unit Under Test (UUT)

Postlab007 uut (.A (A),.B(B),.C (C),.D(D),.E€,.Y (Y));

Initial begin

A = 0; B=0;C=0;D=0; E=0; #100;

A=0; B=0;C=0;D=0;E=1; #100;

A=1;B=0;C=1;D=0;E = 1; #100;

A=1;B=1; C = 1; D = 1; E = 1; #100;

End

Endmodule
```