POST LAB

```verilog
module postlab (Output, Data, RD, WR, Address,clk,rst);

output reg [7:0] Output;

input [7:0] Data;

input [5:0] Address;

input RD, WR, clk, rst;

reg [7:0] memory [63:0];

always @(posedge clk) begin

if (rst) Output=8'b00000000; else if (WR) memory [Address]=Data; else

if (RD) Output=memory [Address];

end

endmodule
```

TEST BENCH

```verilog
module postlab_tb_177_v;

reg [7:0] Data;

reg RD; reg WR;

reg [5:0] Address;

reg clk;

reg rst;

wire [7:0] Output;

postlab uut (.Output (Output), .Data (Data),.RD(RD),.WR(WR),.Address
(Address),.clk(clk),.rst(rst));

initial begin Data=8'b10000000; RD=0;

WR=1; Address=6'b111111;clk=1;

rst=1;#100;RD=1;WR=0;Address=6'b111111;#100;

end always #50 clk=~clk;
```

endmodule