# EXPERIMENT-3

# MULTISTAGE CE AMPLIFIER

**AIM**: To design a Multi stage CE amplifier with following specifications and to study the frequency response of amplifier, calculate voltage gain and bandwidth from the response.

## OBJECTIVES:

1. Design a common emitter amplifier for given specifications.
2. Simulate the designed amplifier.
3. Develop the hardware for designed amplifier.
4. Compare simulated results with practical results.

## APPARATUS:

| S.No. | Name of the Component/ Equipment | Specifications | Quantity |
|---|---|---|---|
| 1 | Transistor (BC-107) | Icmax=100mA<br>PD=300mw<br>Vceo=45V<br>Vbeo=50V | 1 |
| 2 | Capacitors (designed values) | Electrolytic type,<br>Voltage rating=<br>1.6V | 3 |
| 3 | Resistors (designed values) | Power Rating =0.5 W<br>Carbon type | 4 |
| 4 | Function Generator | (0 -1) MHZ | 1 |
| 5 | Cathode Ray Oscilloscope | 20 MHZ | 1 |
| 6 | Regulated Power Supply | (0-30) V,1Amp | 1 |

## THEORY:

Common Emitter amplifier has the emitter terminal as the common terminal between input and output terminals. The emitter base junction is forward biased and collector base junction is reverse biased, so that transistor remains in active region throughout the operation. When a sinusoidal AC signal is applied at input terminals of circuit during positive half cycle the forward bias of base emitter junction VBE is increased resulting in an increase in IB , the collector current Ic is increased by β times the increase in IB, VCE is correspondingly decreased. i.e output voltage gets decreased. Thus in a CE amplifier a positive going signal is converted into a negative going output signal i.e.180o phase shift is introduced between output and input signal and it is an amplified version of input signal.

## DESIGN SPECIFICATION:

DESIGN SPECIFICATIONS: VCC= 12V, IC= 2.5mA (2-3 mA), VCE= 6V (half of max supply), AV= 150,hfe = 150, hie = 9KΩ, Silicon NPN Transistor

## PRE REQUISITIES:

Gain of CE amplifier can be calculated:

GAIN=pull up resistance/ pull down resistance

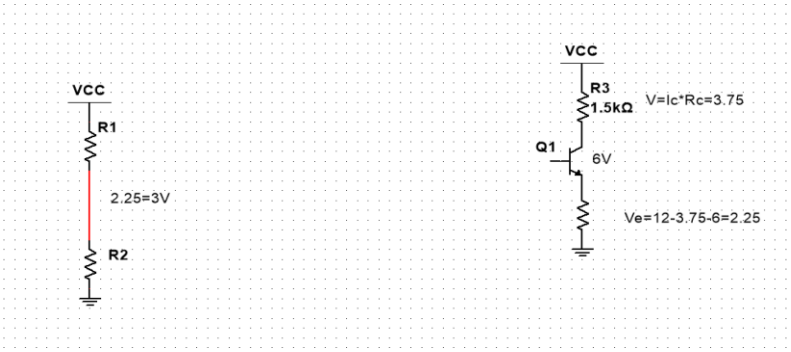
= 1.5K/10

=150-→equation 1

### DESIGN OF CE AMPLIFIER WITH GAIN=150:

## Calculation of $R_C$:

- $I_C$ =2.5mA=$I_E$
- $R_e=V_t/I_E$=26mV/2.5mA=10Ω
- $R_C=150*R_e=150*10$=1.5kΩ----------from eq(1)



## Calculation of $R_E$ :

- $Re=V_E/I_E=2.25/2.5mA=1K\Omega$

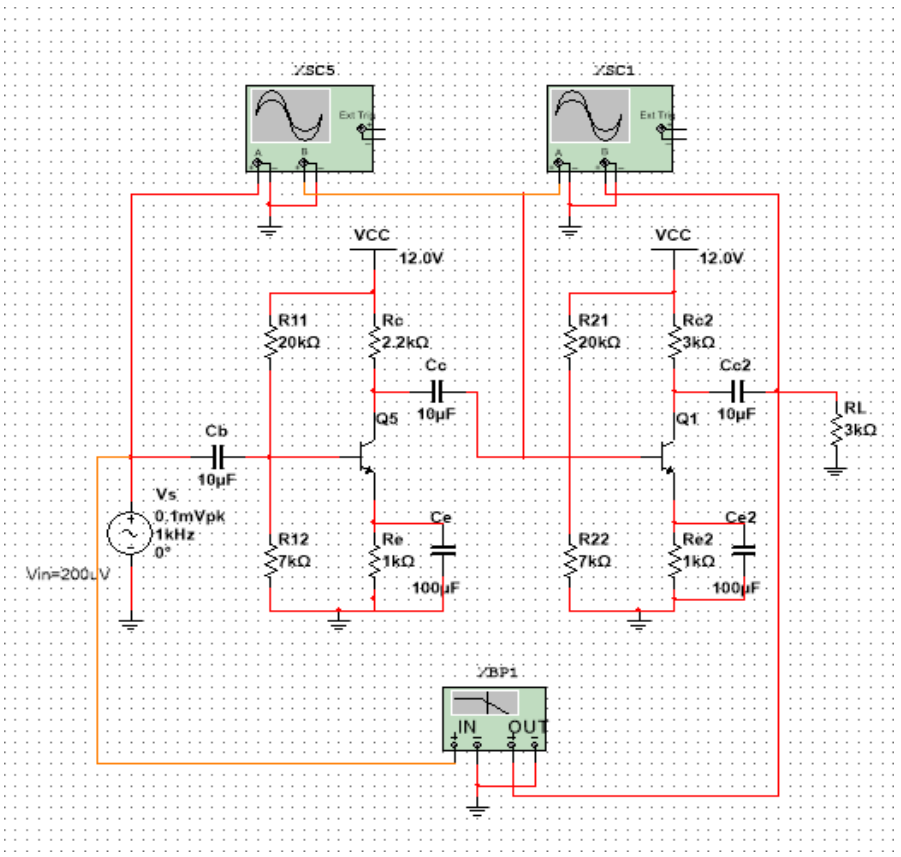
## Calculation of $R_1$ and $R_2$ :

- From voltage analysis:
- R1 ||R2 network should generate 3V from 12V
- $V_{CC}$ *R2/(R1+R2) =3V
- 12*R2/(R1+R2) =3V
- R1=3R2 ---------- eq(2)
  from current analysis:
- Current through base branch should be minimum current
- So $R2<<R_{inb}$
- $R2<<B(R_E)=100(1K\Omega)$
- R2<10(1 KΩ)=7 KΩ
  Chosen the value around 7 KΩ----- eq(3)
  From eq(2), eq(3) R1=21 KΩ
  R2<10(1 KΩ).

## Procedure:

1. Switch ON the computer and open the multisim software
2. Observe Design tool box, Instrumentation tool box, component tool box and its component functionality
3. From above tool boxes,
   Connect the circuit using the designed values of each and every component
4. Connect the function generator with sine wave of 20 mV p-p as input at the input terminals of the circuit. (Or) use signal source.
5. Connect the Cathode Ray Oscilloscope (CRO) to the output terminals of the circuit.
6. Go to simulation button click it for simulation process.
7. From the CRO note the following values1.
   - Input voltage $V_i$ , Output voltage Vout, Voltage Gain Av, Phase Shift
8. To study the frequency response use, Bode platter and calculate bandwidth.

## Multistage CE amplifier:




**Stage 2 : CE Amplifier**

**Theoretical Gain**

Pull Up Resistance = 3k||3k =1.5kΩ.

Pull Down Resistance = Dynamic Resistance = 10Ω

Gain = Pull Up Resistance/ Pull Down Resistance = 1.5kΩ/10Ω

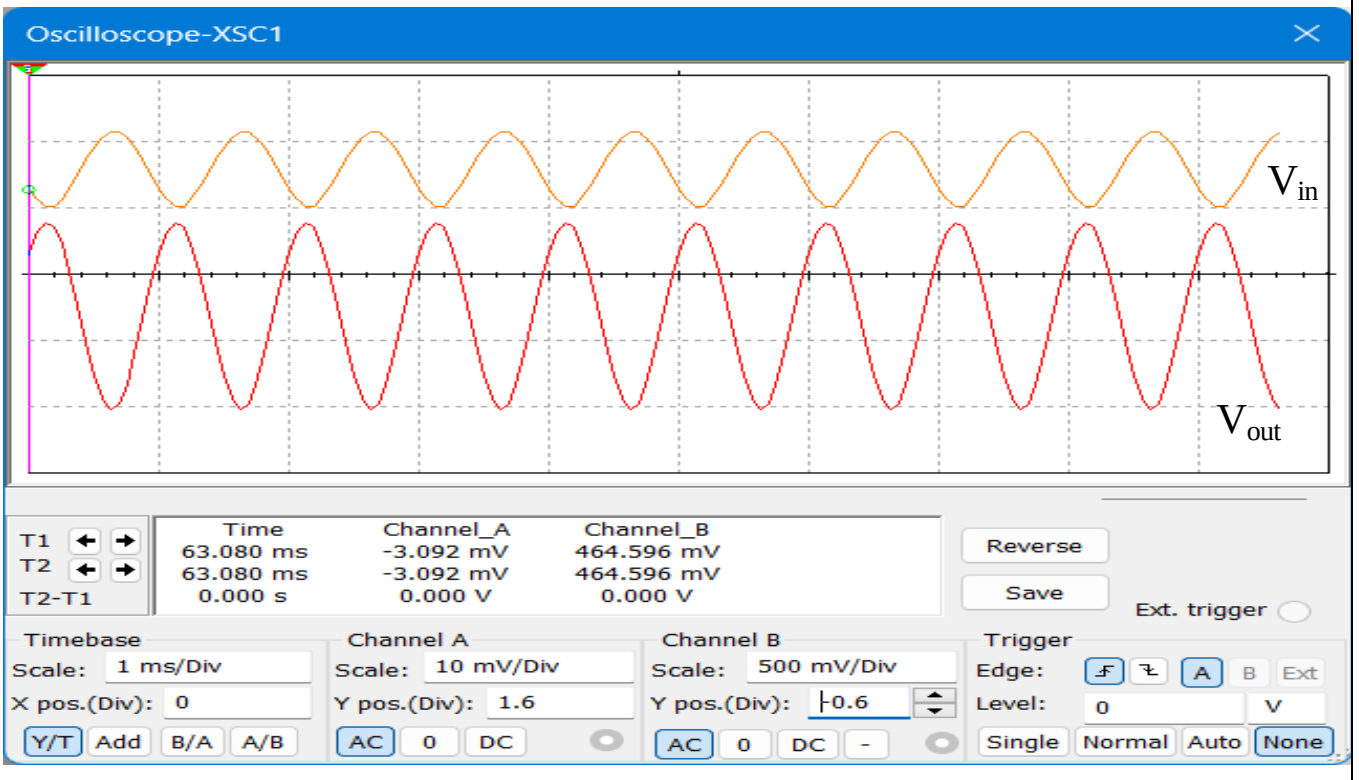
Gain = 150

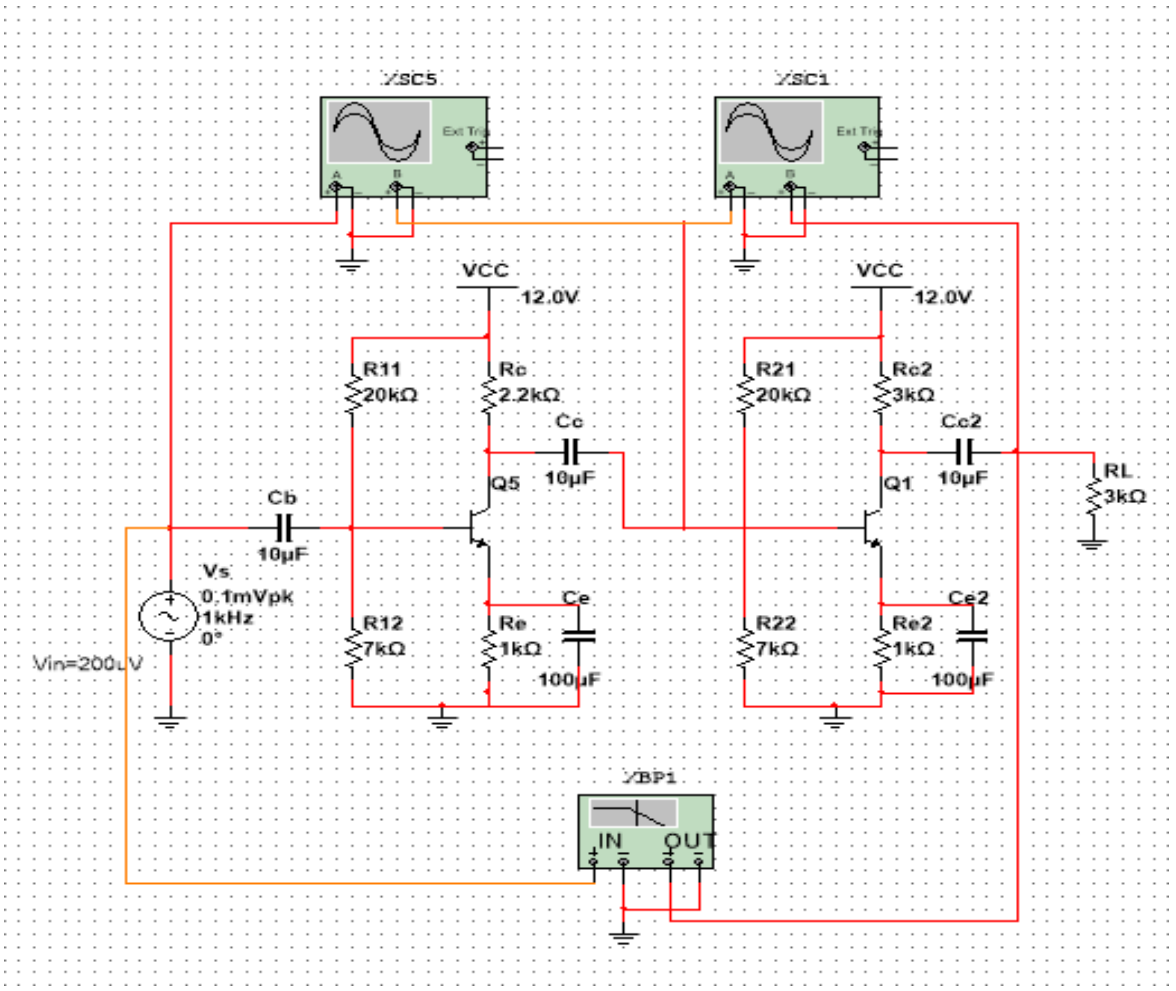
**Practical Gain**

Input Voltage = 12mV

Output Voltage = 1500mV

Gain = Output Voltage/Input Voltage = 1500/12 = 125 Gain2 = 125






**Stage 1 : CE Amplifier:**
**Theoretical Gain=** Pull Up Resistance/ Pull Down Resistance
Pull Down Resistance = 10Ω
Pull Up Resistance = 2.2kΩ || Rin of Stage 2 CE Amplifier
Rin of Stage 2 CE Amplifier = hie2 || R21 || R22 = 1.2K||7k||20k = 0.97kΩ =

Rin of Stage 2 CE Amplifier 1kΩ(approximately)

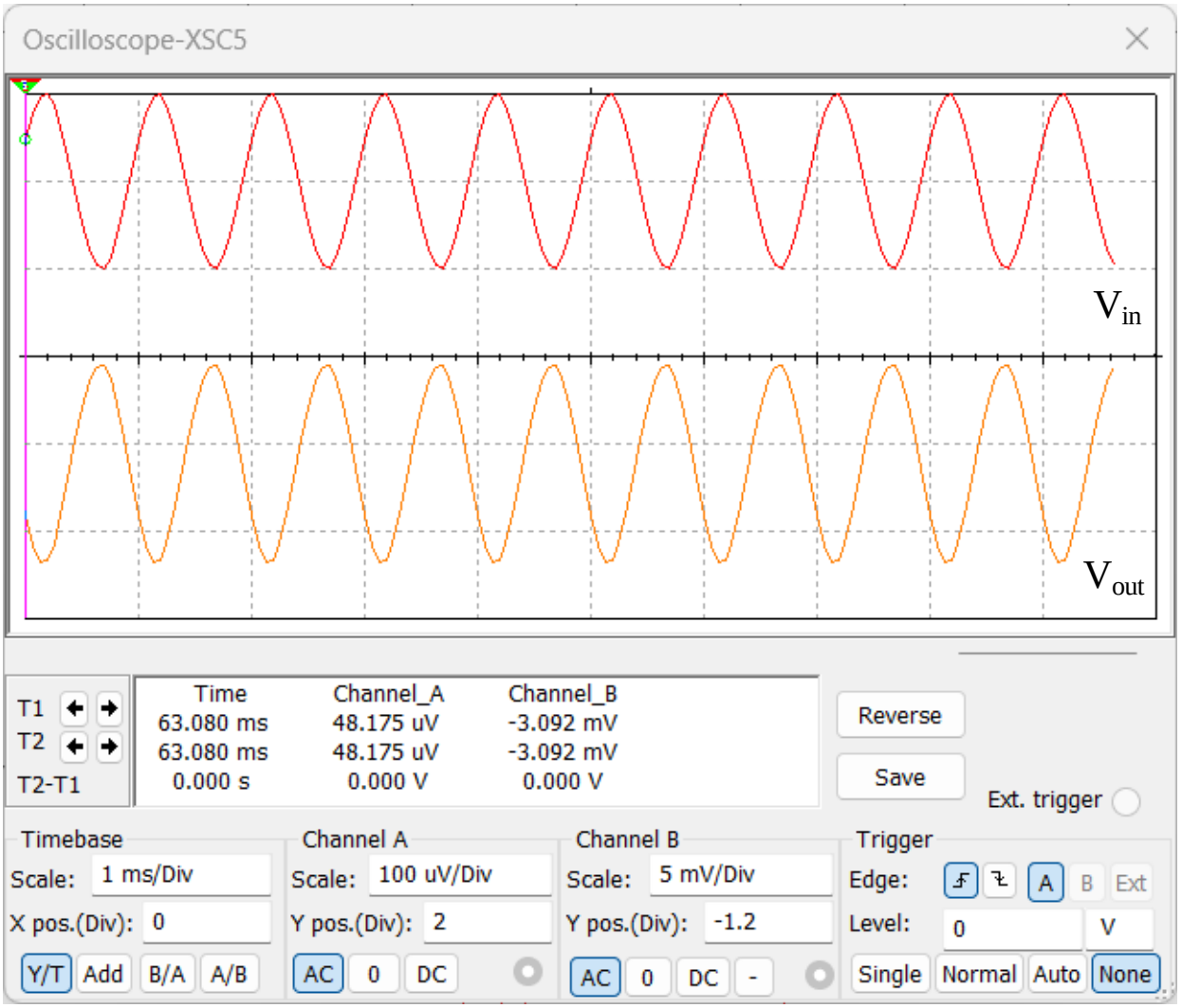
Pull Up Resistance = 2.2k || 1k = 0.6875kΩ

Gain = 0.68k/10 = 68

Gain = 68

**Practical Gain:**
Input Voltage = 200uV
Output Voltage = 12mV
Gain = Output Voltage/Input Voltage = 12000/200 = 60

Gain1 = 60




**Theoretical Voltage Gain:**

The Overall Voltage Gain, Av = Gain1*Gain2

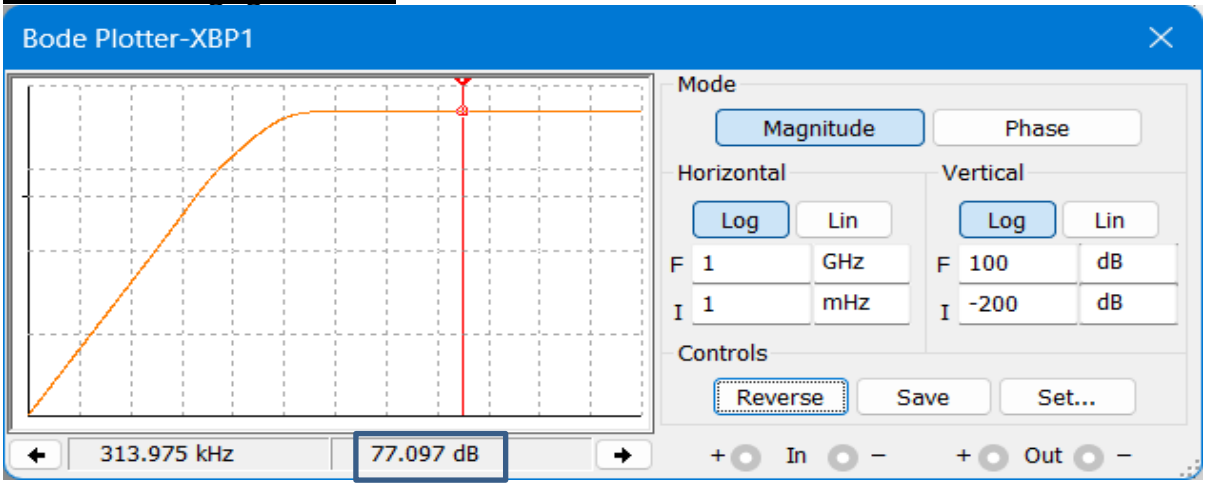
= 60*125 = 7500

Gain in dB = 20log (Av) = 20log (7500) = 77.5dB

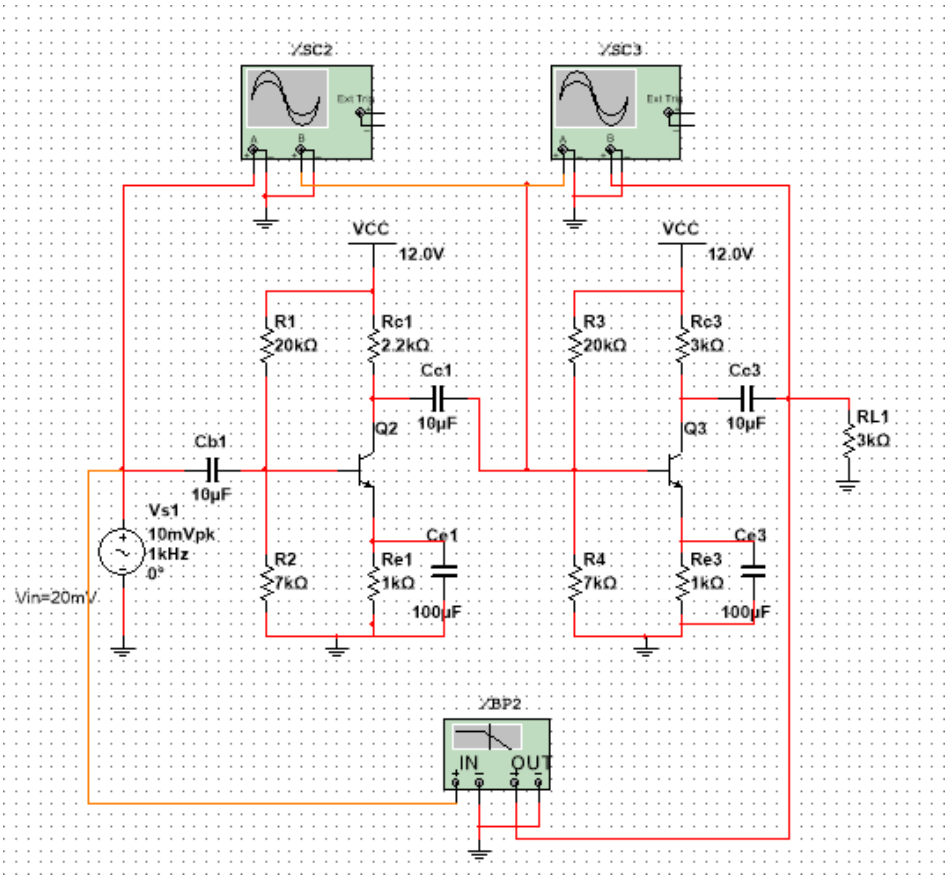
= 20log (Gain1) + 20log (Gain2) = 20log (60) + 20log (125)

= 35.56 + 41.93 = 77.50 dB

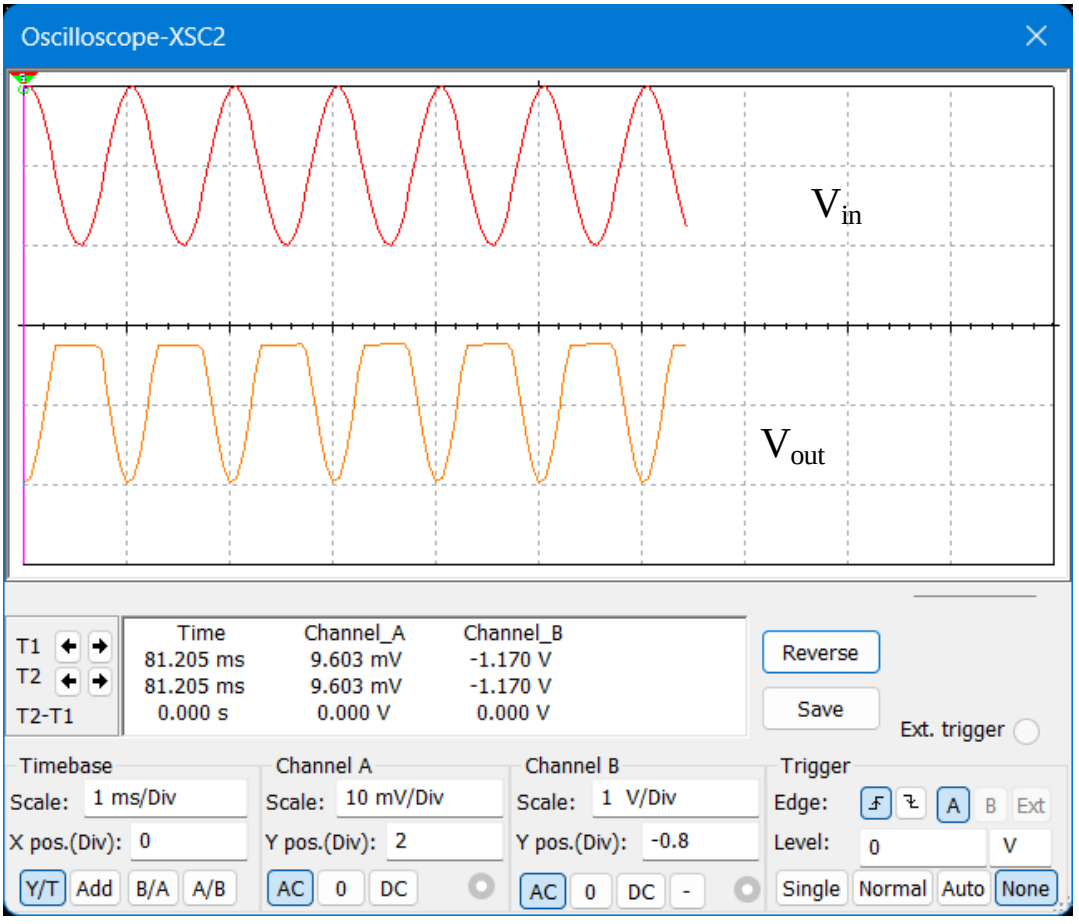
**Practical Voltage gain in dB:**



## For Input Signal Vin = 20mV(high Voltages)



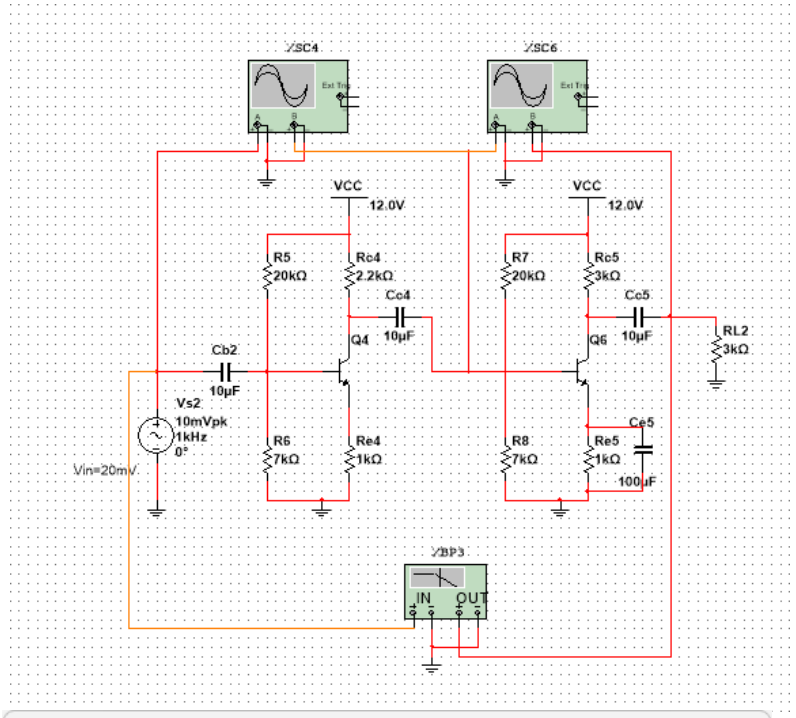

**Conclusion**: if a signal x is passed through a CE amplifier of Gain G1 the output Signal is G1x.
Therefore signal passing through 2nd stage CE Amplifier is very high, which can cause change in the QPoint of Amplifier, as a result Q3 gets into Saturation State and distortion in Output takes place.

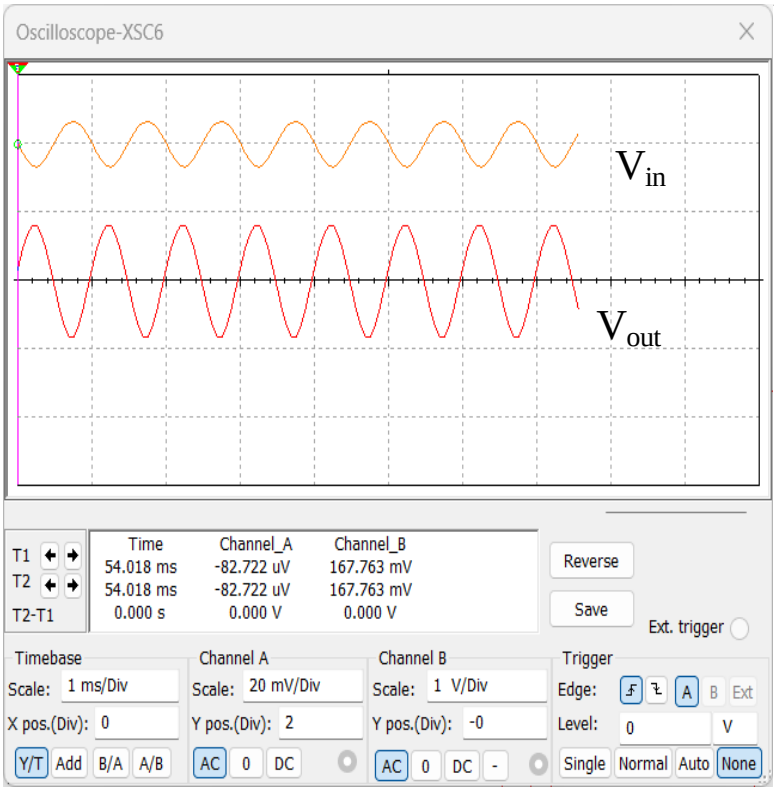


## Methods to overcome distortion in Output:

- Decrease Gain of 1st Stage Amplifier
- Decrease Strength of Input Signal

Case 1: Decrease Gain of 1st Stage Amplifier by removing bypass capacitor of 1st Stage Amplifier:

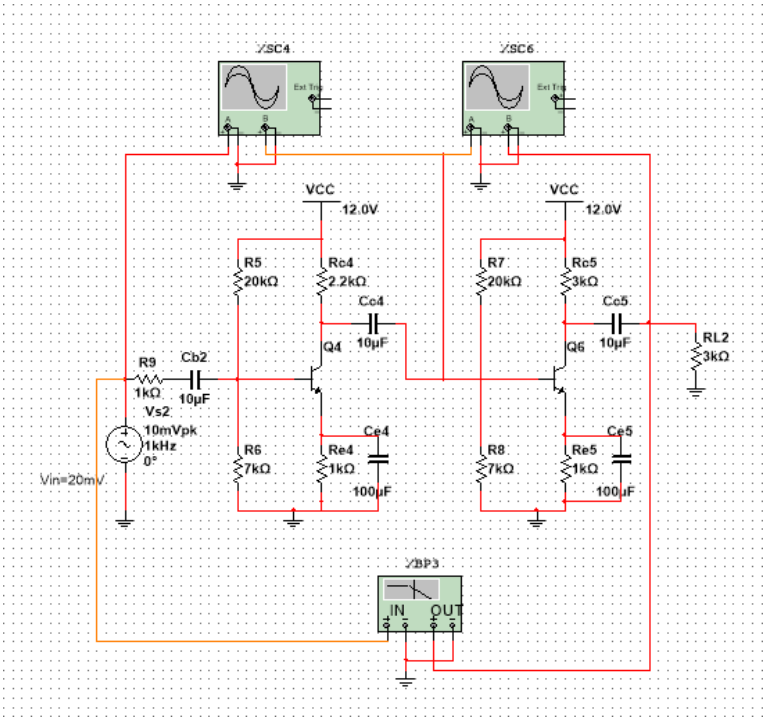


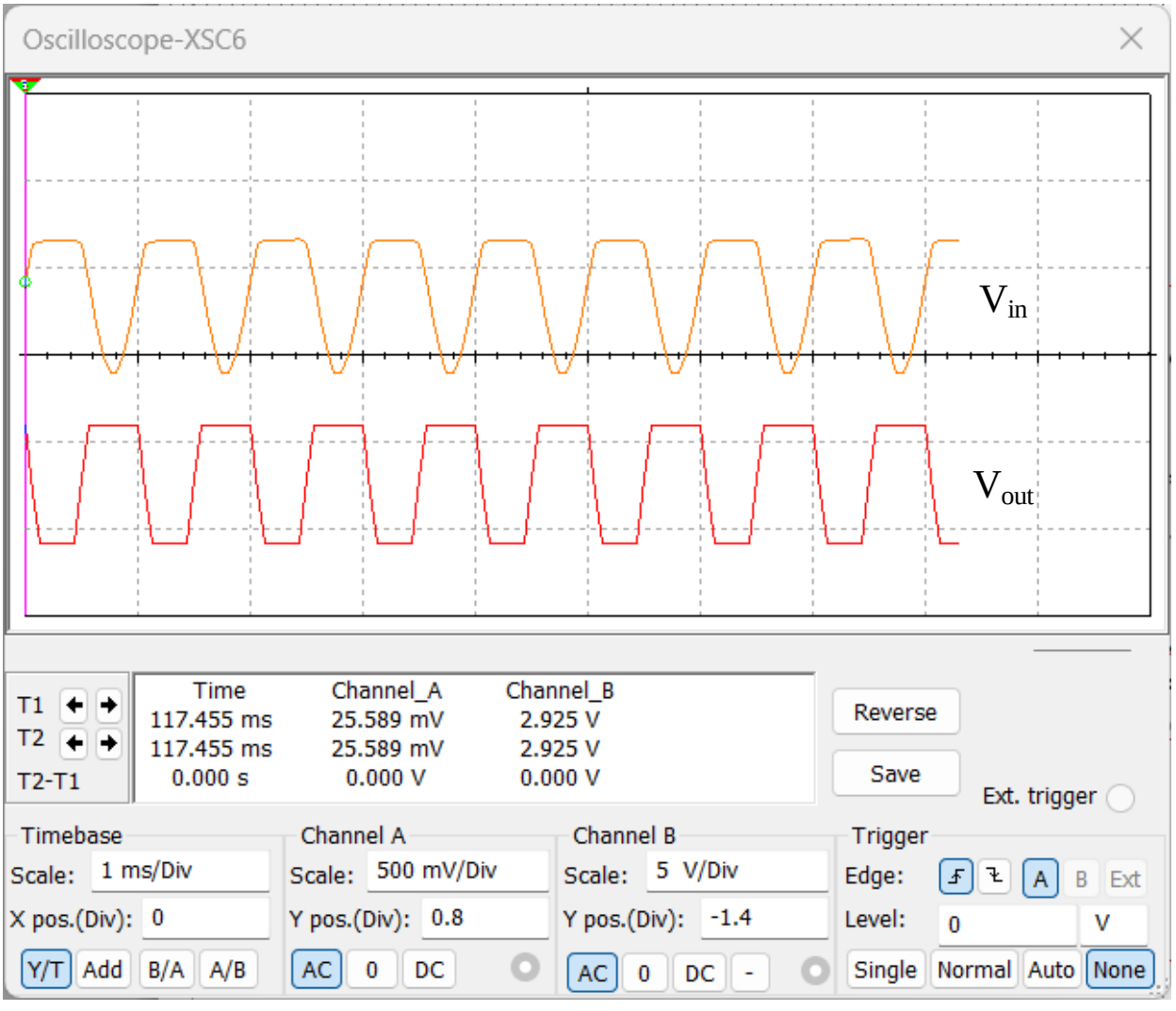




Conclusion: We can obtain faithful amplification after removing the bypass capacitor in 1st Stage so that small signal appears at input of 2nd Stage amplifier.

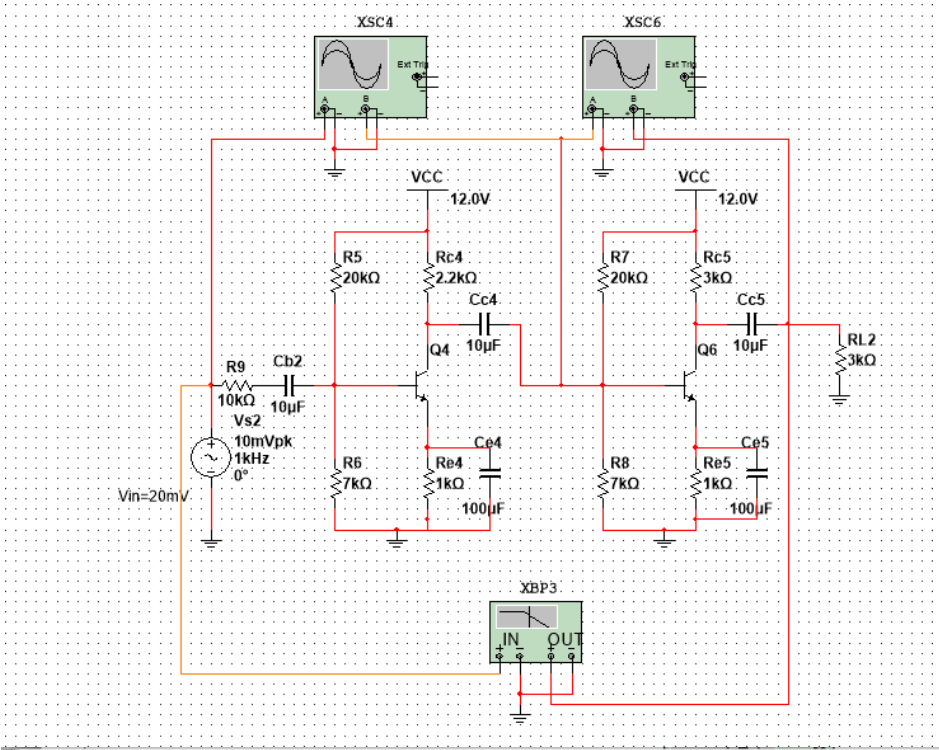
- Case 2: Decrease Strength of Input Signal By placing a series resistance (very High), Rs at input side which attenuates maximum portion of signal.

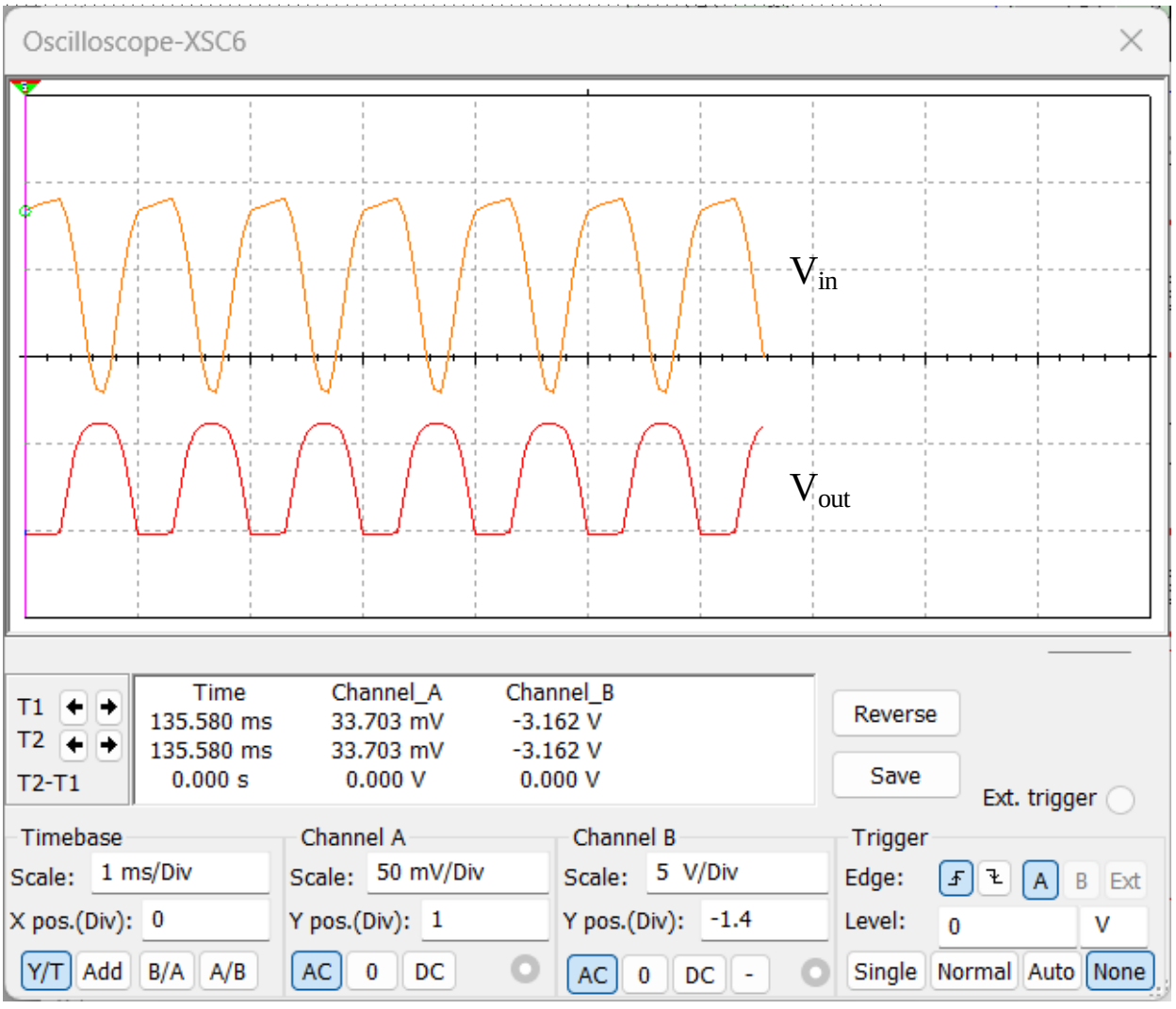
1) Rs = 1KΩ



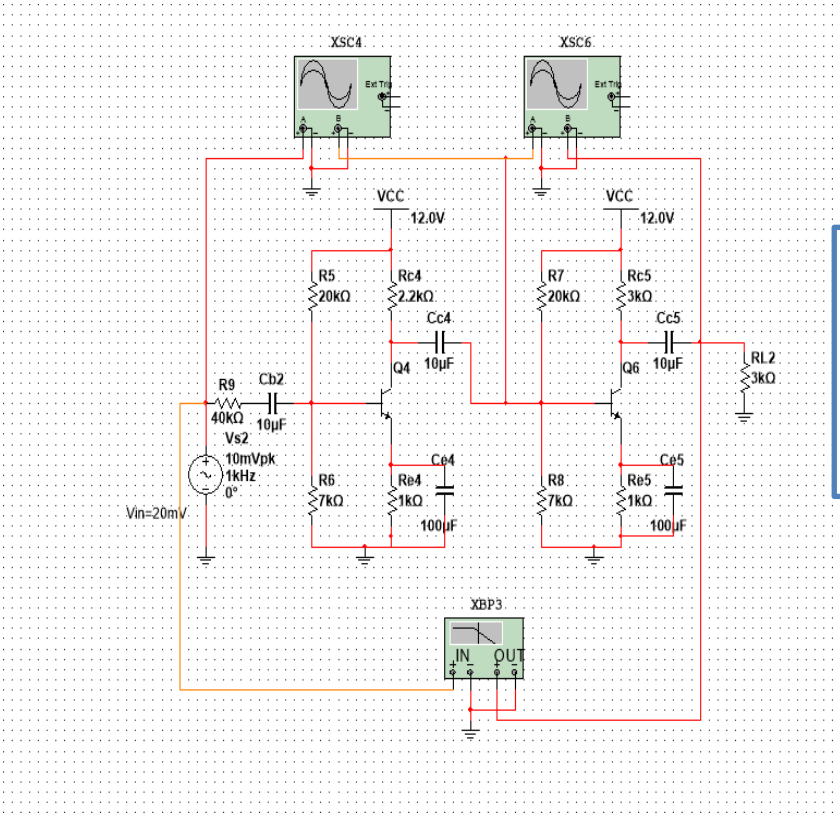



2) Rs = 10KΩ

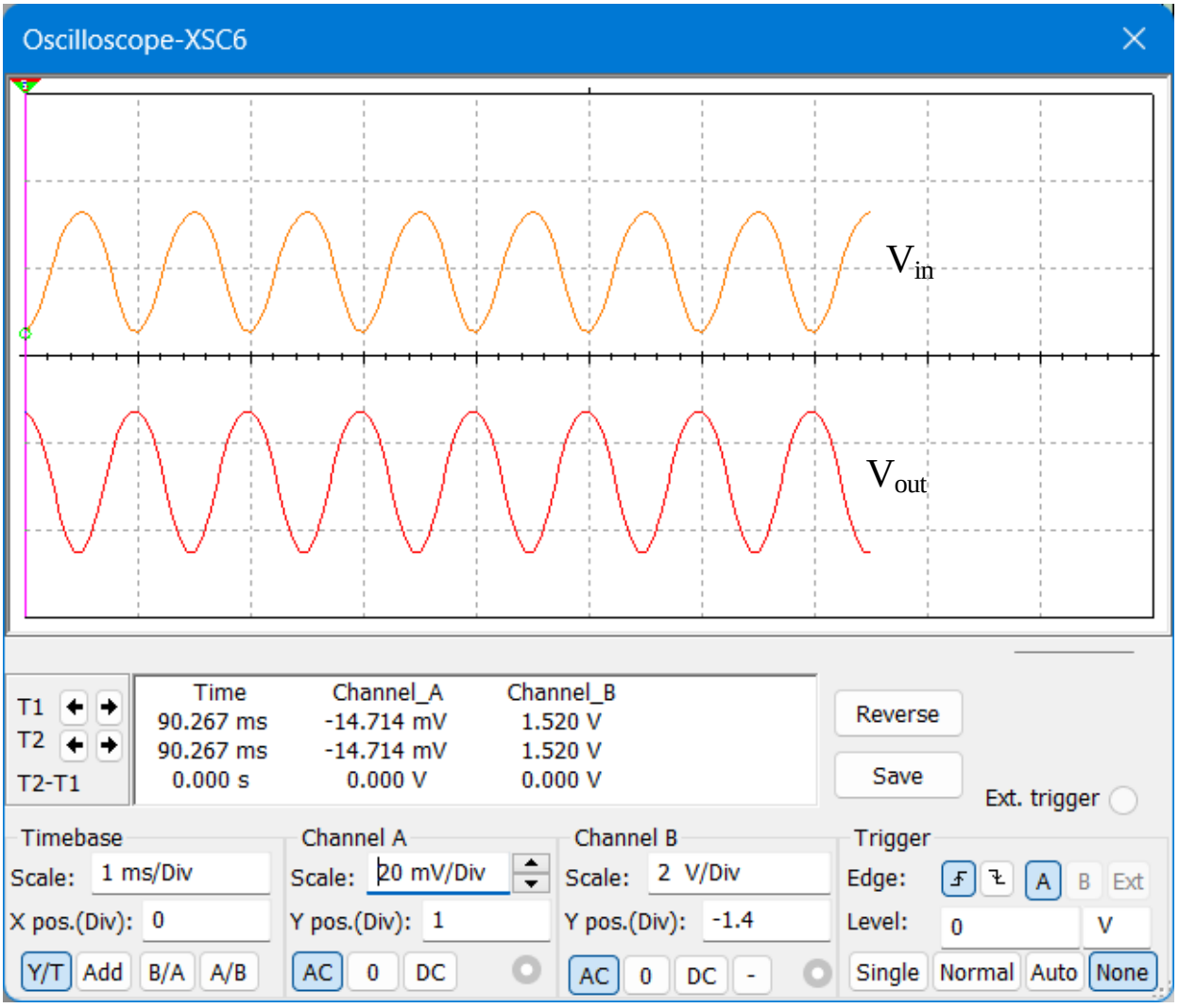

XSC4
XSC6
VCC
12.0V
R5
20kΩ
Rc4
2.2kΩ
Cc4
10µF
Q4
R9
10kΩ
Cb2
10µF
Vs2
10mVpk
1kHz
0°
Vin=20mV
R6
7kΩ
Re4
1kΩ
Ce4
100µF
R7
20kΩ
Rc5
3kΩ
Cc5
10µF
Q6
RL2
3kΩ
R8
7kΩ
Re5
1kΩ
Ce5
100µF
XBP3
IN
OUT


Oscilloscope-XSC6
$V_{in}$
$V_{out}$
T1
T2
T2-T1
Time
135.580 ms
135.580 ms
0.000 s
Channel_A
33.703 mV
33.703 mV
0.000 V
Channel_B
-3.162 V
-3.162 V
0.000 V
Reverse
Save
Ext. trigger
Timebase
Scale: 1 ms/Div
X pos.(Div): 0
Y/T Add B/A A/B
Channel A
Scale: 50 mV/Div
Y pos.(Div): 1
AC 0 DC
Channel B
Scale: 5 V/Div
Y pos.(Div): -1.4
AC 0 DC -
Trigger
Edge: A B Ext
Level: 0 V
Single Normal Auto None

3) Rs = 40KΩ




Conclusion: We can obtain faithful amplification by attenuating maximum portion of signal by placing a series resistance of 40kΩ at input side.



**HARDWARE SIMULATION:**

**Procedure:**

1. Connect the circuit as per the circuit diagram.
2. Apply the supply voltage , $V_{cc}$=12V
3. Make sure that the transistor is operating point in active region by keeping $V_{CE}$ half of $V_{CC}$.
4. Now feed an ac signal of 20mV at the input of the amplifier with different frequencies ranging from 100Hz to 300 MHz and measure the amplifier output voltage.
5. Now calculate the gain in decibels at various input signal frequencies.

Draw a graph with frequencies on X-axis and gain in dBs on Y-axis.
From the graph calculate Bandwidth.

## Observations:

**Multistage CE amplifier without bypass capacitor**

| Frequency (in Hz) | Input (in mV) | Output (in mV) | Voltage Gain (dB) | |
|---|---|---|---|---|
| **10** | 61.1 | 1.5 | 64.014 | |
| **50** | 76.4 | 2.3 | 68.09 | |
| **100** | 92.1 | 4.1 | 75.917 | |
| **200** | 94.9 | 5.9 | 82.59 | |
| **300** | 88.8 | 7.6 | 88.99 | |
| **500** | 87 | 7.4 | 88.86 | |
| **1k** | 87 | 7.6 | 89.39 | **Mid Frequency Gain** |
| **2k** | 88 | 7.4 | 88.63 | |
| **3k** | 88 | 7.6 | 89.19 | |
| **10k** | 88 | 7.2 | 88.08 | |
| **50k** | 88 | 7.2 | 88.08 | |
| **100k** | 92 | 7.2 | 87.20 | |
| **500k** | 92 | 5.0 | 79.9 | |
| **1G** | 93 | 3.2 | 71.97 | |
| **2G** | 92 | 2.4 | 65.2 | |
| **3G** | 91 | 2.2 | 63.7 | |

**Conclusion:** Last Stage Gives the Gain as per designed but the previous stages can't deliver the gain as designed due to loading effect**.**