

EXPERIMENT-3

MULTISTAGE CE AMPLIFIER

AIM: To design a Multi stage CE amplifier with following specifications and to study the frequency response of amplifier, calculate voltage gain and bandwidth from the response.

OBJECTIVES:

1. Design a common emitter amplifier for given specifications.
2. Simulate the designed amplifier.
3. Develop the hardware for designed amplifier.
4. Compare simulated results with practical results.

APPARATUS:

S.No	Name of the Component/ Equipment	Specifications	Quantity
1	Transistor (BC-107)	I _{cmax} =100mA PD=300mw V _{ceo} =45V V _{beo} =50V	1
2	Capacitors (designed values)	Electrolytic type, Voltage rating= 1.6V	3
3	Resistors (designed values)	Power Rating =0.5 W Carbon type	4
4	Function Generator	(0 -1) MHZ	1
5	Cathode Ray Oscilloscope	20 MHZ	1
6	Regulated Power Supply	(0-30) V,1Amp	1

THEORY:

Common Emitter amplifier has the emitter terminal as the common terminal between input and output terminals. The emitter base junction is forward biased and collector base junction is reverse biased, so that transistor remains in active region throughout the operation. When a sinusoidal AC signal is applied at input terminals of circuit during positive half cycle the forward bias of base emitter junction V_{BE} is increased resulting in an increase in I_B , the collector current I_C is increased by β times the increase in I_B , V_{CE} is correspondingly decreased. i.e output voltage gets decreased. Thus in a CE amplifier a positive going signal is converted into a negative going output signal i.e. 180° phase shift is introduced between output and input signal and it is an amplified version of input signal.

DESIGN SPECIFICATION:

DESIGN SPECIFICATIONS: $V_{CC} = 12V$, $I_C = 2.5mA$ (2-3 mA), $V_{CE} = 6V$ (half of max supply), $A_V = 150$, $h_{fe} = 150$, $h_{ie} = 9K\Omega$, Silicon NPN Transistor

PRE REQUISITIES:

Gain of CE amplifier can be calculated:

GAIN = pull up resistance / pull down resistance

$$= 1.5K/10$$

$$= 150 \rightarrow \text{equation 1}$$

DESIGN OF CE AMPLIFIER WITH GAIN=150:

Calculation of R_C :

- $I_C = 2.5mA = I_E$
- $R_e = V_t / I_E = 26mV / 2.5mA = 10\Omega$
- $R_C = 150 * R_e = 150 * 10 = 1.5k\Omega$ -----from eq(1)



Calculation of R_E :

- $R_E = V_E / I_E = 2.25 / 2.5 \text{ mA} = 1 \text{ K}\Omega$

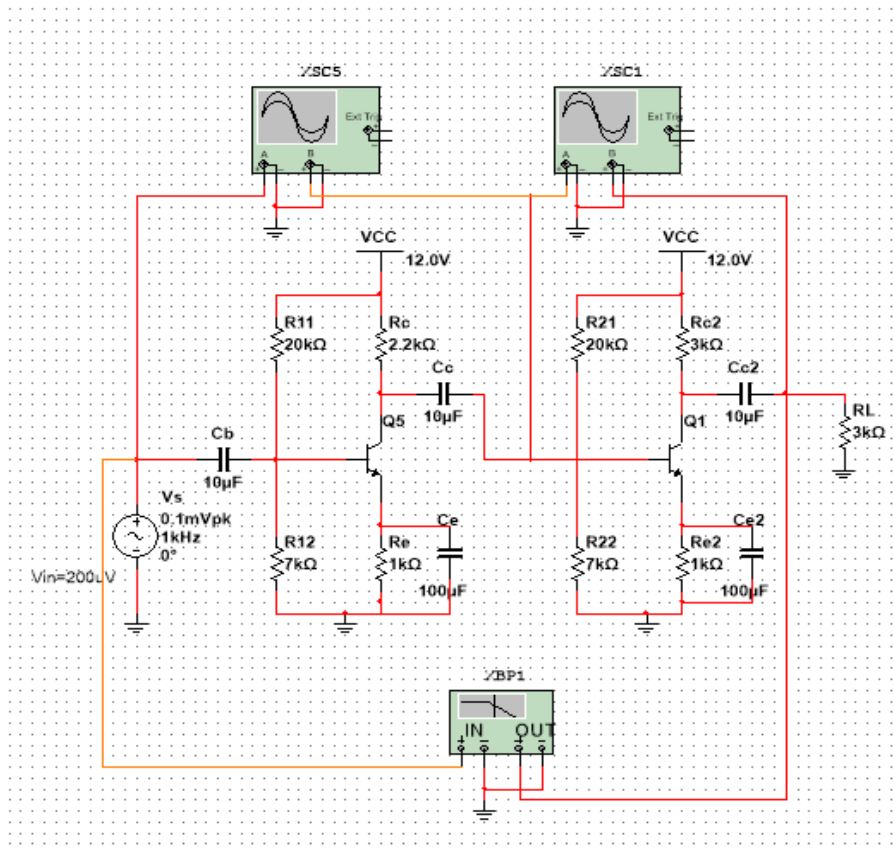
Calculation of R_1 and R_2 :

- From voltage analysis:
- $R_1 \parallel R_2$ network should generate 3V from 12V
- $V_{CC} * R_2 / (R_1 + R_2) = 3 \text{ V}$
- $12 * R_2 / (R_1 + R_2) = 3 \text{ V}$
- $R_1 = 3R_2$ ----- eq(2)
- from current analysis:
- Current through base branch should be minimum current
- So $R_2 \ll R_{inb}$
- $R_2 \ll \beta(R_E) = 100(1 \text{ K}\Omega)$
- $R_2 < 10(1 \text{ K}\Omega) = 7 \text{ K}\Omega$
- Chosen the value around 7 K Ω ----- eq(3)
- From eq(2), eq(3) $R_1 = 21 \text{ K}\Omega$
- $R_2 < 10(1 \text{ K}\Omega)$.

Procedure:

1. Switch ON the computer and open the multisim software
2. Observe Design tool box, Instrumentation tool box, component tool box and its component functionality
3. From above tool boxes,
Connect the circuit using the designed values of each and every component
4. Connect the function generator with sine wave of 20 mV p-p as input at the input terminals of the circuit. (Or) use signal source.
5. Connect the Cathode Ray Oscilloscope (CRO) to the output terminals of the circuit.
6. Go to simulation button click it for simulation process.
7. From the CRO note the following values1.
 - Input voltage V_i , Output voltage V_{out} , Voltage Gain A_v , Phase Shift
8. To study the frequency response use, Bode platter and calculate bandwidth.

Multistage CE amplifier:



Stage 2 : CE Amplifier

Theoretical Gain

Pull Up Resistance =
 $3k \parallel 3k = 1.5k\Omega$.

Pull Down Resistance =
 Dynamic Resistance =
 10Ω

Gain = Pull Up
 Resistance/ Pull Down
 Resistance =
 $1.5k\Omega / 10\Omega$

Gain = 150

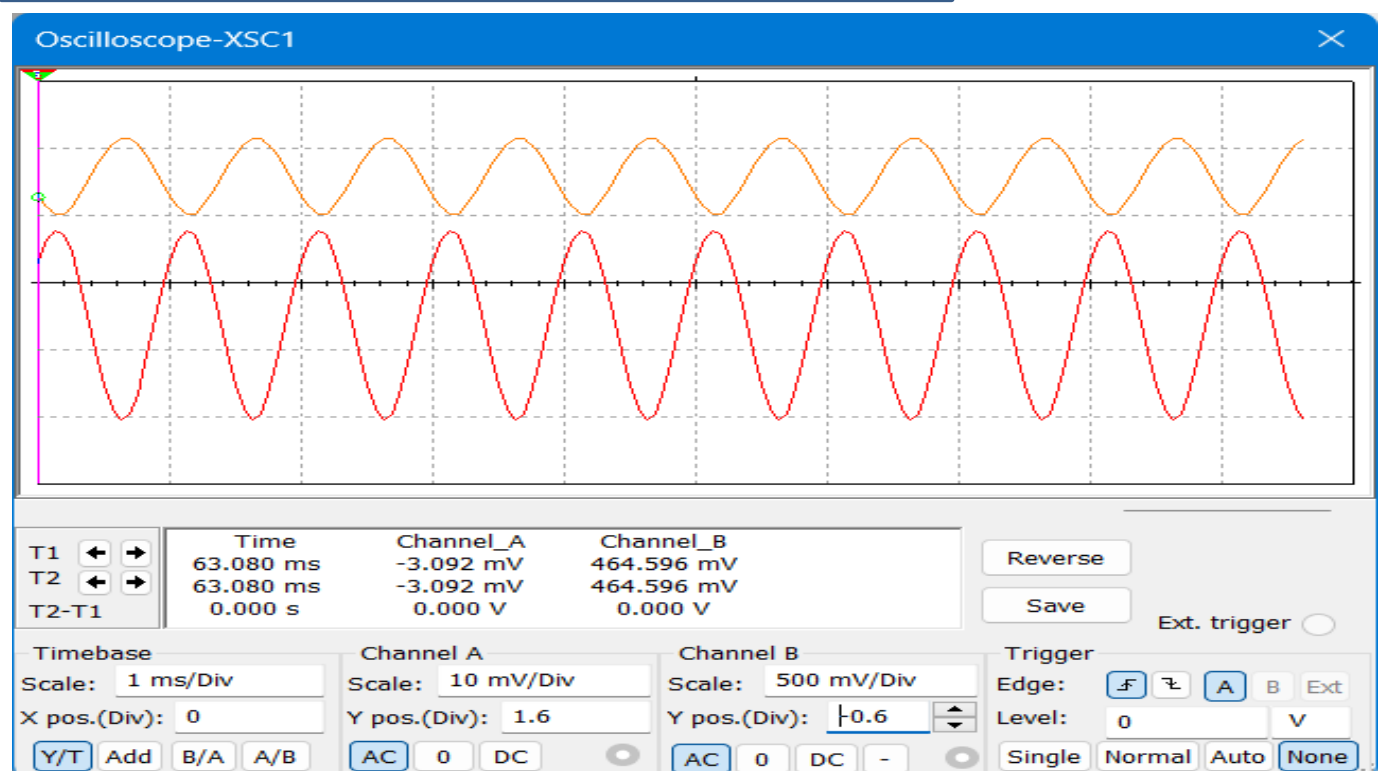
Practical Gain

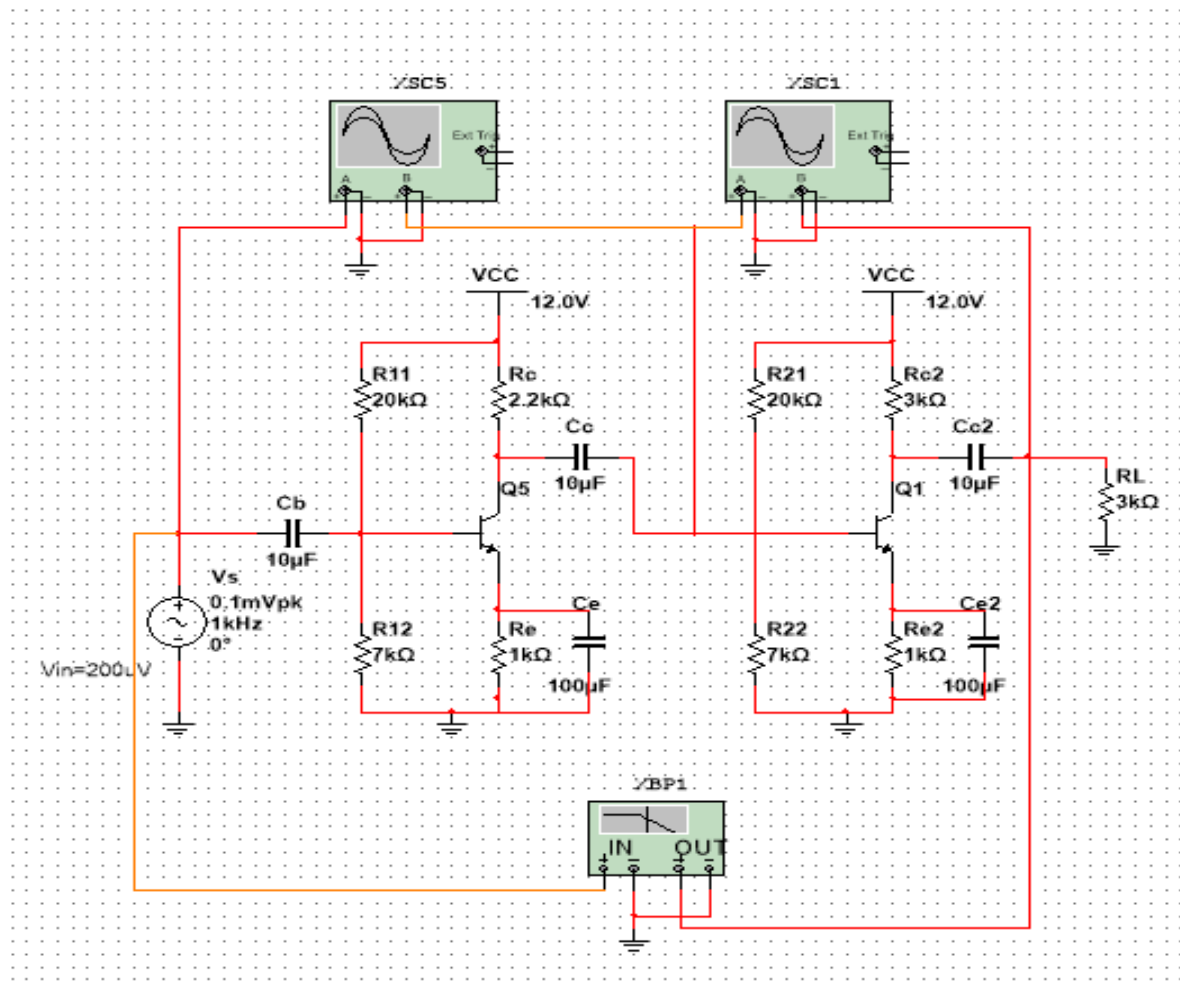
Input Voltage = 12mV

Output Voltage = 1500mV

Gain = Output Voltage/Input Voltage = $1500/12 = 125$

Gain2 = 125





Stage 1 : CE Amplifier:

Theoretical Gain= Pull Up Resistance/ Pull Down Resistance

Pull Down Resistance = 10Ω

Pull Up Resistance = $2.2k\Omega \parallel R_{in} \text{ of Stage 2 CE Amplifier}$

$R_{in} \text{ of Stage 2 CE Amplifier} = h_{ie2} \parallel R_{21} \parallel R_{22} = 1.2K \parallel 7k \parallel 20k = 0.97k\Omega =$

$R_{in} \text{ of Stage 2 CE Amplifier } 1k\Omega \text{ (approximately)}$

Pull Up Resistance = $2.2k \parallel 1k = 0.6875k\Omega$

Gain = $0.68k/10 = 68$

Gain = 68

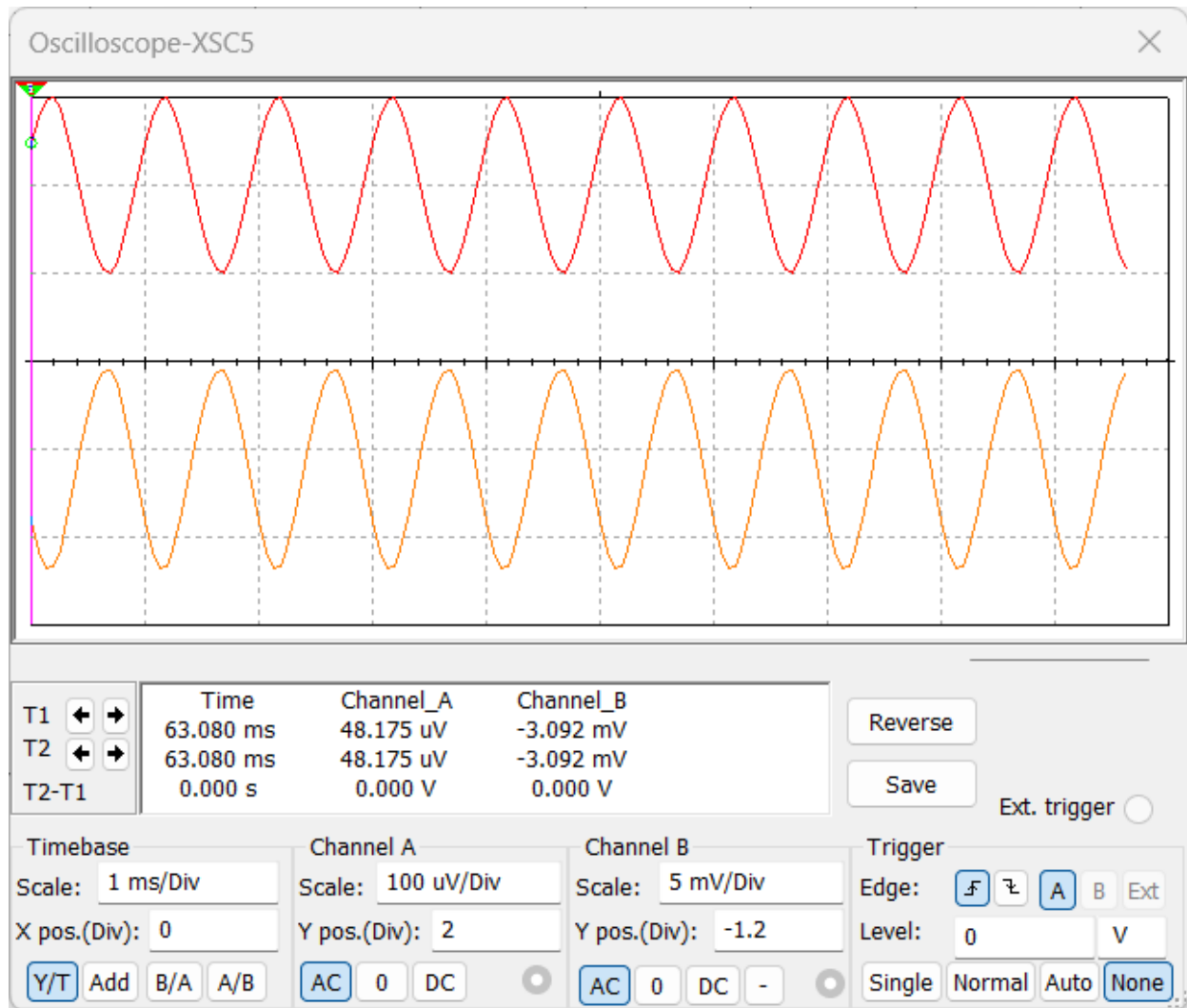
Practical Gain:

Input Voltage = $200\mu V$

Output Voltage = $12mV$

Gain = Output Voltage/Input Voltage = $12000/200 = 60$

Gain1 = 60

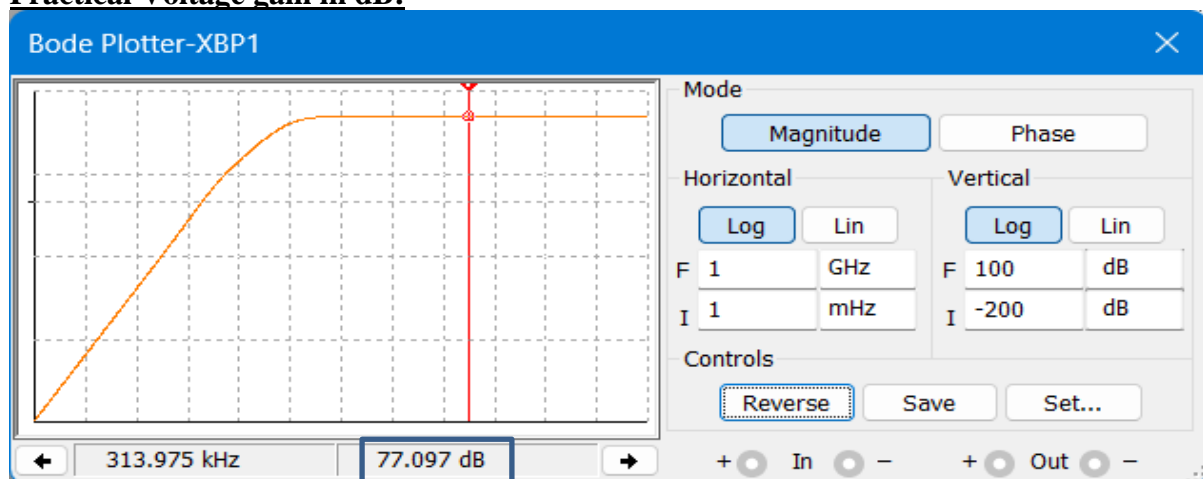


Theoretical Voltage Gain:

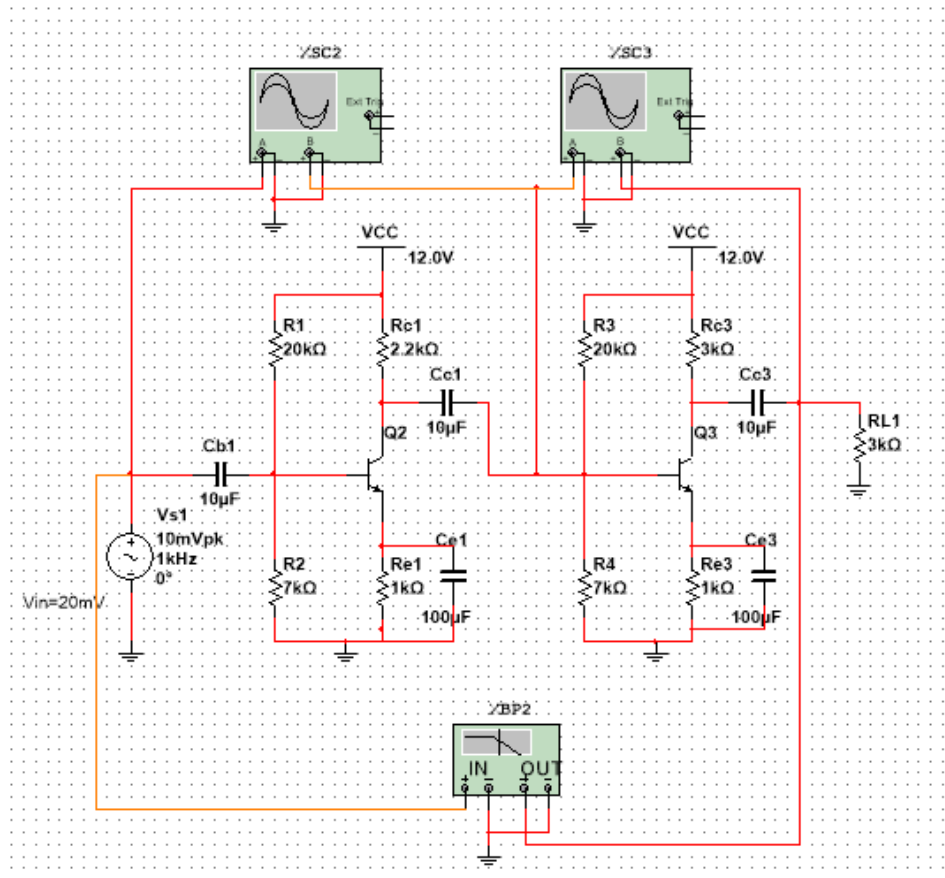
The Overall Voltage Gain, $A_v = \text{Gain}_1 * \text{Gain}_2$
 $= 60 * 125 = 7500$

Gain in dB = $20 \log (A_v) = 20 \log (7500) = 77.5 \text{ dB}$
 $= 20 \log (\text{Gain}_1) + 20 \log (\text{Gain}_2) = 20 \log (60) + 20 \log (125)$
 $= 35.56 + 41.93 = 77.50 \text{ dB}$

Practical Voltage gain in dB:

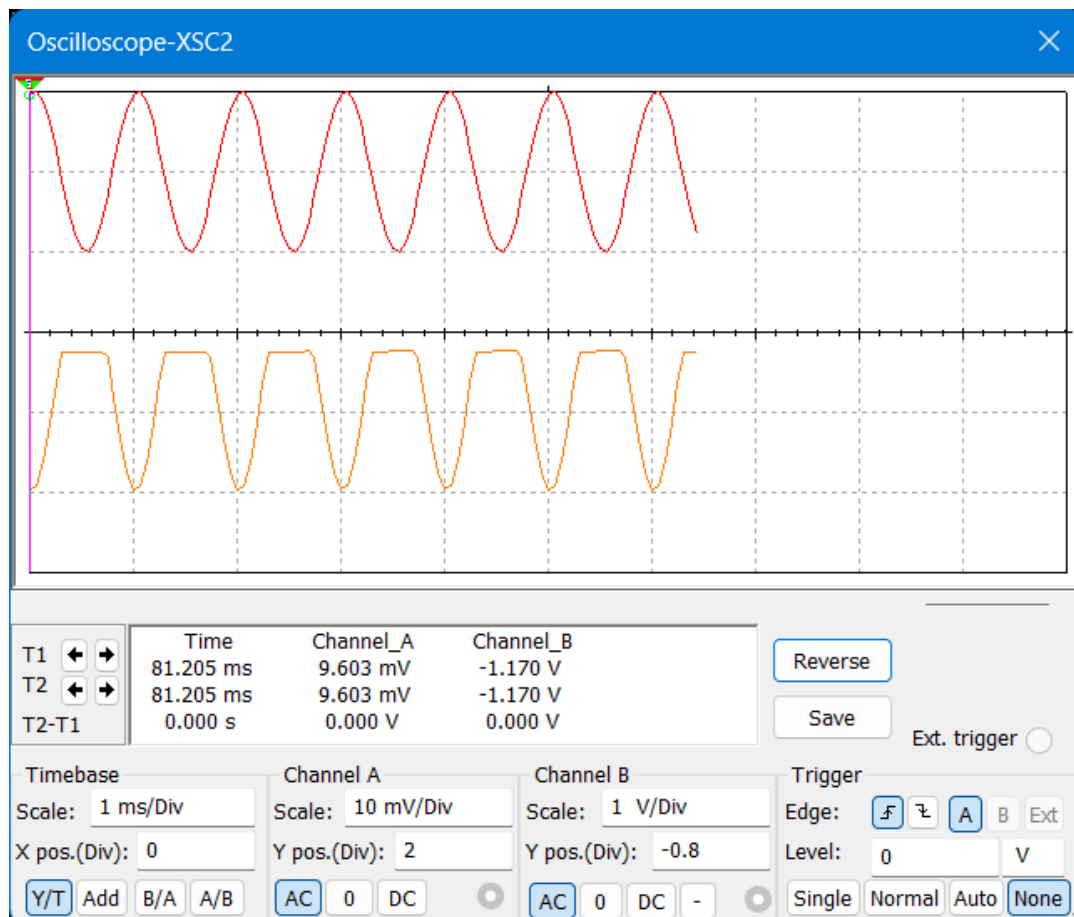


For Input Signal $V_{in} = 20\text{mV}$ (high Voltages)



Conclusion: if a signal x is passed through a CE amplifier of Gain G_1 the output Signal is G_1x .

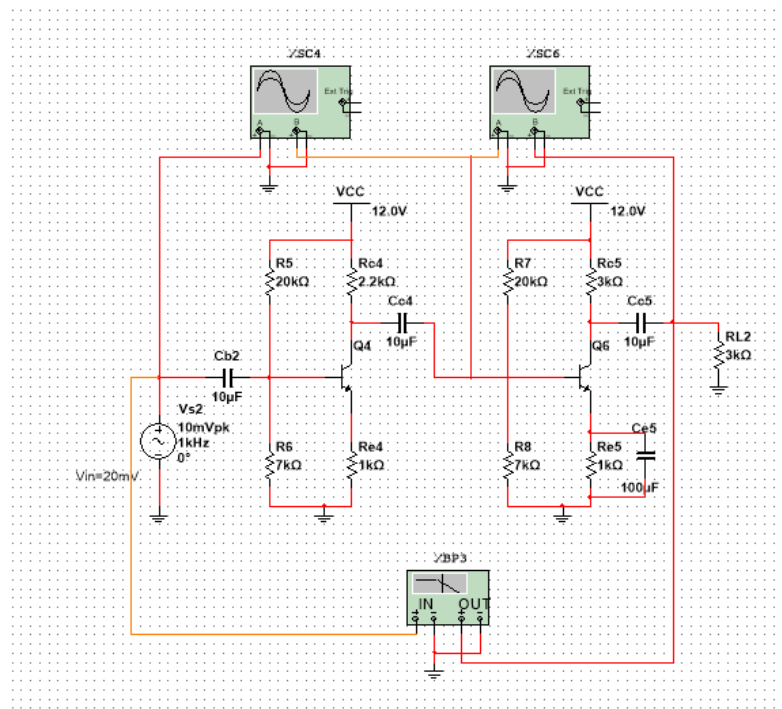
Therefore signal passing through 2nd stage CE Amplifier is very high, which can cause change in the QPoint of Amplifier, as a result Q3 gets into Saturation State and distortion in Output takes place.



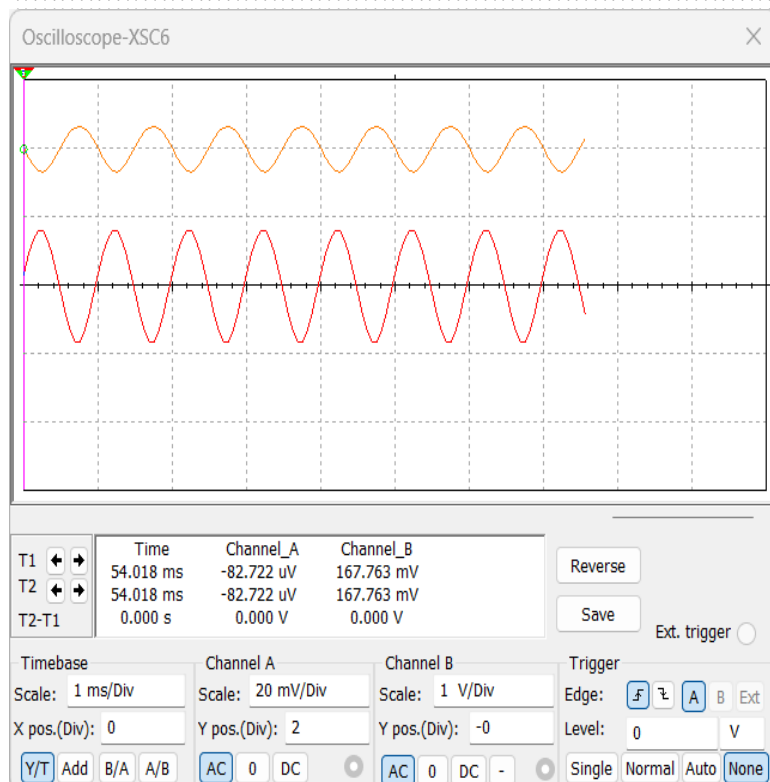
Methods to overcome distortion in Output:

- Decrease Gain of 1st Stage Amplifier
- Decrease Strength of Input Signal

Case 1: Decrease Gain of 1st Stage Amplifier by removing bypass capacitor of 1st Stage Amplifier:

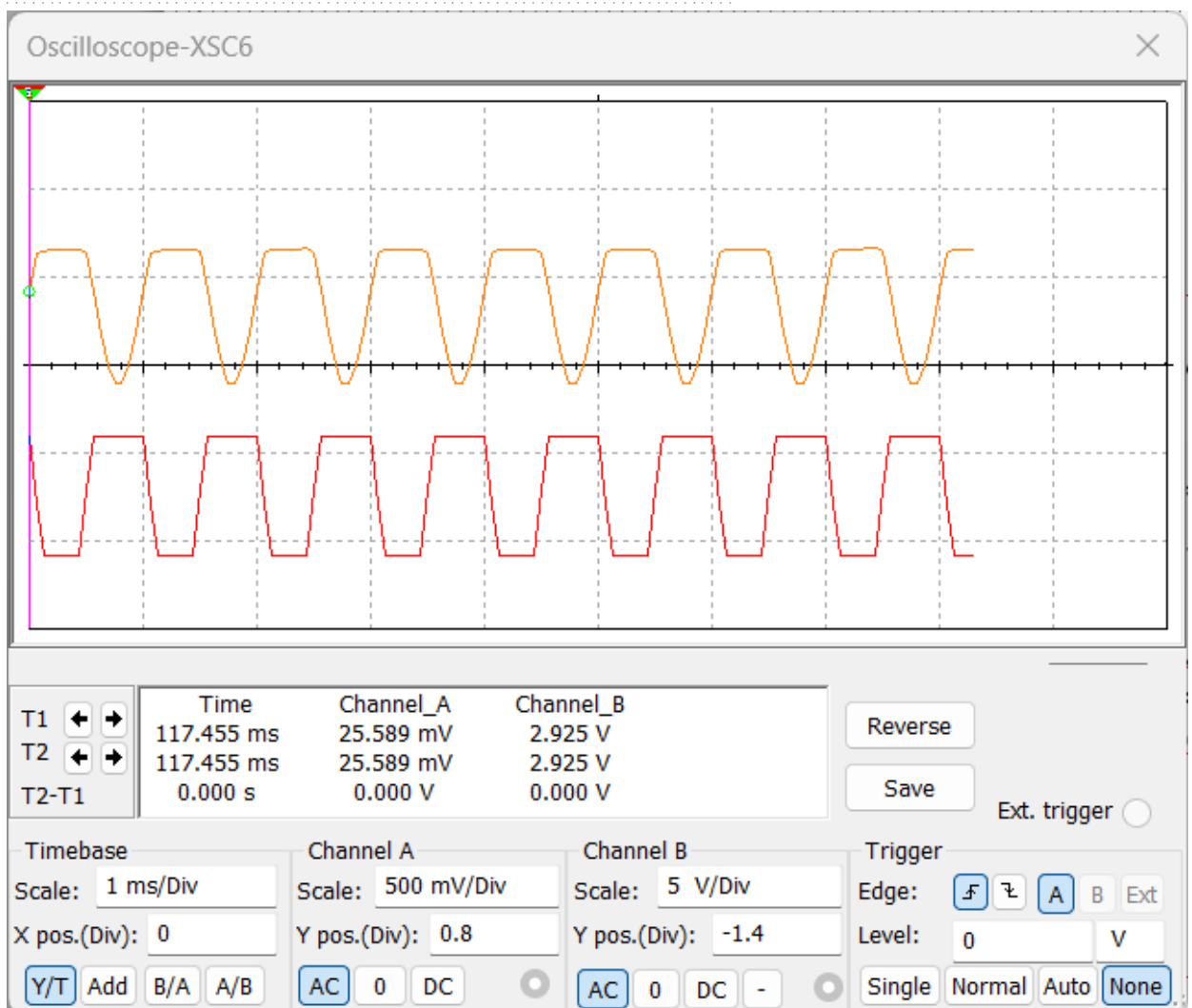
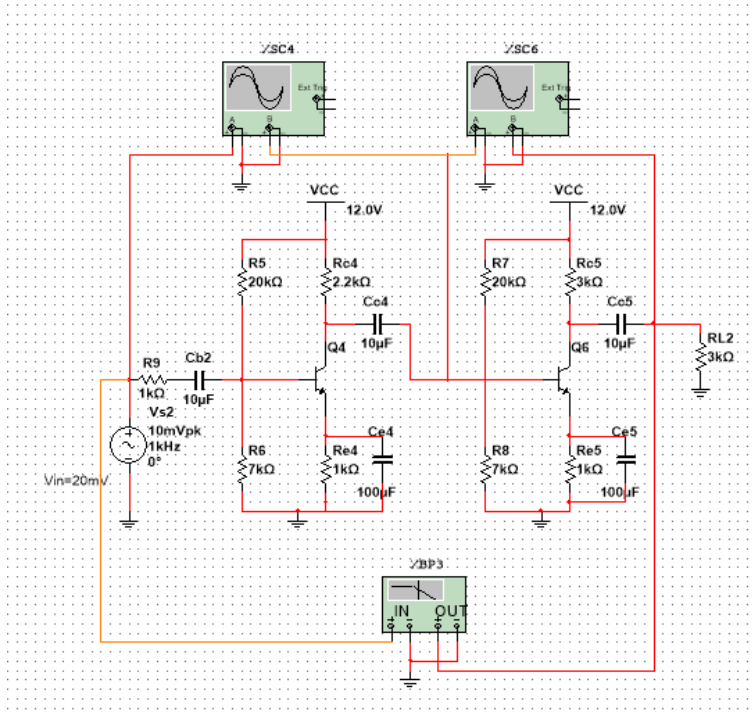


Conclusion: We can obtain faithful amplification after removing the bypass capacitor in 1st Stage so that small signal appears at input of 2nd Stage amplifier.

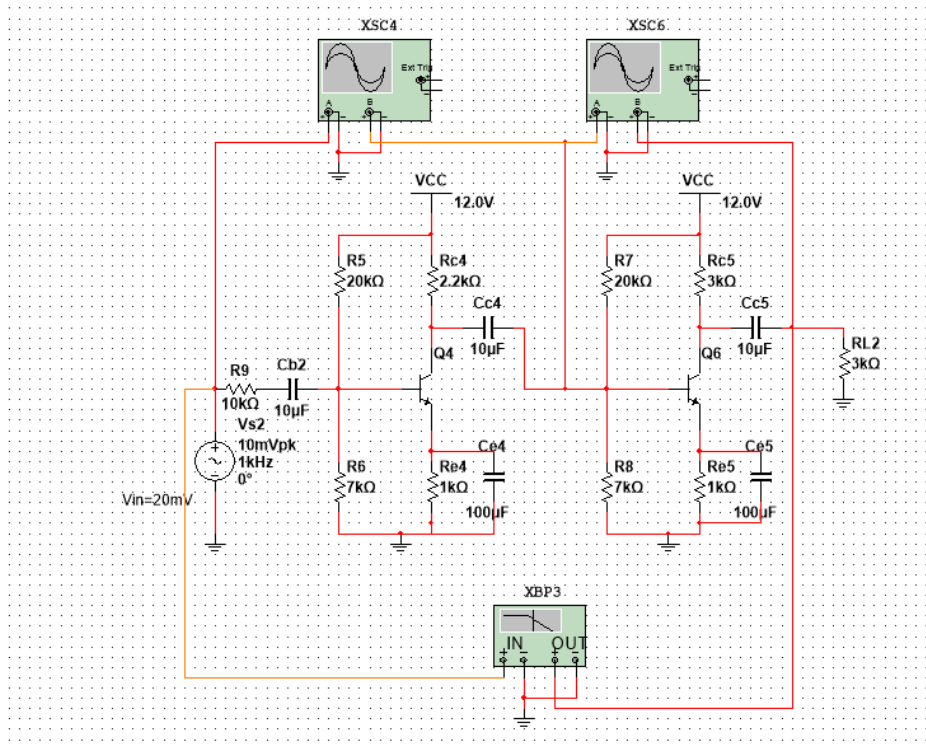


- Case 2: Decrease Strength of Input Signal By placing a series resistance (very High), R_s at input side which attenuates maximum portion of signal.

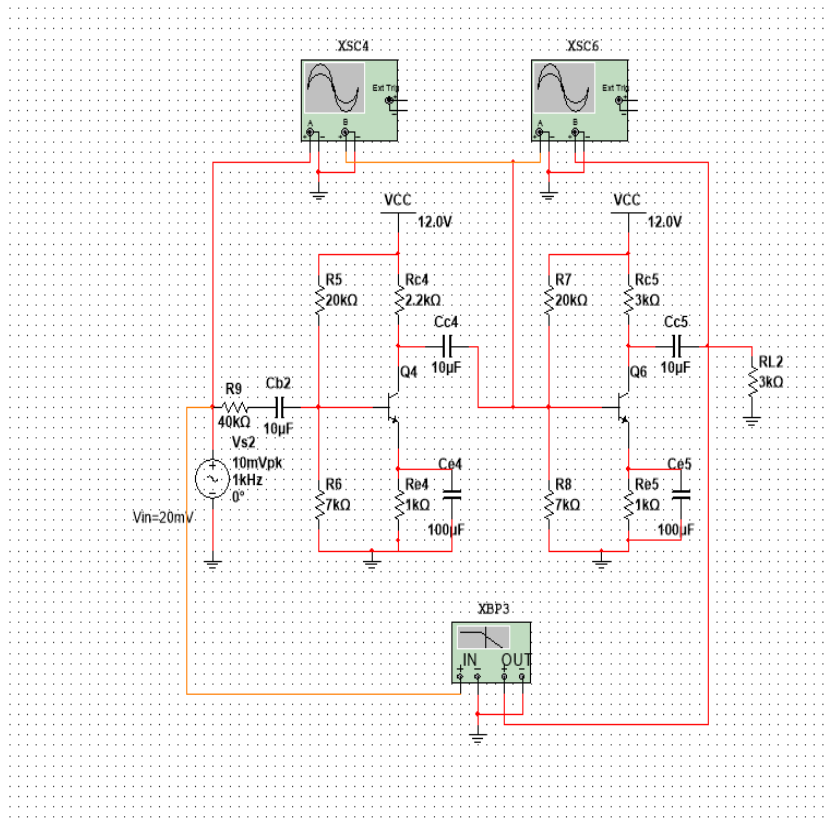
1) $R_s = 1K\Omega$



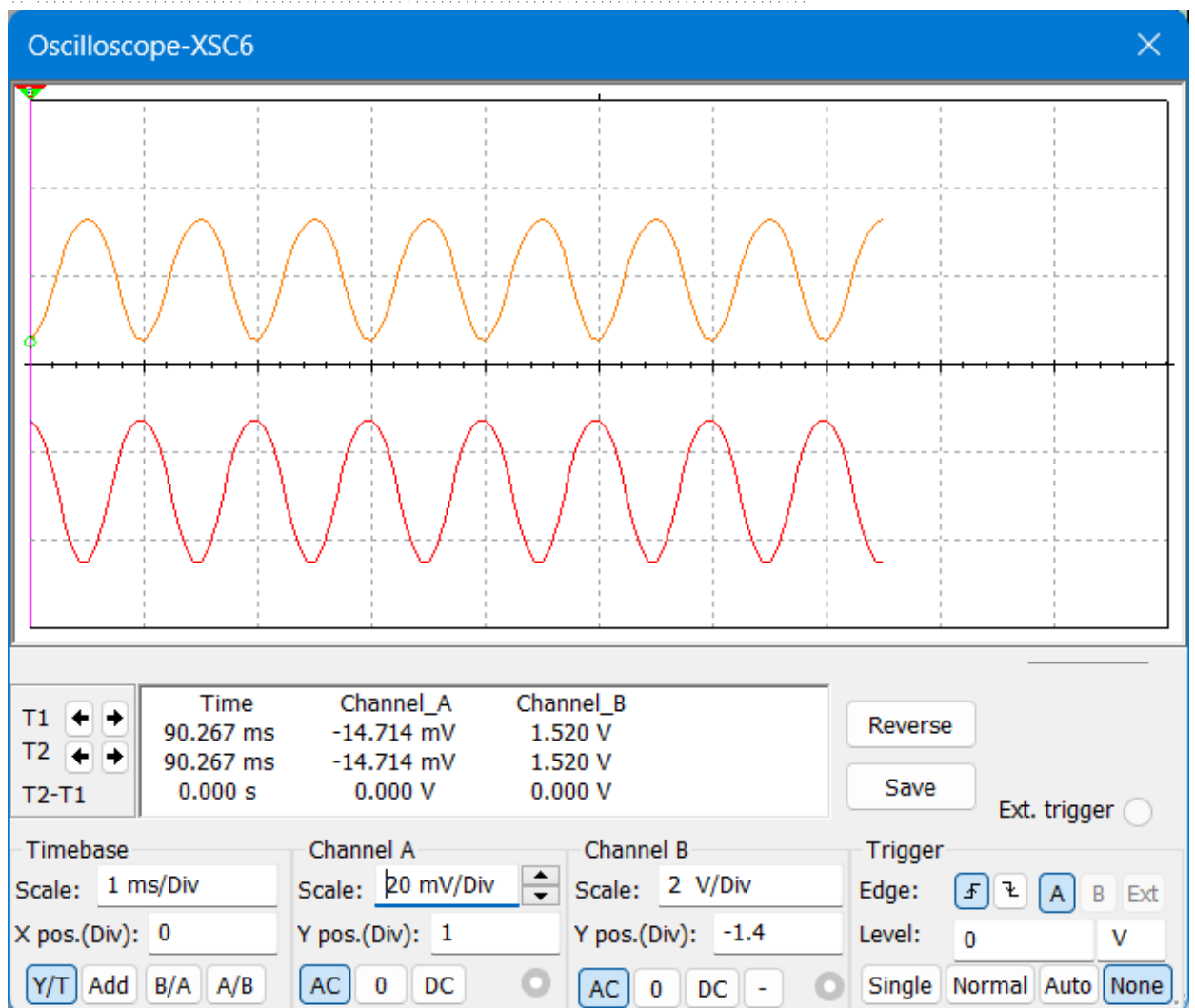
2) $R_s = 10\text{k}\Omega$



3) $R_s = 40k\Omega$



Conclusion: We can obtain faithful amplification by attenuating maximum portion of signal by placing a series resistance of $40k\Omega$ at input side.



HARDWARE SIMULATION:

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Apply the supply voltage , $V_{cc}=12V$
3. Make sure that the transistor is operating point in active region by keeping V_{CE} half of V_{CC} .
4. Now feed an ac signal of 20mV at the input of the amplifier with different frequencies ranging from 100Hz to 300 MHz and measure the amplifier output voltage.
5. Now calculate the gain in decibels at various input signal frequencies.
Draw a graph with frequencies on X-axis and gain in dBs on Y-axis.
From the graph calculate Bandwidth.

Observations:

Multistage CE amplifier without bypass capacitor

Frequency (in Hz)	Input (in mV)	Output (in mV)	Voltage Gain (dB)	
10				
50				
100				
200				
300				
500				
1k				Mid Frequency Gain
2k				
3k				
10k				
50k				
100k				
500k				
1G				
2G				
3G				