EXPERIMENT -7

HARTLEY OSCILLATOR

AIM: To design a Hartley Oscillator with following specifications and to verify the phase shift (180°) and find the frequency of oscillations.

DESIGN SPECIFICATIONS:

Vcc =12v, R1=18.3k, R2=6.8k, Re=1k, Rc=2.2k, L1=L2=1mH, C=1μF, NPN transistor with β value 100.

APPARATUS:

- CRO is
- Regulated DC power supply
- Decade resistance Box
- Decade capacitance Box
- Decade inductance Box
- Resistors
- Capacitors
- Transistor
- Bread board, Single strand wires

SOFTWARE SIMULATION:

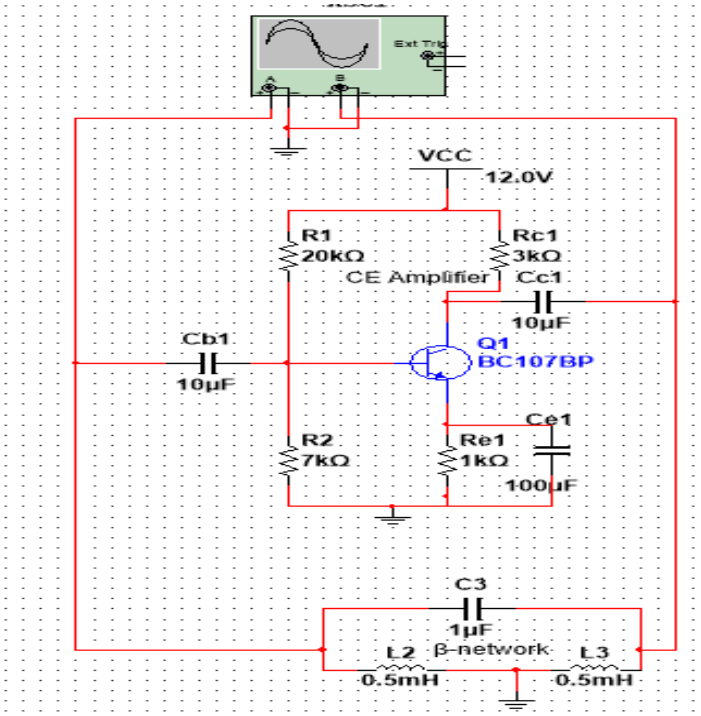
Software used: Multisim Analog Devices Edition 14.0

Procedure:

1. Switch ON the computer and open the Multisim software
2. Observe Design tool box, Instrumentation tool box, component tool box and its component functionality
3. From above tool boxes, Connect the circuit using the designed values of each and every component
4. Connect the output of amplifier to input of β-network[LC Combination] and output of β-network to input of amplifier.
5. Connect the Cathode Ray Oscilloscope (CRO) to the input and output terminals of the circuit.
6. Go to simulation button click it for simulation process.
7. From the CRO observe the following values:

- Frequency of Oscillations
- Phase Shift = 180^o

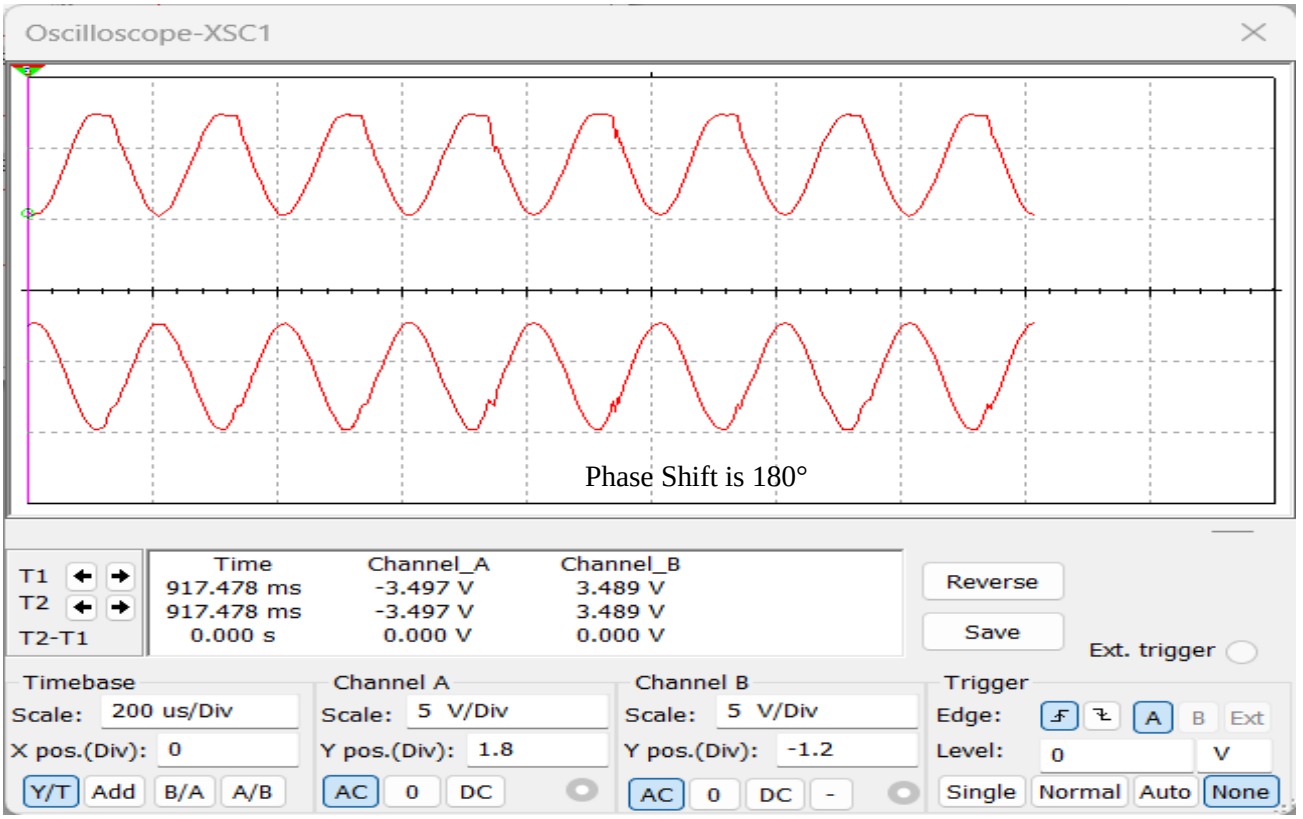
SIMULATION OF THE DESIGN:



Hartley Oscillator Circuit

- **OBSERVATIONS:**

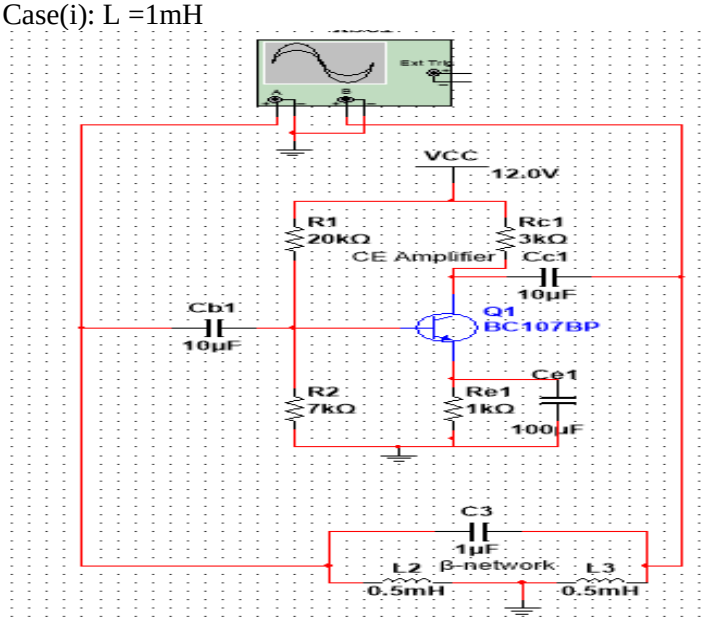
Phase Shift:

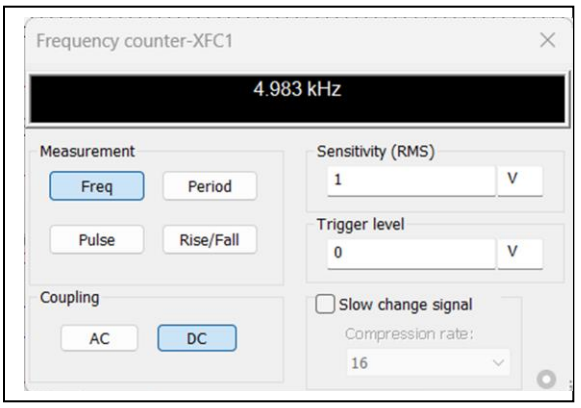


Conclusion:
From the above waveform we can conclude that the phase shift b/w input and output signal is 180°.

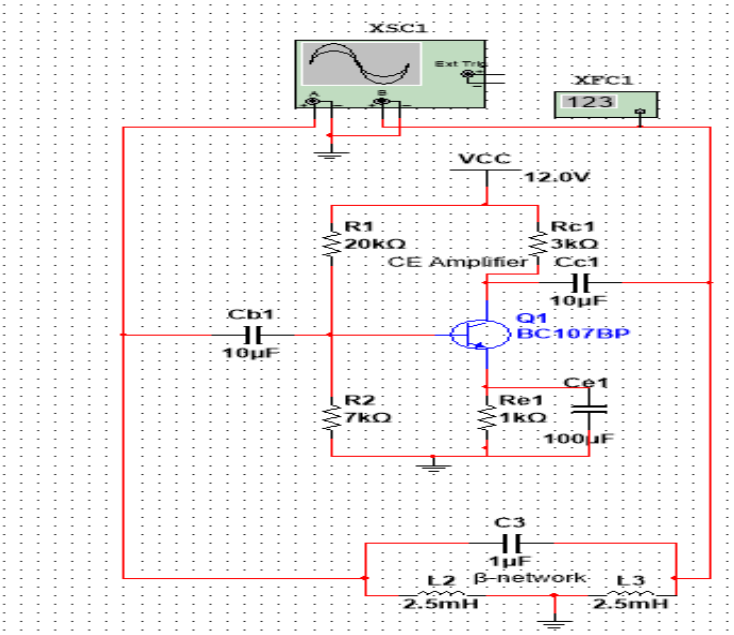
Frequency of Oscillations generated:

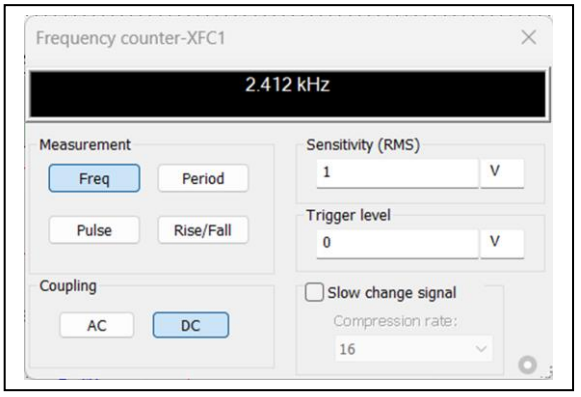
Case(i): L =1mH



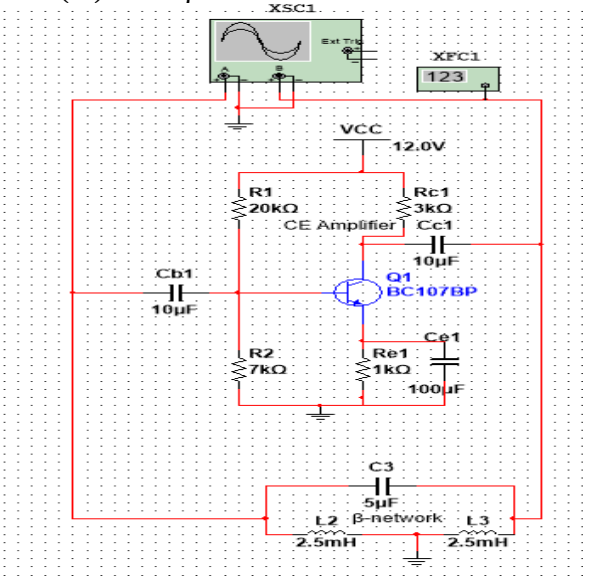


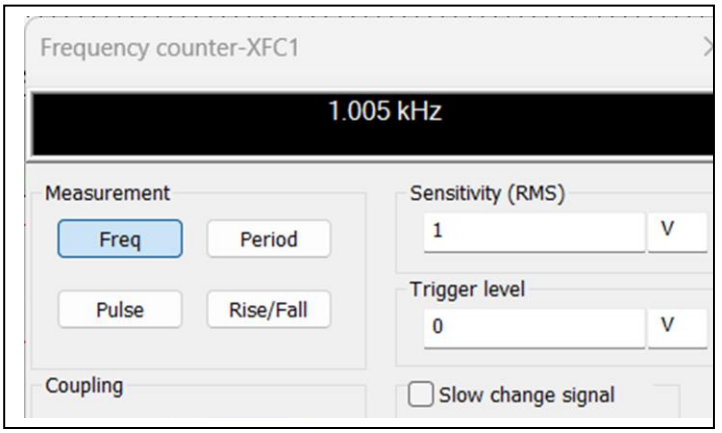
Case(ii): L=5mH





Case(iii): C = 5µF





Conclusion:

From the above values we can conclude that the frequency at which the oscillations are generated is decreased with increase in L and C.

HARDWARE SIMULATION:

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Apply the supply voltage , V_{cc}=12V
3. Make sure that the transistor is operating point in active region by keeping V_{CE} half of V_{CC}.
4. Now note down the frequency of oscillations generated for different inductance values.
5. Now calculate the theoretical frequency of oscillations generated.

Observations:

Hartley Oscillator

Inductance(H)	Frequency(Hz)
1m	15.2K
2m	10.8K
3m	8.8K
4m	7.7K
5m	6.9K
6m	6.2K
7m	5.8K
1	345.1
5	105.5
10	61.1
100	12.8

Conclusion: We can conclude that practically and through simulation we have obtained the frequency of Oscillations generated by the Hartley Oscillator and established a relation b/w the Frequency of oscillations and the L and C Values present in the feedback(β) network.