Voltage gains and frequency response of a Common-Emitter transistor

(with and without by-pass filter)

Aim: To design a Single stage CE amplifier with following specifications and to study the frequency response of amplifier, calculate voltage gain and bandwidth from the response.

Design Specifications:

V_{CC}= 12V, I_c= 2.5mA (2-3 mA), V_{CE}= 6V (half of max supply), A_v= 150, h_{fe} = 150, h_{ie} = 9KΩ, Silicon NPN transistor

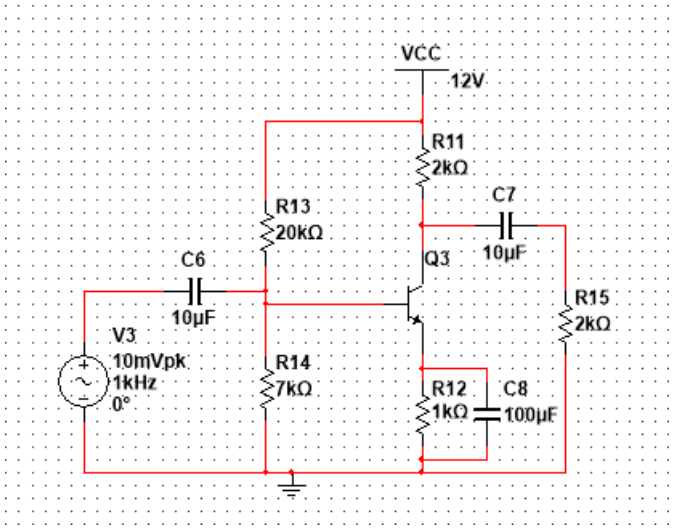
Software Simulation:

Procedure:

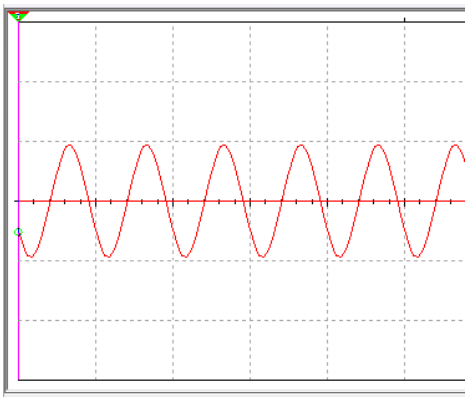
- Switch ON the computer and open the multi-sim 14.0 software.
- Check whether the icons of the instruments are activated and enabled.
- Now connect the circuit using the designed values of each and every component.
- Connect the function generator with sine wave of 50 mV p-p as input at the input terminals of the circuit.
- Connect the Cathode Ray Oscilloscope (CRO) to the output terminals of the circuit.
- Go to simulation button click it for simulation process.
- From the CRO readings, note the following values:
    1. Input voltage Vi
    2. Output voltage Vo
    3. Voltage gain Av
    4. Phase shift
- To study the frequency response use, bode plotter and calculate bandwidth.

Observations:

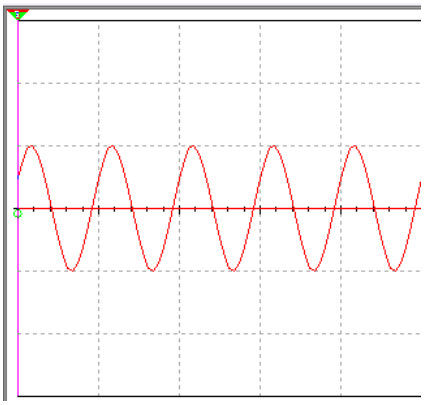
1. **Variation of voltage gain with change in load resistance** (R_L=2kΩ)



Circuit Diagram



Scale: 10mV/div *Input*



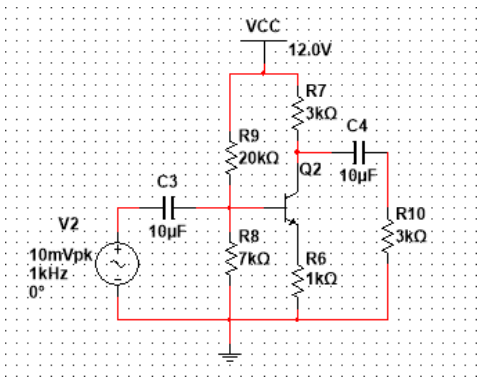
Output

Voltage gain = Vo/Vi

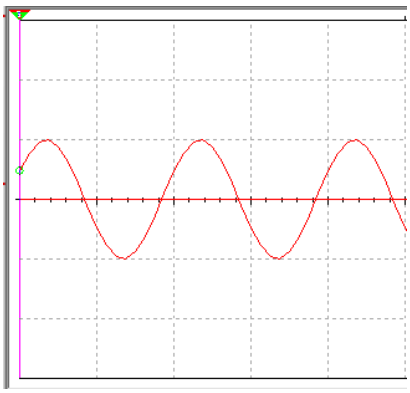
A_v = 20mV/20mV

A_v = 1

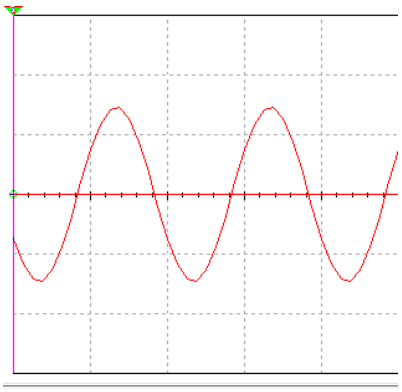
Case (ii): **R_L=3kΩ**



Circuit Diagram



Input



Output

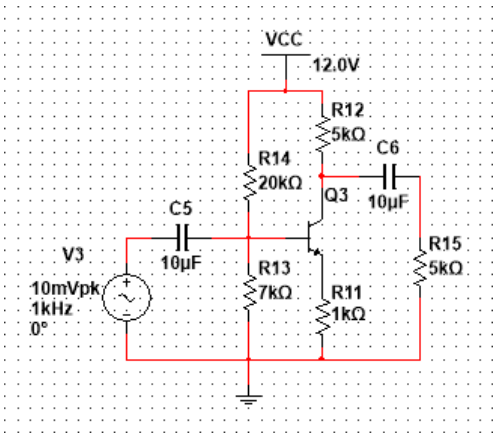
Scale: 10mV/div

Voltage gain = V_o/V_i

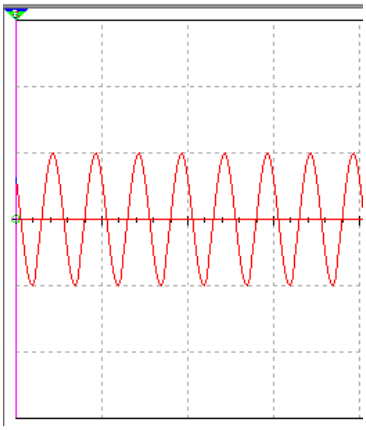
A_v = 30mV/20mV

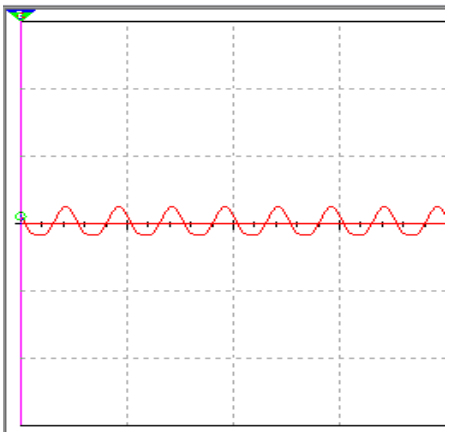
A_v = 1.5

Case (iii): R_L = 5kΩ



Circuit Diagram





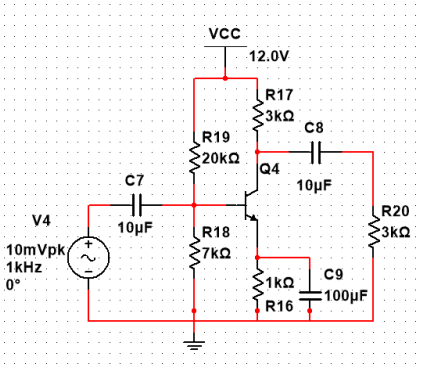
Scale: 10mV/div

Input *Output*

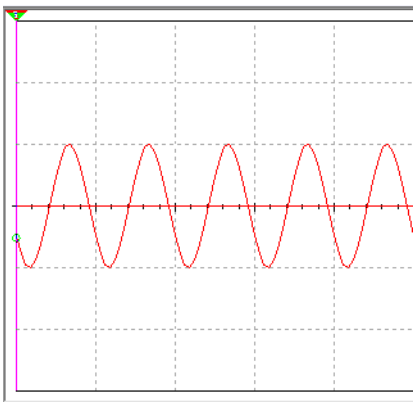
Conclusion:

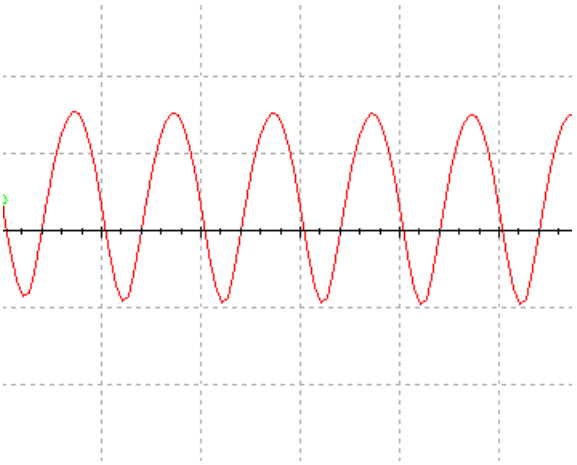
We can conclude from the situations above that voltage gain increases as pull-up resistance is increased. However, after a specific load resistance is reached, the gain drops off since the transistor is no longer operating in the active region. To increase voltage gain, we must lower draw down resistance.
The example with the best amplification for a 3k load resistance out of the first three is case (ii).

2. CE amplifier with by-pass capacitance:



Circuit Diagram





Input

Scale: 10mV/div

Output

Scale: 1V/div

Voltage gain = V_i/V_o

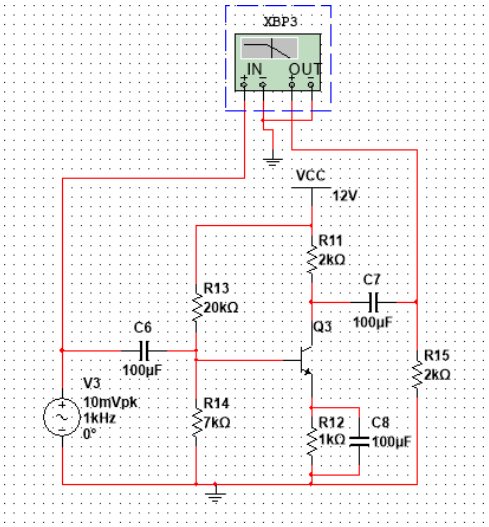
A_v = 2.5V/20mV

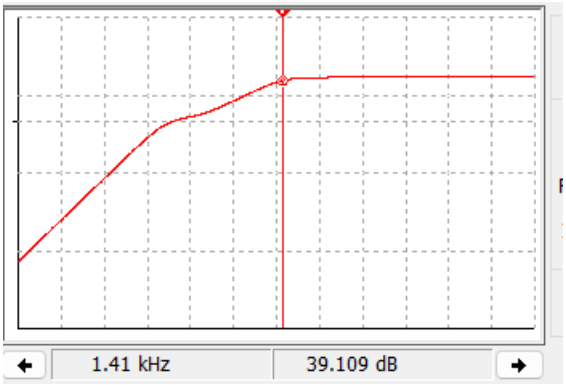
A_v=125

Conclusion:

The voltage gain rapidly rises from 1.5 to 125 as bypass capacitor is introduced.

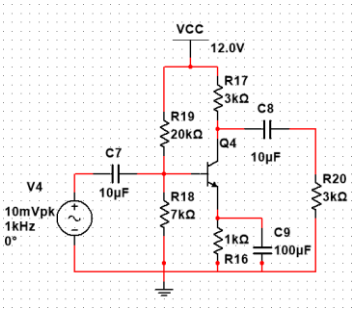
3. Variation of voltage gain with frequency and variation of cutoff frequencies with change in coupling capacitor of CE amplifier:

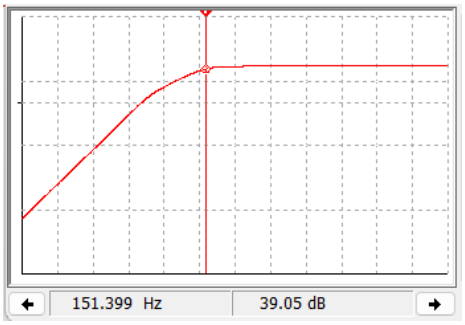




The lower cutoff frequency(f_L)=151.399Hz Coupling Capacitance=100uF
The voltage gain A_v = 42.022

The lower cutoff frequency(f_L)=1.41kHz. Coupling Capacitance=10uF
The voltage gain A_v = 42.022



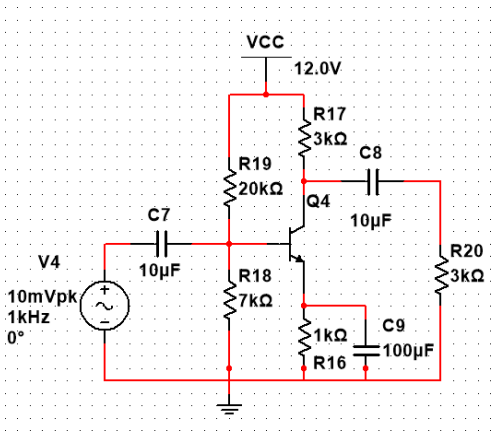


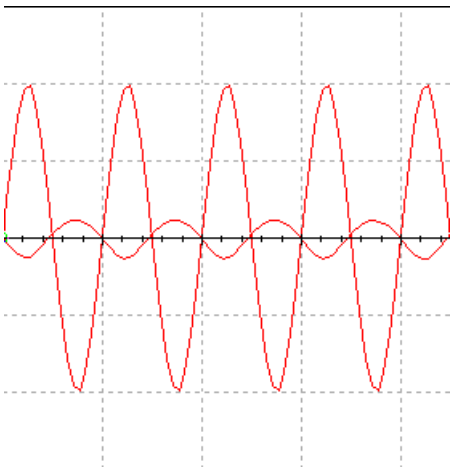
Conclusion:

The value of the bypass capacitor determines the cutoff frequency. As can be seen, the cutoff frequency in case 1 is almost 151 Hz, while it is 1.41 kHz in case 2. The range of coupling capacitor for a respectable cutoff frequency is about 10uF because higher cutoff frequencies are not preferred.

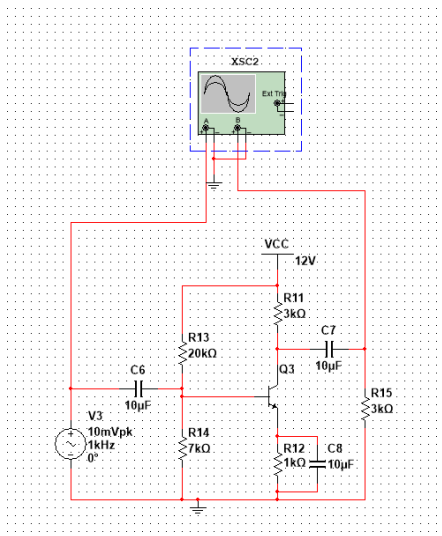
4. Variation of Phase-shift by by-pass capacitor:

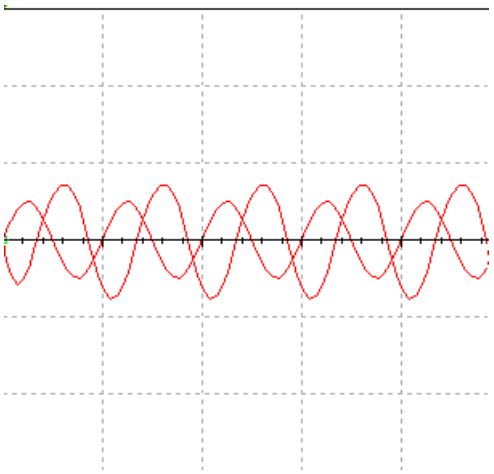
For by-pass capacitance = 100uF, phase shift is 180°





For by-pass capacitance = 10uF, phase shift is less than 180°





Conclusion:

The bypass capacitor will determine the phase shift of the amplifier; in case 1, it is 180^{o}, which is desired, and when we increase the bypass capacitor's value to 10uF, the phase shift decreases and the output signal becomes defective.

HARDWARE SIMULATION:

COMPONENTS & EQUIPMENTS REQUIRED:

S. No.	Apparatus	Range/ Rating	Quantity (in No's)
-	-	-	-
2	Cathode Ray Oscilloscope.	(0-20) MHz	1
3	Function Generator.	0.1 Hz-10 M	1

Observations:

CE amplifier without bypass capacitor

Frequency (in Hz)	Input (in mV)	Output (in mV)	Voltage Gain (dB)	
10	20	27	2.684	
50	20	29	3.303	
100	20	30	3.326	
200	20	30	3.332	
300	20	30	3.334	
500	20	30	3.334	
1k	20	30	3.334	
2k	20	30	3.334	
3k	20	30	3.334	
10k	20	30	3.334	
50k	20	30	3.334	
100k	20	30	3.334	
500k	20	30	3.334	
1G	20	30	3.334	
2G	20	30	3.334	
3G	20	30	3.334	

Mid Frequency Gain Av= 3.334;

Cut-off Frequency F_L= 4.9 Hz; F_H = - ; BW= - ;

CE amplifier with bypass capacitor

Frequency (in Hz)	Input (in mV)	Output (in mV)	Voltage Gain (dB)	
10	20	150	18.136	
50	20	800	31.922	
100	20	1350	36.902	
200	20	2000	40.182	
300	20	2250	41.07	
500	20	2400	41.654	
1k	20	2500	41.946	Mid Frequency Gain
2k	20	2500	42.019	
3k	20	2500	42.033	
10k	20	2500	42.043	
50k	20	2500	42.043	
100k	20	2500	42.043	
500k	20	2500	42.044	
1G	20	2500	42.044	
2G	20			
3G	20			

Mid Frequency Gain Av= 2500

Cut-off Frequency F_L=900 Hz; F_H = -; BW= -;

Result:

	Mid Freq Gain(design)	Mid Freq Gain (software)	Mid Freq Gain(hardware)
CE amplifier without bypass capacitor			
CE amplifier with bypass capacitor			