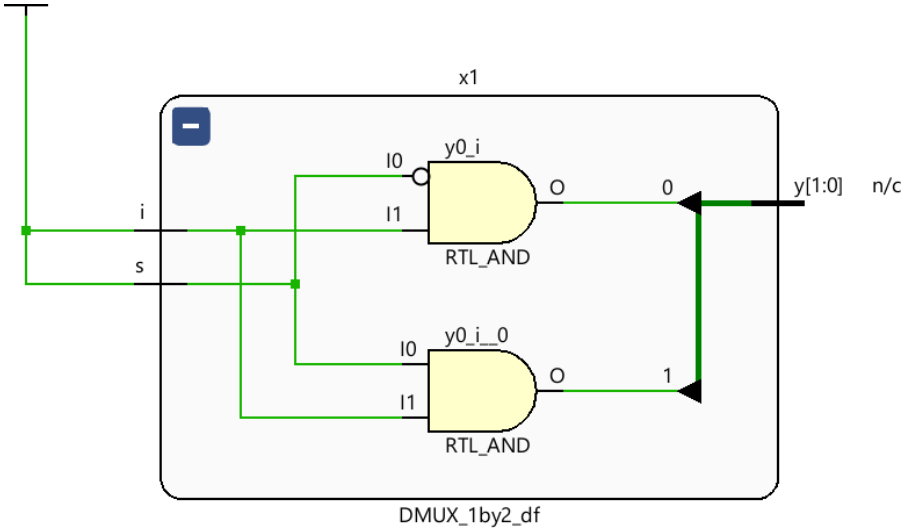
Demultiplexers (Data Flow Modeling)

1.1 AIM: 1x2 Demultiplexer [DMUX]

1.2 SOFTWARE USED: Xilinx Vivado 2022.2

1.3 SYMBOL:



1.4 LOGIC EXPRESSION:

$$Y_0 = (\sim S) \,\&\, i$$
$$Y_1 = S \,\&\, i$$

1.5 BOOLEAN EXPRESSION:

$$Y_0 = \overline{S}i$$
$$Y_1 = Si$$

1.6 TRUTH TABLE [Input Data: i]:

INPUT	OUTPUT	
S	**Y_0**	**Y_1**
0	**i**	**0**
1	**0**	**i**

1.7 VERILOG CODE (DMUX_1by2_df.v):

```
module DMUX_1by2_df(y,s,i);
input i;
input s;

output [1:0]y;

assign y[0] = (~s)&i;
assign y[1] = (s)&i;

endmodule
```

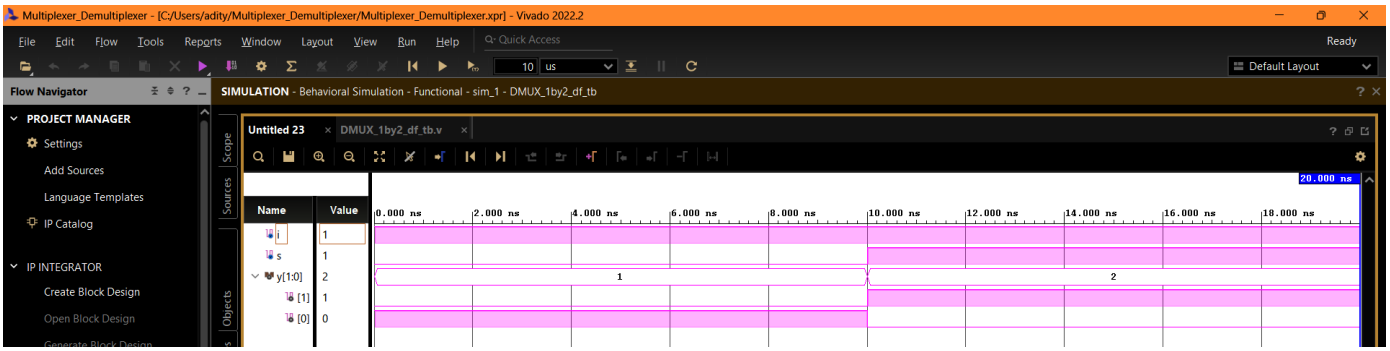
1.8 TEST BENCH (DMUX_1by2_df_tb.v):

```
module DMUX_1by2_df_tb();
reg i,s;
wire [1:0]y;

DMUX_1by2_df x1(y,s,i);

initial
begin
s=1'b0;i=1'b1;
#10 s=1'b1;i=1'b1;
#10 $finish;
end
endmodule
```

1.9 WAVEFORM:



1.10 RESULT:

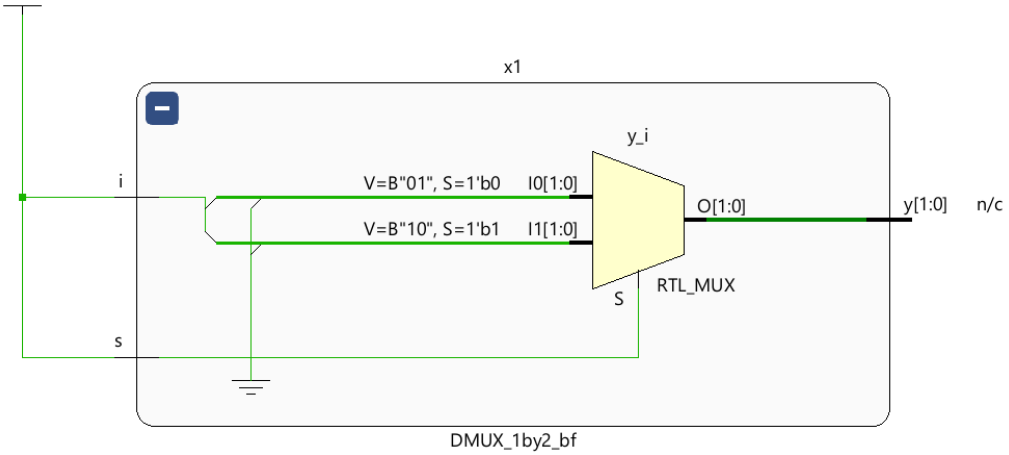
1x2 Demultiplexer is simulated and implemented in Data Flow Modeling.

Demultiplexers (Behavioral Flow Modeling)

1.1 AIM: 1x2 Demultiplexer [DMUX]

1.2 SOFTWARE USED: Xilinx Vivado 2022.2

1.3 SYMBOL:



1.4 LOGIC EXPRESSION:

$$Y_0 = (\sim S) \,\&\, i$$
$$Y_1 = S \,\&\, i$$

1.5 BOOLEAN EXPRESSION:

$$Y_0 = \overline{S}i$$
$$Y_1 = Si$$

1.6 TRUTH TABLE [Input Data: i]:

INPUT	OUTPUT	
S	**Y_0**	**Y_1**
0	**i**	**0**
1	**0**	**i**

1.7 VERILOG CODE (DMUX_1by2_bf.v):

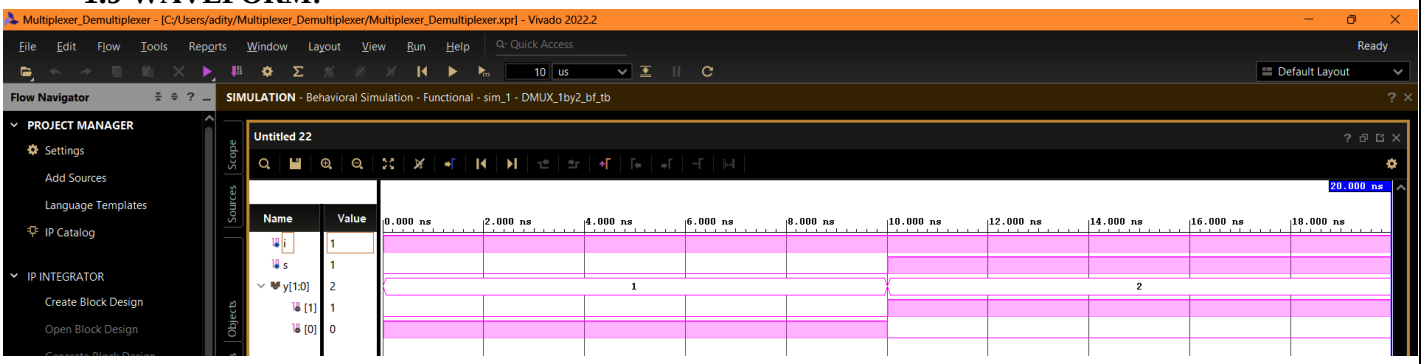
```
module DMUX_1by2_bf(y,s,i);
input i;
input s;
output [1:0]y;
reg [1:0]y;

always@(s,i)
case(s)
1'b0:begin y[0]=i;y[1]=0;end
1'b1:begin y[0]=0;y[1]=i;end
endcase
endmodule
```

1.8 TEST BENCH (DMUX_1by2_bf_tb.v):

```
module DMUX_1by2_bf_tb();
reg i,s;
wire [1:0]y;
DMUX_1by2_bf x1(y,s,i);
initial
begin
s=1'b0;i=1'b1;
#10 s=1'b1;i=1'b1;
#10 $finish;
end
endmodule
```

1.9 WAVEFORM:



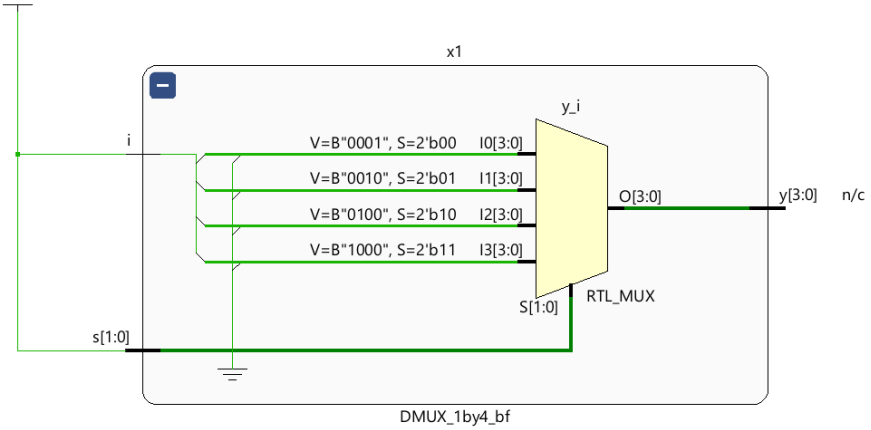
1.10 RESULT:

1x2 Demultiplexer is simulated and implemented in Behavioral Flow Modeling.

1.1 AIM: 1x4 Demultiplexer [DMUX]

1.2 SOFTWARE USED: Xilinx Vivado 2022.2

1.3 SYMBOL:



1.4 LOGIC EXPRESSION:

$$Y_0 = (\sim S_1)\&(\sim S_0)\ \&\ i$$
$$Y_1 = (\sim S_1)\&(S_0)\ \&\ i$$
$$Y_2 = (S_1)\&(\sim S_0)\ \&\ i$$
$$Y_3 = (S_1)\&(S_0)\ \&\ i$$

1.5 BOOLEAN EXPRESSION:

$$Y_0 = \overline{S_1}\,\overline{S_0} i$$
$$Y_1 = \overline{S_1} S_0 i$$
$$Y_2 = S_1 \overline{S_0} i$$
$$Y_3 = S_1 S_0 i$$

1.6 TRUTH TABLE:

INPUT		OUTPUT			
S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	0	i	0	0	0
0	1	0	i	0	0
1	0	0	0	i	0
1	1	0	0	0	i

1.7 VERILOG CODE (DMUX_1by4_bf.v):

```
module DMUX_1by4_bf(y,s,i);
input i;
input [1:0]s;
output [3:0]y;
reg [3:0]y;
always@(s,i)
case(s)
2'b00:begin y=0;y[0]=i;end
2'b01:begin y=0;y[1]=i;end
2'b10:begin y=0;y[2]=i;end
2'b11:begin y=0;y[3]=i;end
endcase
endmodule
```

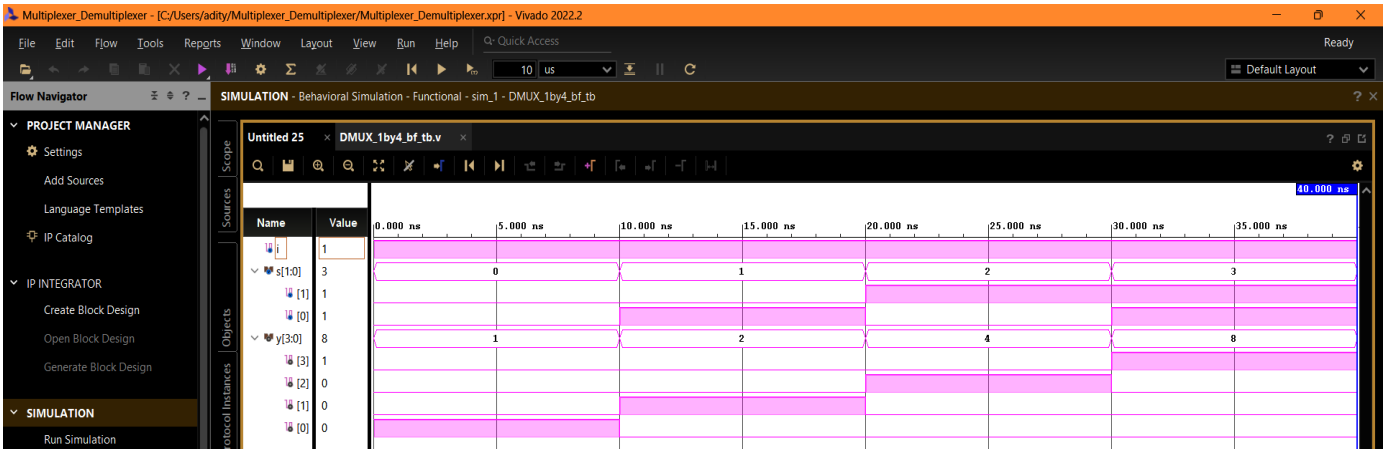
1.8 TEST BENCH (DMUX_1by4_bf_tb.v):

```
module DMUX_1by4_bf_tb();
reg i;
reg [1:0]s;
wire [3:0]y;

DMUX_1by4_bf x1(y,s,i);

initial
begin
s=2'b00;i=1'b1;
#10 s=2'b01;i=1'b1;
#10 s=2'b10;i=1'b1;
#10 s=2'b11;i=1'b1;
#10 $finish;
end
endmodule
```

1.9 WAVEFORM:



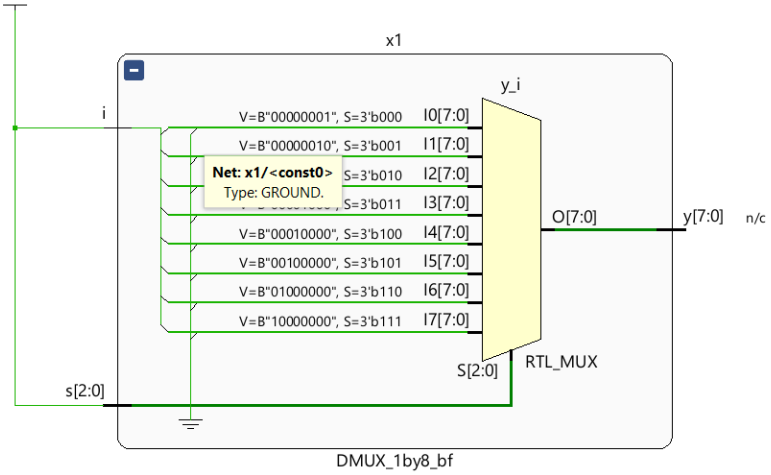
1.10 RESULT:

1x4 Demultiplexer is simulated and implemented in Behavioral Flow Modeling.

1.1 AIM: 1x8 Demultiplexer [DMUX]

1.2 SOFTWARE USED: Xilinx Vivado 2022.2

1.3 SYMBOL:



1.4 LOGIC EXPRESSION:

$Y_0 = (\sim S_2)\&(\sim S_1)\&(\sim S_0)\ \&\ i$
$Y_1 = (\sim S_2)\&(\sim S_1)\&(S_0)\ \&\ i$
$Y_2 = (\sim S_2)\&(S_1)\&(\sim S_0)\ \&\ i$
$Y_3 = (\sim S_2)\&(S_1)\&(S_0)\ \&\ i$
$Y_4 = (S_2)\&(\sim S_1)\&(\sim S_0)\ \&\ i$
$Y_5 = (S_2)\&(S_1)\&(\sim S_0)\ \&\ i$
$Y_6 = (S_2)\&(S_1)\&(\sim S_0)\ \&\ i$
$Y_7 = (S_2)\&(S_1)\&(S_0)\ \&\ i$

1.5 BOOLEAN EXPRESSION:

$Y_0 = \overline{S_2}\,\overline{S_1}\,\overline{S_0}i$
$Y_1 = \overline{S_2}\,\overline{S_1}S_0i$
$Y_2 = \overline{S_2}S_1\overline{S_0}i$
$Y_3 = \overline{S_2}S_1S_0i$
$Y_4 = S_2\overline{S_1}\,\overline{S_0}i$
$Y_5 = S_2\overline{S_1}S_0i$
$Y_6 = S_2S_1\overline{S_0}i$
$Y_7 = S_2S_1S_0i$

1.6 TRUTH TABLE:

INPUT			OUTPUT							
S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	i	0	0	0	0	0	0	0
0	0	1	0	i	0	0	0	0	0	0
0	1	0	0	0	i	0	0	0	0	0
0	1	1	0	0	0	i	0	0	0	0
1	0	0	0	0	0	0	i	0	0	0
1	0	1	0	0	0	0	0	i	0	0
1	1	0	0	0	0	0	0	0	i	0
1	1	1	0	0	0	0	0	0	0	i

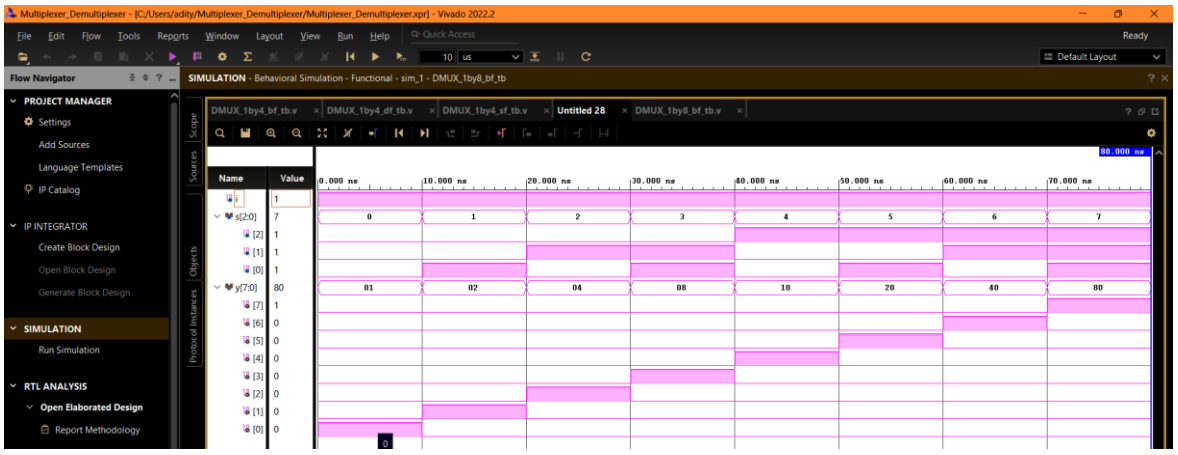
1.7 VERILOG CODE (DMUX_1by8_bf.v):

```
module DMUX_1by8_bf(y,s,i);
input i;
input [2:0]s;
output [7:0]y;
reg [7:0]y;
always@(s,i)
case(s)
3'b000:begin y=0;y[0]=i;end
3'b001:begin y=0;y[1]=i;end
3'b010:begin y=0;y[2]=i;end
3'b011:begin y=0;y[3]=i;end
3'b100:begin y=0;y[4]=i;end
3'b101:begin y=0;y[5]=i;end
3'b110:begin y=0;y[6]=i;end
3'b111:begin y=0;y[7]=i;end
endcase
endmodule
```

1.8 TEST BENCH (DMUX_1by8_bf_tb.v):

```
module DMUX_1by8_bf_tb();
reg i;
reg [2:0]s;
wire [7:0]y;
DMUX_1by8_bf x1(y,s,i);
initial
begin
s=3'b000;i=1'b1;
#10 s=3'b001;i=1'b1;
#10 s=3'b010;i=1'b1;
#10 s=3'b011;i=1'b1;
#10 s=3'b100;i=1'b1;
#10 s=3'b101;i=1'b1;
#10 s=3'b110;i=1'b1;
#10 s=3'b111;i=1'b1;
#10 $finish;
end
endmodule
```

1.9 WAVEFORM:



1.10 RESULT:

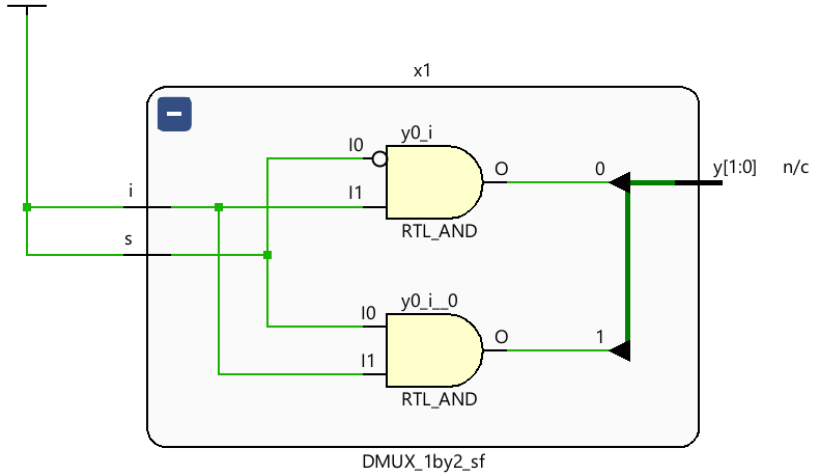
1x8 Demultiplexer is simulated and implemented in Behavioral Flow Modeling

Demultiplexers (Structural Flow Modeling)

1.1 AIM: 1x2 Demultiplexer [DMUX]

1.2 SOFTWARE USED: Xilinx Vivado 2022.2

1.3 SYMBOL:



1.4 LOGIC EXPRESSION:

$$Y_0 = (\sim S) \,\&\, i$$
$$Y_1 = S \,\&\, i$$

1.5 BOOLEAN EXPRESSION:

$$Y_0 = \overline{S}i$$
$$Y_1 = Si$$

1.6 TRUTH TABLE [Input Data: i]:

INPUT	OUTPUT	
S	**Y_0**	**Y_1**
0	**i**	**0**
1	**0**	**i**

1.7 VERILOG CODE (DMUX_1by2_sf.v):

```
module DMUX_1by2_sf(y,s,i);
input i;
input s;
output [1:0]y;
wire [1:0]y;

and (y[0],(~s),i);
and (y[1],(s),i);

endmodule
```

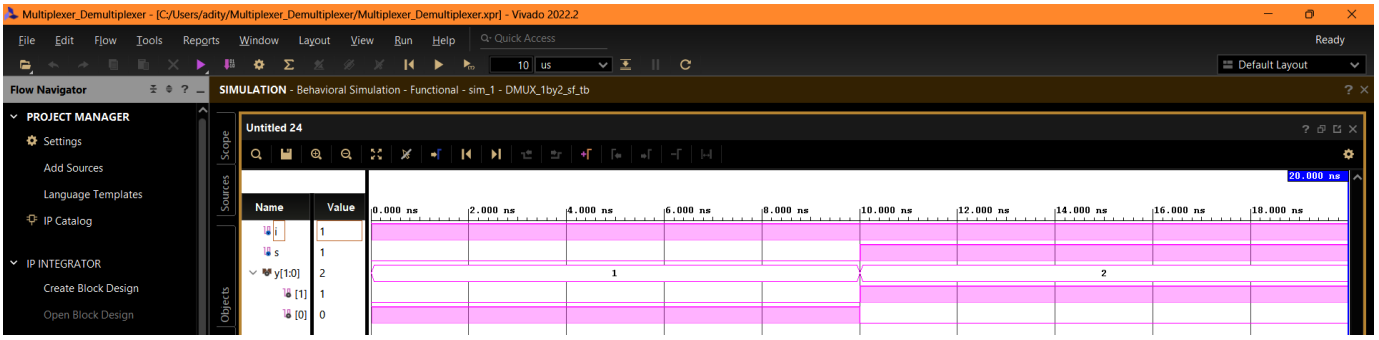
1.8 TEST BENCH (DMUX_1by2_sf_tb.v):

```
module DMUX_1by2_sf_tb();
reg i,s;
wire [1:0]y;

DMUX_1by2_sf x1(y,s,i);

initial
begin
s=1'b0;i=1'b1;
#10 s=1'b1;i=1'b1;
#10 $finish;
end
endmodule
```

1.9 WAVEFORM:



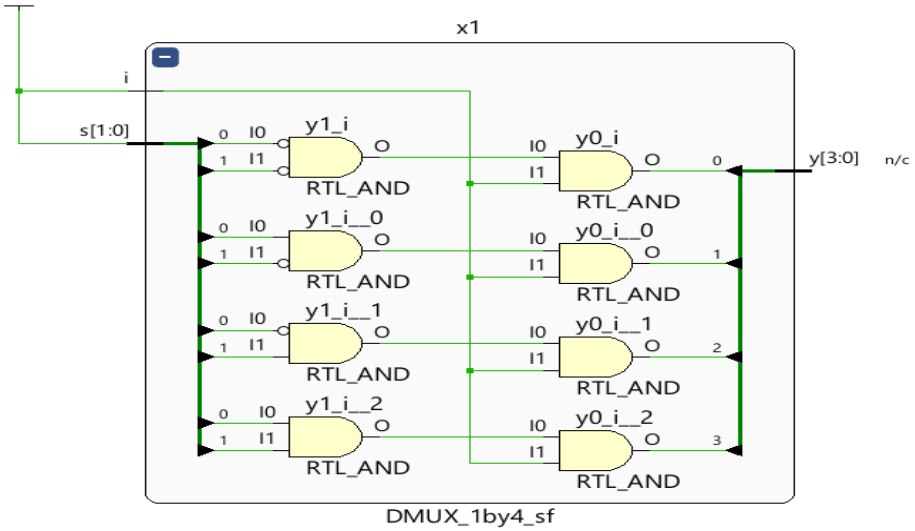
1.10 RESULT:

1x2 Demultiplexer is simulated and implemented in Structural Flow Modeling.

1.6 AIM: 1x4 Demultiplexer [DMUX]

1.7 SOFTWARE USED: Xilinx Vivado 2022.2

1.8 SYMBOL:



1.9 LOGIC EXPRESSION:

$$Y_0 = (\sim S_1)\&(\sim S_0)\ \&\ i$$
$$Y_1 = (\sim S_1)\&(S_0)\ \&\ i$$
$$Y_2 = (S_1)\&(\sim S_0)\ \&\ i$$
$$Y_3 = (S_1)\&(S_0)\ \&\ i$$

1.2 BOOLEAN EXPRESSION:

$$Y_0 = \overline{S_1}\,\overline{S_0}i$$
$$Y_1 = \overline{S_1}S_0i$$
$$Y_2 = S_1\overline{S_0}i$$
$$Y_3 = S_1S_0i$$

1.10 TRUTH TABLE:

INPUT		OUTPUT			
S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	0	i	0	0	0
0	1	0	i	0	0
1	0	0	0	i	0
1	1	0	0	0	i

1.7 VERILOG CODE (DMUX_1by4_sf.v):

```
module DMUX_1by4_sf(y,s,i);
input i;
input [1:0]s;
output [3:0]y;
wire [3:0]y;

 and (y[0],~s[0],~s[1],i);
 and (y[1],s[0],~s[1],i);
and (y[2],~s[0],s[1],i);
and (y[3],s[0],s[1],i);
endmodule
```

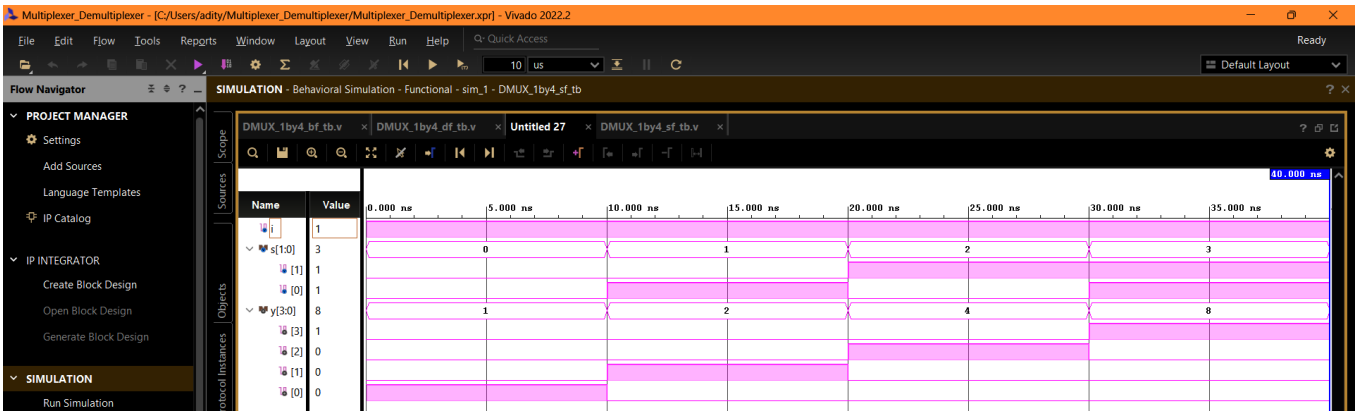
1.11 TEST BENCH (DMUX_1by4_sf_tb.v):

```
module DMUX_1by4_sf_tb();
reg i;
reg [1:0]s;
wire [3:0]y;

DMUX_1by4_sf x1(y,s,i);

initial
begin
s=2'b00;i=1'b1;
#10 s=2'b01;i=1'b1;
#10 s=2'b10;i=1'b1;
#10 s=2'b11;i=1'b1;
#10 $finish;
end
endmodule
```

1.12 WAVEFORM:



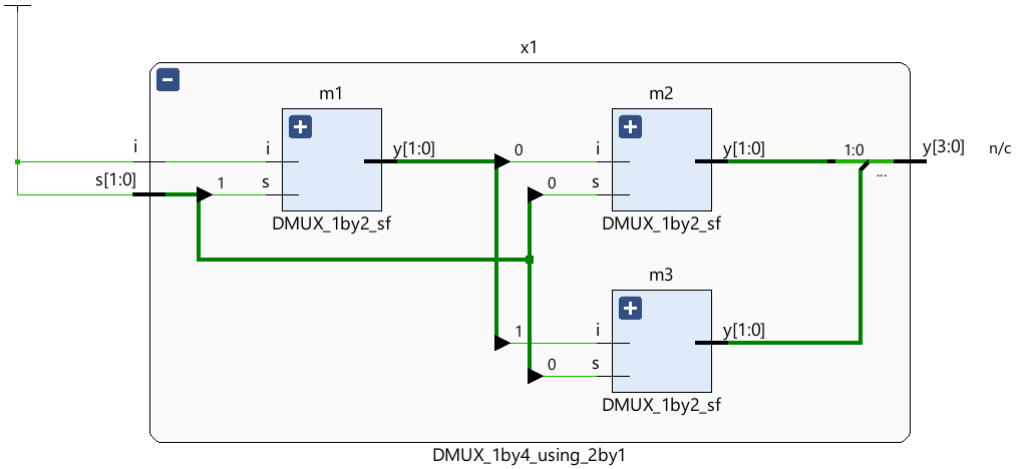
1.13 RESULT:

1x4 Demultiplexer is simulated and implemented in Structural Flow Modeling.

1.1 AIM: 1x4 Demultiplexer using 1x2 Demultiplexer

1.2 SOFTWARE USED: Xilinx Vivado 2022.2

1.3 SYMBOL:



1.4 LOGIC EXPRESSION:

$$Y_0 = (\sim S_1)\&(\sim S_0)\ \&\ i$$
$$Y_1 = (\sim S_1)\&(S_0)\ \&\ i$$
$$Y_2 = (S_1)\&(\sim S_0)\ \&\ i$$
$$Y_3 = (S_1)\&(S_0)\ \&\ i$$

1.1 BOOLEAN EXPRESSION:

$$Y_0 = \overline{S_1}\,\overline{S_0}i$$
$$Y_1 = \overline{S_1}S_0i$$
$$Y_2 = S_1\overline{S_0}i$$
$$Y_3 = S_1S_0i$$

1.5 TRUTH TABLE:

INPUT		OUTPUT			
S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	0	i	0	0	0
0	1	0	i	0	0
1	0	0	0	i	0
1	1	0	0	0	i

1.7 VERILOG CODE (DMUX_1by4_using_2by1.v):

```
module DMUX_1by4_using_2by1(y,s,i);
input i;
input [1:0]s;
output [3:0]y;

wire [1:0]a;

DMUX_1by2_sf m1(a,s[1],i);
DMUX_1by2_sf m2(y[1:0],s[0],a[0]);
DMUX_1by2_sf m3(y[3:2],s[0],a[1]);

endmodule
```

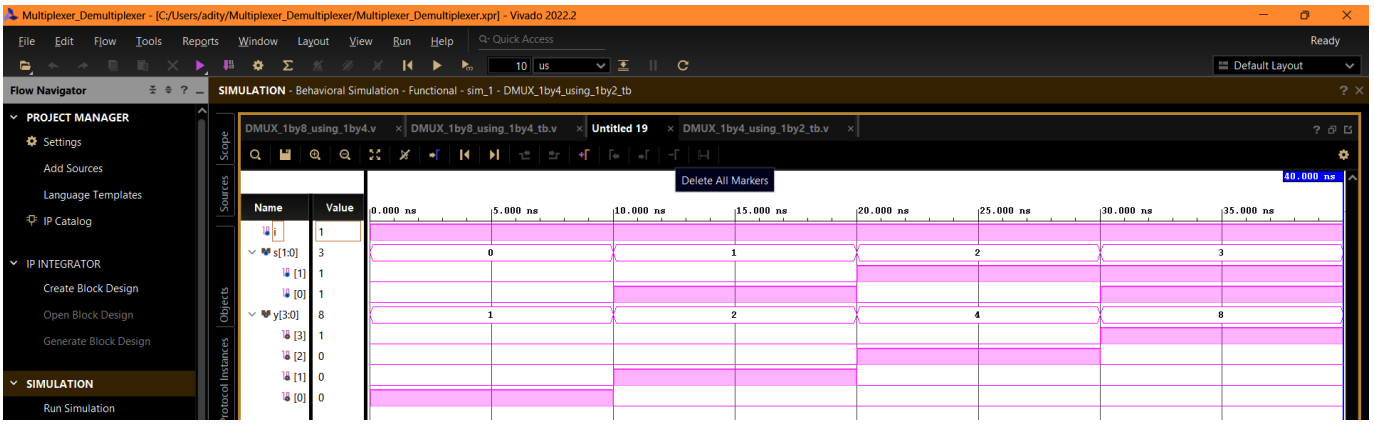
1.8 TEST BENCH (DMUX_1by4_using_2by1_tb.v):

```
module DMUX_1by4_using_1by2_tb();
reg i;
reg [1:0]s;
wire [3:0]y;

DMUX_1by4_using_2by1 x1(y,s,i);

initial
begin
s=2'b00;i=1'b1;
#10 s=2'b01;i=1'b1;
#10 s=2'b10;i=1'b1;
#10 s=2'b11;i=1'b1;
#10 $finish;
end
endmodule
```

1.9 WAVEFORM:



1.10 RESULT:

1x4 Demultiplexer using 1x2 Demultiplexer is simulated and implemented