5

## EXPERIMENT-5
## REALIZATION OF COMPARATORS

1. **AIM:** To Design, simulate and implement Comparators in 3 different modeling styles(Data Flow, Behavioral Flow Modeling, Structural Flow Modeling)

2. **SOFTWARE USED:** Xilinx Vivado 2022.2

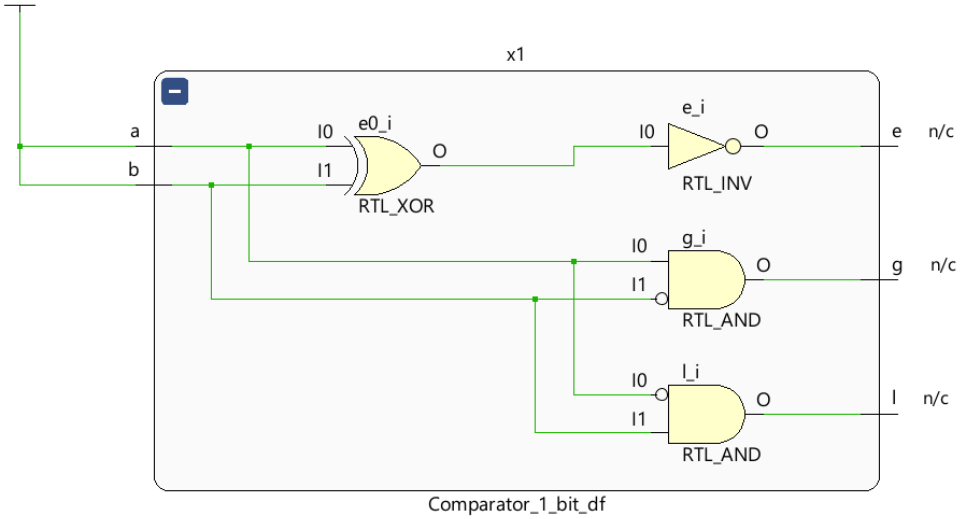
3. **PROCEDURE:**
    - Open the Xilinx Vivado project navigator.
    - Open the Design source and go to add / create sources
    - Create new file, give appropriate name save it.
    - Open the file in the editor and write the Verilog code.
    - Open the Design source and go to add / create sources to create the test bench
    - Open the editor and write the Verilog code for test bench.
    - After completion of Verilog code set your test bench as top module in simulation settings and Run Simulation.
    - To view RTL schematic, select RTL Analysis in which select open elaborate design, select Schematic.

## Comparators (Data Flow Modeling)

**1.1 AIM:** 1 Bit Comparator

**1.2 SOFTWARE USED:** Xilinx Vivado 2022.2

**1.3 SYMBOL:**




**1.4 LOGIC EXPRESSION:**

E = ~ (A^B)
G = (~B) & A
L = (~A) & B

**1.5 BOOLEAN EXPRESSION:**

$E = \bar{A}\bar{B} + AB$
$G = A\bar{B}$
$L = \bar{A}B$

**1.6 TRUTH TABLE:**

| INPUT | | OUTPUT | | |
|---|---|---|---|---|
| **A** | **B** | **E[$\sum_m$=(0,3)]** | **G[$\sum_m$=(2)]** | **L[$\sum_m$=(1)]** |
| **0** | **0** | **1** | **0** | **0** |
| **0** | **1** | **0** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **1** | **1** | **0** | **0** |

**2.1 VERILOG CODE (Comparator_1_bit_df.v):**

```
module Comparator_1_bit_df(e,g,l,a,b);
output e,g,l;
input a,b;

assign e = ~(a^b);  // XNOR Gate
assign g = a&(~b);
assign l = (~a)&b;

endmodule
```

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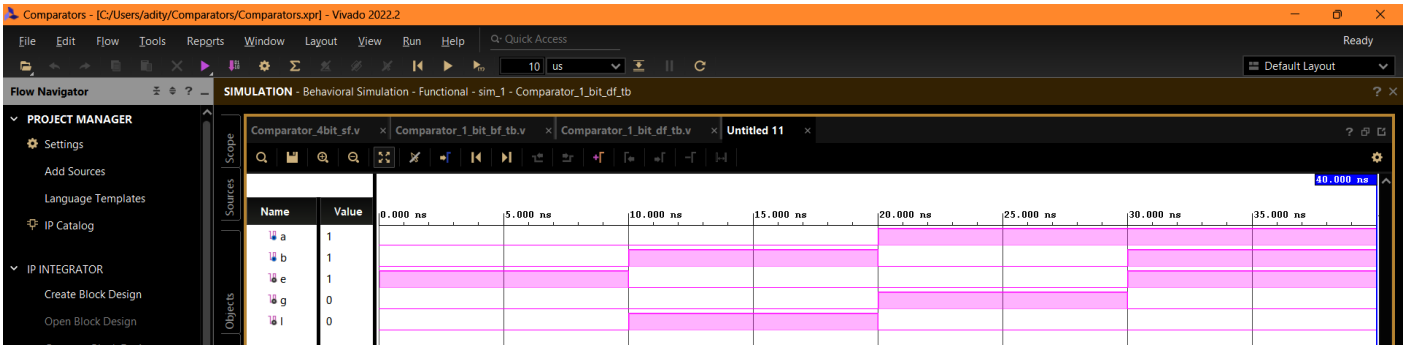
## 1.8 TEST BENCH (Comparator_1_bit_df _tb.v):

```
module Comparator_1_bit_df_tb();
reg a,b;
wire e,g,l;
Comparator_1_bit_df x1(e,g,l,a,b);
initial
begin
a=1'b0;b=1'b0;
#10 a=1'b0;b=1'b1;
#10 a=1'b1;b=1'b0;
#10 a=1'b1;b=1'b1;
#10 $finish;
end
endmodule
```

## 1.9 WAVEFORM:




## 1.10 RESULT:

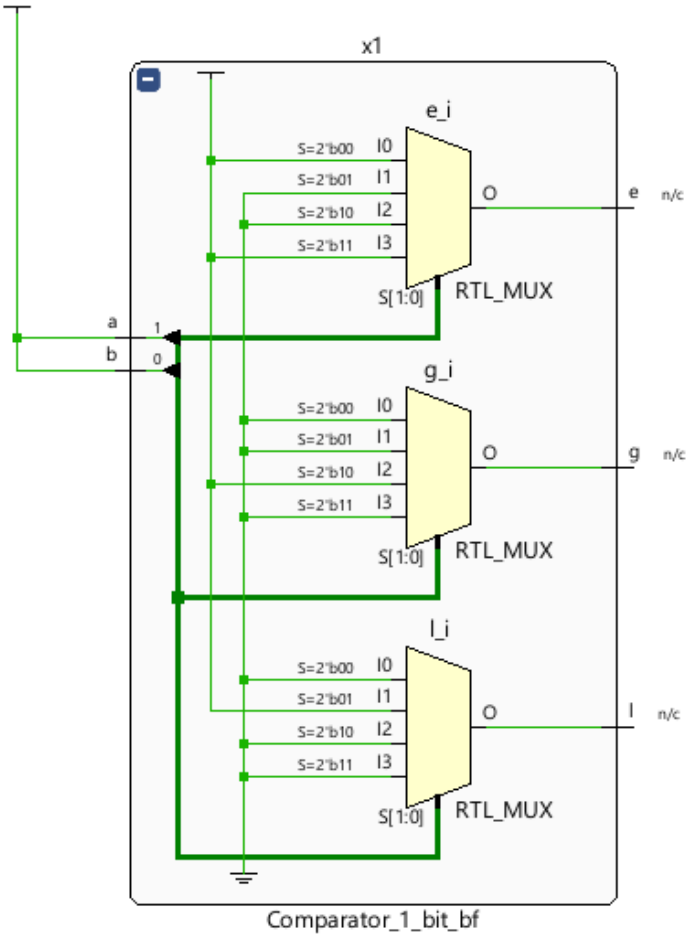
1 Bit Comparator is simulated and implemented in Data Flow Modeling.

**Comparators (Behavioral Flow Modeling)**

**1.1 AIM:** 1 Bit Comparator

**1.2 SOFTWARE USED:** Xilinx Vivado 2022.2

**1.3 SYMBOL:**




**1.4 LOGIC EXPRESSION:**

E = ~ (A^B)
G = (~B) & A
L = (~A) & B

**1.5 BOOLEAN EXPRESSION:**

$E = \bar{A}\bar{B} + AB$
$G = A\bar{B}$
$L = \bar{A}B$

**1.6 TRUTH TABLE:**

| INPUT | | OUTPUT | | |
|---|---|---|---|---|
| **A** | **B** | **E[$\sum_m$=(0,3)]** | **G[$\sum_m$=(2)]** | **L[$\sum_m$=(1)]** |
| **0** | **0** | **1** | **0** | **0** |
| **0** | **1** | **0** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **1** | **1** | **0** | **0** |

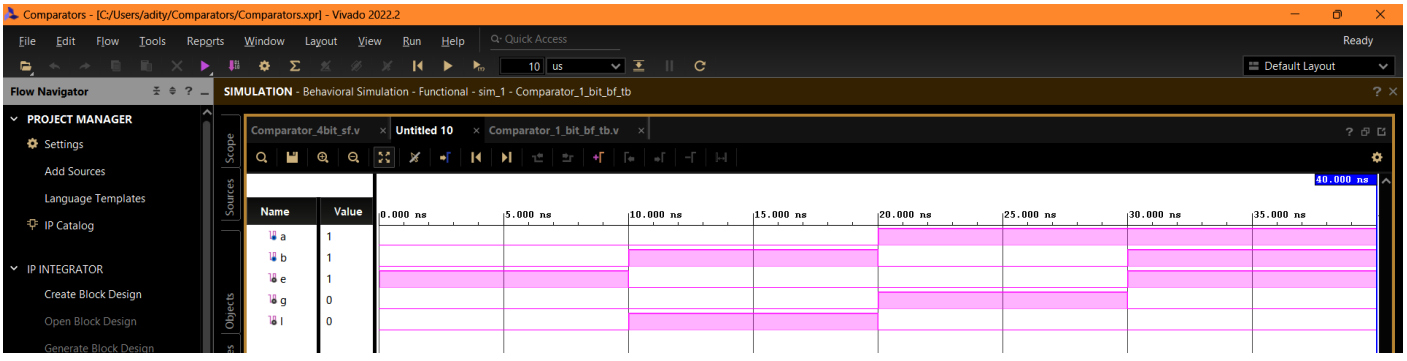
### 1.7 VERILOG CODE (Comparator_1_bit_bf.v):

```
module Comparator_1_bit_bf(e,g,l,a,b);
output e,g,l;
input a,b;
reg e,g,l;
always@(a,b)
case({a,b})
2'b00:begin e=1;g=0;l=0; end
2'b01:begin e=0;g=0;l=1; end
2'b10:begin e=0;g=1;l=0; end
2'b11:begin e=1;g=0;l=0; end
default:begin e=0;g=0;l=0; end
endcase
endmodule
```

### 1.8 TEST BENCH (Comparator_1_bit_bf _tb.v):

```
module Comparator_1_bit_df_tb();
reg a,b;
wire e,g,l;
Comparator_1_bit_bf x1(e,g,l,a,b);
initial
begin
a=1'b0;b=1'b0;
#10 a=1'b0;b=1'b1;
#10 a=1'b1;b=1'b0;
#10 a=1'b1;b=1'b1;
#10 $finish;
end
endmodule
```

### 1.9 WAVEFORM:




### 1.10 RESULT:

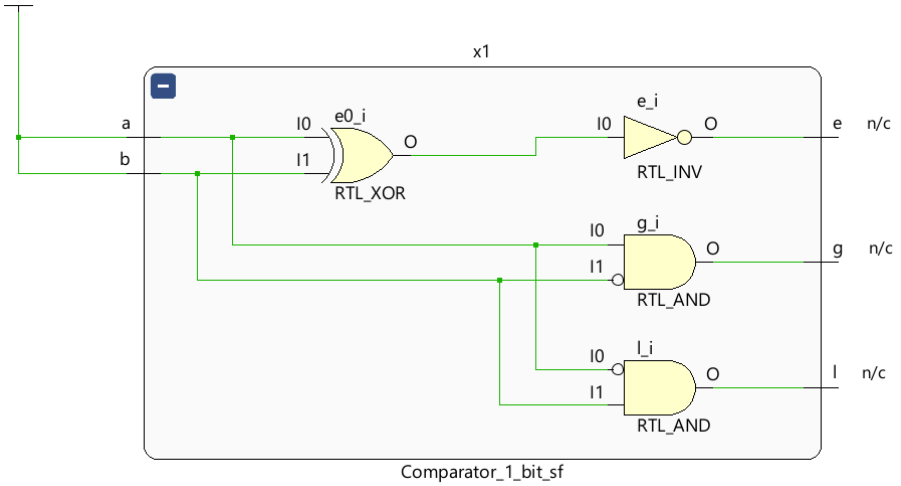
1 Bit Comparator is simulated and implemented in Behavioral Flow Modeling.

## Comparators(Structural Flow Modeling)

**1.1 AIM:** 1 Bit Comparator

**1.2 SOFTWARE USED:** Xilinx Vivado 2022.2

**1.3 SYMBOL:**




**1.4 LOGIC EXPRESSION:**

E = ~ (A^B)
G = (~B) & A
L = (~A) & B

**1.5 BOOLEAN EXPRESSION:**

$E = \bar{A}\bar{B} + AB$
$G = A\bar{B}$
$L = \bar{A}B$

**1.6 TRUTH TABLE:**

| INPUT | | OUTPUT | | |
|---|---|---|---|---|
| **A** | **B** | **E[$\sum_m$=(0,3)]** | **G[$\sum_m$=(2)]** | **L[$\sum_m$=(1)]** |
| **0** | **0** | **1** | **0** | **0** |
| **0** | **1** | **0** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **1** | **1** | **0** | **0** |

**1.7 VERILOG CODE (Comparator_1_bit_sf.v):**

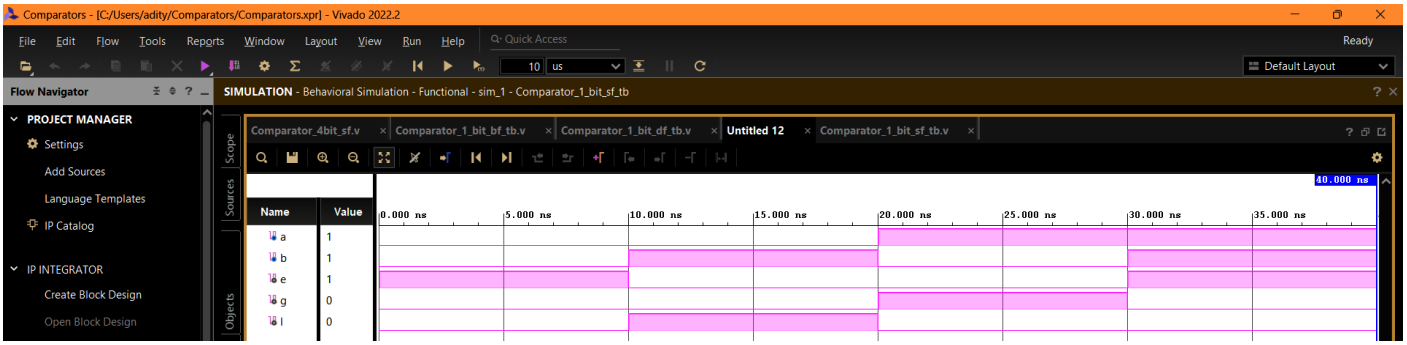
```
module Comparator_1_bit_sf(e,g,l,a,b);
output e,g,l;
input a,b;

xnor (e,a,b);
and (g,a,~b);
and (l,~a,b);
endmodule
```

## 1.8 TEST BENCH (Comparator_1_bit_sf _tb.v):

```
module Comparator_1_bit_sf_tb();
reg a,b;
wire e,g,l;
Comparator_1_bit_sf x1(e,g,l,a,b);
initial
begin
a=1'b0;b=1'b0;
#10 a=1'b0;b=1'b1;
#10 a=1'b1;b=1'b0;
#10 a=1'b1;b=1'b1;
#10 $finish;
end
endmodule
```

## 1.9 WAVEFORM:



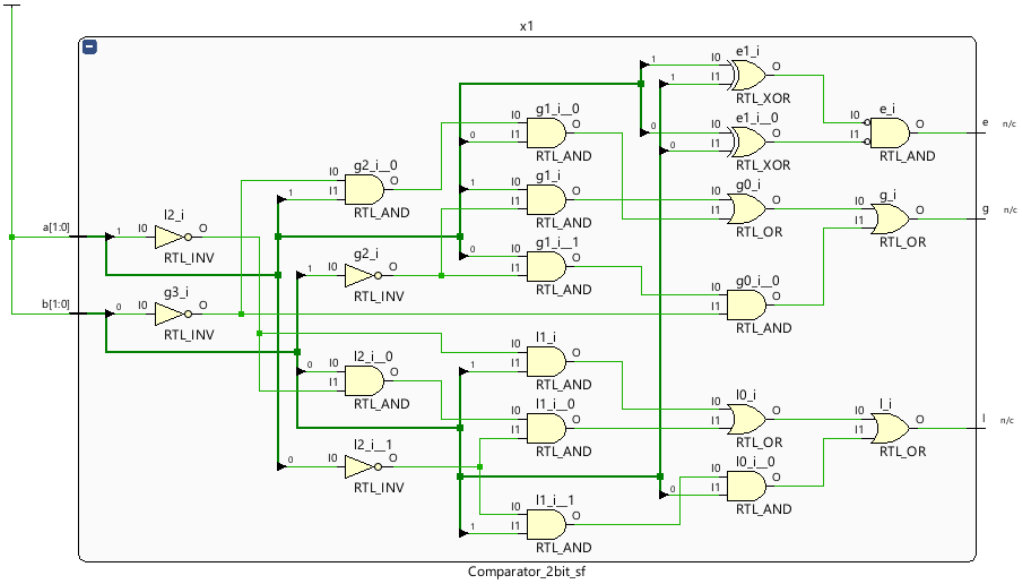

## 1.10 RESULT:

1 Bit Comparator is simulated and implemented in Structural Flow Modeling.

**2.1 AIM:** 2 Bit Comparator

**2.2 SOFTWARE USED:** Xilinx Vivado 2022.2

**2.3 SYMBOL:**




**2.4 LOGIC EXPRESSION:**

E = (~(A1^B1)) & (~(A0^B0))
G = (A1& (~B1)) | ((~B0) & A1&A0) | (A0& (~B1)&(~B0)))
L = (B1& (~A1)) | (B0 & (~A1)&(~A0)) | ((~A0)& B1&B0))

**2.5 BOOLEAN EXPRESSION:**

$E = (\overline{A1}\,\overline{B1}+A1B1)(\overline{A0}\,\overline{B0}+A0B0)$
$G = A1\overline{B1} + A0A1\overline{B0} + A0\overline{B1}\,\overline{B0}$
$L = \overline{A1}B1 + \overline{A0}\,\overline{A1}B0 + \overline{A0}B1B0$

**2.6 TRUTH TABLE:**

| INPUT | | | | OUTPUT | | |
|---|---|---|---|---|---|---|
| **A1** | **A0** | **B1** | **B0** | **E** | **G** | **L** |
| **0** | **0** | **0** | **0** | **1** | **0** | **0** |
| **0** | **0** | **0** | **1** | **0** | **0** | **1** |
| **0** | **0** | **1** | **0** | **0** | **0** | **1** |
| **0** | **0** | **1** | **1** | **0** | **0** | **1** |
| **0** | **1** | **0** | **0** | **0** | **1** | **0** |
| **0** | **1** | **0** | **1** | **1** | **0** | **0** |
| **0** | **1** | **1** | **0** | **0** | **0** | **1** |
| **0** | **1** | **1** | **1** | **0** | **0** | **1** |
| **1** | **0** | **0** | **0** | **0** | **1** | **0** |
| **1** | **0** | **0** | **1** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **1** | **0** | **0** |
| **1** | **0** | **1** | **1** | **0** | **0** | **1** |
| **1** | **1** | **0** | **0** | **0** | **1** | **0** |
| **1** | **1** | **0** | **1** | **0** | **1** | **0** |
| **1** | **1** | **1** | **0** | **0** | **1** | **0** |
| **1** | **1** | **1** | **1** | **1** | **0** | **0** |

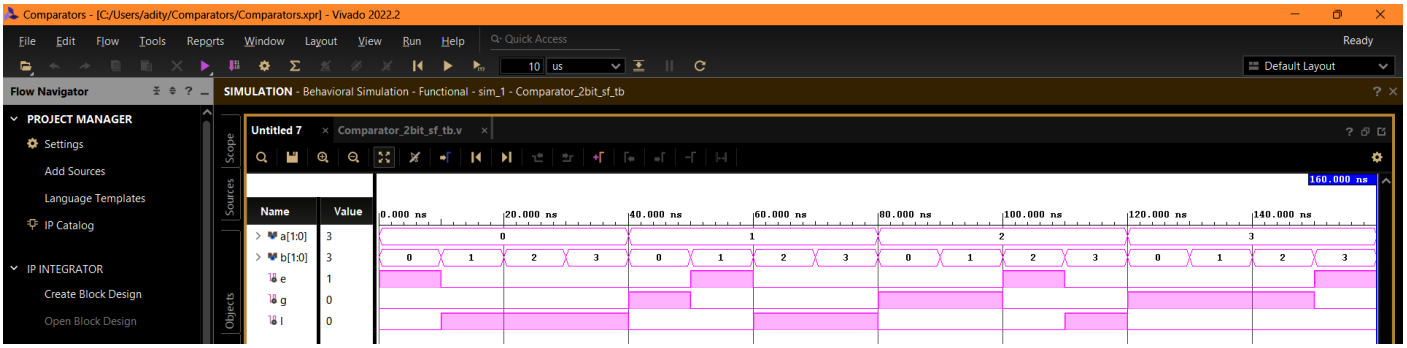
**2.7 VERILOG CODE (Comparator_2bit_sfv):**

```
module Comparator_2bit_sf(e,g,l,a,b);
output e,g,l;
input [1:0]a;
input [1:0]b;
wire e,g,l;
or (g,(a[1]&(~b[1])),((~b[0])&a[1]&a[0]),(a[0]&(~b[1])&(~b[0])));
or (l,(~(a[1])&b[1]),(b[0]&(~a[1])&(~a[0])),((~a[0])&b[1]&b[0]));
and(e,(~(a[1]^b[1])),(~(a[0]^b[0])));
endmodule
```

**2.8 TEST BENCH (Comparator_2bit_sf_tb.v):**

```
module Comparator_2bit_sf_tb();
reg [1:0]a;
reg [1:0]b;
wire e,g,l;
Comparator_2bit_sf x1(e,g,l,a,b);
initial
begin
{a,b}=4'b0000;
#10 {a,b}=4'b0001;
#10 {a,b}=4'b0010;
#10 {a,b}=4'b0011;
#10 {a,b}=4'b0100;
#10 {a,b}=4'b0101;
#10 {a,b}=4'b0110;
#10 {a,b}=4'b0111;
#10 {a,b}=4'b1000;
#10 {a,b}=4'b1001;
#10 {a,b}=4'b1010;
#10 {a,b}=4'b1011;
#10 {a,b}=4'b1100;
#10 {a,b}=4'b1101;
#10 {a,b}=4'b1110;
#10 {a,b}=4'b1111;
#10 $finish ;
end
endmodule
```

## 2.9 WAVEFORM:




## 2.10 RESULT:

2 Bit Comparator is simulated and implemented in Structural Flow Modeling.