RISC-V for MedTech: Open Innovation to Solve the Organ Donor Problem

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Abstract

This white paper explores how the RISC-V open-source processor architecture can support the development of a MedTech ecosystem to address the global organ donor shortage. With its customizable instruction set and permissive licensing model, RISC-V enables the creation of specialized, energy-efficient, and cost-effective medical devices, surgical robotics, and artificial organ systems. This paper maps the intersection of technical innovation and biomedical need to propose a scalable, engineer-driven approach to organ replacement and monitoring technologies.

1 Introduction

Organ failure remains one of the most urgent, global healthcare crises of our time. For many patients, organ transplantation is the only viable treatment option. Yet, access to donor organs is limited, unpredictable, and often inequitable. This shortage has created a fragile system built on waiting lists, chance compatibility, and the death of others. Moreover, it has fueled a thriving black market and created lifelong medical burdens for transplant recipients, including immunosuppression, re-transplantation, and psychological trauma.

In response, an engineering-centric vision is emerging: one that reframes organ failure as a solvable systems problem. By integrating surgical robotics, artificial organs, and connected diagnostic and therapeutic devices, we can build an ecosystem that shifts from donor dependency to designed longevity.

At the heart of this vision lies the need for flexible, cost-effective, and customizable computing hardware. Traditional processor architectures such as ARM and x86 are often encumbered by proprietary licensing, limited extensibility, and opaque supply chains—barriers to innovation in regulated medical environments.

RISC-V, an open-source instruction set architecture (ISA), presents a compelling alternative. Free from royalties and designed for extensibility, RISC-V enables hardware-software co-design at all scales, from ultra-low-power implants to high-performance AI-enabled surgical systems. Its transparency and customizability make it ideally suited for developing next-generation medical technologies that must be secure, certifiable, and mission-critical.

This paper explores how RISC-V can serve as the foundational hardware layer in a MedTech ecosystem aimed at solving what I define as the *Organ Donor Problem*. By leveraging RISC-V's openness, adaptability, and ecosystem momentum, we can accelerate the

development of devices that monitor, assist, or even replace vital organ functions—reducing reliance on human donors and expanding access to life-saving care.

2 RISC-V Advantages: Licensing and Customization

RISC-V is an open-standard instruction set architecture (ISA) that stands apart from legacy ISAs like ARM and x86 by offering a royalty-free, vendor-neutral foundation for processor design. In the context of MedTech — a domain characterized by high regulatory burden, long product cycles, and tightly integrated hardware-software systems — RISC-V's licensing and customization advantages are particularly transformative.

Open Licensing and Vendor Independence

Unlike ARM, which requires licensing fees and often locks designers into specific silicon vendors, RISC-V allows developers to design and fabricate processors without paying royalties or seeking approval from a central authority. This open model significantly lowers barriers to entry, especially for startups, research institutions, and companies in cost-sensitive healthcare markets.

Vendor independence also mitigates long-term supply chain risk. A medical device company using RISC-V is not bound to a single chip supplier and can port its design across multiple silicon platforms. This is crucial in a field where devices may require decades of support and traceability for regulatory reasons.

Customizability and Hardware-Software Co-Design

RISC-V's modular structure allows implementers to tailor the ISA to match application needs — including adding or omitting extensions such as floating-point, vector processing, or custom instructions. This enables the creation of domain-specific processors optimized for tasks like biosignal analysis, low-power telemetry, or motor control in surgical systems.

For example, a RISC-V-based processor in a wearable cardiac monitor might include only integer arithmetic and ultra-low-power sleep modes, while a processor embedded in a robotic surgery system might include DSP or AI acceleration features. Designers can even define proprietary instructions for specialized medical workloads without compromising ISA compliance.

Transparency, Trust, and Formal Verification

In medicine, trust and certification are paramount. RISC-V's openness means that processor implementations can be audited, verified, and even formally proven to behave correctly — a critical factor in achieving regulatory approval for life-critical devices.

Medical companies can build or adopt RISC-V cores with full access to source HDL (hardware description language) and validation suites, allowing them to demonstrate compliance with safety standards such as IEC 60601, ISO 13485, or ISO 26262 (adapted for medical use). This is far more difficult when using opaque, proprietary IP cores where internal behavior is undocumented or protected under non-disclosure agreements.

Security and Lifecycle Control

Medical devices face increasing scrutiny around cybersecurity, especially those connected to networks or implanted in patients. RISC-V allows implementers to build custom secure enclaves, cryptographic modules, and hardware-based isolation features directly into the processor — ensuring that security is not bolted on but architected in from the beginning.

Additionally, because the ISA is stable and openly governed, companies can rely on long-term compatibility and support. They are not at the mercy of commercial IP vendors discontinuing cores, changing licensing terms, or obfuscating hardware errata.

In summary, RISC-V's open licensing and deep customizability offer a rare alignment of engineering freedom, regulatory friendliness, and strategic control — making it an ideal platform for the next wave of secure, efficient, and patient-centered medical technologies.

3 RISC-V for Medical Devices

Medical devices are increasingly defined by their embedded intelligence — from continuous monitoring wearables to life-sustaining implantables. These systems must meet extreme constraints in power, reliability, security, and form factor. RISC-V offers a uniquely adaptable computing platform to meet these demands across the full spectrum of medical electronics.

Ultra-Low Power for Implantable Devices

Implantable devices such as pacemakers, neurostimulators, and artificial pancreas systems must operate reliably for years on a single battery. Traditional microcontrollers used in such applications are typically fixed-function and proprietary, limiting innovation.

RISC-V enables custom ultra-low-power cores, often consuming less than 50 μA/MHz, and as little as 20 nA in sleep modes. The *Siwa* core, for example, is a 32-bit RISC-V processor specifically developed for implantable biomedical applications. It demonstrated safe operation at low voltage while directly controlling biological stimulus circuits, validating RISC-V's suitability in high-reliability implantable systems.

Wearables and Anomaly Detection

Medical-grade wearables are transitioning from passive sensors to active analyzers. Devices like ECG patches, blood oxygen monitors, and seizure detectors increasingly perform on-device signal processing to reduce latency and bandwidth needs.

RISC-V's ability to be tailored for signal-processing workloads — including support for fixed-point arithmetic, fast interrupt handling, and even custom AI inference extensions — makes it ideal for these edge intelligence applications. In one study, researchers designed a dual-mode RISC-V system that shifted between energy-sipping "Night" mode and high-performance "Day" mode, enabling continuous anomaly detection in wearable monitors with minimal power draw.

Connected Diagnostics and Secure Data Handling

Many diagnostic devices — from glucose meters to smart stethoscopes — now operate in connected environments, transmitting sensitive data to smartphones or hospital networks. This raises concerns about privacy, authentication, and real-time responsiveness.

RISC-V's extensible architecture allows integration of custom cryptographic engines, secure enclaves, and encrypted memory regions directly in hardware. This is especially beneficial for meeting HIPAA or GDPR requirements in data-sensitive applications. Furthermore, because the entire processor implementation can be reviewed and validated, medical device makers can more easily certify these features for safety and compliance.

Case Studies in Practice

- **Siwa Microcontroller:** Developed for implantable medical use, Siwa is a 32-bit RISC-V core that integrates biological stimulation circuits, demonstrating low-leakage operation suitable for cardiac pacing and neurostimulation devices.
- **ESP32-C3 Platform:** Espressif's RISC-V-based microcontroller with integrated Bluetooth and Wi-Fi has been used in commercial-grade wearables and health IoT devices, showcasing strong energy efficiency and secure wireless communication in consumer medical tech.
- **Anomaly Detection Research:** A RISC-V system was created to toggle between high-performance and low-power modes for anomaly detection in physiological signals — enabling on-device intelligence while maximizing battery life.

Through its low-power potential, flexibility, and robust toolchain support, RISC-V empowers engineers to build smarter, safer, and more efficient medical devices — from everyday monitors to the most demanding implantables.

4 RISC-V for Surgical Robotics

Surgical robotics represents one of the most demanding applications of embedded computing in medicine — requiring precise motion control, real-time sensor fusion, safety-critical operation, and integration with high-resolution imaging. RISC-V's open and customizable architecture makes it a strong candidate for powering both the low-level motor controllers and high-level computational modules in next-generation robotic surgery systems.

Real-Time Control and Deterministic Behavior

The arms and instruments in surgical robots rely on real-time feedback loops for position, force, and velocity control. These loops demand microsecond-level latency and deterministic execution — properties often difficult to achieve with general-purpose cores.

RISC-V cores can be designed with simplified pipelines, predictable interrupt latency, and customized instruction sets optimized for control algorithms. By stripping down the ISA to

only the essential features and adding precise timing control logic, RISC-V can outperform many commercial MCUs in tightly constrained robotic control loops. This deterministic behavior is vital in preventing drift, overshoot, or unsafe movements during critical surgical operations.

Sensor Fusion and AI Inference at the Edge

Modern surgical systems use 3D cameras, force sensors, ultrasound, and haptics to augment the surgeon's perception. Some even employ AI models to detect anatomical structures or flag anomalies in real time.

RISC-V supports vector processing and custom accelerators for edge AI inference. With NVIDIA announcing CUDA support for RISC-V, surgical platforms will increasingly be able to use RISC-V as the main host or co-processor to interact with GPU-based workloads — enabling seamless AI-assisted surgery and data-driven robotics. This modular architecture allows combining high-throughput image processing and precise control in a single system without vendor lock-in.

Safety, Redundancy, and Remote Operation

Robotic surgery must account for system failures. RISC-V enables the implementation of redundant core architectures (e.g., dual-core lockstep) and hardware-based fault detection. Designers can also incorporate watchdog systems and real-time safety monitors within the processor using custom logic.

Additionally, the open-source nature of RISC-V makes it ideal for teleoperated and remote surgical robots. Control software running on RISC-V platforms can be formally verified, audited, and certified to ensure patient safety even when operating across a network — particularly valuable in rural or emergency settings where expertise is remotely deployed.

Integration with Surgical Platforms

While legacy surgical platforms may run on ARM or x86 architectures, RISC-V cores can be introduced incrementally. For example, a new robotic instrument or sensor module can be equipped with a RISC-V controller that communicates over standard buses (SPI, I^2C, CAN) with existing systems. Over time, more subsystems can migrate to RISC-V — especially those requiring security, efficiency, or application-specific performance enhancements.

In surgical robotics, where precision, safety, and intelligence converge, RISC-V offers a hardware foundation that is not only powerful and energy-efficient, but also transparent, customizable, and increasingly AI-capable. It turns surgical precision into programmable logic — enabling broader, safer, and smarter surgical access.

5 RISC-V for Artificial Organs

Artificial organs — including ventricular assist devices (VADs), artificial pancreases, dialysis systems, and synthetic lungs — represent a complex integration of biomedical sensing,

feedback control, fluid dynamics, and embedded intelligence. These systems must operate continuously, safely, and autonomously, often in direct contact with biological processes. RISC-V provides a flexible and certifiable computing foundation for managing such complexity.

Closed-Loop Control in Biomedical Systems

Most artificial organs rely on closed-loop systems: continuously sensing biological signals (e.g., blood glucose, pressure, oxygen levels), computing control outputs, and actuating mechanical responses (e.g., insulin release, blood pumping). This real-time control loop must be reliable, low-latency, and fault-tolerant.

RISC-V enables lightweight, deterministic processors tailored for these control tasks. Designers can reduce the instruction set to only the necessary components (e.g., integer math, basic timing) and integrate sensor drivers and actuator interfaces directly into custom SoC logic. The result is a processor core that is tightly focused on the medical control function — reducing overhead, improving responsiveness, and simplifying certification.

Sensor-Actuator Integration and SoC Design

Artificial organs often integrate multiple sensors (temperature, flow, pressure, chemical) and actuators (motors, valves, pumps) into a compact embedded system. RISC-V is well-suited for System-on-Chip (SoC) designs where these elements are tightly coupled to the processor.

Using RISC-V, engineers can develop chips where the CPU, sensor interfaces, analog front-ends, and control logic coexist in a single verified layout. This results in reduced power consumption, faster response times, and minimal interconnect complexity — all crucial in wearable or implantable organ-support systems.

Custom Signal Processing and Fault Detection

In organs like the heart or pancreas, signal patterns can indicate early signs of failure or physiological instability. Custom instructions can be added to RISC-V processors to perform real-time filtering, thresholding, or machine learning inference directly in hardware — enabling predictive diagnostics and adaptive control.

For example, a RISC-V core in an artificial heart controller might include custom multiply-accumulate (MAC) units and pattern recognition logic to detect arrhythmias and automatically adjust pump flow. These capabilities extend the intelligence of the artificial organ, moving it beyond mechanical support to proactive health intervention.

Lifecycle, Certifiability, and Transparency

Artificial organs must operate for years — often with life-critical implications. RISC-V enables transparent certification workflows by allowing full access to HDL code, simulation vectors, and formal models. This is essential for regulatory approval under standards such as ISO 13485 or IEC 60601.

Moreover, since RISC-V cores are not tied to a specific vendor, designers can ensure long-term availability and maintainability of the hardware. This prevents obsolescence and allows for safe updates, re-verification, and eventual system upgrades — a common pain point in legacy ASIC-based designs.

By giving medical engineers precise control over processor function, performance, and certification, RISC-V is poised to become a key enabling technology for artificial organs — making them smarter, safer, and more adaptive to individual patient needs.

6 Integrating RISC-V with x86 and ARM

While RISC-V offers compelling advantages in terms of openness and customization, most current medical systems still rely on legacy architectures like ARM (common in embedded and mobile platforms) and x86 (dominant in clinical workstations and data centers). To accelerate adoption, RISC-V must coexist and interoperate with these platforms — forming a heterogeneous computing ecosystem optimized for MedTech.

RISC-V as a Co-Processor or Peripheral Controller

One of the most effective integration strategies is to use RISC-V cores as co-processors or subsystem controllers within larger ARM or x86-based systems. For example, in a surgical robot or wearable health hub, an ARM Cortex-A processor may manage the operating system and user interface, while a RISC-V microcontroller handles real-time motor control, biosignal processing, or secure data handling.

This division of labor allows RISC-V to offload time-sensitive or domain-specific tasks — enhancing performance and reducing the burden on the primary CPU. It also enables engineers to explore RISC-V's benefits incrementally without overhauling existing architectures.

Standard Interfaces and Interoperability

RISC-V cores can communicate with other architectures via standard bus protocols such as SPI, I^2C, UART, and CAN. More advanced interconnects, like AXI or TileLink, enable high-speed data exchange when integrating RISC-V into complex SoCs or FPGA systems.

Additionally, toolchains such as LLVM, GCC, and Zephyr RTOS support multi-architecture builds, allowing cross-compilation and debugging across heterogeneous systems. This interoperability ensures that RISC-V-based modules can fit cleanly into ARM or x86 development pipelines, minimizing integration friction.

Bridging Through FPGA and Soft-Core Solutions

FPGA-based RISC-V implementations are increasingly used to prototype or supplement existing medical platforms. Many x86-based systems (e.g., ultrasound consoles or diagnostics workstations) include FPGAs that can host RISC-V soft cores for tasks such as data acquisition, preprocessing, or security isolation.

This strategy offers rapid development and flexibility without changing the host CPU. Medical device manufacturers can iterate quickly, test custom extensions, and validate behavior in sandboxed environments — all while maintaining compatibility with legacy software and hardware stacks.

Case Examples

- **Microchip PolarFire SoC:** Combines a hard RISC-V core with FPGA fabric, enabling secure and deterministic subsystem control within larger medical imaging and instrumentation systems.
- **NVIDIA and RISC-V:** NVIDIA has announced that future GPUs will include RISC-V cores as microcontrollers. This opens the door for RISC-V-based orchestration within high-performance AI accelerators used in diagnostics or robotic surgery.
- **Arduino Portenta X8:** This hybrid board features both Linux-capable ARM cores and a RISC-V real-time core, showing how consumer-grade and medical research devices can leverage both platforms simultaneously.

Migration Strategies and Long-Term Coexistence

In regulated environments like healthcare, full architectural migration is often impractical. A gradual approach — starting with peripheral RISC-V controllers, then moving to main application processors — enables technical and regulatory continuity.

RISC-V cores can also be integrated into legacy systems as trusted security enclaves, watchdogs, or compliance monitoring agents. Over time, as RISC-V toolchains and silicon mature, the ecosystem can shift toward more RISC-V-centric designs while maintaining compatibility with existing ARM and x86-based infrastructure.

Rather than replace x86 or ARM outright, RISC-V extends the MedTech computing landscape by enabling modular, open, and specialized components that complement legacy systems. This hybrid architecture model is the most realistic path to widespread adoption and lasting innovation in medical hardware.

7 Conclusion

The Organ Donor Problem is not merely a biological challenge — it is an engineering systems problem at scale. Solving it demands a coordinated ecosystem of intelligent medical devices, responsive artificial organs, and autonomous surgical systems. At the foundation of this vision must be hardware that is secure, reliable, energy-efficient, and deeply customizable.

RISC-V, as an open-source instruction set architecture, offers a powerful enabler for such a transformation. Its royalty-free licensing and modular design allow engineers to create specialized processors optimized for medical workloads — from ultra-low-power implants to AI-enhanced robotics. Unlike proprietary architectures, RISC-V empowers full hardware-software co-design, promotes supply chain transparency, and aligns with the long lifecycles and regulatory demands of medical innovation.

Across wearable monitors, closed-loop insulin pumps, surgical robots, and artificial hearts, RISC-V is already proving its value — either as a standalone processor or as a complement to existing x86 and ARM platforms. It lowers the cost of experimentation while raising the ceiling of what is technically possible in life-critical applications.

By embracing RISC-V, we can reimagine MedTech from the transistor level up — building tools not just to treat illness, but to restore autonomy, dignity, and life itself. As engineers, this is our opportunity and our responsibility: to open up the hardware layer so that innovation can flow where it is needed most — into the bodies and lives of patients waiting for a second chance.