Digital Design Document

DTMF

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1 SCOPE

This Digital Design Document details the requirements and design for design of the FPGA system that will read a phone number and produce the appropriate DTFS sounds.

1.1 System Identification

The system produces multiple frequencies according to 2 numericaly controlled oscillators(NCO's) and sums them to for a DTMF frequency.

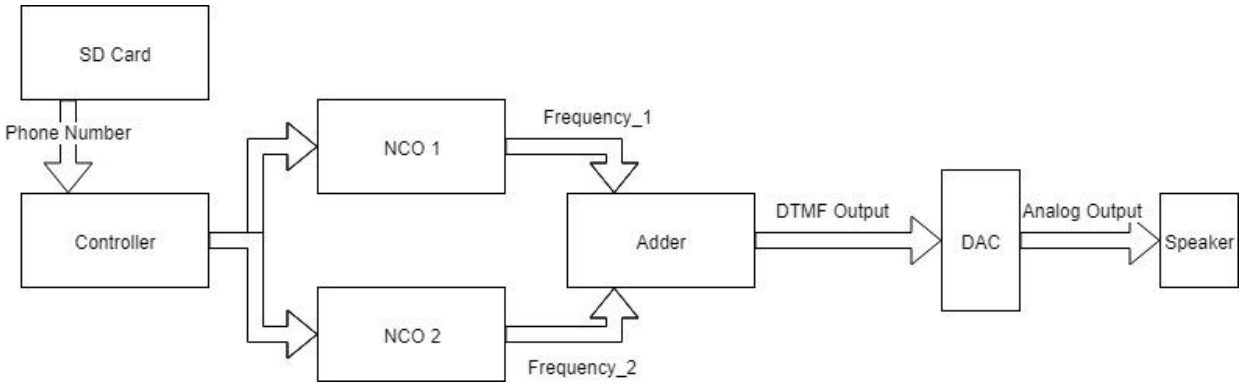


Figure 1 - System Block Diagram

1.2 Document Overview

This document establishes the requirements for the system and details the system, subsystem, and component level designs.

2 APPLICABLE DOCUMENTS

The following documents of the exact issue shown form a part of this specification to the extent specified herein. In the event of an inconsistency between the documents referenced herein and the content of this specification, this specification shall be considered a superseding requirement.

2.1 Internal Documents

Not applicable.

2.2 External Documents

Not applicable.

3 SYSTEM REQUIREMENTS

Detail the requirements for the system in this section. The content provided is example detail that is not applicable to this assignment.

3.1 Interfaces

3.1.1 Phone Number

The only input needed by the system is an SD Card to read the phone number off .

3.1.1.1 DTMF Output

The output of the system is a DTMF output. This is output is to be given to a DAC, which would produce audible sound waves when given to a speaker.

3.1.1.2 Clock Input

Each channel of the Digital Receiver shall receive a clock signal input.

3.1.2 Power Interface

The system will run off of a 5V TTL power source.

3.2 Environmental Conditions

The digital system shall operate under normal lab conditions.

3.3 Safety Requirements

The digital system shall support normal lab requirements.

3.4 System Design

The block diagram shown in Figure 2 shows the block diagram design for the system level. Each of the blocks will be examined in the sections below.

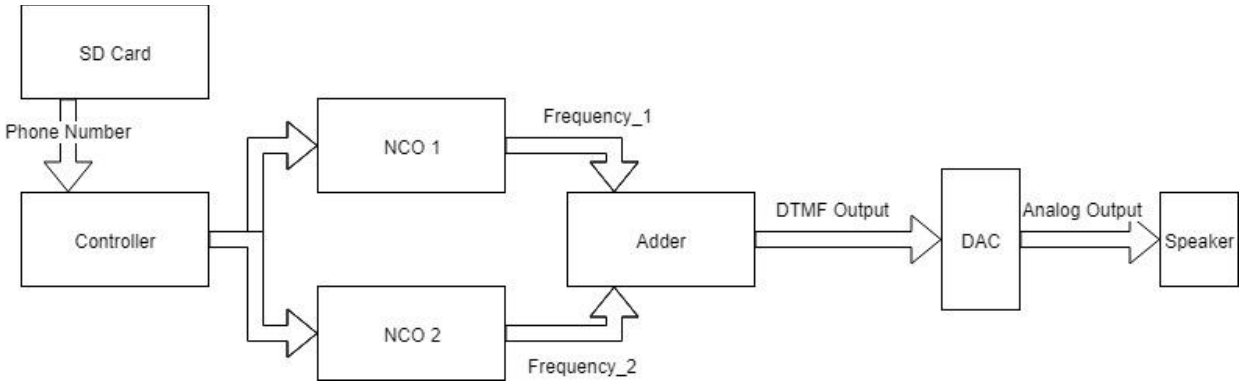


Figure 2 - System Block Diagram

3.4.1 SC Card

The SD card will be used to provide the Phone Number.

3.4.2 NCO

The NCO will generate a signal of the frequency provided to it.

3.4.3 Controller

The controller will read the phone number off the SD card and find the corresponding frequencies to give to both NCO's for each number. They are decided as:

Frequency:	1209 Hz	1336 Hz	1477 Hz
697 Hz	1	2	3
770 Hz	4	5	6
852 Hz	7	8	9
941 Hz	*	0	#

3.4.4 Adder

The adder will perform addition of both waves and output the result to the DAC.

3.4.5 DAC

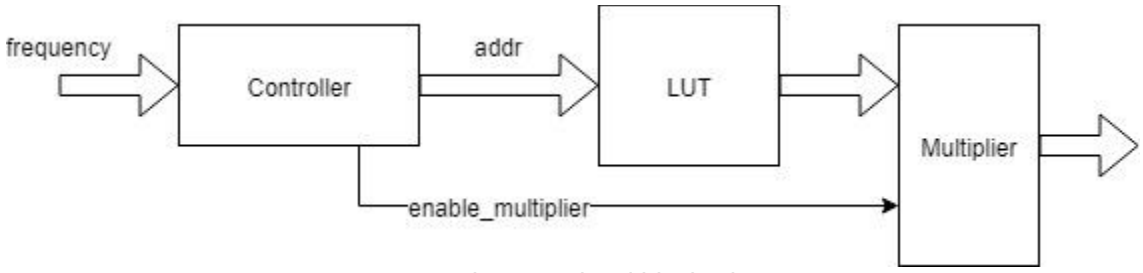
The DAC is 24 bits wide. It can support a sampling rate of 8kHz to 96kHz. We use the sampling frequency as 96kHz.It will take the sum of both NCO's and create the DTMF signal.

3.4.6 Speaker

Needed to play the tones generated by the DAC.

3.5 Sub-System Design for the NCO Module

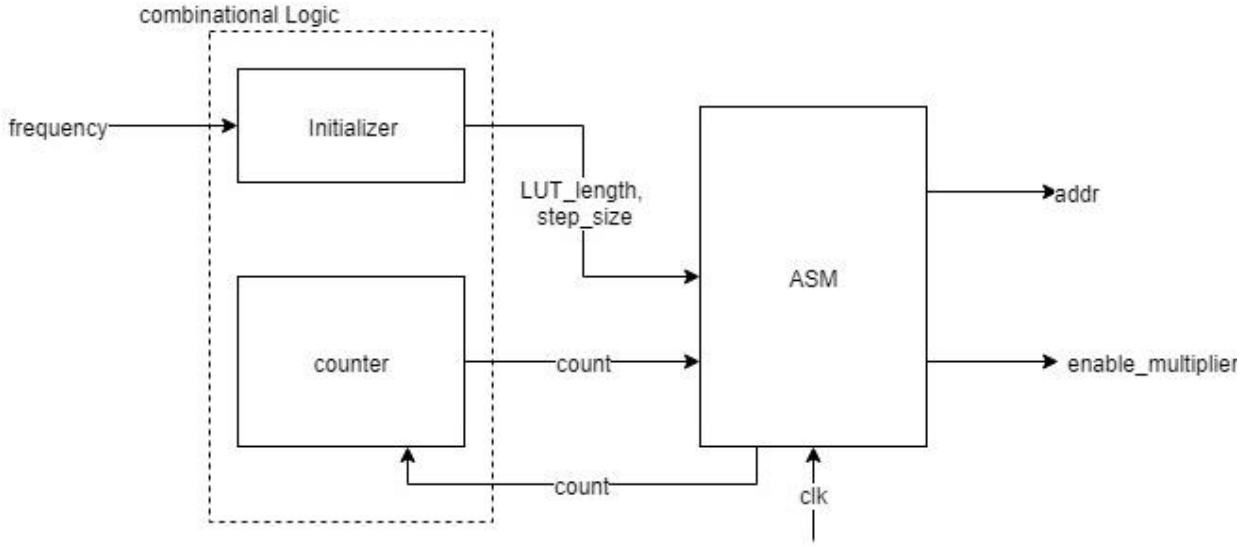
The block diagram shown in the figure shows the block diagram design for the sub-system level of the NCO module. Each of the blocks will be examined in the sections below.



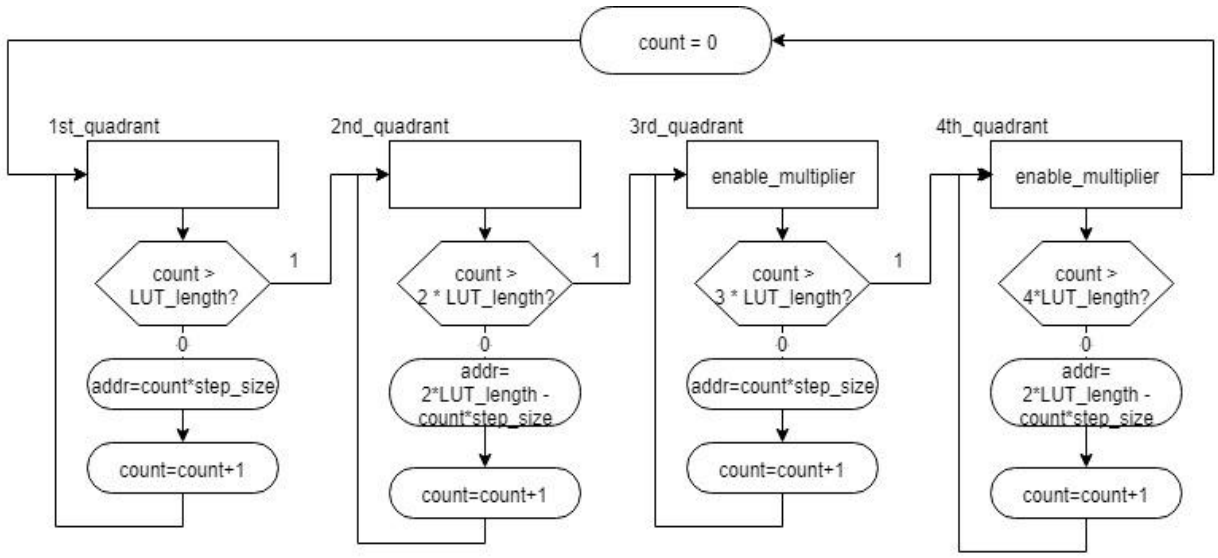
Subsystem level block Diagram

3.5.1 Controller

The controller will generate addresses to generate signals of frequencies that it gets. The lookup table only contains quarter of a wave, so after the first quarter, the wave is read from the LUT in reverse, this is done again, with the amplitude being negative in magnitude, to create the negative cycle of the sine wave. Sampling frequency set to 96kHz.



Component Level Block Diagram



ASM of controller

3.5.1.1 Initializer

Step_size is set to change the frequency. It is calculated as freq/fs*resolution of LUT.The LUT length is set to 90.

3.5.1.2 Counter

Keeps track of the count. Resets to 0 at 4* LUT_length.

3.5.2 LUT

The LUT contains amplitudes of quarter of the wave. The width of each entry can be 24 bits maximum, as the length of the DAC is 24. For practical purposes, we can set it to store 8 bits and just zero pad the LSB bits.

3.5.3 Multiplier

This module will multiply the output by -1 if enable_multiplier is HIGH or just let the data pass if it is LOW.

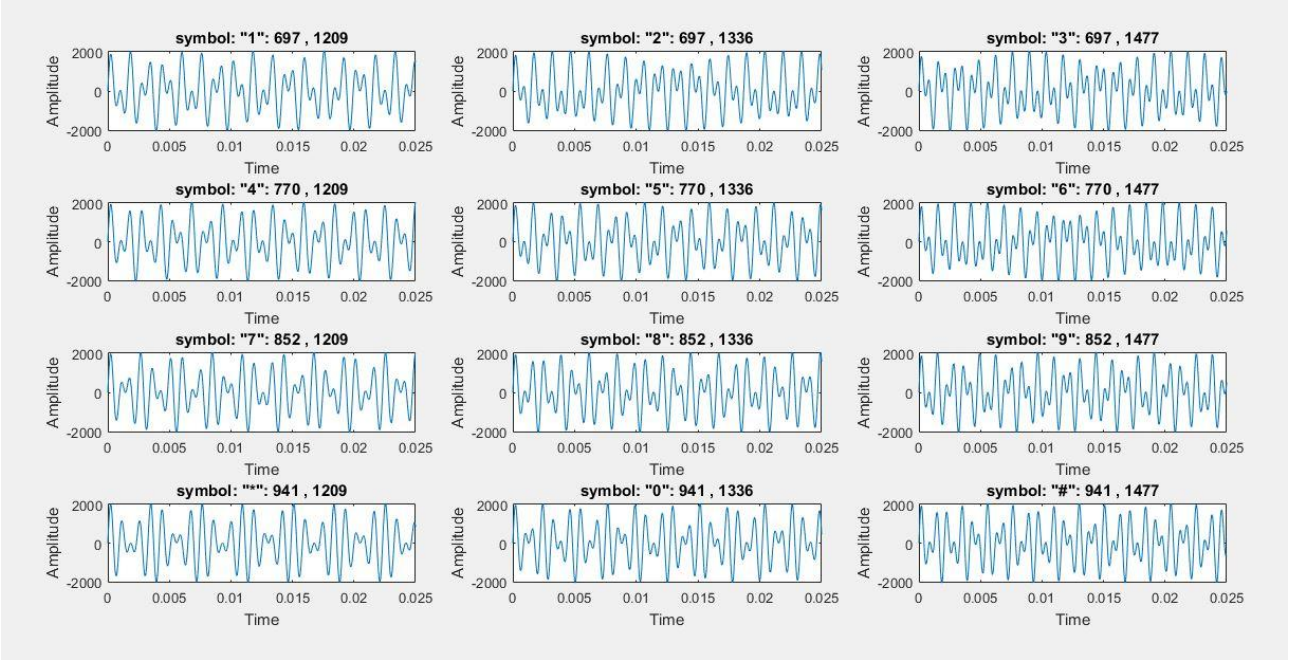
3.6 Component Level Design For the Controller

The controller will read the phone number off the SD card and find the corresponding frequencies to give to both NCO's for each number. They are decided as:

Frequency:	1209 Hz	1336 Hz	1477 Hz
697 Hz	1	2	3
770 Hz	4	5	6
852 Hz	7	8	9
941 Hz	*	0	#

Each of the frequency from the row and the column will be given to one NCO. After a predetermined delay, it will move on to the next number from the input.

3.7 Outputs:



Outputs corresponding to the 12 symbols are shown.

The amplitude varies from 2048 to -2048, or in 12 bits in binary. These are to be set as the 12 MSB bits as an input to the DAC.

Sampling frequency set to 96kHz.

4 APPENDIX A

4.1 Acronyms and Definitions.

ADC	Analog to Digital Converter
CW	Continuous Wave
dB	Decibels
dBFS	Decibels, referenced to full scale
dBm	Decibels, referenced to 1 milliwatt
ES	Electronic Support
FPGA	Field Programmable Gate Array
IF	Intermediate Frequency
kHz	Kilohertz
MHz	Megahertz
ns	Nanoseconds
RF	Radio Frequency
TBD	To Be Determined
µW	Microwatts