Team Leader: Muya Chang

Work detail:

- Muya Chang: FPGA Sub-system design, combine work from the team members, ICD of GPS
- Aditya Chavan: SD Card Component Design, ASM of SD Card, DDD of SD Card, ICD of SD Card
- Derin Ozturk: GPS Component Design, ASM of GPS
- Andrew James Fillingim: Group Leader

Digital Design Document

Sprinkler Controller 15

Date: Feb 19th 2018

Revision Record

Date	Author	Comments
Feb/08/2018	Muya	First Edition: 1.0.0
Feb/08/2018	Muya	Block diagrams included: 1.0.1
Feb/09/2018	Muya	Finalize this DDD: 1.0.2
Feb/19/2019	Aditya	Update the ICD:1.0.3

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1 SCOPE

This Digital Design Document details the requirements and design for automatic irrigation system.

1.1 System Identification

The system is an irrigation control system. It will utilize a GPS, a Rain Sensor, a SD Card, and four pre-built 12V solenoid water vales to irrigate. The system allows the user to program watering times for 4 different zones. Figure 1 shows a block diagram of the system.

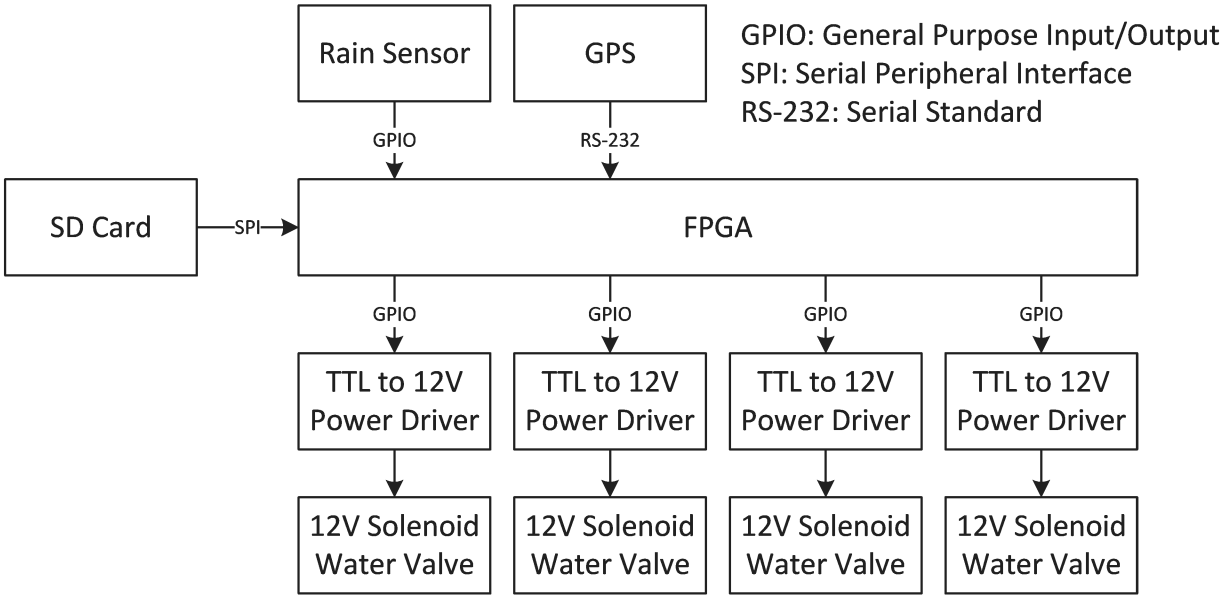

Figure 1 - System Block Diagram

1.2 Document Overview

This document establishes the requirements for the system and details the system, subsystem, and component level designs.

2 APPLICABLE DOCUMENTS

The following documents of the exact issue shown form a part of this specification to the extent specified herein. In the event of an inconsistency between the documents referenced herein and the content of this specification, this specification shall be considered a superseding requirement.

2.1 Internal Documents

Not applicable.

2.2 External Documents

Not applicable.

3 SYSTEM REQUIREMENTS

Detail the requirements for the system in this section. The content provided is example detail that is not applicable to this assignment.

3.1 Interfaces

3.1.1 SD Card

This module is used to store the information of multi periods that the irrigation should water. Since a specific SD Card IP is used, between this module and the system only the important information will be transmitted. Such as zone number, start time, and stop time.

3.1.2 GPS

This module will transmit the time information along with a data valid flag to the system once every second.

3.1.3 Rain Sensor

This module will transmit a high signal when it's raining and a low signal otherwise.

3.2 Environmental Conditions

The digital system shall operate under normal lab conditions.

3.3 Safety Requirements

The digital system shall support normal lab requirements.

3.4 System Design

The block diagram shown in Figure 2 shows the block diagram design for the system level. Each of the blocks will be examined in the sections below.

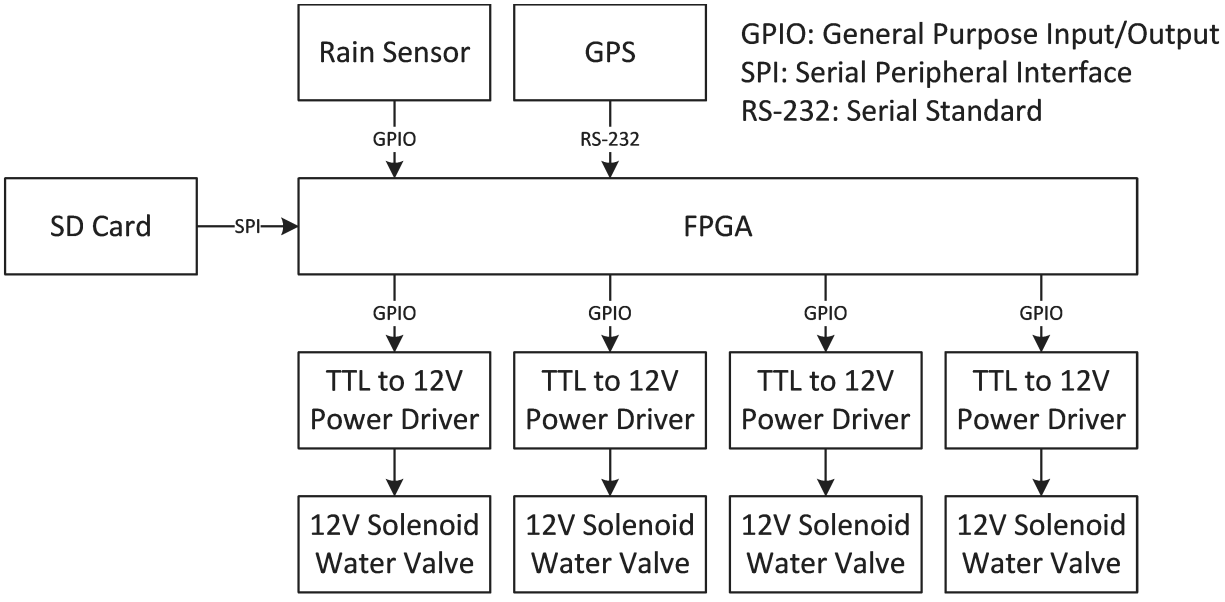

Figure 2 - System Block Diagram

3.5 Component Level Design

For this system, we mainly have three blocks, SD Card, Rain Sensor, and GPS modules. The block diagrams of each module as well as the component design will be shown in detail in the sections below.

3.6 Design for the FPGA Module

Figure 3 shows the block diagram design for the sub-system level of the FPGA module. Figure 4 shows the ASM design for the sub-system level of the FPGA module. Each of the blocks will be examined in the sections below. Several things to be noted here:

- The system will measure the duration of the rain and adjust the irrigation duration thus maintaining the fixed amount of water irrigated every day.
- Line Counter is implemented such that the user can define multiple irrigation periods for the same zone. The system can be configured to water all zones upto 20 times a day.

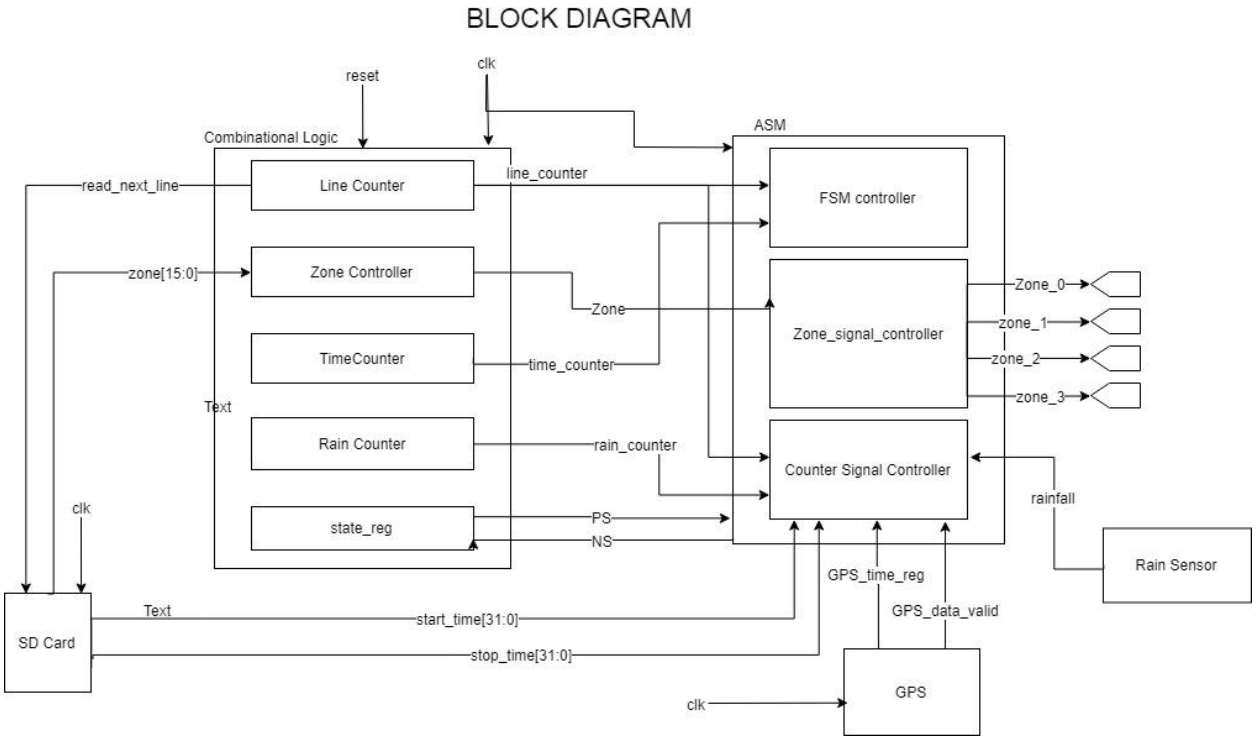

Figure 3 Block diagram of the FPGA Controller

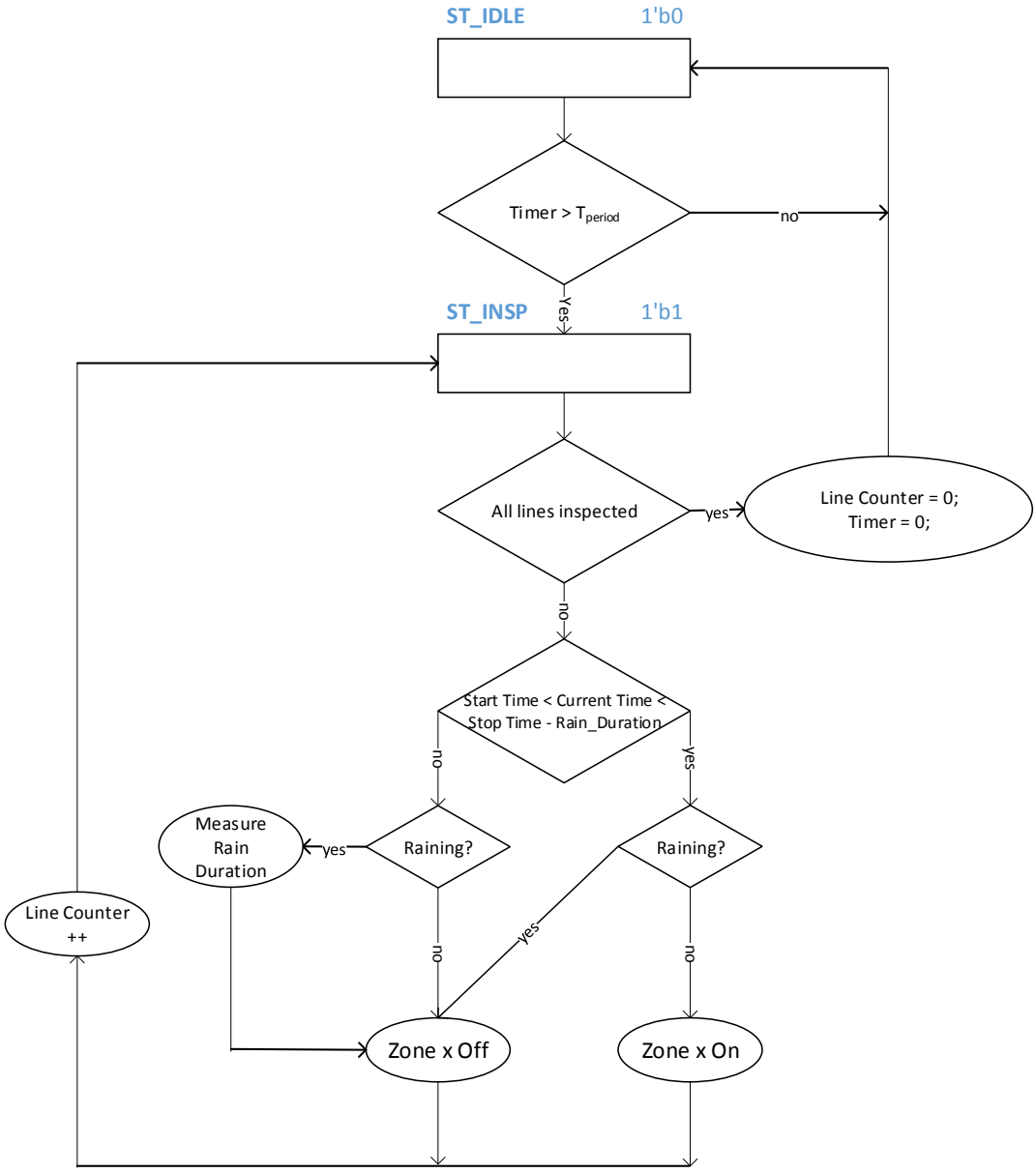

Figure 4 ASM of the Controller

Line Counter: Counts the line currently being read

Time Counter: Keeps count of the current time

Rain Counter: Keeps count how much time it has rained for.

State_reg: Stores all the necessary registers

FSM Controller: This block decides what the next state should be.

Zone Signal Controller: Controlls the output to the zones

Counter Signal Controller: Checks the Present state and other inputs and sets each signal accordingly.

3.6.1 SD Card

The SD card will be used to provide the timing setting to the irrigation system. It will contain the detail when each of the four zones should water. The interface between the SD module and the system will be “read_next_line”, “zone [1:0]”, “start_time[47:0]”, “stop_time[47:0]. The file format for the SD card is shown in Table 1.

Format: “`zone 01 0800 to 0900`” -> 25 bytes, so no more than 20 lines (512 bytes max).

Table 1 File format for the SD card

Name	File Format	Description
read_next_line	1’b0 or 1’b1	0: don’t read; 1: read
zone [1:0]	2’b00, 2’b01, 2’b10, 2’b11	One for each zone
start_time [47:0]	hhmmss	The same as the format from GPS
stop_time [47:0]	hhmmss	The same as the format from GPS

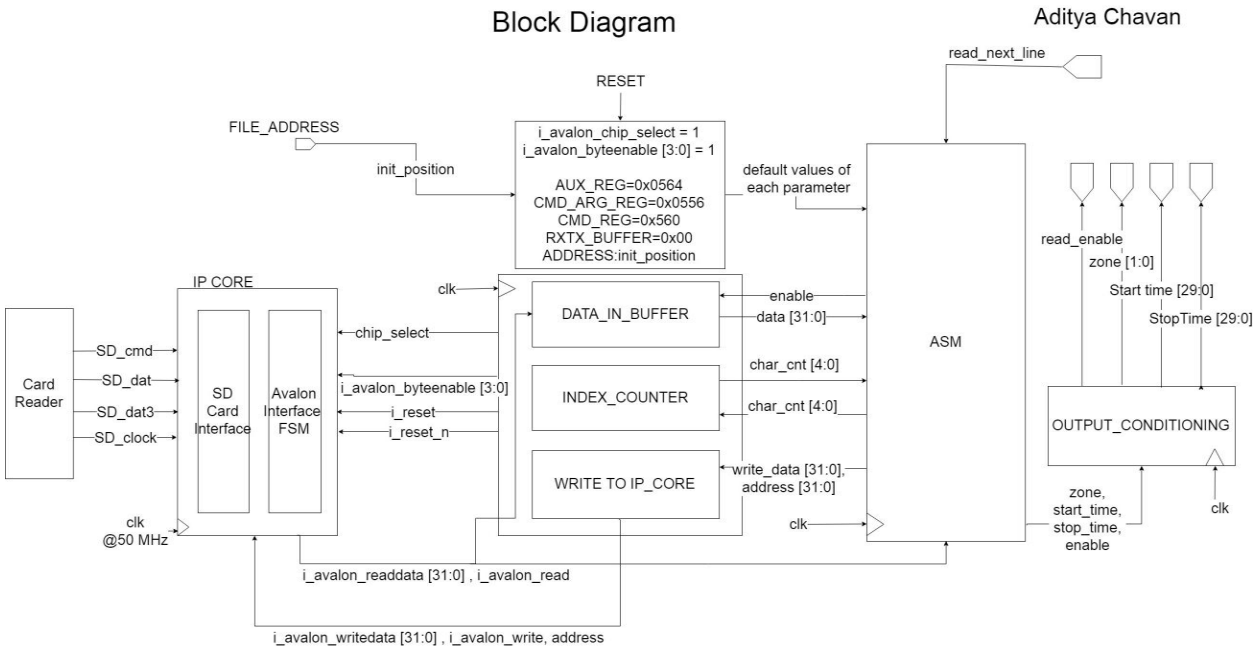

Figure 5 Block Diagram of SD Card

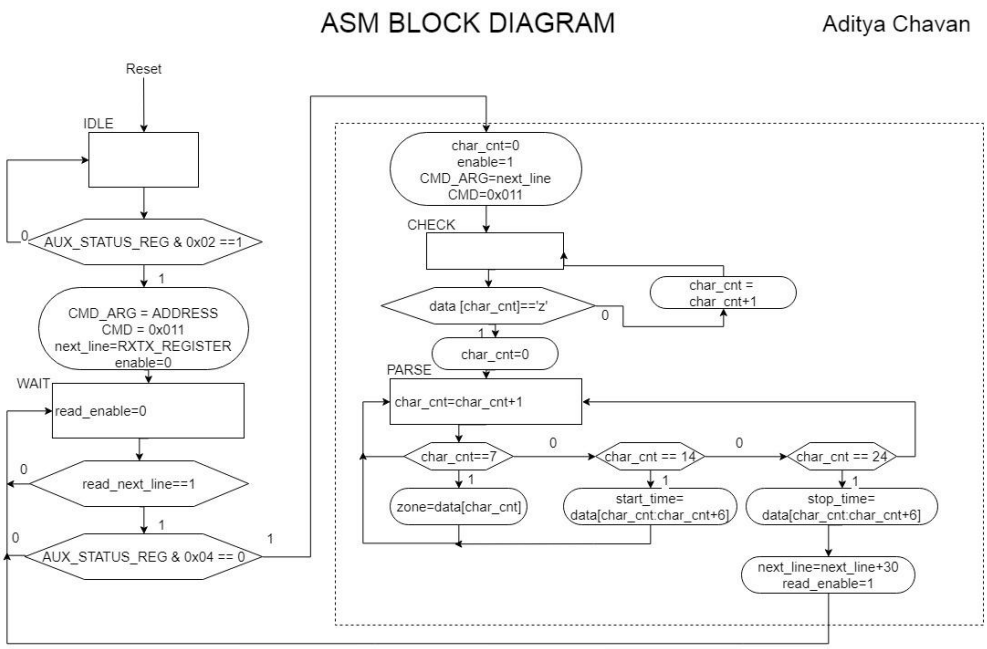

Figure 6 ASM of SD Card

The block diagram of SD Card is shown in Figure 5. The ASM design of SD Card is shown in Figure 6.

3.6.1.1 IP CORE by Avalon

The SD card will be used to provide information to the FPGA about when each of the four zones are to be watered. Must be clocked at 50 MHz.

3.6.1.2 SD CARD Interface

Reads the SD card using SPI interface and provides data to the Avalon core.

3.6.1.3 AVALON Interface FSM

Reads the input signal from the

3.6.1.4 1.5 DATA_IN BUFFER

Reads 32 bytes of data at a time, from signal next_line to next_line+32. The ASM only uses the first 30 bytes each time.(That's the size of each line). It will only read when enabled by the ASM

3.6.1.5 1.6 INDEX COUNTER

Will iterate the char_cnt signal from 0 to 29, to read from the first to the last alphabet of each line

3.6.1.6 1.7 WRITE TO IP CORE

Commands like address of the starting file must be written to the IP core. This block will write data to the core by using the address,i_avalon_datawrite and i_avalon_write pin.

3.6.1.7 1.8 OUTPUT CONDITIONING

Holds output values.

3.6.2 Rain Sensor

The rain sensor for the system will be a Rain Bird Model CPRSDBEX Wired Rain Sensor. The sensor provides an input to the system when rain is detected.

We assume this module is simple: If it's raining, it transmits 1'b1, and 1'b0 otherwise.

3.6.3 GPS

The GPS will be a NMEA compliant RS-232 based commercially available GPS unit. The overall design is similar to the one for HW4, the modification is regarding the parsing range and the leading identifier string is different.

Name	Example Data	Description
Sentence Identifier	$GPGGA	Global Positioning System Fix Data
Time	170834	17:08:34 Z
Data Valid	1	1: valid; 0: not valid

The block diagram of GPS is shown in Figure 7. The component level design of GPS is shown in Figure 8.

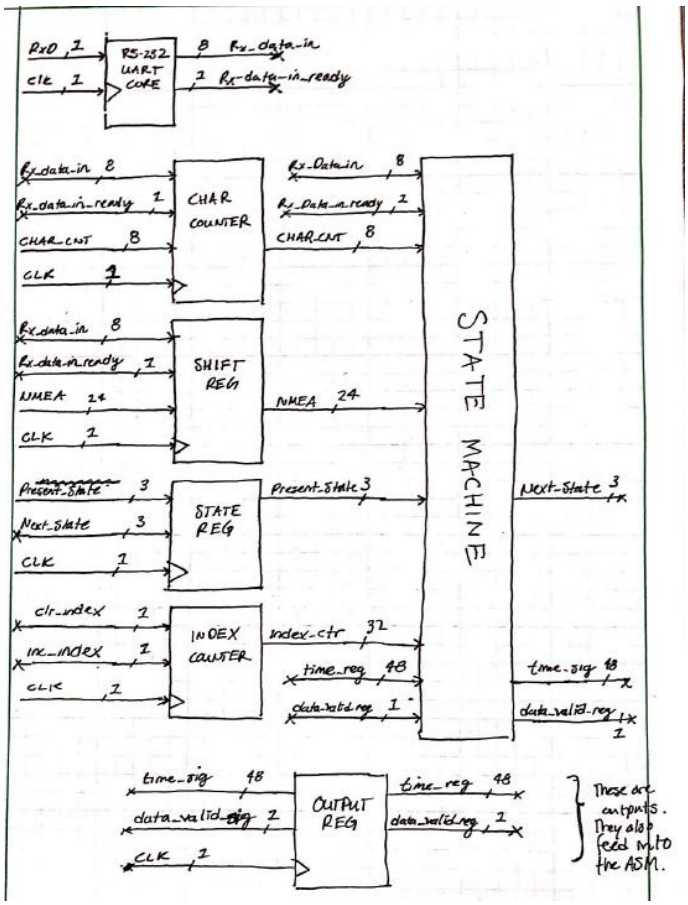

Figure 7 Block Diagram of GPS module

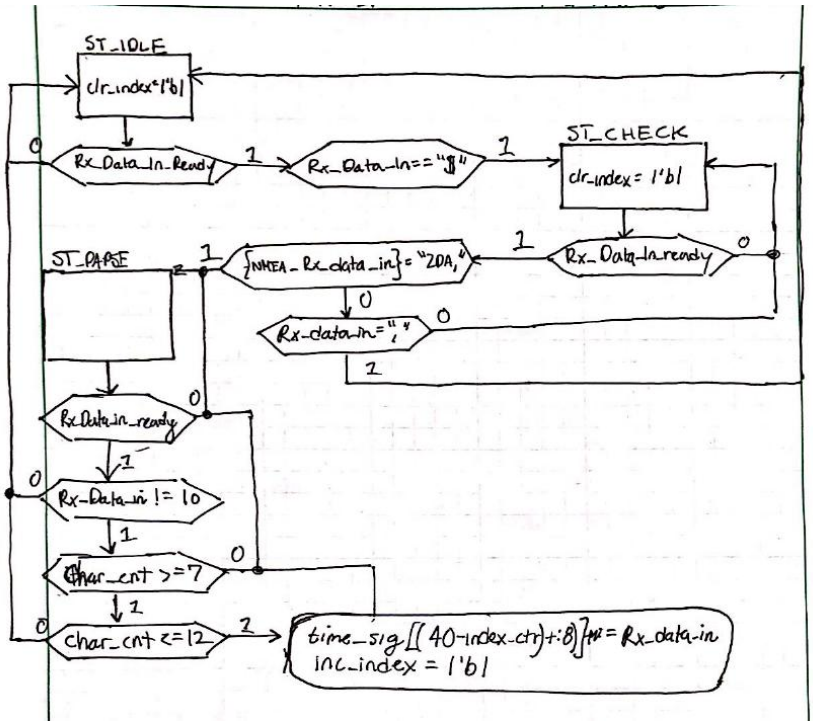

Figure 8 ASM of the GPS module

3.6.4 TTL to 12V Power Driver

The TTL to 12V Power Driver is a voltage translation board. This board will convert the output of the FPGA to the 12V power required by the Solenoid Water Valves.

3.6.5 12V Solenoid Water Valve

The water valves are from various manufacturers and are currently on use on the farm. The new control system will interface to the existing infrastructure.

3.6.6 FPGA

The FPGA board that will be used for this design is a DE10-Standard board from Terasic. Please see the subsystem and component sections of this document that detail the FPGA design.

Interface Control Document

Sprinkler Controller 15

Date: Feb 19th 2018

MAIN SYSTEM:

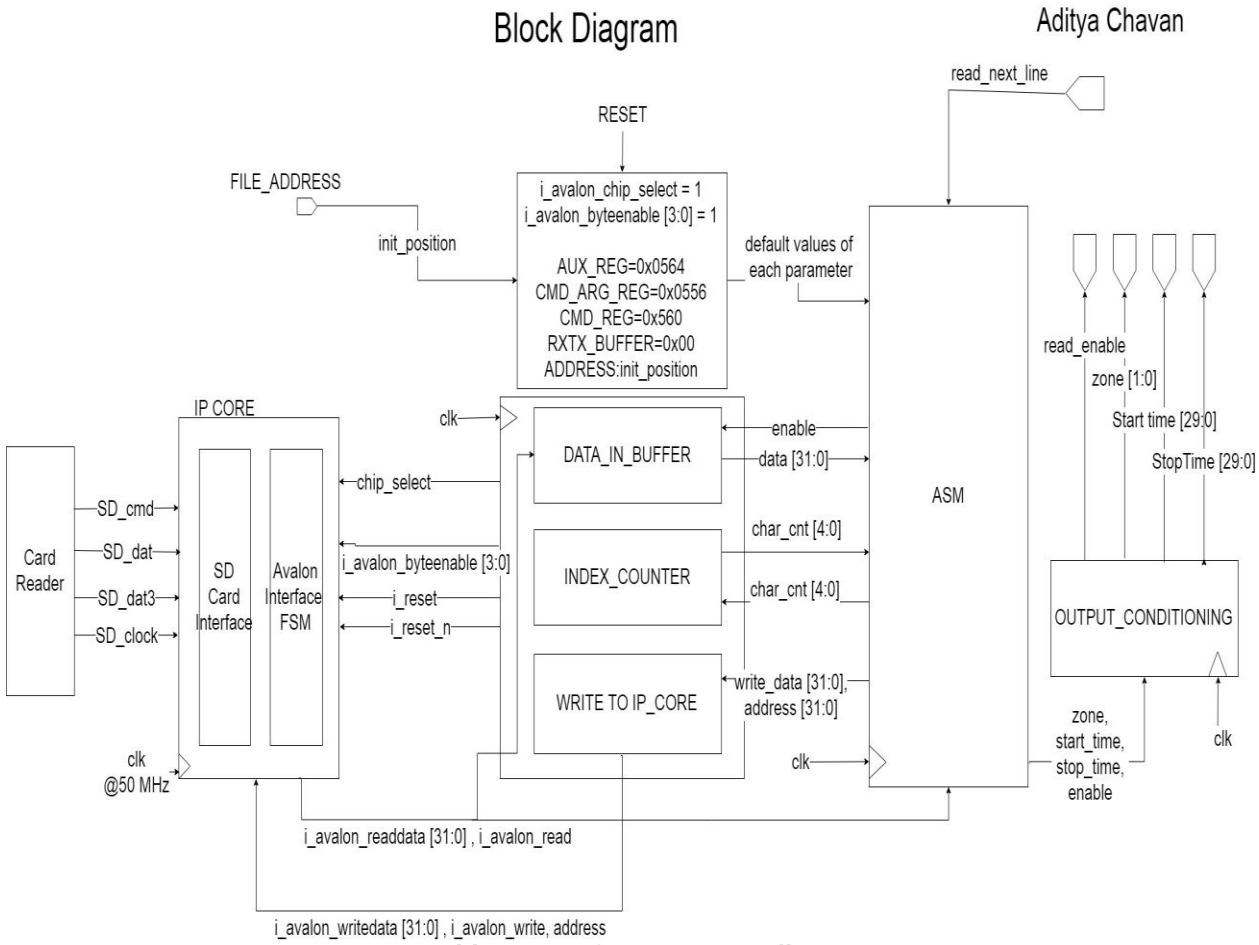

Table 2 ICD of FPGA Controller

PIN NAME	FORMAT	DESCRIPTION
gps_time_reg	Input, [31:0]	Timing Information from the CPU
gps_data_valid	Input, 1 bit	Notifies if the GPS data is valid
zones	input, [1:0]	Indicates zone number
start_time	input,[31:0]	Start time for the indicated zone
stop_time	input,[31:0]	Stop time for the indicated zone
read_next_line	1 bit	HIGH to read next line, LOW otherwise
line_counter	[5:0]	Counts the current line

time_counter	integer	Counts the current time
rain_counter		Counts the duration it has rained.
zone_0 to 4	outputs, 1 bit each	GPIO outputs to be connected to the output solenoids
rst	input, 1 bit	Reset Signal
clk	input,1 bit	Clock
PS	[1:0]	indicates Present State
NS	[1:0]	indicates Next State
rainfall	input,1 bit	HIGH when raining, LOW otherwise. Assuming signal is debounced.

SD CARD:

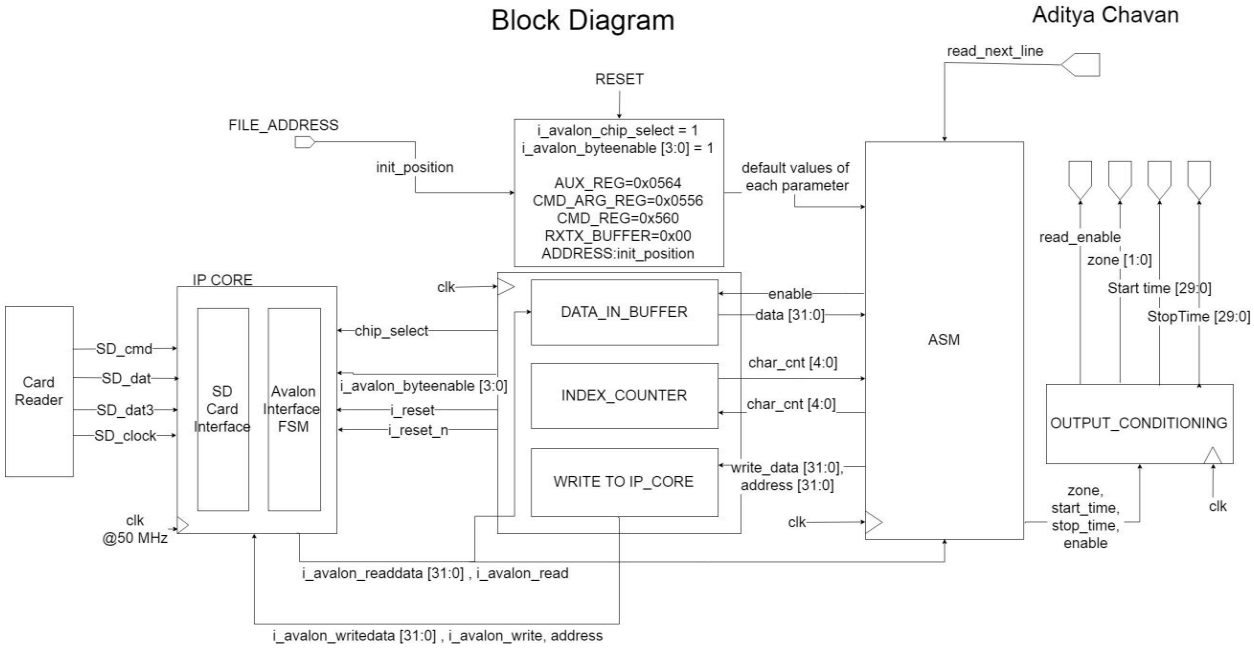

Table 3 ICD of SD Card

PIN NAME	FORMAT	DESCRIPTION
file_address	Input,[31:0]	This 32 bit line will contain the memory location of the file to be read.
read_next_line	input,1 bit	When this bit is set to 1, the next line will be read from the SD card and data will be produced at the output pins. Read_enable will indicate when the operation is done.
read_enable	Output,1 bit	Pulled up to 1 to acknowledge that data on the output busses is valid (when we finish reading the data from the SD card.) 0 when read operation is still being performed.
zone	Output,[1:0]	2 bit wide signal indicating which of the 4 zones are to be watered.
start_time	Output,[24:0]	30 bit wide signal containing time when sprinklers are to be started in HHMMSS format, (in integer values).
stop_time	Output,[24:0]	30 bit wide signal containing time when sprinklers are to be stopped in HHMMSS format, (in integer values).
data	[31:0]	Data read from the SD Card
char_cnt	[4:0]	Counter for storing which character to read
write_data	[31:0]	Line for writing commands or data to the SD Card
address	[31:0]	Indicates the address from wich to read or write
init_position	[31:0]	Defines the starting address of the file
i_avalon_byteenable	[3:0]	enables Byte reads for the Avalon core
i_avalon_read	1 bit	Pulled HIGH to read from SD Card
i_avalon_readdata	[31:0]	data read from the IP Core
i_avalon_write	1 bit	Pulled HIGH to write to the IP Core
i_avalon_write_data	[31:0]	data read from the IP Core
clk	1 bit	Clock
i_reset,i_reset_n	1 bit	reset signal for the IP Core
RESET	1 bit	reset signal for the SD Card sub system

GPS MODULE:

BLOCK DIAGRAM:

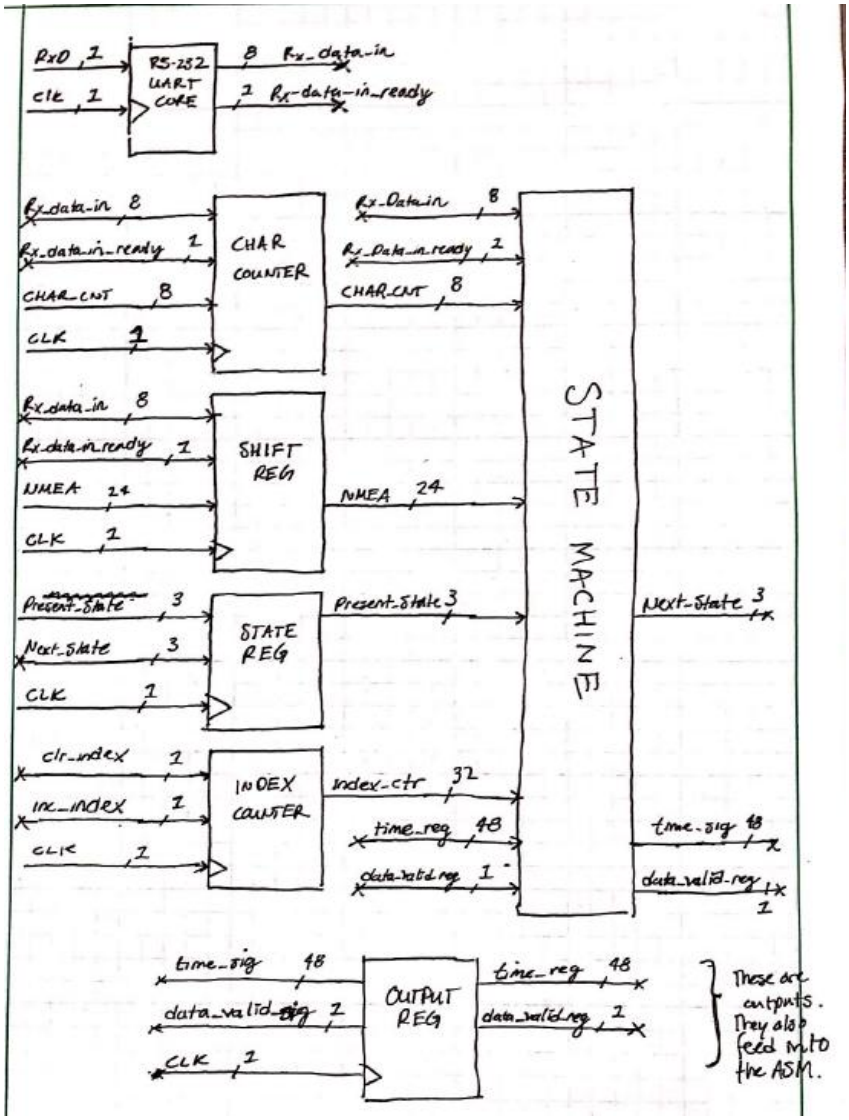

Table 3 ICD of GPS

PIN NAME	FORMAT	DESCRIPTION
RxD_Data_in_ready	Input, 1 bit	States whether the data is ready

RxD_data_in	Input, [7:0]	Data_in for the GPS
time_out	output, [47:0]	Time information from the GPS
data_valid_out	output,1 bit	Indicates whether the time indicated is valid or not
NMEA	[23:0]	Shift Register Output
PS	[2:0]	Present State
NS	[2:0]	Next State
clr_index	1 bit	Clears the Index counter
inc_index	1 bit	increments the Index counter
time_reg	[47:0]	Communicates the time
time_sig	[47:0]	Time signal
clk	input,1 bit	Clock
data_valid_sig	1 bit	Indicates if the data is valid or not

3.6.7 Rain Sensor

We assume this module is simple: If it's raining, it transmits 1'b1, and 1'b0 otherwise.

3.6.7.1 INTERFACE CONTROL DIAGRAM

Table 5 ICD of Rain Sensor

Outputs	Description
raining	1'b1 when it's raining; 1'b0 otherwise

4 APPENDIX A

4.1 Acronyms and Definitions.

ADC	Analog to Digital Converter
CW	Continuous Wave
dB	Decibels
dBFS	Decibels, referenced to full scale
dBm	Decibels, referenced to 1 milliwatt
ES	Electronic Support
FPGA	Field Programmable Gate Array
IF	Intermediate Frequency
kHz	Kilohertz
MHz	Megahertz
ns	Nanoseconds
RF	Radio Frequency
TBD	To Be Determined
µW	Microwatts

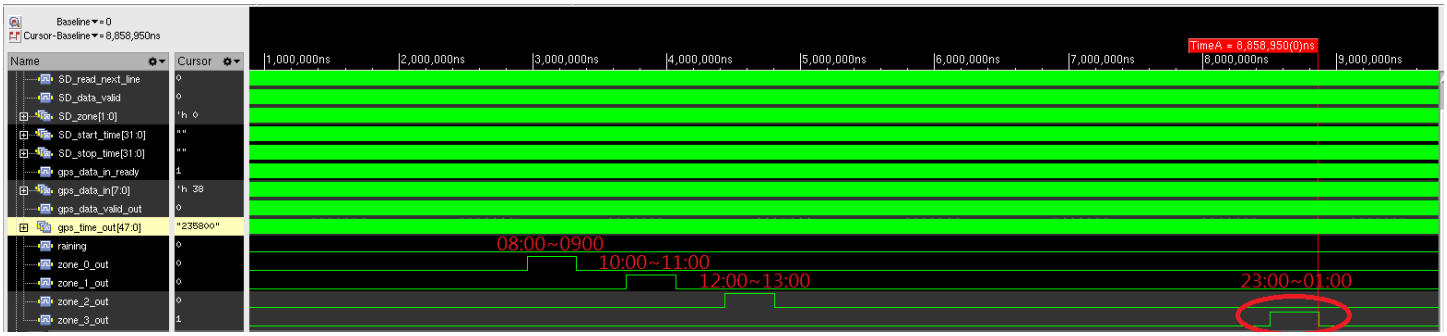

Figure 1: Top Level Testbench

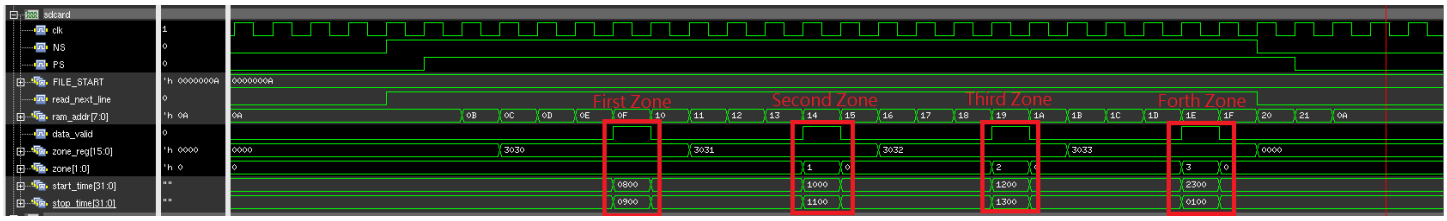

Figure 2: SD Card Testbench

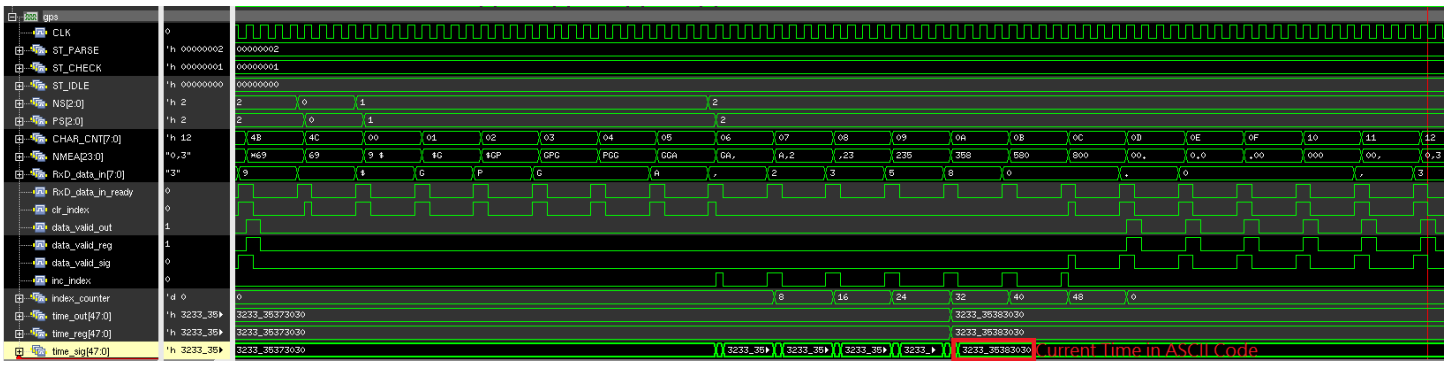

Figure 3: GPS Testbench