SEMINAR ON

VLSI Design: Modern Challenges

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Aditya Kumar Jha (2022UEE1038)

Submitted By:

Aditya Kumar Jha (2022UEE1038)

Supervised By:

Dr. Saravana Prakash P.

Assistant Professor

DEPARTMENT OF ELECTRICAL ENGINEERING
MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY JAIPUR, INDIA
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MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY, JAIPUR

CERTIFICATE

This is to certify that the seminar entitled “VLSI Design: Modern Challenges” submitted by Mr. Aditya Kumar Jha (2022UEE1038) at Malaviya National Institute of Technology Jaipur towards partial fulfilment of the requirements for the award of the degree of Bachelor of Technology in Electrical Engineering at Department of Electrical Engineering has been carried out by him under my supervision.

Dr. Saravana Prakash P.
Assistant Professor
Department of Electrical Engineering
MNIT Jaipur
Jaipur -302017, India

Place: Jaipur
Date:

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Thank you.

Aditya Kumar Jha

2022UEE1038

Malaviya National Institute of Technology Jaipur

ABSTRACT

The realm of Very Large-Scale Integration (VLSI) design stands at a crucial juncture, driven by the relentless push for miniaturization, enhanced performance, and energy efficiency in semiconductor devices. As the semiconductor industry approaches the physical limits of Moore's Law, VLSI design faces a confluence of challenges that necessitate innovative approaches and solutions. This paper explores the contemporary landscape of VLSI design, highlighting the primary challenges, emerging trends, and innovative solutions shaping the future of semiconductor technologies.

Key challenges in modern VLSI design include scaling limitations, power dissipation, variability, reliability, and design complexity. As feature sizes approach the atomic scale, quantum mechanical effects and process variations significantly impact device performance and yield. Furthermore, the increasing complexity of VLSI systems, coupled with stringent power and thermal constraints, poses significant hurdles for designers.

The exploration of novel design methodologies and tools emerges as a pivotal theme, emphasizing the role of machine learning and artificial intelligence in automating design optimization and verification processes. These technologies not only promise to accelerate the design cycle but also enhance the robustness and efficiency of VLSI systems.

In addressing power challenges, the paper reviews advances in low-power design techniques and energy-efficient architectures. Innovative approaches, such as approximate computing and adaptive voltage scaling, are examined for their potential to significantly reduce power consumption without substantially compromising performance.

In conclusion, navigating the modern challenges of VLSI design demands a multidisciplinary approach, leveraging advances in materials science, computational methods, and engineering innovations. As the paper illustrates, while the obstacles are formidable, the ongoing evolution of VLSI design methodologies and technologies holds the promise of overcoming these barriers, paving the way for the next generation of semiconductor devices.

LIST OF CONTENTS

LIST OF FIGURES

LIST OF ABBREVIATIONS

1.	VLSI	Very Large-scale Integration
2.	IC	Integrated Circuit
3.	SSI	Small Scale Integration
4.	MSI	Medium Scale Integration
5.	LSI	Large Scale Integration
6.	STA	Static Timing Analysis
7.	SoC	System on Chip
8.	**ASIC**	Application-Specific Integrated Circuit
9.	CMOS	Complementary MOSFET
10.	TDDB	Time-Dependent Dielectric Breakdown
11.	ALU	Arithmetic and Logic Unit
12.	LVS	Layout versus Schematic
13.	BFS	Breadth-First Search
14.	DFS	Depth First Search

Chapter-1

Introduction

1.1 General

VLSI represents a pivotal era in the evolution of circuit technology, marking the phase where the integration of thousands to millions of transistors onto a single semiconductor silicon chip became feasible. This technological marvel has been the cornerstone of the modern electronics revolution, enabling the development of powerful, compact, and energy-efficient electronic devices that pervade almost every aspect of contemporary life. From smartphones and computers to advanced medical devices and automotive systems, VLSI technology plays a fundamental role in driving innovation and functionality in a wide array of electronic products.

The journey toward VLSI began in the late 1950s and early 1960s with the advent of the integrated circuit (IC), which allowed for multiple transistors to be fabricated on a single chip. However, it was in the 1970s and 1980s that the VLSI era truly took shape, characterized by the rapid escalation in the complexity and capabilities of ICs. This period witnessed the transition from Small Scale Integration (SSI) and Medium Scale Integration (MSI), where circuits contained dozens to hundreds of transistors, to Large Scale Integration (LSI) and eventually VLSI, pushing the transistor counts into the millions.

The essence of VLSI technology lies in its ability to miniaturize electronic components and integrate them into compact chips, thus offering several significant advantages:

- **Increased Performance:** By reducing the size of transistors and the distances between them, VLSI chips achieve higher speed and lower power consumption.
- **Reduced Cost:** Integrating a vast number of components on a single chip reduces the per-component cost significantly, making advanced electronic devices more affordable.
- **Enhanced Functionality:** VLSI enables the integration of complex circuits and systems (e.g., microprocessors, memory chips, and sensors) onto a single chip, facilitating sophisticated functionalities within compact devices.
- **Improved Reliability:** With fewer interconnections compared to discrete component circuits, VLSI chips exhibit higher reliability and lower failure rates.

1.2Moore’s Law

Moore's Law is a pivotal observation in the semiconductor industry that has significantly influenced the development and evolution of electronic devices over the past several decades. It was first articulated by Gordon Moore, co-founder of Intel, in 1965. Moore observed that the number of transistors on a microchip doubles approximately every two years, though the cost of computers is halved. This observation not only described a trend but also set an expectation for the pace of technological advancement in the semiconductor industry.

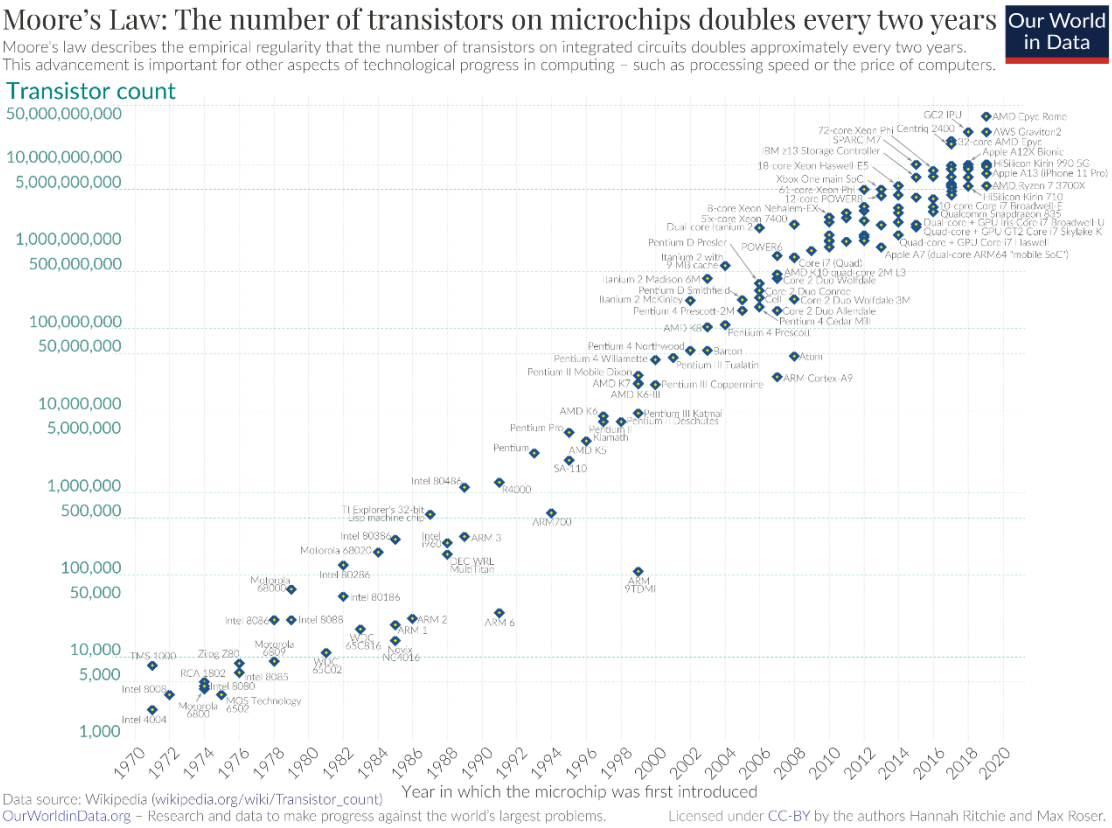

Figure 1.2: Graph of Moore’s Law

Chapter-2

VLSI Physical Design Automation

2.1 Partitioning and Floorplanning

Partitioning and floorplanning are fundamental stages in the design process of Very Large Scale Integration (VLSI) circuits, crucial for optimizing chip layout, performance, and functionality. These processes play a significant role in determining how components are organized and interconnected on a semiconductor chip, ultimately influencing factors such as signal propagation delays, power consumption, and manufacturing yield.

Partitioning involves dividing the entire VLSI design into smaller, manageable blocks or modules, each responsible for specific functions or tasks. This division is typically based on factors such as functionality, performance requirements, and design constraints. There are several types of partitioning techniques commonly used in VLSI design:

Hierarchical Partitioning: Involves dividing the design into multiple hierarchical levels, with each level representing increasingly finer-grained partitions. This approach simplifies the design process by breaking down complex systems into more manageable sub-blocks.

Functional Partitioning: Groups together components that perform related functions or tasks, facilitating modular design and enabling independent optimization of each functional block.

Physical Partitioning: Considers physical constraints such as chip area, routing resources, and manufacturing considerations to divide the design into spatially separated regions.

Constraint-Driven Partitioning: Takes into account specific design constraints such as timing requirements, power consumption targets, and area constraints to guide the partitioning process and ensure optimal design outcomes.

Effective partitioning is essential for balancing trade-offs between various design metrics, such as performance, area, power, and manufacturability. It enables efficient utilization of resources, reduces design complexity, and facilitates parallel development of different design blocks by different teams.

Floorplanning involves determining the physical placement of partitions/modules within the chip layout, as well as defining the interconnections between them. This stage is critical for optimizing chip area utilization, minimizing signal routing delays, and meeting design constraints.

- **Chip Area Allocation**: Allocating appropriate chip area for each partition/module based on its size, functionality, and performance requirements.
- **Module Placement**: Placing partitions/modules within the chip layout while considering factors such as signal interconnectivity, power distribution, and thermal considerations.

- **Routing Regions**: Defining routing regions and allocating space for signal routing channels to ensure efficient signal propagation and minimize routing congestion.
- **Design Constraints**: Incorporating various design constraints such as timing constraints, power delivery requirements, and manufacturing constraints into the floorplan to meet design specifications.

Effective floorplanning requires careful consideration of design trade-offs and iterative refinement to achieve optimal results. Advanced floorplanning tools and methodologies leverage techniques such as iterative optimization algorithms, constraint-driven placement, and floorplan-aware routing to streamline the floorplanning process and improve design quality.

Figure 2.1 represents floorplanning of a silicon wafer

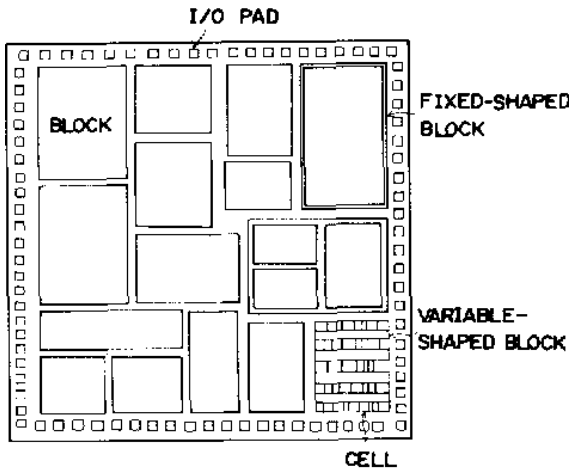

Figure 2.1: Floorplanning of chip

2.2 Placement

Placement in Very Large Scale Integration (VLSI) design refers to the process of determining the physical locations of electronic components, such as transistors, gates, and cells, within the layout of a semiconductor chip. It is a crucial step in the overall design process and significantly impacts the performance, power consumption, and manufacturability of the integrated circuit (IC).

Key Aspects of Placement:

a. Optimization Objectives: Placement aims to optimize various design metrics, including:

- **Timing**: Minimizing signal propagation delays and meeting timing constraints to ensure proper functionality and performance.
- **Area**: Efficiently utilizing chip area to accommodate all components while minimizing the overall chip size.
- **Power**: Reducing power consumption by optimizing the spatial arrangement of components and minimizing switching activities.

- **Routing Resources**: Facilitating efficient routing by organizing components in a way that minimizes wire lengths and congestion.

b. Hierarchical Placement: Involves organizing components into hierarchical levels and performing placement at each level, from macro-level (top-level placement of large blocks) to micro-level (placement of individual cells within blocks). This approach enables manageable design complexity and facilitates design refinement at different abstraction levels.

Some of the methods of placement are:

Analytical Placement: Utilizes mathematical optimization techniques, such as simulated annealing, quadratic placement, and linear programming, to explore placement solution spaces and identify optimal placements based on specified objectives and constraints.

Machine Learning-Based Placement: Applies machine learning algorithms, such as reinforcement learning and neural networks, to learn placement patterns from historical placement data and automatically generate placement solutions that optimize specific design metrics.

Figure 2.2 depicts standard placed cells on a silicon wafer.

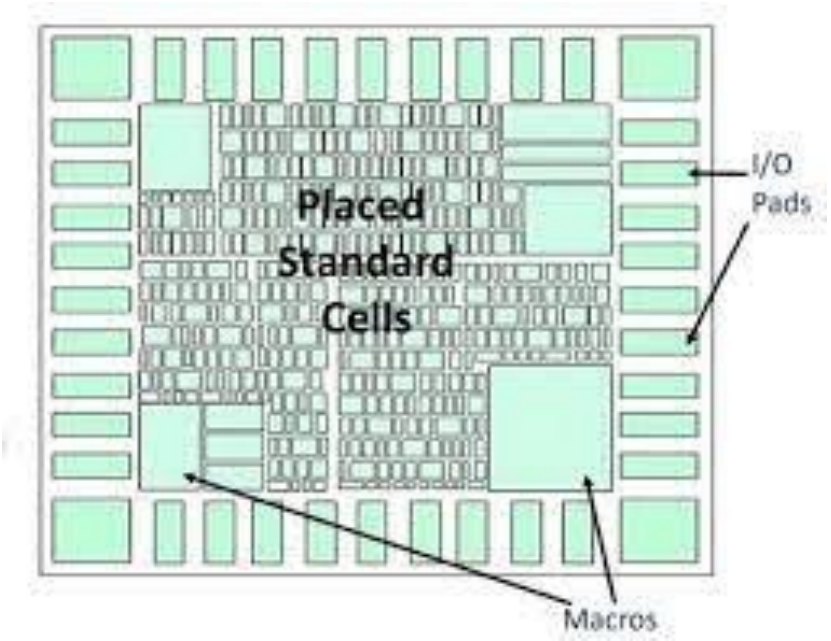

Figure 2.2: Standard cell placement on chip

2.3 Routing

Routing in Very Large Scale Integration (VLSI) design refers to the process of establishing physical connections between the various electronic components (such as transistors, gates, and cells) within a semiconductor chip. These connections, often referred to as nets, facilitate the flow of signals between different components, enabling the functionality of the integrated circuit (IC).

Routing in VLSI design is a critical step that involves establishing efficient and reliable connections between electronic components within a semiconductor chip. Routing takes 30% of the design time and a large percentage of the layout area. Good placement is also very crucial for routing. Advanced routing techniques and algorithms play a vital role in addressing the complexities of modern semiconductor designs and enabling the development of high-performance, high-quality integrated circuits.

We also need to consider clock and power routing as well. Issues in clock routing can create clock skews which may disrupt the working of the circuit and power routing rails should be made very carefully as the high voltage signal running through this rail may create crosstalk issues due to the development of parasitic capacitance and induce delays.

Figure 2.3 represents how placement can increase the difficulty of routing

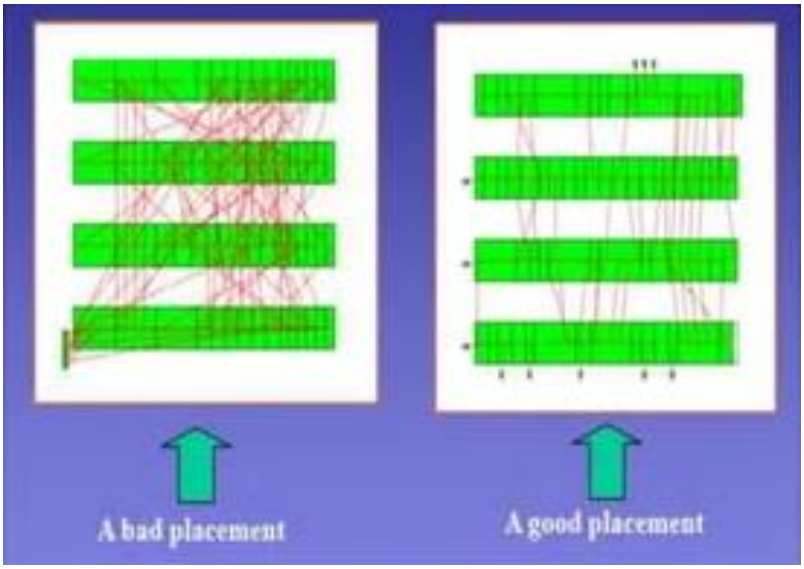

Figure 2.3: Routing with good and bad placement

2.4 Static Timing Analysis

Static Timing Analysis (STA) is a critical step in the design and verification process of Very Large Scale Integration (VLSI) circuits. It plays a crucial role in ensuring that the timing requirements of the circuit are met, which is essential for its proper functionality and performance. STA involves analysing the timing behaviour of a digital circuit under a specific set of conditions, typically considering factors such as signal propagation delays, clock timing, and setup and hold times.

The Circuit Netlist is analysed to determine the worst-case circuit delays to predict maximum possible clock frequency. Thus, timing optimization is performed so that circuit can run faster.

2.5 Physical Verification and Design Signoff

Physical Verification and Design Signoff are critical stages in the VLSI (Very Large Scale Integration) design flow, ensuring that the designed chip meets the specifications and is ready

for fabrication. These processes involve rigorous checks and analyses to verify the correctness, integrity, and manufacturability of the design layout.

Physical Verification encompasses a series of checks to ensure that the layout design adheres to design rules, meets fabrication constraints, and is free from manufacturing defects. Key aspects of physical verification include:

1.**Design Rule Check (DRC**): DRC verifies whether the layout design complies with the manufacturing rules specified by the foundry or fabrication facility. It detects violations such as spacing violations, overlap violations, width violations, and other geometric violations that could lead to manufacturing defects.

2. **Layout vs. Schematic (LVS) Check**: LVS compares the layout design against the corresponding schematic representation to ensure that they are functionally equivalent. It verifies that the connections, device sizes, and electrical properties in the layout match the intended circuit functionality defined in the schematic.

3. **Electrical Rule Check (ERC)**: ERC verifies electrical connectivity and integrity within the layout design. It detects issues such as floating nodes, missing connections, and incorrect net connections that could lead to functional failures or reliability issues in the fabricated chip.

4. **Antenna Rule Check (ARC)**: ARC ensures that the layout design has adequate protection against electrostatic discharge (ESD) and latch-up by verifying the presence of properly sized and connected diodes or other protection structures around signal inputs and outputs.

5. **Design for Manufacturing (DFM) Checks**: DFM checks and analyses the layout design for manufacturability issues, such as lithography hotspots, metal density variations, and other factors that could affect the yield and reliability of the fabricated chip.

Design Signoff marks the culmination of the design process, indicating that the chip design has met all necessary requirements and is ready for fabrication. Key aspects of design signoff include:

1. **Timing Signoff**: Timing signoff verifies that the design meets timing requirements, including setup and hold times, clock skew, and other timing constraints. It ensures that the chip operates within specified performance targets and meets timing closure objectives.

2. **Power Signoff**: Power signoff analyzes power consumption and distribution within the chip to ensure that it meets power budget constraints and thermal requirements. It includes static and dynamic power analysis, power grid integrity checks, and thermal simulations to ensure reliable operation under different operating conditions.

3. **Area Signoff**: Area signoff verifies that the chip layout meets area constraints and utilizes the available silicon area efficiently. It ensures that the chip size is within budget and that no unnecessary overheads are introduced during the design process.

4. **Functional Signoff**: Functional signoff ensures that the chip design functions correctly and meets the intended specifications. It involves comprehensive simulation and verification tests to validate the functionality of the design under different operating conditions and corner cases.

5. **Reliability Signoff**: Reliability signoff evaluates the chip design for reliability and robustness against aging, process variations, and environmental factors. It includes reliability analysis such as electromigration, time-dependent dielectric breakdown (TDDB), and other reliability metrics to ensure long-term reliability and performance.

By performing thorough physical verification and design signoff, VLSI designers ensure that the chip design is free from errors, meets all specifications, and is ready for successful fabrication and deployment in electronic devices. These stages are critical for achieving high-quality, reliable, and manufacturable semiconductor products in today's competitive market.

Chapter-3

Main Challenges and Solutions

The consumer market for VLSI ASIC is expanding rapidly every day due to mobile devices like Smartphones, Tablets, and Laptops. The new HCI rapidly became available at the hands of every person which made the market bloom and also opened opportunities for SoC. However, it has also brought many challenges:

- Mobile devices are wireless and run on batteries corresponding VLSI must consume low power.
- The Figure of Merit (performance/watt) should still be maximized
- Technology is advancing as per Moore's Law and faces physical limitations

3.1 Routing problem and maze algorithm

In the context of VLSI design, routing refers to the process of determining the physical paths for interconnecting various components (such as transistors, gates, and cells) on a semiconductor chip. The routing problem involves finding efficient and optimized routes for connecting all required signal paths while adhering to design constraints and minimizing signal delays, power consumption, and routing congestion.

The routing problem in VLSI design can be complex due to the following factors:

1. **Design Constraints:** Routing must adhere to various design constraints such as timing requirements, signal integrity, power delivery, and manufacturability constraints imposed by the fabrication process.

2. **Routing Resources:** The availability of routing resources, such as metal layers, vias, and routing channels, imposes limitations on the routing topology and affects routing feasibility and congestion.

3. **Timing Closure:** Achieving timing closure, i.e., ensuring that signal paths meet timing requirements, is a critical aspect of routing. Timing-driven routing algorithms prioritize routing paths to minimize signal delays and meet timing constraints.

4. **Congestion Management:** Routing congestion occurs when multiple signal paths compete for limited routing resources, leading to routing delays and potential signal integrity issues. Efficient congestion management algorithms are essential for mitigating congestion and ensuring smooth signal routing.

Maze routing algorithms can be used to solve the routing problem in VLSI design. These algorithms are inspired by maze-solving techniques and aim to find paths through a maze-like grid that represents the chip layout. Key characteristics of maze routing algorithms include:

1. **Grid Representation:** The chip layout is represented as a grid of cells, where each cell corresponds to a routing track or routing channel. The grid contains obstacles representing fixed objects such as cells, blocks, and routing obstructions.

2. **Pathfinding:** Maze routing algorithms use pathfinding techniques, such as breadth-first search (BFS), depth-first search (DFS), Dijkstra's algorithm, or A* algorithm, to explore possible routing paths from source to destination points on the grid.

3. **Obstacle Avoidance:** Maze routing algorithms consider obstacles and routing constraints during pathfinding to avoid collisions with fixed objects and ensure feasible routing paths.

4. **Optimization:** Various optimization techniques, such as wire length minimization, congestion-aware routing, and timing-driven routing, are integrated into maze routing algorithms to optimize routing paths and meet design objectives.

3.2 Power optimization

Power consumption is a very big challenge in modern-day VLSI design. Almost all portable devices run on battery power and as such sometimes optimizing power consumption is more crucial than increasing the performance of IC.

There are majorly 3 types of power dissipation which need to be taken care of when considering VLSI design:

1. Dynamic Power
2. Short Circuit Power
3. Static Power

3.2.1 Dynamic Power

Dynamic power is a significant component of total power consumption in VLSI (Very Large Scale Integration) design, representing the power dissipated due to the switching activity of digital circuits. It is primarily associated with the charging and discharging of capacitive loads within the circuit during the transition of logic states, such as from high to low or vice versa. Dynamic power consumption occurs when transistors switch states, causing current to flow momentarily and dissipate energy.

Some factors affecting the dynamic power dissipation are:

1. **Switching Activity**: Dynamic power consumption is directly proportional to the frequency and magnitude of switching events within the digital circuit. Higher switching activity, resulting from frequent transitions between logic states, leads to increased dynamic power.

2. **Capacitive Load**: The capacitance of interconnects, gates and other components in the circuit influences dynamic power consumption. Higher capacitance results in increased charging and discharging currents, leading to higher dynamic power.

3. **Supply Voltage**: Dynamic power consumption is proportional to the square of the supply voltage. As the supply voltage increases, the energy dissipated per switching event increases, resulting in higher dynamic power consumption.

4. **Clock Frequency**: Dynamic power consumption scales linearly with the clock frequency of the circuit. Higher clock frequencies lead to more frequent switching events and increased dynamic power consumption.

5. **Technology Node**: The feature size and technology node of the semiconductor process affect dynamic power consumption. Smaller feature sizes reduce capacitance and switching energy, resulting in lower dynamic power consumption.

Some techniques to reduce Dynamic Power are:

1. **Clock Gating**: Disabling clock signals to inactive circuit blocks during idle periods reduces switching activity and dynamic power consumption.

2. **Power Gating**: Temporarily shutting down power to unused circuit blocks or modules minimizes dynamic power consumption.

3. **Dynamic Voltage and Frequency Scaling (DVFS)**: Adjusting the supply voltage and clock frequency dynamically based on workload or performance requirements reduces dynamic power while maintaining desired performance levels.

4. **Low-Power Design Techniques**: Utilizing energy-efficient circuit design techniques such as asynchronous logic, multi-threshold CMOS, and low-power arithmetic and logic units (ALUs) reduces dynamic power consumption.

5. **Gate Sizing and Placement**: Optimizing gate sizes and placement to minimize capacitive load and reduce signal transition activity helps reduce dynamic power consumption.

By implementing these techniques and optimizing circuit design, VLSI designers can effectively reduce dynamic power consumption and improve the overall energy efficiency of digital circuits, leading to longer battery life and reduced operating costs in electronic devices.

3.2.2 Static Power

Static power, also known as leakage power, is a significant component of total power consumption in VLSI (Very Large Scale Integration) design. Unlike dynamic power, which is associated with the switching activity of digital circuits, static power represents the power dissipated by transistors even when they are not actively switching. It occurs due to leakage currents flowing through transistors and other components, resulting in power dissipation without any meaningful work being performed.

Factors Contributing to Static Power:

1. **Subthreshold Leakage**: Subthreshold leakage occurs when transistors operate in the subthreshold region, where the gate-source voltage is below the threshold voltage (Vth). In this region, transistors exhibit leakage currents due to the diffusion of carriers through the channel, leading to static power dissipation.

2. **Gate Leakage**: Gate leakage occurs due to the flow of reverse-biased leakage currents through the gate oxide of transistors. As transistor feature sizes shrink, gate leakage becomes more pronounced, contributing significantly to static power consumption.

3. **Reverse Bias Leakage**: Reverse bias leakage occurs when transistors are subject to reverse bias conditions, such as in isolation structures and diode-connected transistors. Reverse bias leakage currents flow through the substrate and junctions, contributing to static power dissipation.

4. **Temperature and Process Variations**: Temperature variations and process variations affect transistor characteristics, leading to variations in leakage currents and static power consumption. Higher temperatures and process variations can exacerbate static power dissipation.

Techniques to Reduce Static Power:

1. **Transistor Sizing**: Increasing the transistor threshold voltage (Vth) and reducing the subthreshold leakage current by sizing transistors appropriately.

2. **Power Gating**: Temporarily shutting down power to unused circuit blocks or modules using power gating techniques to reduce leakage currents.

3 **Gate Oxide Thickness**: Optimizing gate oxide thickness to minimize gate leakage currents, especially in advanced CMOS processes.

4. **Sleep Transistors**: Inserting sleep transistors at the input ports of unused circuit blocks to isolate them from the power supply and reduce leakage currents.

5. **Substrate Biasing**: Applying substrate biasing techniques to control leakage currents in isolation structures and diode-connected transistors.

6. **Low-Power Design Methodologies**: Incorporating low-power design methodologies such as voltage scaling, clock gating, and multi-threshold CMOS to reduce both static and dynamic power consumption.

By implementing these techniques and optimizing circuit design, VLSI designers can effectively reduce static power consumption, leading to improved energy efficiency and longer battery life in electronic devices. Static power management is essential for achieving the desired power-performance trade-offs in modern semiconductor designs.

Conclusion

In conclusion, this report has provided a comprehensive overview of Very Large-Scale Integration (VLSI) design, tracing its evolution from the early integrated circuit era to the modern-day semiconductor technology landscape. VLSI technology has played a pivotal role in revolutionizing the electronics industry, enabling the development of powerful, compact, and energy-efficient electronic devices that permeate various aspects of contemporary life.

Throughout the report, we have explored key concepts and stages in the VLSI design process, including partitioning, floorplanning, placement, routing, static timing analysis, physical verification, and design signoff. Each stage contributes to the overall success of a VLSI design by optimizing chip layout, functionality, performance, and manufacturability.

Moreover, the report has highlighted the main challenges faced by VLSI designers in today's rapidly evolving semiconductor landscape. These challenges include power consumption optimization, technology scaling limitations, routing complexity, and meeting design specifications within shrinking time-to-market windows.

To address these challenges, various solutions and techniques have been discussed, ranging from power optimization strategies to advanced routing algorithms and design verification methodologies. These solutions aim to improve energy efficiency, enhance design reliability, and streamline the VLSI design flow to meet the demands of modern electronic devices.

However, as our technology advances we switch and we face physical limitations to Moore’s Law we switch to Modern FinFet technology but this overhauls all the design parameters we have been using to design chips as the lambda parameter is no more useful.

Overall, this report serves as a valuable resource for VLSI designers, engineers, and researchers, providing insights into the complexities of VLSI design and offering practical solutions to overcome the challenges encountered in the field. As technology continues to advance, the principles and methodologies outlined in this report will remain essential for achieving high-quality, reliable, and manufacturable semiconductor products in today's competitive market.

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