Design and Analysis of a Fully Differential Two-Stage CMOS Op-Amp with Miller Compensation

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Abstract

The paper presents a design and implementation of fully differential, two stage CMOS operational amplifier using a miller capacitor for compensation. The design is to be implemented using 28ηm synopsis PDK. Op-amp designed here exhibits DC gain of >50 dB, 30MHz unity gain bandwidth, phase margin of >45^0, and slew rate >10 V/µS for typical 1 pF differential capacitive load. The power dissipation should be <500µW.

1. Reference Circuits Details

An op-amp produces an output voltage that is typically hundreds of thousands times larger than the voltage difference between its input terminals. The differential stage of opamp is formed using transistor M1, M2, M3 and M4 form the differential stage of the op-amp. The two nMOS transistors M1 and M2 form the differential inputs of the amplifier. The resistance of the input transistors and active load transistors which are M3 and M4 are the main resistances that contribute to the output. The transistors M6 and M7 forms a current sink load inverter. Compensation capacitor (CC) is connected to the output of the first stage. Its function is to reduce the frequency of the dominant pole and move the output pole away from the origin (Razavi, 2001).

The 7 pack two stage opamp is designed for the following specifications for 180ηm.

Table I: Design Parameters of proposed Opamp Design

Sl.No	Parameter	Specification
1.	I_{REF}	1µA
2.	DC Gain	>50dB
3.	Unity Gain Bandwidth	30MHz
4.	Phase Margin	>45^0
5.	C_L	1pF
6.	Power Dissipation	<500µW
7.	Slew Rate	>10V/µs

2. Final Schematic Circuit

The figure 1 shows the schematic of two stage Op-Amp with miller compensation.

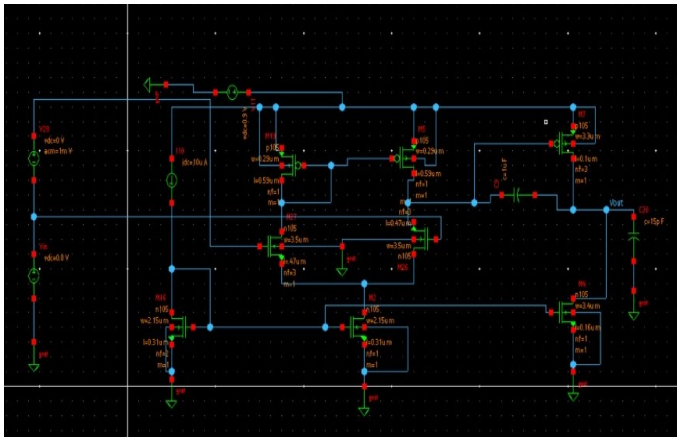

Fig. 1: Schematic of two stage Op-Amp with Miller Compensation

3. Simulation Results

Figure 2 shows the frequency plot of two stage Op-Amp with Miller Compensation.

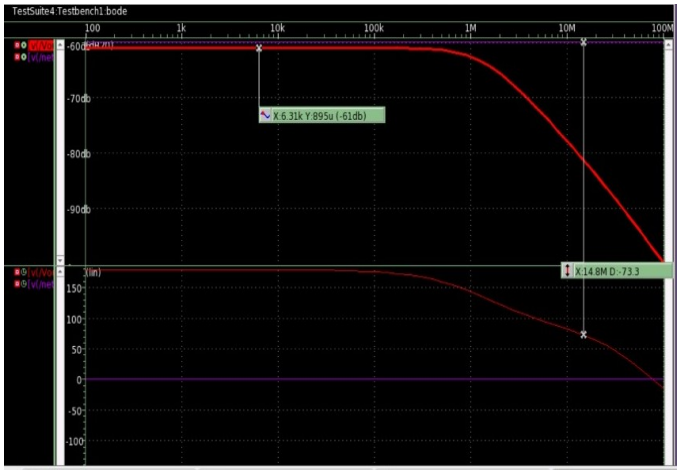

Fig. 2: Frequency Response of two stage Op-Amp with Miller Compensation

References

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