# **Contents**

User Requirements & Technical Specifications ………………………………………………………2

Assumptions & Justifications ……………………………………………………………………………2

Assumptions ……………………………………………………………………………………. 2

Justification ………………………………………………………………………………………2

Components used with justification …………………………………………………………………….3

Address Map ……………………………………………………………………………………………...5

Memory Map ……………………………………………………………………………………..5

I/O Map …………………………………………………………………………………………...6

Flow Chart ………………………………………………………………………………………………...7

Main Program ……………………………………………………………………………………7

Write ………………………………………………………………………………………………8

Read ………………………………………………………………………………………………9

Display PASS …………….…………………………………………………………………….10

Display FAIL …………….………………………………………………………………………11

## **User Requirements & Technical Specifications**

Design a microprocessor-based RAM tester that tests a RAM bit by bit and displays PASS/FAIL on a 7-segment LED display

The technical specifications are as follows

* The tester should be able to test 6164 RAM chips.
* The tester tests each bit of the RAM individually.
* User will place the 6164 chip in the zip socket, then press a switch labeled TEST.

## **Assumptions and Justifications**

**Assumptions:**

The user shall not replace/remove the test RAM being tested after pressing the switch before the result is displayed.

## **Justification:**

1. We are using the first 8255 for displaying the result and to take the input of the test switch. Port C is connected to the 4 7 segment displays. Port B is used for enabling and disabling the 7 segment display.
2. We are using the second 8255 for giving data and control signals to the test RAM . Port A is not used. Port B and Port C (PC0 - PC4) is used for giving addresses to the RAM chip. Port C (PC5 - PC7) is used for giving read, write and chip enable signals.
3. We are using a third 8255 to give addresses to the test RAM. Port A is made to toggle between input and output. It works as output to write data on the RAM chip and as input to read data from the RAM chip.

## **Components used with justification**

| **CHIP. NO.** | **QUANTITY** | **CHIP** | **PURPOSE** |
| --- | --- | --- | --- |
| 8086 | 1 | Microprocessor | Central Processing Unit |
| 8255 | 3 | Programmable Peripheral Interface (PPI) with 24 I/O lines | To control the I/O devices and interfaces the CPU to the test ram, 7-segment LED display and start switch |
| 6164 | 1 | 8K SRAM | For storing samples |
| 6116 | 2 | 2K SRAM | For storing samples and memory |
| 2716 | 4 | 2K EROM | For interrupt vector table and RESET signal |
| 74LS138 | 3 | 3 Line to 8 Line Decoder | One to select between 8255’s and other two for memory interfacing |
| 74LS373 | 3 | Octal D-type Transparent Latches with 3 state outputs | To latch outputs |
| 74LS245 | 2 | Octal Bus Transceivers with tristate output/Bidirectional Buffer | To strengthen signals |
| 8284 | 1 | 5MHz Clock | Input clock to 8086 |

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### **Other Hardware devices :**

1. **Switches**:

Interactive SW-SPDT-MOM Latched Action (Single Pole Double Throw Switch). One input terminal and two output terminals used to start the memory testing.

1. **LED**:

7 segment-MPX1-CC uses Red,1-digit, Common Cathode, 7-segment display.

1. **Zip socket**:

It is used for the easy insertion of the test RAM in the circuit.

## **Memory Mapping**

We require 2 X 4kb of ROM and 1 X 4kb of RAM for which we have used 4 chips of 2716 ROM and 2 chips of 6116 RAM.

| RAM1 (EVEN) | 01000h - 01FFEh |
| --- | --- |
| RAM1 (ODD) | 01001h - 01FFFh |
| ROM1 (EVEN) | 00000h - 00FFEh |
| ROM1 (ODD) | 00001h - 00FFFh |
| ROM2(EVEN) | FF000h - FFFFEh |
| ROM2(ODD) | FF001h - FFFFFh |

01000 - 01FFF

| A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

00000-00FFF

| A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

FF000 - FFFFF

| A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## **I/O Mapping**

**8255(1)**

| PART A | 00H |
| --- | --- |
| PART B | 02H |
| PART C | 04H |
| CONTROL REGISTER | 06H |

**8255(2)**

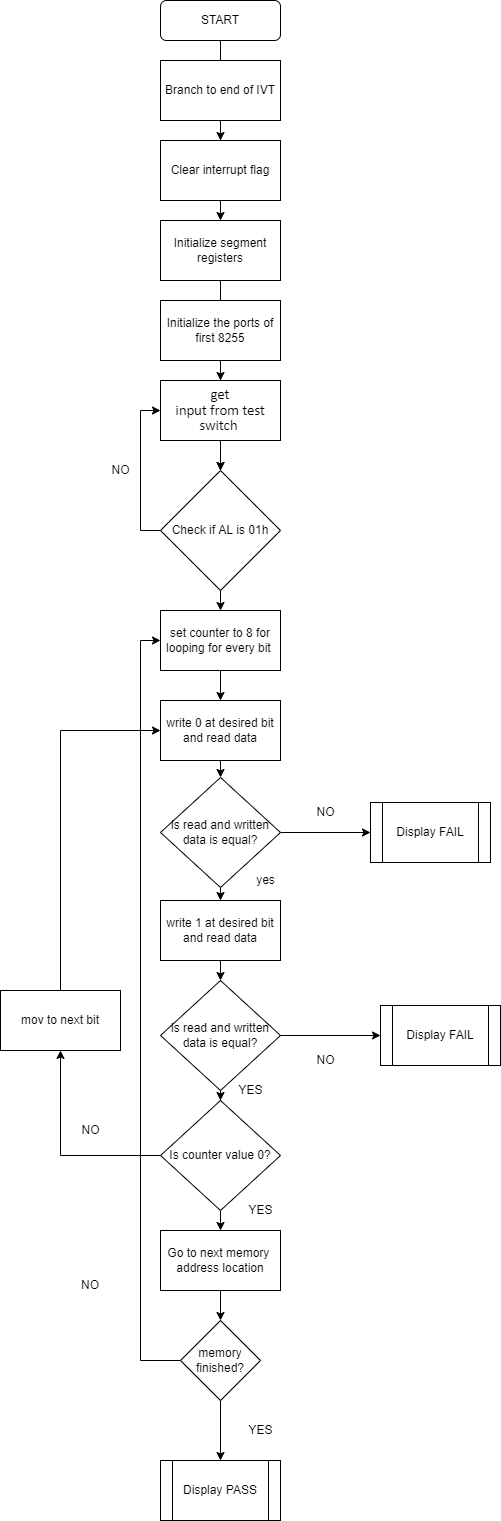
| PART A | 08H |
| --- | --- |
| PART B | 0AH |
| PART C | 0CH |
| CONTROL REGISTER | 0EH |

**8255(3)**

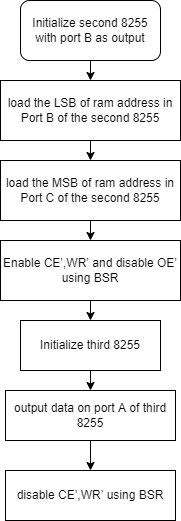
| PART A | 10H |
| --- | --- |
| PART B | 12H |
| PART C | 14H |
| CONTROL REGISTER | 16H |

## **Flow Chart**

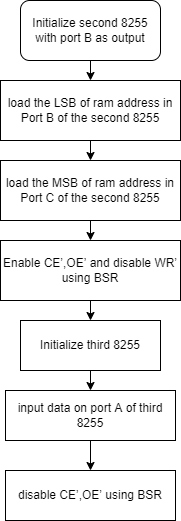
**Main Program:**



## **WRITE :**



## **READ :**



## **Display PASS:**

## **Display FAIL**