

Team Kaiser

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The Two Stage Op-Amp

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PS Overview

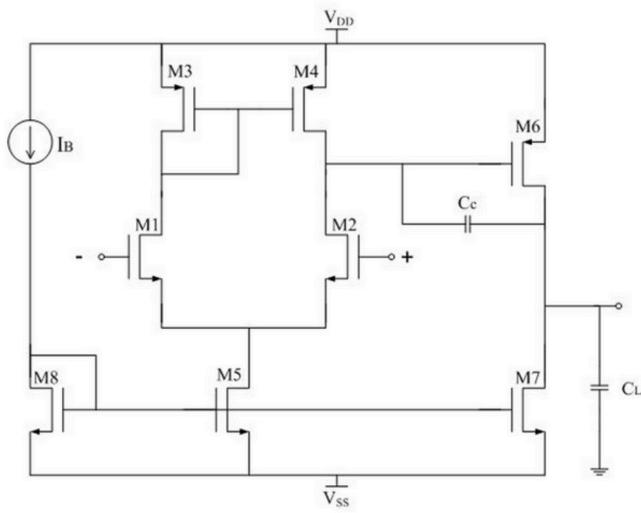


Figure 1: NMOS Two Stage op amp

In designing a two-stage miller-compensated op-amp with a capacitive load, the engineer sets V_{SS} in the provided figure to 0, representing ground. A typical two-stage op-amp configuration serves as the basis for this design transformation. The engineer proceeds to convert this configuration into third-person form, ensuring clarity and precision in the description of the design process and components involved.

Design Specifications

DC gain = 2000

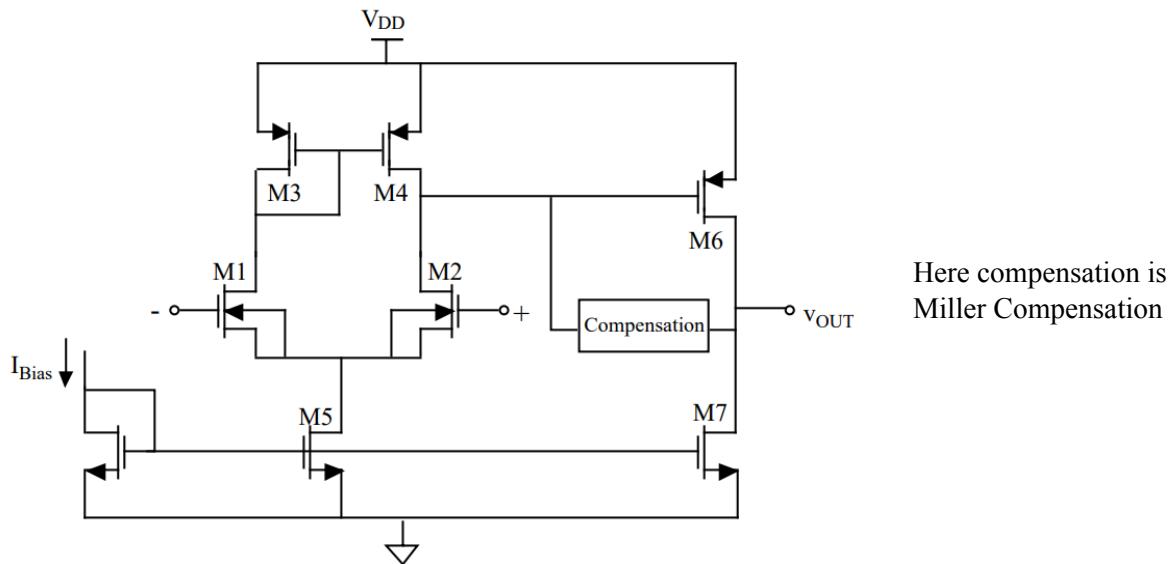
- ❖ Input Common Mode Range 0.7V to 1.6V..
- ❖ Phase Margin > 60°
- ❖ Capacitive load of 5pF

- ❖ Gain-bandwidth(GBW) product of 50 MHz
- ❖ For NMOS, $\mu_n C_{ox} = 100 \mu A/V^2$ and $V_{th} = (0.7 \pm 0.15) V$
- ❖ For PMOS, $\mu_p C_{ox} = 50 \mu A/V^2$ and $V_{th} = (-0.7 \pm 0.15) V$
- ❖ Also, $\lambda_n = 0.05 V^{-1}$ and $\lambda_p = 0.04 V^{-1}$ where λ is the channel length modulation parameter

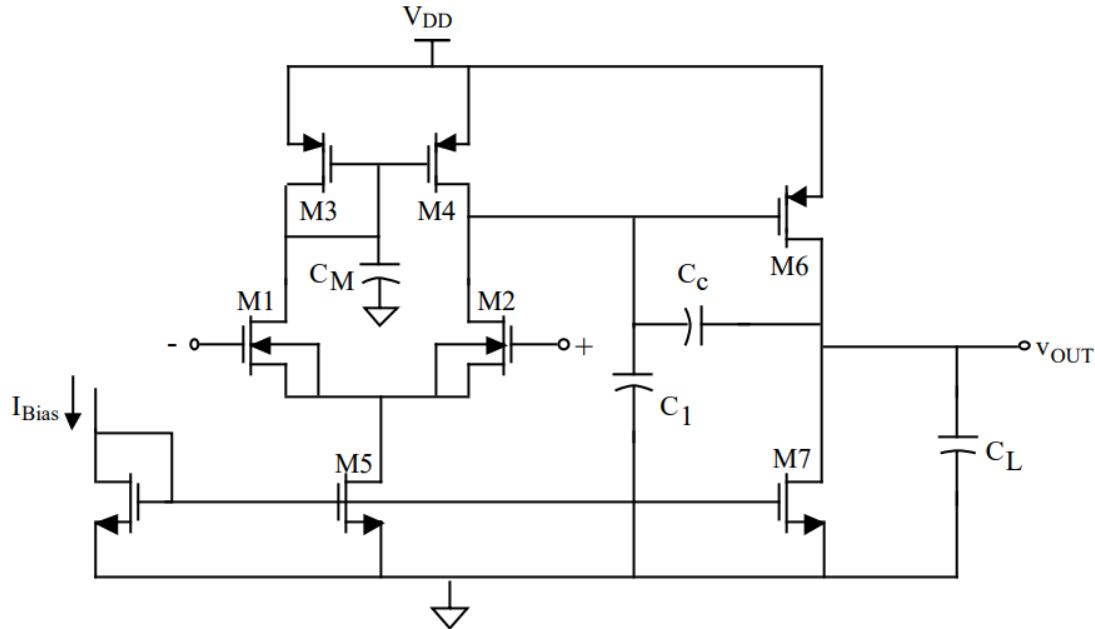
Design Equations

Our aim is to design a two stage operational amplifier with above given specifications with Miller capacitor compensation.

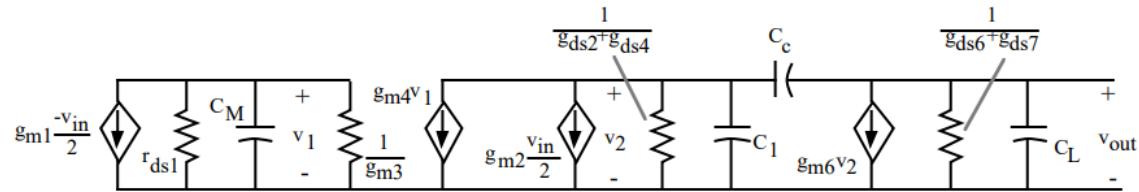
Op Amp Architecture



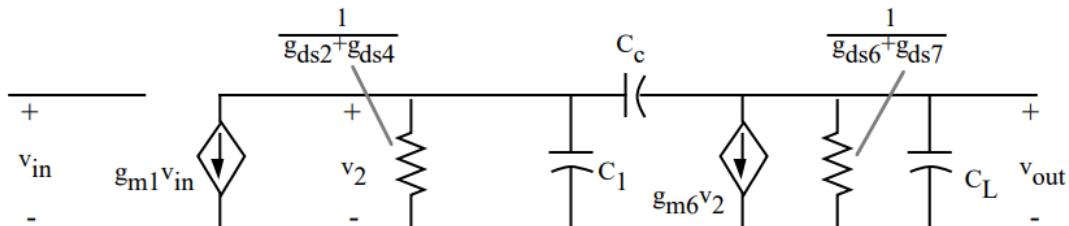
Miller Compensation



Small-signal model



Simplified small-signal model



Analysis

$$\frac{V_o(s)}{V_{in}(s)} = \frac{(g_{mI})(g_{mII})(R_I)(R_{II})(1 - sC_c/g_{mII})}{1 + s[R_I(C_1 + C_c) + R_{II}(C_L + C_c) + g_{mII}R_I R_{II}C_c] + s^2 R_I R_{II}[C_1 C_L + C_c(C_1 + C_L)]}$$

$$p_1 \equiv \frac{-1}{g_{mII} R_I R_{II} C_c}$$

$$p_2 \equiv \frac{-g_{mII} C_c}{C_1 C_L + C_L C_c + C_1 C_c}$$

$$p_2 \equiv \frac{-g_{mII}}{C_L}$$

$$z_1 = \frac{g_{mII}}{C_c}$$

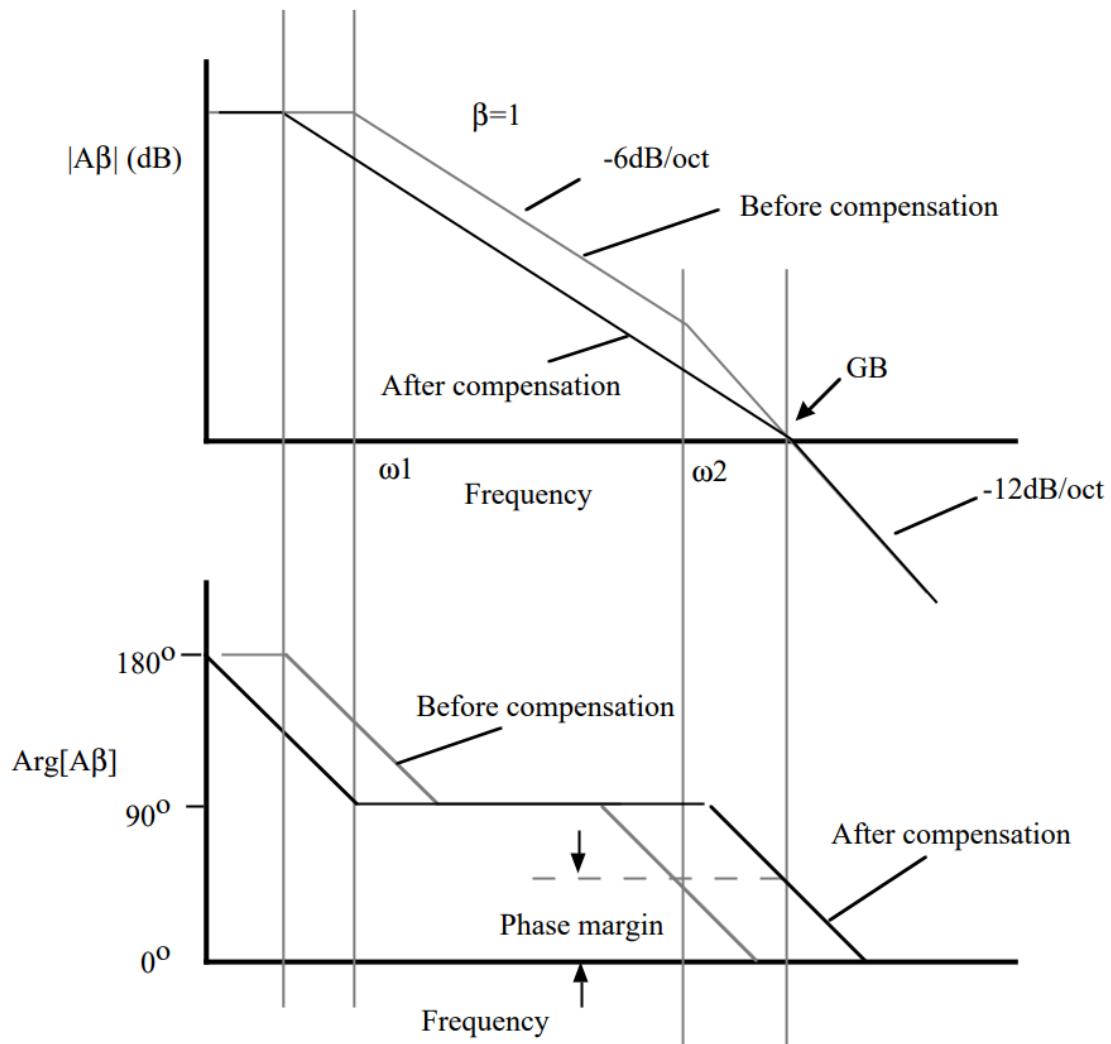
where

$$g_{mI} = g_{m1} = g_{m2} \quad g_{mII} = g_{m6}$$

$$R_I = \frac{1}{g_{ds2} + g_{ds4}}$$

$$R_{II} = \frac{1}{g_{ds6} + g_{ds7}}$$

Miller Compensation



Conditions for Stability

Unity-gainbandwidth is given as:

$$GB = A_v(0) \cdot |p_1| = (g_{mI}g_{mII}R_I R_{II}) \cdot \left(\frac{1}{g_{mII}R_I R_{II}C_c} \right) = \frac{g_{mI}}{C_c}$$

- The requirement for 60° phase margin:

$$|p_2| \geq 2.2GB \text{ if } z \geq 10GB$$

- If 60° phase margin is required, then the following relationships apply:

$$\frac{g_{mII}}{C_c} > \frac{10g_{mI}}{C_c} \Rightarrow g_{mII} > 10g_{mI}$$

Furthermore,

$$\frac{g_{mII}}{C_2} > \frac{2.2g_{mI}}{C_c}$$

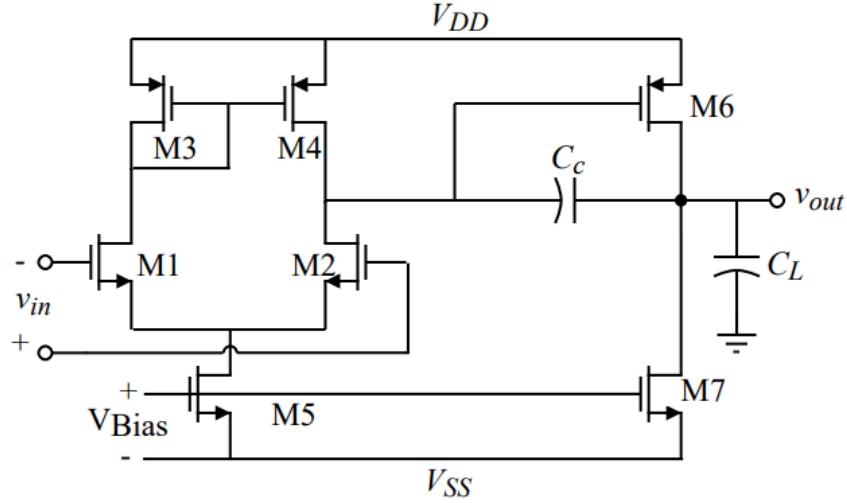
which after substitution gives:

$$C_c > 0.22C_2$$

Note:

$$g_{mI} = g_{m1} = g_{m2} \quad \text{and} \quad g_{mII} = g_{m6}$$

Two-Stage Operational Amplifier Design



Important relationships:

$$g_{m1} = g_{m2} = g_{mI}, \quad g_{m6} = g_{mII}, \quad g_{ds2} + g_{ds4} = G_I, \text{ and } g_{ds6} + g_{ds7} = G_{II}$$

$$\text{Slew rate } SR = \frac{I_5}{C_c} \quad (1)$$

$$\text{First-stage gain } A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_5(\lambda_2 + \lambda_4)} \quad (2)$$

$$\text{Second-stage gain } A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6(\lambda_6 + \lambda_7)} \quad (3)$$

$$\text{Gain-bandwidth } GB = \frac{g_{m1}}{C_c} \quad (4)$$

$$\text{Output pole } p_2 = \frac{-g_{m6}}{C_L} \quad (5)$$

$$\text{RHP zero } z_1 = \frac{g_{m6}}{C_c} \quad (6)$$

$$\text{Positive CMR } V_{\text{in(max)}} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|_{\text{(max)}} + V_{T1(\min)} \quad (7)$$

$$\text{Negative CMR } V_{\text{in(min)}} = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1(\text{max})} + V_{DS5(\text{sat})} \quad (8)$$

$$\text{Saturation voltage } V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}} \quad (9)$$

All transistors are in saturation for the above relationships.

The following design procedure assumes that specifications for the following parameters are given.

1. DC gain, A_v
2. Gain-bandwidth, GB
3. Input common-mode range, ICMR
4. Load Capacitance, C_L
5. Slew-rate, SR

Choose a device length to establish the channel-length modulation parameter λ .

Design the compensation capacitor C_c . It was shown that placing the loading pole p_2 2.2 times higher than the GB permitted a 60° phase margin (assuming that the RHP zero z_1 is placed at or beyond ten times GB). This results in the following requirement for the minimum value for C_c .

$$C_c \geq (2.2/10)C_L$$

Next, determine the minimum value for the tail current I_5 , based upon slew-rate requirements. Using Eq. (1), the value for I_5 is determined to be

$$I_5 = SR(C_c)$$

The aspect ratio of M3 can now be determined by using the requirement for positive input common-mode range. The following design equation for $(W/L)_3$ was derived from Eq. (7).

$$S_3 = (W/L)_3 = \frac{I_5}{\mu_p C_{ox} [V_{DD} - V_{\text{in(max)}} - |V_{T03}|(\text{max}) + V_{T1(\text{min})}]^2}$$

Requirements for the transconductance of the input transistors can be determined from knowledge of C_c and GB. The transconductance g_{m2} can be calculated using the following equation

$$g_{m1} = GB(C_c)$$

The aspect ratio $(W/L)_1$ is directly obtainable from g_{m1} as shown below

$$S_1 = (W/L)_1 = \frac{g_{m1}^2}{\mu_n C_{ox} (I_5)}$$

Now calculate the saturation voltage of the transistor M5, using the relation from Eq. (8).

$$V_{DS5} = V_{in}(\min) - V_{SS} - \left(\frac{I_5}{\beta_1} \right)^{1/2} - V_{T1}(\max)$$

If the value for V_{DS5} is less than about 100 mV then the possibility of a rather large $(W/L)_5$ may result. It might not be appropriate to accept this. The ICMR specification might be overly strict if the value for V_{DS5} is less than zero. To solve this problem, I_5 can be reduced or $(W/L)_1$ increased. Previous design phases need to take these modifications' consequences into consideration. Iterations are necessary to reach the intended outcome. After determining V_{DS5} , $(W/L)_5$ can be derived in the manner described below using Eq. (9).

$$S_5 = (W/L)_5 = \frac{2(I_5)}{\mu_n C_{ox} (V_{DS5})^2}$$

The transconductance g_{m6} can be calculated using the following equation

$$g_{m6} \geq 10g_{m1}$$

Generally we take, $\mathbf{g_{m6} = 10g_{m1}}$

The aspect ratio $(W/L)_6$, S_6 is given as

$$S_6 = S_3 \left(\frac{g_{m6}}{g_{m3}} \right)$$

I_6 can be calculated from the consideration of the “proper mirroring” of first-stage the current mirror load. For accurate current mirroring, we want V_{SD3} to be equal to V_{SD4} . This will occur if V_{SG4} is equal to V_{SG6} . V_{SG4} will be equal to V_{SG6} if

$$I_6 = \frac{(W/L)_6}{(W/L)_4} I_1 = \left(\frac{S_6}{S_4} \right) I_1$$

The device size of M7 can be determined from the balance equation given below

$$S_7 = (W/L)_7 = (W/L)_5 \left(\frac{I_6}{I_5} \right) = S_5 \left(\frac{I_6}{I_5} \right)$$

Width to Length ratio of M8 is equal to Width to Length ratio of M5

$$S_8 = S_5$$

DC gain A_v is calculated with the formula used below

$$A_v = \frac{(2)(g_{m2})(g_{m6})}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)}$$

Our Approach

First of all we have assumed the length of the all the transistors to be equal to $1 \mu m$. So their width can be calculated by multiplying the (W/L) ratio with $1 \mu m$.

We do most of our calculations using the code written in Python. The code is as follows:

```
Vth_n = [0.55, 0.7, 0.85]
Vth_p_mod = [0.55, 0.7, 0.85]
param_n = 100e-6
param_p = 50e-6
lamb_n = 0.04
lamb_p = 0.05

def func(gbw, sr, icmr_max, icmr_min, cc, Vdd, Vss):
    i5 = sr * cc
    gm1 = gbw * cc * 2 * np.pi
    ratio1 = ((gm1)**2)/(param_n * i5)
    ratio2 = ratio1
    ratio3 = i5/(param_p * (Vdd - icmr_max - max(Vth_p_mod) + min(Vth_n))**2)
    ratio4 = ratio3
    Vds5sat = icmr_min - Vss - np.sqrt(i5/(param_n * ratio1)) - max(Vth_n)
    ratio5 = (2*i5)/(param_n * (Vds5sat)**2)
    ratio8 = ratio5
    gm6 = 10 * gm1
    i4 = i5/2
    gm4 = np.sqrt(2*param_p * i4 * ratio4)
    ratio6 = (ratio4 * gm6)/gm4
    i6 = (ratio6/ratio4) * i4
    i7 = i6
    ratio7 = (i7/i5) * ratio5

    gm2 = np.sqrt(param_n * i5 * ratio2)
    Av = (2*gm2 * gm6)/(i5 * i6 * (lamb_n + lamb_p)**2)

    return (Av, ratio1, ratio2, ratio3, ratio4, ratio5, ratio6, ratio7, ratio8, i5, Vds5sat)
```

Our design equations have the terms $V_{th(min)}$ and $V_{th(max)}$. Therefore we define the V_{th} for nmos and pmos as an array and then we will use the **max()** and **min()** function to use their maximum and minimum values when needed.

Since the threshold voltage(Vth) is in the range 0.7V to 1.6V.

- The defined **param_n** and **param_p** respectively are the value of μC_{ox} for NMOS and PMOS. They are set to the values specified in the problem.

The function **func()** accepts the following parameters as arguments:

- Gain Bandwidth product: **gbw**
- Slew rate: **sr**
- Maximum common mode input: **icmr_max**
- Minimum common mode input: **icmr_min**
- Miller capacitance: **cc**(It is assumed to be greater than **1.1pF** because $0.22 * c_L = 0.22 * 5pF = 1.1pF$)
- Supply voltage: **Vdd**
- Down voltage: **Vss**

The **ratios** written in the code are basically the (W/L) ratios of the MOS transistors.

The function **func()** returns the dc voltage gain(A_v), (W/L) ratios of all the 8 transistors, the current through M_5 NMOS and its saturation voltage (V_{ds5sat}).

There are a total of 4 parameters in the circuit which could be varied to get the desired response. These are slew rate(**sr**), miller capacitance(**cc**), supply voltage(**Vdd**) and down voltage(**Vss**).

Results

After iterating through a lot of combinations, the following configuration has been obtained which is most similar to the required design outputs.

- $sr = 140 \text{ V}/(\mu\text{s})$
- $cc = 6 \text{ pF}$
- $V_{dd} = 2.5 \text{ V}$
- $V_{ss} = -1 \text{ V}$

Operating point

---	Operating Point	---			
$V(n001)$:	2.5	voltage	$Ig(M5)$:	0	device_current
$V(n006)$:	0.0957944	voltage	$Ib(M5)$:	-1.46793e-12	device_current
$V(output)$:	0.875692	voltage	$Is(M5)$:	-0.000851657	device_current
$V(n004)$:	1.2144	voltage	$Id(M8)$:	0.00084	device_current
$V(vin+)$:	1.6	voltage	$Ig(M8)$:	0	device_current
$V(inp)$:	0	voltage	$Ib(M8)$:	-1.10579e-12	device_current
$V(vin-)$:	1.6	voltage	$Is(M8)$:	-0.00084	device_current
$V(n002)$:	1.22465e-21	voltage	$Id(M7)$:	0.00582417	device_current
$V(n003)$:	1.2144	voltage	$Ig(M7)$:	0	device_current
$V(n005)$:	0.457932	voltage	$Ib(M7)$:	-1.88569e-12	device_current
$V(vss)$:	-1	voltage	$Is(M7)$:	-0.00582417	device_current
$Id(M1)$:	0.000425828	device_current	$Id(M4)$:	-0.000425828	device_current
$Ig(M1)$:	0	device_current	$Ig(M4)$:	-0	device_current
$Ib(M1)$:	-7.66469e-13	device_current	$Ib(M4)$:	1.2956e-12	device_current
$Is(M1)$:	-0.000425828	device_current	$Is(M4)$:	0.000425828	device_current
$Id(M2)$:	0.000425828	device_current	$Id(M6)$:	-0.00582417	device_current
$Ig(M2)$:	0	device_current	$Ig(M6)$:	-0	device_current
$Ib(M2)$:	-7.66469e-13	device_current	$Ib(M6)$:	1.63431e-12	device_current
$Is(M2)$:	-0.000425828	device_current	$Is(M6)$:	0.00582417	device_current
$Id(M5)$:	0.000851657	device_current	$Id(M3)$:	-0.000425828	device_current
$Ig(M5)$:	0	device_current	$Ig(M3)$:	-0	device_current
			$Ib(M3)$:	1.2956e-12	device_current
			$Is(M3)$:	0.000425828	device_current
			$I(Cc)$:	-2.03225e-24	device_current
			$I(C1)$:	-4.37846e-24	device_current
			$I(Ib)$:	0.00084	device_current
			$I(Vdd)$:	-0.00751583	device_current
			$I(V2)$:	0	device_current
			$I(V3)$:	0	device_current
			$I(V4)$:	0	device_current
			$I(V5)$:	0	device_current
			$I(V6)$:	0.00751583	device_current

If we set the other parameters in the function to their specified values(i.e.

$gbw = 50\text{MHz}$, $icmr_{min} = 0.7V$ and $icmr_{max} = 1.6V$, the we get the following output:

```

# func(gbw, sr, icmr_max, icmr_min, cc, Vdd, Vss):
# return (Av, ratio1, ratio2, ratio3, ratio4, ratio5, ratio6, ratio7, ratio8, i5, Vds5sat
func(50e6, 140e6, 1.6, 0.7, 6e-12, 2.5, -1)
print(f"Theoretical DC gain = {round(func(50e6, 140e6, 1.6, 0.7, 6e-12, 2.5, -1) [0], 2)}")
print(f"Ratios of individual MOS transistors = {np.array(func(50e6, 140e6, 1.6, 0.7, 6e-12, 2.5, -1) [1:-2]).round(2)}")
print(f"The current through fifth transistor = {func(50e6, 140e6, 1.6, 0.7, 6e-12, 2.5, -1) [-2]}")
print(f"The saturation voltage of the fifth transistor = {round(func(50e6, 140e6, 1.6, 0.7, 6e-12, 2.5, -1) [-1], 2)}")

[89] ✓ 0.0s
...
Theoretical DC gain = 1846.91
Ratios of individual MOS transistors = [ 42.3  42.3   46.67  46.67 102.74 628.32 691.68 102.74]
The current through fifth transistor = 0.00084
The saturation voltage of the fifth transistor = 0.4

```

From this, we infer that although the DC gain was assumed to be 2000, the **theoretical calculated DC gain is 1847.**

The width to length ratios of the transistors are as follows:

$(W/L)_1$	42.3
$(W/L)_2$	42.3
$(W/L)_3$	46.67
$(W/L)_4$	46.67
$(W/L)_5$	102.74
$(W/L)_6$	628.32
$(W/L)_7$	691.68
$(W/L)_8$	102.74

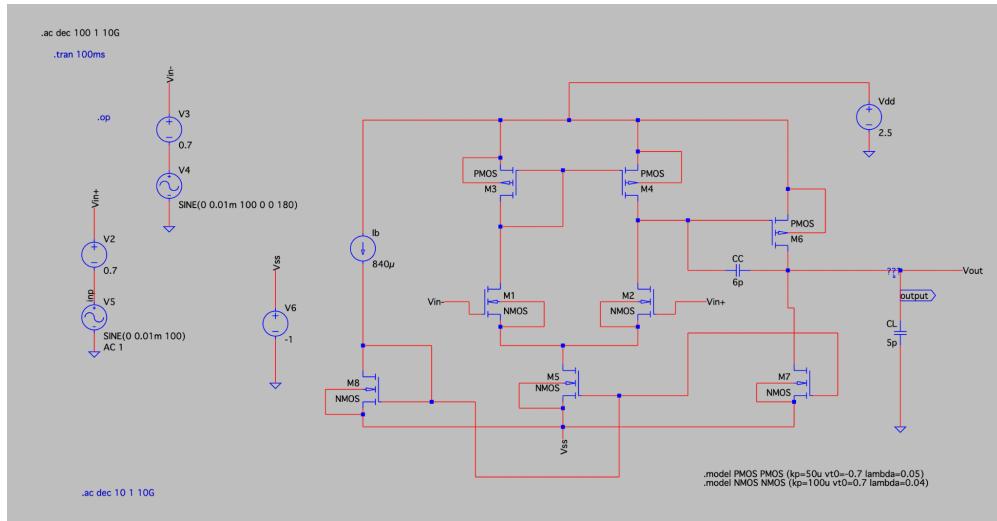
Also the current $i_5 = 840 \mu A$

And the saturation voltage of M5 $V_{ds5(sat)} = 0.4V$ (This value is acceptable as it's greater than $100mV$).

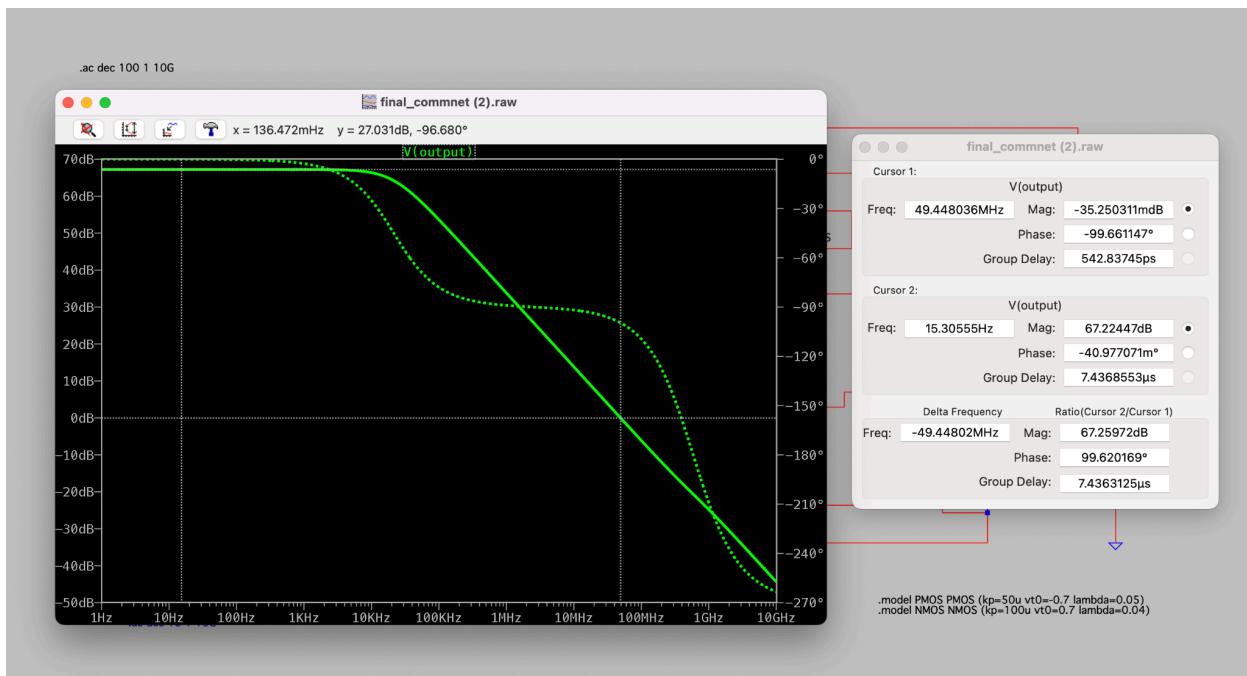
Since the common mode input is from $0.7V$ to $1.6V$. Therefore, we will have to evaluate the output and compare it to the theoretical output for two cases.

Parameter	Required output	Simulation output at $V_{cm} = 0.7V$	Simulation output at $V_{cm} = 1.6V$
DC Gain(dB)	66.02	67.22	66.75
DC Gain	2000	2296	2143
Gain-Bandwidth Product(MHz)	50	49.5	49.3
Phase Margin(degrees)	> 60	80.34	80.38

For $V_{cm} = 0.7V$: The circuit diagram:

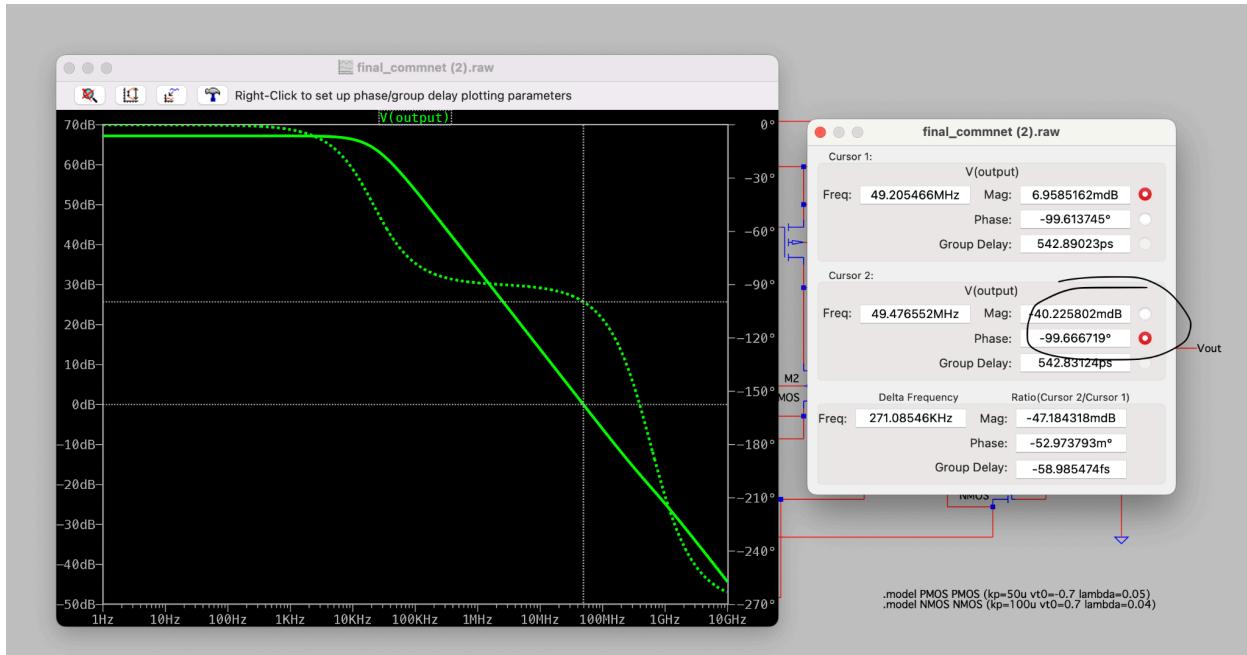


Simulation for the same:



The first cursor represents the gain-bandwidth which is the frequency at **0 dB** which is approximately **49.5 MHz**.

The second cursor represents the dc gain which is approximately **67.22 dB**.

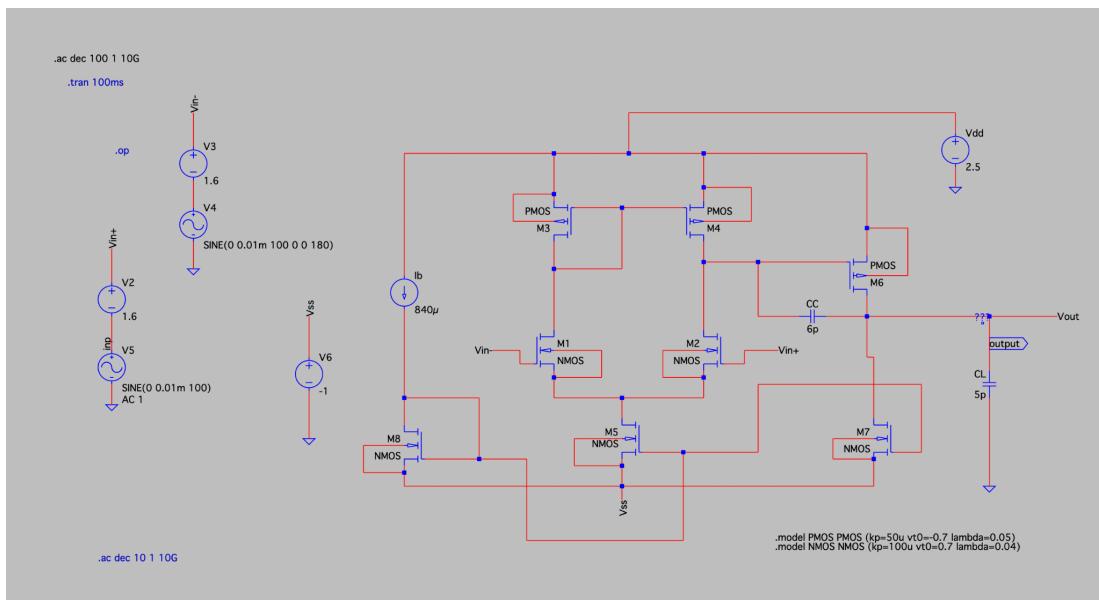


The above image is for the phase margin. We can clearly see that the phase of the second cursor is -99.66 degrees.

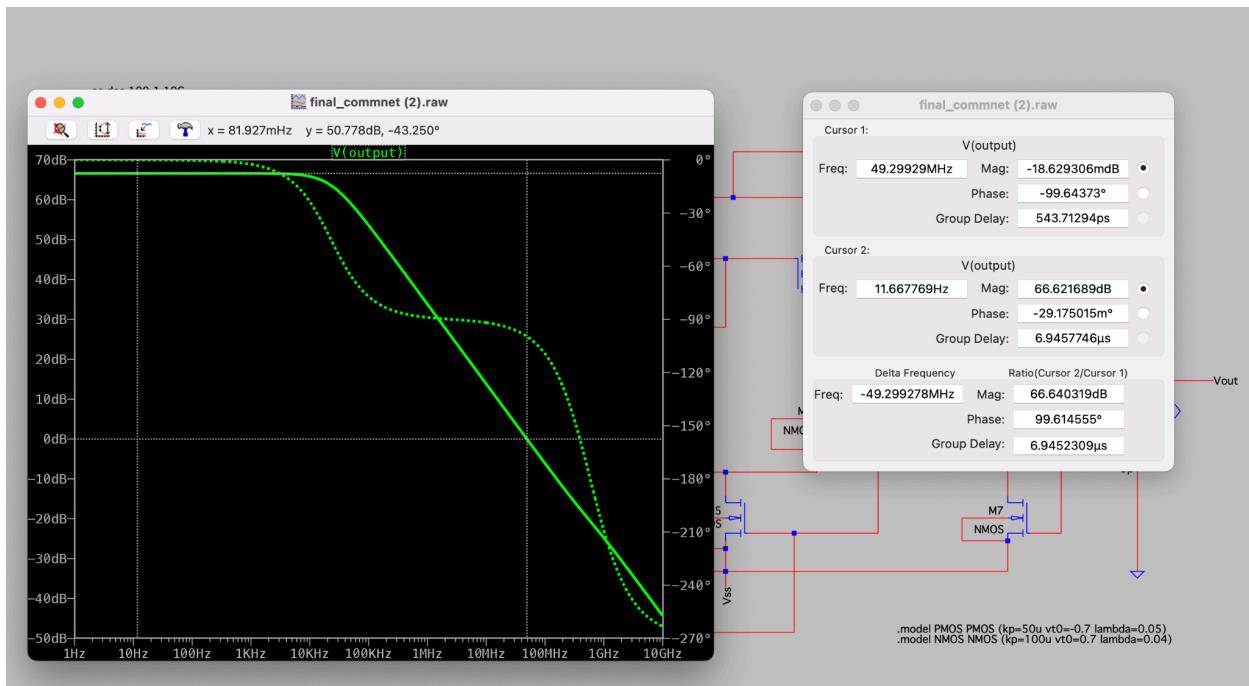
Therefore, the phase margin(PM) is:

$$PM = 180 + (-99.66) = 80.34^{\circ}$$

For $V_{cm} = 1.6 V$: The circuit diagram:

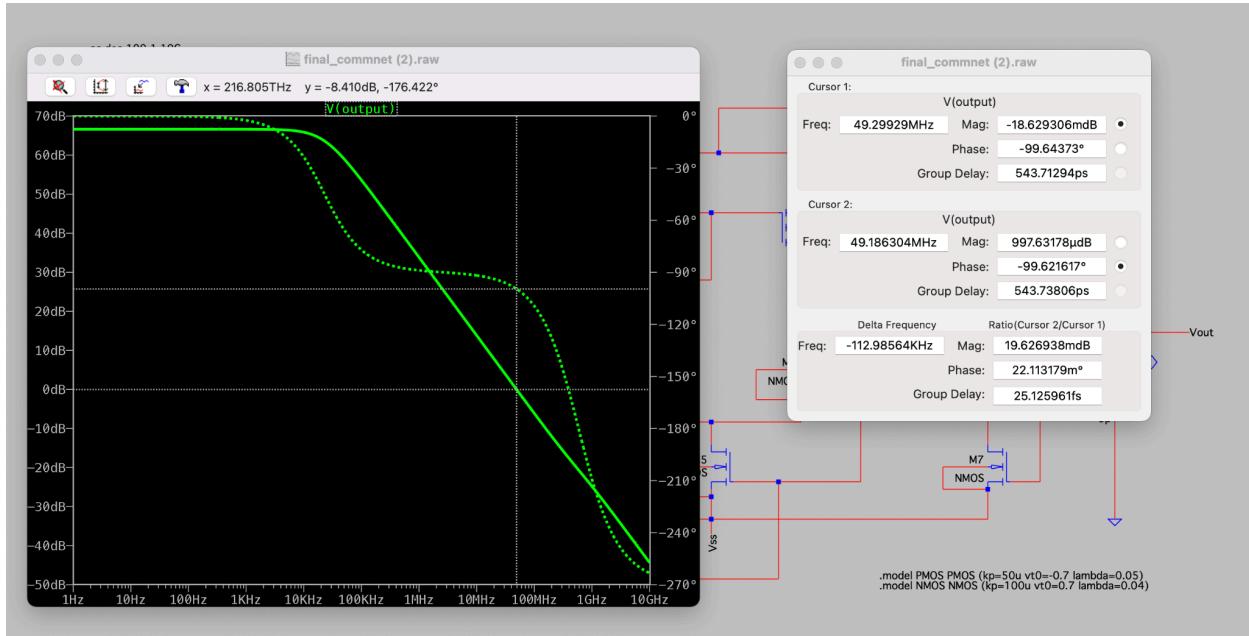


Simulation for the same:



The first cursor represents the gain-bandwidth which is the frequency at **0 dB** which is approximately **49.3 MHz**.

The second cursor represents the dc gain which is approximately **66.62 dB**.



The above image is for the phase margin. We can clearly see that the phase of the second cursor is **-99.62 degrees**.

Therefore, the phase margin(PM) is:

$$PM = 180 + (-99.62) = 80.38^{\circ}$$

Conclusion

Integrated circuit systems are designed to appear as a single-pole system over a wide frequency range to avoid stability issues with second-order and larger systems. Therefore, compensation techniques must be improved to meet design constraints such as higher unity gain frequency and better phase margin.