Lite-ON install OAI gNB LOG

Lite-ON install OAI gNB LOG

```
[ HW ]
      # /dev/cpu_dma_latency set to 2 us
[Om[ENB_APP]
              nfapi running mode: MONOLITHIC
[Om[GNB APP]
               Getting GNBSParams
[Om[ITTI]
            Starting itti queue: TASK_UNKNOWN as task 0
[Om[ITTI]
            Starting itti queue: TASK TIMER as task 1
[Om[ITTI]
            Starting itti queue: TASK L2L1 as task 2
[Om[ITTI]
            Starting itti queue: TASK BM as task 3
[Om[ITTI]
            Starting itti queue: TASK PHY ENB as task 4
[Om[ITTI]
            Starting itti queue: TASK MAC GNB as task 5
[Om[ITTI]
            Starting itti queue: TASK_RLC_ENB as task 6
[Om[ITTI]
            Starting itti queue: TASK_RRC_ENB_NB_IoT as task 7
[Om[ITTI]
            Starting itti queue: TASK PDCP ENB as task 8
            Starting itti queue: TASK_PDCP_GNB as task 9
[Om[ITTI]
[Om[ITTI]
            Starting itti queue: TASK_DATA_FORWARDING as task 10
[Om[ITTI]
            Starting itti queue: TASK_END_MARKER as task 11
[Om[ITTI]
            Starting itti queue: TASK_RRC_ENB as task 12
[Om[ITTI]
            Starting itti queue: TASK_RRC_GNB as task 13
[Om[ITTI]
            Starting itti queue: TASK_RAL_ENB as task 14
[Om[ITTI]
            Starting itti queue: TASK_S1AP as task 15
[Om[ITTI]
            Starting itti queue: TASK_NGAP as task 16
            Starting itti queue: TASK_X2AP as task 17
[Om[ITTI]
[Om[ITTI]
            Starting itti queue: TASK_M2AP_ENB as task 18
            Starting itti queue: TASK_M2AP_MCE as task 19
[Om[ITTI]
[Om[ITTI]
            Starting itti queue: TASK M3AP as task 20
            Starting itti queue: TASK_M3AP_MME as task 21
[Om[ITTI]
[Om[ITTI]
            Starting itti queue: TASK M3AP MCE as task 22
[Om[ITTI]
            Starting itti queue: TASK_SCTP as task 23
            Starting itti queue: TASK_ENB_APP as task 24
[Om[ITTI]
[Om[ITTI]
            Starting itti queue: TASK GNB APP as task 25
[Om[ITTI]
            Starting itti queue: TASK_MCE_APP as task 26
            Starting itti queue: TASK_MME_APP as task 27
[Om[ITTI]
[Om[ITTI]
            Starting itti queue: TASK_PHY_UE as task 28
[Om[ITTI]
            Starting itti queue: TASK MAC UE as task 29
[Om[ITTI]
            Starting itti queue: TASK_RLC_UE as task 30
[Om[ITTI]
            Starting itti queue: TASK_PDCP_UE as task 31
            Starting itti queue: TASK_RRC_UE as task 32
[Om[ITTI]
[Om[ITTI]
            Starting itti queue: TASK_RRC_NRUE as task 33
[Om[ITTI]
            Starting itti queue: TASK_NAS_UE as task 34
            Starting itti queue: TASK_RAL_UE as task 35
[Om[ITTI]
[Om[ITTI]
            Starting itti queue: TASK_GTPV1_U as task 36
[Om[ITTI]
            Starting itti queue: TASK_CU_F1 as task 37
[Om[ITTI]
            Starting itti queue: TASK_DU_F1 as task 38
```

```
[Om[ITTI]
            Starting itti queue: TASK CUCP E1 as task 39
            Starting itti queue: TASK_CUUP_E1 as task 40
[Om[ITTI]
[Om[ITTI]
            Starting itti queue: TASK_RRC_UE_SIM as task 41
            Starting itti queue: TASK_RRC_GNB_SIM as task 42
[Om[ITTI]
[Om[ITTI]
           Starting itti queue: TASK RRC NSA UE as task 43
[Om[ITTI]
            Starting itti queue: TASK RRC NSA NRUE as task 44
[Om[ITTI]
           Starting itti queue: TASK_NAS_NRUE as task 45
[Om[OPT]
          OPT disabled
[Om[HW]
         Version: Branch: use_msgq Abrev. Hash: ffee14b30c Date: Tue Mar 21 10:50:4
[Om[NR_PHY]
             RC.gNB = 0x34942a0
[Om[NR_PHY]
             PRB blacklist
[Om[NR PHY]
             Copying 0 blacklisted PRB to L1 context
[Om[PHY]
          TX_AMP = 3276 (-20 dBFS)
[Om[PHY]
          L1_RX_THREAD_CORE -1 (17)
[Om[PHY]
          l1_north_init_gNB() RC.nb_nr_L1_inst:1
[Om[PHY]
          Installing callbacks for IF_Module - UL_indication
[Om[MAC]
          Allocating shared L1/L2 interface structure for instance 0 @ 0x3498f20
[Om[PHY]
          l1_north_init_gNB() RC.gNB[0] installing callbacks
[Om[PHY]
          create qNB tasks() Task ready initialize structures
[Om[NR_PHY]
             PRB blacklist
[Om[NR PHY]
             Copying 0 blacklisted PRB to L1 context
[Om[PHY]
          TX AMP = 3276 (-20 dBFS)
[Om[PHY]
          L1_RX_THREAD_CORE -1 (17)
[Om[PHY]
          l1_north_init_gNB() RC.nb_nr_L1_inst:1
[Om[PHY]
          Installing callbacks for IF_Module - UL_indication
[Om[PHY]
          l1 north init qNB() RC.qNB[0] installing callbacks
[Om[1;31m[PHY] No prs_config configuration found..!!
[Om[MAC]
           [MAIN] Init function start:nb_nr_macrlc_inst=1
           threadCreate for MAC_STATS, affinity ffffffff, priority 2
[Om[UTIL]
            threadCreate for rlc_data_req_thread, affinity ffffffff, priority 97
[Om[UTIL]
[Om[PHY]
          Installing callbacks for IF_Module - UL_indication
[Om[NR_MAC]
             PUSCH Target 300, PUCCH Target 200, PUCCH Failure 10, PUSCH Failure 10
[Om[PHY]
          create_gNB_tasks() RC.nb_nr_L1_inst:1
[Om[PHY]
          l1_north_init_gNB() RC.nb_nr_L1_inst:1
[Om[PHY]
          Installing callbacks for IF_Module - UL_indication
[Om[PHY]
           l1_north_init_gNB() RC.gNB[0] installing callbacks
[Om[GNB_APP] Allocating gNB_RRC_INST for 1 instances
          create_gNB_tasks() RC.nb_nr_inst:1 RC.nrrrc:0x34aa480
[Om[PHY]
[Om[PHY]
          create_gNB_tasks() Creating RRC instance RC.nrrrc[0]:0x34ad9a0 (1 of 1)
[Om[RRC]
          Read in ServingCellConfigCommon (PhysCellId 0, ABSFREQSSB 643392, DLBand
[Om[NR_MAC]
             NR band duplex spacing is 0 KHz (nr_bandtable[37].band = 78)
[Om[NR_MAC]
             NR band 78, duplex mode TDD, duplex spacing = 0 KHz
```

```
[OmCMDLINE: "./nr-softmodem" "-0" "../../targets/PROJECTS/GENERIC-NR-5GC/CONF/ora
[CONFIG] get parameters from libconfig ../../targets/PROJECTS/GENERIC-NR-5GC/CONF
[CONFIG] function config_libconfig_init returned 0
[CONFIG] config module libconfig loaded
[LIBCONFIG] config: 2/2 parameters successfully set, (2 to default value)
[CONFIG] debug flags: 0x00000000
[LIBCONFIG] log_config: 3/3 parameters successfully set, (1 to default value)
[LIBCONFIG] log_config: 54/54 parameters successfully set, (46 to default value)
[LIBCONFIG] log_config: 54/54 parameters successfully set, (54 to default value)
[LIBCONFIG] log_config: 16/16 parameters successfully set, (16 to default value)
[LIBCONFIG] log_config: 16/16 parameters successfully set, (16 to default value)
log init done
Reading in command-line options
[LIBCONFIG] (root): 37/37 parameters successfully set, (33 to default value)
[LIBCONFIG] (root): 6/6 parameters successfully set, (5 to default value)
[LIBCONFIG] (root): 2/2 parameters successfully set, (0 to default value)
[LIBCONFIG] THREAD STRUCT.[0]: 2/2 parameters successfully set, (0 to default value)
[LIBCONFIG] THREAD STRUCT.[0]: 2/2 parameters successfully set, (0 to default value)
[CONFIG] parallel conf is set to 0
[CONFIG] worker_conf is set to 1
Configuration: nb rrc inst 1, nb nr L1 inst 1, nb ru 1
[LIBCONFIG] TTracer: 3/3 parameters successfully set, (3 to default value)
configuring for RAU/RRU
CPU Freq is 2.496120
[LIBCONFIG] opt: 3/3 parameters successfully set, (3 to default value)
[LIBCONFIG] (root): 2/2 parameters successfully set, (0 to default value)
[LIBCONFIG] qNBs.[0]: 28/28 parameters successfully set, (17 to default value)
[LIBCONFIG] L1s.[0]: 19/19 parameters successfully set, (12 to default value)
Initializing northbound interface for L1
[LIBCONFIG] (root): 2/2 parameters successfully set, (0 to default value)
[LIBCONFIG] gNBs.[0]: 28/28 parameters successfully set, (17 to default value)
[LIBCONFIG] L1s.[0]: 19/19 parameters successfully set, (12 to default value)
Initializing northbound interface for L1
[LIBCONFIG] list prs_config not found in config file ../../targets/PROJECTS/GENER
[LIBCONFIG] (root): 2/2 parameters successfully set, (0 to default value)
[LIBCONFIG] gNBs.[0]: 28/28 parameters successfully set, (17 to default value)
[LIBCONFIG] MACRLCs.[0]: 33/33 parameters successfully set, (26 to default value)
[LIBCONFIG] qNBs.[0]: 28/28 parameters successfully set, (17 to default value)
[LIBCONFIG] MACRLCs.[0]: 33/33 parameters successfully set, (26 to default value)
[LIBCONFIG] list gNBs.[0].E1_INTERFACE not found in config file ../../targets/PRO
[LIBCONFIG] gNBs.[0]: 28/28 parameters successfully set, (17 to default value)
[LIBCONFIG] MACRLCs.[0]: 33/33 parameters successfully set, (26 to default value)
```

```
[LIBCONFIG] list qNBs.[0].E1 INTERFACE not found in config file ../../targets/PRO
[LIBCONFIG] gNBs.[0]: 28/28 parameters successfully set, (17 to default value)
[LIBCONFIG] MACRLCs.[0]: 33/33 parameters successfully set, (26 to default value)
[LIBCONFIG] list gNBs.[0].E1_INTERFACE not found in config file ../../targets/PRO
[LIBCONFIG] (root): 2/2 parameters successfully set, (0 to default value)
[LIBCONFIG] qNBs.[0]: 28/28 parameters successfully set, (17 to default value)
[LIBCONFIG] gNBs.[0].servingCellConfigCommon.[0]: 60/60 parameters successfully set,
[LIBCONFIG] list qNBs.[0].servingCellConfigDedicated not found in config file ../../
NRRRC 0: Southbound Transport local_mac
[LIBCONFIG] gNBs.[0]: 28/28 parameters successfully set, (17 to default value)
[LIBCONFIG] MACRLCs.[0]: 33/33 pa[GNB_APP] pdsch_AntennaPorts N1 1
[Om[GNB_APP]
              pdsch AntennaPorts N2 1
[Om[GNB_APP]
               pdsch_AntennaPorts XP 2
[Om[GNB_APP]
               pusch_AntennaPorts 2
[Om[GNB_APP]
               minTXRXTIME 4
[Om[GNB_APP]
               SIB1 TDA 15
[Om[GNB APP]
               Do CSI-RS 1
               Do SRS 0
[Om[GNB_APP]
[Om[GNB APP]
               256 QAM: may be on
[Om[GNB_APP]
               SDAP layer is disabled
[Om[GNB_APP]
               Data Radio Bearer count 1
[Om[GNB APP]
               RRC starting with node type 2
[Om[GNB_APP]
               Sending configuration message to NR RRC task
[Om[PDCP]
           pdcp init, usegtp
[Om[GNB_APP]
               default drx 0
[Om[GNB APP]
               [qNB 0] qNB app register for instance 0
            threadCreate for TASK_SCTP, affinity ffffffff, priority 50
[Om[UTIL]
[Om[ITTI]
            Created Posix thread TASK SCTP
[0m[X2AP]
           X2AP is disabled.
            threadCreate for TASK_NGAP, affinity ffffffff, priority 50
[Om[UTIL]
[Om[NGAP]
            Starting NGAP layer
[Om[NGAP]
            Registered new gNB[0] and macro gNB id 3584
[Om[NGAP]
            [gNB 0] check the amf registration state
[Om[ITTI]
            Created Posix thread TASK_NGAP
[Om[NGAP]
            3584 -> 0000e000
[Om[NGAP]
            servedGUAMIs.list.count 1
[Om[NGAP]
            PLMNSupportList.list.count 1
[Om[NGAP]
            PLMNSupportList.list.count 1
            threadCreate for TASK_GNB_APP, affinity ffffffff, priority 50
[Om[UTIL]
[Om[GNB_APP]
              [gNB 0] Received NGAP_REGISTER_GNB_CNF: associated AMF 1
[Om[ITTI]
            Created Posix thread TASK_GNB_APP
[Om[NR_RRC]
              Creating NR RRC gNB Task, that will also create TASKS
```

```
[Om[UTIL]
            threadCreate for TASK RRC GNB, affinity ffffffff, priority 50
[Om[NR RRC]
              Entering main loop of NR RRC message task
[Om[NR_RRC]
              [gNB 0] Received NRRRC_CONFIGURATION_REQ : 0x34ae8d0
[Om[NR_RRC]
              [FRAME 00000][gNB][MOD 00][RNTI 0] Init...
[Om[NR MAC]
             NR band duplex spacing is 0 KHz (nr bandtable[37].band = 78)
[Om[NR MAC]
             NR band 78, duplex mode TDD, duplex spacing = 0 KHz
[Om[NR_RRC]
              [FRAME 00000][gNB][MOD 00][RNTI 0] Checking release
[Om[NR_RRC]
             SIB1 freq: absoluteFrequencySSB 643392, absoluteFrequencyPointA 642816
             SIB1 freq: absolute_diff 576, 2*(absolute_diff/(12*2) - 10) 28
[Om[NR_RRC]
[Omrameters successfully set, (26 to default value)
[LIBCONFIG] list gNBs.[0].E1_INTERFACE not found in config file ../../targets/PRO
[LIBCONFIG] gNBs.[0].plmn list.[0]: 3/3 parameters successfully set, (0 to default v
[LIBCONFIG] security: 4/4 parameters successfully set, (0 to default value)
[LIBCONFIG] gNBs.[0]: 28/28 parameters successfully set, (17 to default value)
[LIBCONFIG] MACRLCs.[0]: 33/33 parameters successfully set, (26 to default value)
[LIBCONFIG] list gNBs.[0].E1_INTERFACE not found in config file ../../targets/PRO
[LIBCONFIG] qNBs.[0]: 28/28 parameters successfully set, (17 to default value)
[LIBCONFIG] MACRLCs.[0]: 33/33 parameters successfully set, (26 to default value)
[LIBCONFIG] list qNBs.[0].E1 INTERFACE not found in config file ../../targets/PRO
[LIBCONFIG] eNBs.[0]: 1/1 parameters successfully set, (1 to default value)
[LIBCONFIG] gNBs.[0]: 1/1 parameters successfully set, (1 to default value)
[LIBCONFIG] (root): 2/2 parameters successfully set, (0 to default value)
[LIBCONFIG] gNBs.[0]: 28/28 parameters successfully set, (17 to default value)
[LIBCONFIG] gNBs.[0].plmn_list.[0]: 3/3 parameters successfully set, (0 to default v
[LIBCONFIG] gNBs.[0].plmn_list.[0].snssaiList.[0]: 2/2 parameters successfully set,
[LIBCONFIG] gNBs.[0].amf ip address.[0]: 4/4 parameters successfully set, (0 to defa
[LIBCONFIG] gNBs.[0].SCTP: 2/2 parameters successfully set, (0 to default value)
[LIBCONFIG] gNBs.[0].NETWORK_INTERFACES: 10/10 parameters successfully set, (3 to de
[LIBCONFIG] gNBs.[0].NETWORK_INTERFACES: 10/10 parameters successfully set, (3 to de
[LIBCONFIG] gNBs.[0]: 28/28 parameters successfully set, (17 to default value)
[LIBCONFIG] MACRLCs.[0]: 33/33 parameters successfully set, (26 to default value)
[LIBCONFIG] list gNBs.[0].E1_INTERFACE not found in config file ../../targets/PRO
<SIB1>
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        <q-RxLevMin>-65</q-RxLevMin>
    </cellSelectionInfo>
    <cellAccessRelatedInfo>
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```

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                    <subcarrierSpacing><kHz30/></subcarrierSpacing>
                    <carrierBandwidth>273</carrierBandwidth>
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        </frequencyInfoDL>
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```

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   <setup>
        <controlResourceSetZero>11</controlResourceSetZero>
        <searchSpaceZero>0</searchSpaceZero>
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                    <aggregationLevel4><n1/></aggregationLevel4>
                    <aggregationLevel8><n0/></aggregationLevel8>
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            </SearchSpace>
            <SearchSpace>
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                    <aggregationLevel2><n0/></aggregationLevel2>
                    <aggregationLevel4><n1/></aggregationLevel4>
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```

```
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        <searchSpaceOtherSystemInformation>3</searchSpaceOtherSystem</pre>
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        <ra-SearchSpace>1</ra-SearchSpace>
    </setup>
</pdch-ConfigCommon>
<pdsch-ConfigCommon>
    <setup>
        <pdsch-TimeDomainAllocationList>
```

Lite-ON install OAI gNB LOG - HackMD

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                        <startSymbolAndLength>40</startSymbolAndLength>
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```

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               <ra-ResponseWindow><sl20/></ra-ResponseWindow>
           </rach-ConfigGeneric>
           <ssb-perRACH-OccasionAndCB-PreamblesPerSSB>
               <oneHalf><n64/></oneHalf>
           </ssb-perRACH-OccasionAndCB-PreamblesPerSSB>
           <ra-ContentionResolutionTimer><sf64/></ra-ContentionResoluti</pre>
           <rsrp-ThresholdSSB>19</rsrp-ThresholdSSB>
           ch-RootSequenceIndex>
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    </rach-ConfigCommon>
    <pusch-ConfigCommon>
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                   <mappingType><typeB/></mappingType>
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```

```
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                <pucch-ResourceCommon>0</pucch-ResourceCommon>
                <pucch-GroupHopping><neither/></pucch-GroupHopping>
                <hoppingId>0</hoppingId>
                <p0-nominal>-76</p0-nominal>
            </setup>
        </pucch-ConfigCommon>
    </initialUplinkBWP>
    <timeAlignmentTimerCommon><infinity/></timeAlignmentTimerCommon>
</uplinkConfigCommon>
<n-TimingAdvanceOffset><n25600/></n-TimingAdvanceOffset>
<ssb-PositionsInBurst>
    <inOneGroup>
        10000000
    </inOneGroup>
</ssb-PositionsInBurst>
<ssb-PeriodicityServingCell><ms20/></ssb-PeriodicityServingCell>
<tdd-UL-DL-ConfigurationCommon>
    <referenceSubcarrierSpacing><kHz30/></referenceSubcarrierSpacing>
    <pattern1>
        <dl-UL-TransmissionPeriodicity><ms2p5/></dl-UL-TransmissionPeriodici</pre>
        <nrofDownlinkSlots>3</nrofDownlinkSlots>
        <nrofDownlinkSymbols>6/nrofDownlinkSymbols>
        <nrofUplinkSlots>1/nrofUplinkSlots>
        <nrofUplinkSymbols>4</nrofUplinkSymbols>
```

```
</pattern1>
        </tdd-UL-DL-ConfigurationCommon>
        <ss-PBCH-BlockPower>-25</ss-PBCH-BlockPower>
   </servingCellConfigCommon>
   <ue-TimersAndConstants>
        <t300><ms400/></t300>
        <t301><ms400/></t301>
        <t310><ms2000/></t310>
        <n310><n10/></n310>
        <t311><ms3000/></t311>
        <n311><n1/></n311>
        <t319><ms400/></t319>
   </ue-TimersAndConstants>
</SIB1>
[NR_RRC]
           do_SIB23_NR, size 9
[Om[NR_RRC]
              Done init_NR_SI
[Om[NR MAC]
              Configuring common parameters from NR ServingCellConfig
[Om[NR_MAC]
              config common() dl BandwidthP:100
[Om[NR_MAC]
             NR band duplex spacing is 0 KHz (nr bandtable[37].band = 78)
[Om[NR_MAC]
              Computing frequency (pointA 642816 => 3642240 KHz (freq_min 3300000 KH
              config common() dl BandwidthP:100
[Om[NR MAC]
[Om[NR MAC]
             NR band duplex spacing is 0 KHz (nr bandtable[37].band = 78)
[Om[NR_MAC]
              Computing frequency (pointA 642816 => 3642240 KHz (freq_min 3300000 KH
[Om[NR_MAC]
             NR band duplex spacing is 0 KHz (nr_bandtable[37].band = 78)
[Om[NR_MAC]
             NR band 78, duplex mode TDD, duplex spacing = 0 KHz
              Set RX antenna number to 2, Set TX antenna number to 2 (num ssb 1: 800
[Om[NR MAC]
[Om[NR_MAC]
              Setting TDD configuration period to 5
[Om[NR_MAC]
             TDD has been properly configurated
[Om[PHY]
          DL frequency 3691380000 Hz, UL frequency 3691380000 Hz: band 77, uldl off
              Configuring MIB for instance 0, : (Nid_cell 0,DL freq 3691380000, UL
[Om[32m[PHY]
[Om[PHY]
          Initializing frame parms for mu 1, N_RB 273, Ncp 0
              Init: N_RB_DL 273, first_carrier_offset 2458, nb_prefix_samples 288,n
[0m[93m[PHY]
[Om[PHY]
          Doing symbol rotation calculation for gNB TX/RX, f0 3691380000.000000 Hz,
[Om[PHY]
           Symbol rotation 0/28 => tl 0.000000 (-3212,-32610) (0.265625)
[Om[PHY]
          Symbol rotation 1/28 => tl 0.000036 (30272,12539) (0.937500)
[Om[PHY]
           Symbol rotation 2/28 => tl 0.000072 (-25330,20787) (0.609375)
[Om[PHY]
           Symbol rotation 3/28 => tl 0.000108 (-6393,-32138) (0.281250)
[Om[PHY]
          Symbol rotation 4/28 => tl 0.000143 (31356,9511) (0.953125)
[Om[PHY]
           Symbol rotation 5/28 => tl 0.000179 (-23170,23169) (0.625000)
[Om[PHY]
          Symbol rotation 6/28 => tl 0.000215 (-9512,-31357) (0.296875)
[Om[PHY]
          Symbol rotation 7/28 => tl 0.000250 (32137,6392) (0.968750)
[Om[PHY]
          Symbol rotation 8/28 => tl 0.000286 (-20788,25329) (0.640625)
```

```
[Om[PHY]
           Symbol rotation 9/28 \Rightarrow tl 0.000322 (-12540, -30273) (0.312500)
[Om[PHY]
           Symbol rotation 10/28 => tl 0.000357 (32609,3211) (0.984375)
[Om[PHY]
           Symbol rotation 11/28 => tl 0.000393 (-18205,27244) (0.656250)
[Om[PHY]
           Symbol rotation 12/28 => tl 0.000429 (-15447,-28898) (0.328125)
[Om[PHY]
           Symbol rotation 13/28 => tl 0.000464 (32767,-1) (0.000000)
[Om[PHY]
           Symbol rotation 14/28 \Rightarrow tl \ 0.000500 \ (-3212, -32610) \ (0.265625)
[Om[PHY]
           Symbol rotation 15/28 => tl 0.000536 (30272,12539) (0.937500)
[Om[PHY]
           Symbol rotation 16/28 => tl 0.000572 (-25330,20787) (0.609375)
           Symbol rotation 17/28 => tl 0.000608 (-6393,-32138) (0.281250)
[Om[PHY]
[Om[PHY]
           Symbol rotation 18/28 => tl 0.000643 (31356,9511) (0.953125)
[Om[PHY]
           Symbol rotation 19/28 => tl 0.000679 (-23170,23169) (0.625000)
[Om[PHY]
           Symbol rotation 20/28 => tl 0.000715 (-9512,-31357) (0.296875)
[Om[PHY]
           Symbol rotation 21/28 \Rightarrow tl \ 0.000750 \ (32137,6392) \ (0.968750)
[Om[PHY]
           Symbol rotation 22/28 => tl 0.000786 (-20788,25329) (0.640625)
[Om[PHY]
           Symbol rotation 23/28 => tl 0.000822 (-12540,-30273) (0.312500)
[Om[PHY]
           Symbol rotation 24/28 \Rightarrow 10.000857 (32609, 3211) (0.984375)
[Om[PHY]
           Symbol rotation 25/28 => tl 0.000893 (-18205,27244) (0.656250)
           Symbol rotation 26/28 \Rightarrow tl \ 0.000929 \ (-15447, -28898) \ (0.328125)
[Om[PHY]
[Om[PHY]
           Symbol rotation 27/28 => tl 0.000964 (32767,0) (1.000000)
[Om[PHY]
           Doing symbol rotation calculation for gNB TX/RX, f0 3691380000.000000 Hz,
[Om[PHY]
           Symbol rotation 0/28 \Rightarrow tl \ 0.000000 \ (-3212, -32610) \ (0.265625)
[Om[PHY]
           Symbol rotation 1/28 \Rightarrow tl \ 0.000036 \ (30272, 12539) \ (0.937500)
[Om[PHY]
           Symbol rotation 2/28 => tl 0.000072 (-25330,20787) (0.609375)
[Om[PHY]
           Symbol rotation 3/28 => tl 0.000108 (-6393,-32138) (0.281250)
[Om[PHY]
           Symbol rotation 4/28 => tl 0.000143 (31356,9511) (0.953125)
[Om[PHY]
           Symbol rotation 5/28 \Rightarrow tl \ 0.000179 \ (-23170,23169) \ (0.625000)
[Om[PHY]
           Symbol rotation 6/28 \Rightarrow tl \ 0.000215 \ (-9512, -31357) \ (0.296875)
[Om[PHY]
           Symbol rotation 7/28 => tl 0.000250 (32137,6392) (0.968750)
[Om[PHY]
           Symbol rotation 8/28 => tl 0.000286 (-20788,25329) (0.640625)
[Om[PHY]
           Symbol rotation 9/28 => tl 0.000322 (-12540,-30273) (0.312500)
[Om[PHY]
           Symbol rotation 10/28 => tl 0.000357 (32609,3211) (0.984375)
           Symbol rotation 11/28 => tl 0.000393 (-18205,27244) (0.656250)
[Om[PHY]
[Om[PHY]
           Symbol rotation 12/28 => tl 0.000429 (-15447,-28898) (0.328125)
[Om[PHY]
           Symbol rotation 13/28 => tl 0.000464 (32767,-1) (0.000000)
[Om[PHY]
           Symbol rotation 14/28 = 10.000500 (-3212, -32610) (0.265625)
[Om[PHY]
           Symbol rotation 15/28 => tl 0.000536 (30272,12539) (0.937500)
[Om[PHY]
           Symbol rotation 16/28 => tl 0.000572 (-25330,20787) (0.609375)
[Om[PHY]
           Symbol rotation 17/28 => tl 0.000608 (-6393,-32138) (0.281250)
           Symbol rotation 18/28 => tl 0.000643 (31356,9511) (0.953125)
[Om[PHY]
[Om[PHY]
           Symbol rotation 19/28 => tl 0.000679 (-23170,23169) (0.625000)
[Om[PHY]
           Symbol rotation 20/28 => tl 0.000715 (-9512,-31357) (0.296875)
[Om[PHY]
           Symbol rotation 21/28 => tl 0.000750 (32137,6392) (0.968750)
```

```
Symbol rotation 22/28 => tl 0.000786 (-20788,25329) (0.640625)
[Om[PHY]
[Om[PHY]
           Symbol rotation 23/28 => tl 0.000822 (-12540,-30273) (0.312500)
[Om[PHY]
           Symbol rotation 24/28 => tl 0.000857 (32609,3211) (0.984375)
[Om[PHY]
           Symbol rotation 25/28 => tl 0.000893 (-18205,27244) (0.656250)
[Om[PHY]
           Symbol rotation 26/28 => tl 0.000929 (-15447,-28898) (0.328125)
[Om[PHY]
           Symbol rotation 27/28 \Rightarrow tl 0.000964 (32767,0) (1.000000)
[Om[PHY]
           Timeshift symbol rotation 0 \Rightarrow (32767,0) \ 0.000000
[Om[PHY]
           Timeshift symbol rotation 1 \Rightarrow (32717, 1809) - 0.055223
[Om[PHY]
           Timeshift symbol rotation 2 \Rightarrow (32567, 3612) -0.110447
[Om[PHY]
           Timeshift symbol rotation 3 \Rightarrow (32318, 5404) - 0.165670
[Om[PHY]
           Timeshift symbol rotation 4 \Rightarrow (31971,7179) -0.220893
[Om[PHY]
           Timeshift symbol rotation 5 \Rightarrow (31526,8933) -0.276117
[Om[PHY]
           Timeshift symbol rotation 6 \Rightarrow (30985, 10659) -0.331340
[Om[PHY]
           Timeshift symbol rotation 7 => (30349, 12353) -0.386563
[Om[PHY]
           Timeshift symbol rotation 8 = (29621, 14010) - 0.441786
[Om[PHY]
           Timeshift symbol rotation 9 => (28803, 15623) -0.497010
[Om[PHY]
           qNB 0 configured
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 0 DL 1 UL 0
[Om[NR MAC]
              In rrc_mac_config_req_gNB: slot 1 DL 1 UL 0
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 2 DL 1 UL 0
              In rrc_mac_config_req_gNB: slot 3 DL 1 UL 1
[Om[NR_MAC]
[Om[NR MAC]
              In rrc mac config reg qNB: slot 4 DL 0 UL 1
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 5 DL 1 UL 0
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 6 DL 1 UL 0
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 7 DL 1 UL 0
[Om[NR MAC]
              In rrc_mac_config_req_gNB: slot 8 DL 1 UL 1
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 9 DL 0 UL 1
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 10 DL 1 UL 0
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 11 DL 1 UL 0
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 12 DL 1 UL 0
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 13 DL 1 UL 1
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 14 DL 0 UL 1
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 15 DL 1 UL 0
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 16 DL 1 UL 0
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 17 DL 1 UL 0
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 18 DL 1 UL 1
[Om[NR_MAC]
              In rrc_mac_config_req_gNB: slot 19 DL 0 UL 1
[Om[ITTI]
            Created Posix thread TASK RRC GNB
            Configuring GTPu
[Om[GTPU]
[Om[GTPU]
            SA mode
[Om[GTPU]
            Configuring GTPu address : 192.168.120.68, port : 2152
[Om[GTPU]
            Initializing UDP for local address 192.168.120.68 with port 2152
```

```
[Om[GTPU]
            Created gtpu instance id: 100
[Om[UTIL]
            threadCreate for TASK GTPV1 U, affinity ffffffff, priority 50
[Om[ITTI]
            Created Posix thread TASK_GTPV1_U
          Initializing gNB 0 single thread flag:1
[Om[PHY]
[Om[PHY]
          Initializing qNB 0
[Om[PHY]
          Registering with MAC interface module (before 0x3498f20)
[Om[PHY]
          Installing callbacks for IF_Module - UL_indication
[Om[PHY]
          Registering with MAC interface module (after 0x3498f20)
[Om[PHY]
          Setting indication lists
[Om[PHY]
          [nr-gnb.c] gNB structure allocated
[Om[PHY]
          Setting clock source to internal
[Om[PHY]
          Setting time source to internal
          number of L1 instances 1, number of RU 1, number of CPU cores 16
[Om[PHY]
[Om[1;31m[PHY] DJP - delete code above this ../../executables/nr-ru.c:1763
[Om[PHY]
          Copying frame parms from gNB in RC to gNB 0 in ru 0 and frame_parms in ru
[0mDL frequency 3691380000: band 77, UL frequency 3691380000
[LIBCONFIG] (root): 2/2 parameters successfully set, (0 to default value)
[LIBCONFIG] qNBs.[0]: 28/28 parameters successfully set, (17 to default value)
[LIBCONFIG] gNBs.[0].plmn list.[0]: 3/3 parameters successfully set, (0 to default v
[LIBCONFIG] (root): 2/2 parameters successfully set, (0 to default value)
[LIBCONFIG] qNBs.[0].NETWORK INTERFACES: 10/10 parameters successfully set, (3 to de
START MAIN THREADS
RC.nb nr L1 inst:1
Initializing gNB threads single_thread_flag:1 wait_for_sync:0
wait_gNBs()
Waiting for gNB L1 instances to all get configured ... sleeping 50ms (nb nr sL1 inst
gNB L1 are configured
About to Init RU threads RC.nb_RU:1
Initializing RU threads
configuring RU from file
[LIBCONFIG] RUS.[0]: 42/42 parameters successfully set, (27 to default value)
Set RU mask to 1
Creating RC.ru[0]:0x34dcfe0
RU 0: Transport raw_if4p5
[RU 0] Setting nr_flag 0, nr_band 78, nr_scs_for_raster 1
[RU 0] Setting half-slot parallelization to 1
[LIBCONFIG] device.recplay: 8/8 parameters successfully set, (8 to default value)
[LIBCONFIG] device: 1/1 parameters successfully set, (1 to default value)
[LIBCONFIG] loader: 2/2 parameters successfully set, (2 to default value)
[LIBCONFIG] loader.oai_transpro: 2/2 parameters successfully set, (1 to default value)
shlib_path liboai_transpro.so
[LOADER] library liboai transpro.so successfully loaded
```

```
UP VF [0000:04:02.0], CP VF [0000:04:02.1]
wrapper.hpp: m xranInit.io cfq.dpdk dev[0] =0000:04:02.0, m xranInit.io cfq.dpdk dev
*** Numerology []
*** Number of Slot [20]
*** IO Width []
*** Compression Method [ ]
ORAN: transport_init
Machine is not synchronized using PTP (1)!
0-DU MAC address: 00:11:22:33:44:66
O-RU MAC address: 00:FFFFFFAA:FFFFFFFFFFFFBB:FFFFFFFFFFFCC
eAxCID - 12:8:4:0 (f000, 0f00, 00f0, 000f)
Total BF Weights: 32
xran_init: MTU 1500
total cores 16 c_mask 0x7 core 1 [id] system_core 0 [id] pkt_proc_core 0x4 [mask] pk
xran_ethdi_init_dpdk_io: Calling rte_eal_init:wls -c 0x7 -n2 --iova-mode=pa --socket
EAL: Probing VFIO support...
EAL: VFIO support initialized
EAL: No legacy callbacks, legacy socket not created
EAL: Invalid NUMA socket, default to 0
EAL: using IOMMU type 1 (Type 1)
EAL: Probe PCI driver: net_i40e_vf (8086:154c) device: 0000:04:02.0 (socket 0)
initializing port 0 for TX, drv=net i40e vf
Port 0 MAC: 00 11 22 33 44 66
Port 0: nb_rxd 4096 nb_txd 4096
Checking link status portid [0] ... done
Port 0 Link Up - speed 10000 Mbps - full-duplex
EAL: Invalid NUMA socket, default to 0
EAL: Probe PCI driver: net_i40e_vf (8086:154c) device: 0000:04:02.1 (socket 0)
initializing port 1 for TX, drv=net_i40e_vf
Port 1 MAC: 00 11 22 33 44 66
Port 1: nb_rxd 4096 nb_txd 4096
Checking link status portid [1] ... done
Port 1 Link Up - speed 10000 Mbps - full-duplex
vf 0 local SRC MAC: 00 11 22 33 44 66
vf 0 remote DST MAC: 00 aa ff bb ff cc
vf 1 local SRC MAC: 00 11 22 33 44 66
vf 1 remote DST MAC: 00 aa ff bb ff cc
wrapper.hpp: nFpgaToSW_FTH_RxBufferLen=13168 , nSW_ToFpga_FTH_TxBufferLen=15696
XRAN front haul xran_mm_init
xran_sector_get_instances [0]: CC 0 handle 0x358b440
```

```
Handle: 0x7f234317cc70 Instance: 0x358b440
init memory [0]: CC 0 handle 0x358b440
Sucess xran_mm_init
wrapper.hpp: Init memory *** XRANFTHTX OUT ***
Call xran bm init 0
ru 0 cc 0 idx 0: [ handle 0x358b440 0 0 ] [nPoolIndex 0] nNumberOfBuffers 1120 nBuff
CC: [ handle 0x358b440 ru 0 cc_idx 0 ] [nPoolIndex 0] mb pool 0x2ea2f6700
wrapper.hpp: Init memory *** XRANFTHTX_SEC_DESC_OUT ***
ru_0_cc_0_idx_1: [ handle 0x358b440 0 0 ] [nPoolIndex 1] nNumberOfBuffers 17920 nBuf
CC: [ handle 0x358b440 ru 0 cc_idx 0 ] [nPoolIndex 1] mb pool 0x2e9020bc0
wrapper.hpp: Init memory *** XRANFTHTX_PRB_MAP_OUT ***
ru 0 cc 0 idx 2: [ handle 0x358b440 0 0 ] [nPoolIndex 2] nNumberOfBuffers 1120 nBuff
CC: [ handle 0x358b440 ru 0 cc_idx 0 ] [nPoolIndex 2] mb pool 0x2e8486580
wrapper.hpp: Init memory *** XRANFTHRX_IN ***
ru_0_cc_0_idx_3: [ handle 0x358b440 0 0 ] [nPoolIndex 3] nNumberOfBuffers 1120 nBuff
CC: [ handle 0x358b440 ru 0 cc_idx 0 ] [nPoolIndex 3] mb pool 0x2e4ea8a40
wrapper.hpp: Init memory *** XRANFTHTX SEC DESC IN ***
ru_0_cc_0_idx_4: [ handle 0x358b440 0 0 ] [nPoolIndex 4] nNumberOfBuffers 17920 nBuf
CC: [ handle 0x358b440 ru 0 cc idx 0 ] [nPoolIndex 4] mb pool 0x2e3bd2f00
wrapper.hpp: Init memory *** XRANFTHRX_PRB_MAP_IN ***
ru 0 cc 0 idx 5: [ handle 0x358b440 0 0 ] [nPoolIndex 5] nNumberOfBuffers 1120 nBuff
CC:[ handle 0x358b440 ru 0 cc idx 0 ] [nPoolIndex 5] mb pool 0x2e30388c0
wrapper.hpp: Init memory *** XRANFTHRACH IN ***
ru_0_cc_0_idx_6: [ handle 0x358b440 0 0 ] [nPoolIndex 6] nNumberOfBuffers 1120 nBuff
CC:[ handle 0x358b440 ru 0 cc_idx 0 ] [nPoolIndex 6] mb pool 0x2dfa5ad80
wrapper.hpp: Init memory *** XRANSRS IN ***
ru_0_cc_0_idx_7: [ handle 0x358b440 0 0 ] [nPoolIndex 7] nNumberOfBuffers 1120 nBuff
CC:[ handle 0x358b440 ru 0 cc_idx 0 ] [nPoolIndex 7] mb pool 0x2def74f40
INIT DONE
[HW] [RAU] has loaded ETHERNET trasport protocol.
[Om[PHY]
          Starting ru_thread 0
[Om[PHY]
          Initializing RU proc 0 (NGFI_RAU_IF4p5,synch_to_ext_device),
[Om[UTIL] threadCreate for ru_thread, affinity 8, priority 97
[Om[PHY]
          Starting RU 0 (NGFI_RAU_IF4p5, synch_to_ext_device) on cpu 0
[Om[PHY]
          Initializing frame parms for mu 1, N_RB 273, Ncp 0
[0m[93m[PHY]
              Init: N_RB_DL 273, first_carrier_offset 2458, nb_prefix_samples 288,n
[Om[PHY]
          fp->scs=30000
[Om[PHY]
          fp->ofdm symbol size=4096
[Om[PHY]
          fp->nb_prefix_samples0=352
[Om[PHY] fp->nb_prefix_samples=288
[Om[PHY]
          fp->slots_per_subframe=2
[Om[PHY]
          fp->samples per subframe wCP=114688
```

```
fp->samples per frame wCP=1146880
[Om[PHY]
           fp->samples per subframe=122880
[Om[PHY]
[Om[PHY]
           fp->samples_per_frame=1228800
           fp->dl CarrierFreg=3691380000
[Om[PHY]
[Om[PHY]
           fp->ul CarrierFreg=3691380000
[Om[PHY]
           Setting RF config for N RB 273, NB RX 2, NB TX 2
[Om[PHY]
           Channel 0: setting tx_gain offset 0, rx_gain offset 0, tx_freq 3691380000
[Om[PHY]
           Channel 1: setting tx_gain offset 0, rx_gain offset 0, tx_freg 3691380000
[Om[PHY]
           Initializing RU signal buffers (if_south IF4p5 RRU) nb_tx 2, nb_rx 2
[Om[PHY]
           nb_tx 2
[Om[PHY]
           rxdata_7_5kHz[0] 0x7f232361e040 for RU 0
[Om[PHY]
           rxdata 7 5kHz[1] 0x7f232343d040 for RU 0
[Om[PHY]
           [INIT] common.txdata_BF= 0x7f23180009a0 (16 bytes)
[Om[PHY]
           txdataF_BF[0] 0x7f23180009e0 for RU 0
[Om[PHY]
           txdataF_BF[1] 0x7f2318070a40 for RU 0
[Om[PHY]
           rxdataF[0] 0x7f23180e0b20 for RU 0
[Om[PHY]
           rxdataF[1] 0x7f23181c0b80 for RU 0
[Om[PHY]
           [INIT] nr_phy_init_RU() ru->num_gNB:1
[Om[PHY]
           Starting IF interface for RU 0, nb rx 2
[Om[PHY]
           RU 0 Setting N_TA_offset to 1600 samples (factor 4.000000, UL Freq 364224
[Om[PHY]
           Signaling main thread that RU 0 is ready, sl ahead 5
[Om[PHY]
           Waiting for RUs to be configured ... RC.ru mask:00
[Om[PHY]
          RUs configured
[Om[PHY]
           init_eNB_afterRU() RC.nb_nr_inst:1
[Om[PHY]
          RC.nb_nr_CC[inst:0]:0x7f23bda88010
[Om[PHY]
           [qNB 0] phy init nr qNB() About to wait for qNB to be configured
[Om[PHY]
           Initialise nr transport
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 0/32
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 1/32
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 2/32
[Om[PHY]
           Allocating Transport Channel Buffers for PUCCH 3/32
           Allocating Transport Channel Buffers for PUCCH 4/32
[Om[PHY]
           Allocating Transport Channel Buffers for PUCCH 5/32
[Om[PHY]
[Om[PHY]
           Allocating Transport Channel Buffers for PUCCH 6/32
[Om[PHY]
           Allocating Transport Channel Buffers for PUCCH 7/32
[Om[PHY]
           Allocating Transport Channel Buffers for PUCCH 8/32
[Om[PHY]
           Allocating Transport Channel Buffers for PUCCH 9/32
[Om[PHY]
           Allocating Transport Channel Buffers for PUCCH 10/32
[Om[PHY]
           Allocating Transport Channel Buffers for PUCCH 11/32
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 12/32
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 13/32
[Om[PHY]
           Allocating Transport Channel Buffers for PUCCH 14/32
```

```
[Om[PHY]
           Allocating Transport Channel Buffers for PUCCH 15/32
           Allocating Transport Channel Buffers for PUCCH 16/32
[Om[PHY]
[Om[PHY]
           Allocating Transport Channel Buffers for PUCCH 17/32
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 18/32
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 19/32
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 20/32
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 21/32
[Om[PHY]
           Allocating Transport Channel Buffers for PUCCH 22/32
          Allocating Transport Channel Buffers for PUCCH 23/32
[Om[PHY]
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 24/32
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 25/32
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 26/32
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 27/32
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 28/32
[Om[PHY]
           Allocating Transport Channel Buffers for PUCCH 29/32
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 30/32
[Om[PHY]
          Allocating Transport Channel Buffers for PUCCH 31/32
          Allocating Transport Channel Buffers for SRS 0/4
[Om[PHY]
[Om[PHY]
          Allocating Transport Channel Buffers for SRS 1/4
[Om[PHY]
          Allocating Transport Channel Buffers for SRS 2/4
[Om[PHY]
          Allocating Transport Channel Buffers for SRS 3/4
[Om[PHY]
          Allocating Transport Channel Buffers for ULSCH 0/16
[Om[PHY]
          Allocating Transport Channel Buffers for ULSCH 1/16
[Om[PHY]
          Allocating Transport Channel Buffers for ULSCH 2/16
          Allocating Transport Channel Buffers for ULSCH
[Om[PHY]
                                                           3/16
[Om[PHY]
          Allocating Transport Channel Buffers for ULSCH 4/16
[Om[PHY]
           Allocating Transport Channel Buffers for ULSCH 5/16
          Allocating Transport Channel Buffers for ULSCH 6/16
[Om[PHY]
[Om[PHY]
          Allocating Transport Channel Buffers for ULSCH 7/16
[Om[PHY]
          Allocating Transport Channel Buffers for ULSCH 8/16
[Om[PHY]
          Allocating Transport Channel Buffers for ULSCH
                                                           9/16
           Allocating Transport Channel Buffers for ULSCH 10/16
[Om[PHY]
          Allocating Transport Channel Buffers for ULSCH 11/16
[Om[PHY]
[Om[PHY]
          Allocating Transport Channel Buffers for ULSCH 12/16
[Om[PHY]
          Allocating Transport Channel Buffers for ULSCH 13/16
[Om[PHY]
          Allocating Transport Channel Buffers for ULSCH 14/16
[Om[PHY]
          Allocating Transport Channel Buffers for ULSCH 15/16
[Om[PHY]
           Mapping RX ports from 1 RUs to qNB 0
[Om[PHY]
           qNB->num RU:1
[Om[PHY]
          Attaching RU 0 antenna 0 to gNB antenna 0
[Om[PHY]
           Attaching RU 0 antenna 1 to gNB antenna 1
[Om[UTIL]
            threadCreate for Tpoolo_-1, affinity ffffffff, priority 97
```

```
threadCreate for Tpool1 -1, affinity ffffffff, priority 97
[Om[UTIL]
            threadCreate for Tpool2 -1, affinity ffffffff, priority 97
[Om[UTIL]
[Om[UTIL]
            threadCreate for Tpool3_-1, affinity ffffffff, priority 97
            threadCreate for Tpool4_-1, affinity ffffffff, priority 97
[Om[UTIL]
[Om[UTIL]
            threadCreate for Tpool5 -1, affinity ffffffff, priority 97
            threadCreate for Tpool6 -1, affinity ffffffff, priority 97
[Om[UTIL]
[Om[UTIL]
            threadCreate for Tpool7_-1, affinity ffffffff, priority 97
[Om[UTIL]
            threadCreate for L1_rx_thread, affinity ffffffff, priority 97
[Om[PHY]
           Allocating Transport Channel Buffers for DLSCH 0/16
[Om[PHY]
          Allocating 72 segments (MAX 36, N_PRB 273)
[Om[PHY]
          Allocating Transport Channel Buffers for DLSCH 1/16
[Om[PHY]
          Allocating 72 segments (MAX 36, N_PRB 273)
          Allocating Transport Channel Buffers for DLSCH 2/16
[Om[PHY]
[Om[PHY]
          Allocating 72 segments (MAX 36, N_PRB 273)
[Om[PHY]
           Allocating Transport Channel Buffers for DLSCH 3/16
[Om[PHY]
          Allocating 72 segments (MAX 36, N_PRB 273)
[Om[PHY]
          Allocating Transport Channel Buffers for DLSCH 4/16
[Om[PHY]
          Allocating 72 segments (MAX 36, N_PRB 273)
[Om[PHY]
          Allocating Transport Channel Buffers for DLSCH 5/16
[Om[PHY]
          Allocating 72 segments (MAX 36, N_PRB 273)
[Om[PHY]
           Allocating Transport Channel Buffers for DLSCH 6/16
[Om[PHY]
          Allocating 72 segments (MAX 36, N PRB 273)
[Om[PHY]
          Allocating Transport Channel Buffers for DLSCH 7/16
[Om[PHY]
          Allocating 72 segments (MAX 36, N_PRB 273)
[Om[PHY]
          Allocating Transport Channel Buffers for DLSCH 8/16
[Om[PHY]
           Allocating 72 segments (MAX 36, N PRB 273)
[Om[PHY]
           Allocating Transport Channel Buffers for DLSCH 9/16
[Om[PHY]
          Allocating 72 segments (MAX 36, N_PRB 273)
[Om[PHY]
          Allocating Transport Channel Buffers for DLSCH 10/16
[Om[PHY]
          Allocating 72 segments (MAX 36, N_PRB 273)
[Om[PHY]
           Allocating Transport Channel Buffers for DLSCH 11/16
[Om[PHY]
           Allocating 72 segments (MAX 36, N_PRB 273)
[Om[PHY]
          Allocating Transport Channel Buffers for DLSCH 12/16
[Om[PHY]
          Allocating 72 segments (MAX 36, N_PRB 273)
[Om[PHY]
          Allocating Transport Channel Buffers for DLSCH 13/16
[Om[PHY]
          Allocating 72 segments (MAX 36, N_PRB 273)
[Om[PHY]
          Allocating Transport Channel Buffers for DLSCH 14/16
[Om[PHY]
          Allocating 72 segments (MAX 36, N PRB 273)
[Om[PHY]
           Allocating Transport Channel Buffers for DLSCH 15/16
[Om[PHY]
          Allocating 72 segments (MAX 36, N_PRB 273)
[Om[UTIL]
           threadCreate for L1_stats, affinity ffffffff, priority 1
[OmSetUp ORAN. Done
```

```
**__**__**__**__**__**__**__**__**
ORAN Configuration
* Numerology
                 = 1
* Duplex Type
                = 1
* Number CC
                = 1
* Number eAxc
                = 2
* Number eAxc UL = 0
* Number RBs DL = 273
* Number RBs UL = 273
**__**__**__**__**__**__**__**__**
physide_dl_tti_call_backRegister physide callbacks. Done
Open Oran callbacks. Done
Init Oran. Done
xran open: 5G NR Category A
xRAN open PRACH config: Numerology 1 ConfIdx 159, preambleFmrt 10 startsymb 0, numSy
PRACH: x \ 1 \ y[0] \ 0, \ y[1] \ 0 \ prach \ slot: 9 ...
PRACH start symbol 0 lastsymbol 11
xran_open: interval_us=500
XRAN UP VF: 0x0000
XRAN_CP_VF: 0x0001
xran_timing_source_thread [CPU 1] [PID: 4424]
ring_processing_thread [CPU 2] [PID: 4424]
xran_open. Done
openairO_transport_init returns 0 for ru_id 0
ORAN: get_internal_parameter
ORAN: get_internal_parameter
ORAN: trx_oran_start
Start ORAN. Done
setup_RU_buffers: frame_parms = 0x34e2a90
waiting for sync (ru_thread, -1/0x12a8a14,0x20319e0,0x1f26f00)
wait RUs
ALL RUS READY!
RC.nb_RU:1
ALL RUs ready - init gNBs
Not NFAPI mode - call init_eNB_afterRU()
[LIBCONFIG] loader.dfts: 2/2 parameters successfully set, (1 to default value)
shlib_path libdfts.so
[LOADER] library libdfts.so successfully loaded
[LIBCONFIG] loader.ldpc: 2/2 parameters successfully set, (1 to default value)
```

```
shlib path libldpc.so
[LOADER] library libldpc.so successfully loaded
O-DU: thread_run start time: 07/06/23 09:50:36.000000004 UTC [500]
Start C-plane DL -5 us after TTI [trigger on sym 120260]
Start C-plane UL -5 us after TTI [trigger on sym 120260]
Start U-plane DL 505 us before OTA [offset in sym -14]
Start U-plane UL 180 us OTA
                                   [offset in sym 6]
C-plane to U-plane delay 510 us after TTI
Start Sym timer 71428 ns
interval_us 500
create a thread for core -1
waiting for sync (L1_stats_thread, -1/0x12a8a14,0x20319e0,0x1f26f00)
ALL RUs ready - ALL gNBs ready
Sending sync to all threads
Entering ITTI signals handler
TYPE <CTRL-C> TO TERMINATE
got sync (ru_thread)
got sync (L1_stats_thread)
        RU 0 no rf device
[PHY]
          RU 0 RF started opp_enabled 0
[Om[PHY]
[Om[PHY]
          before adjusting, OAI: frame=0 slot=0, XRAN: frame=0 slot=1
[Om[PHY]
          After adjusting, OAI: frame=0 slot=1, XRAN: frame=0 slot=1
[Om[NR_MAC]
             Frame.Slot 128.0
[Om[NR_MAC]
              Frame.Slot 256.0
[Om[NR_MAC]
              Frame.Slot 384.0
[Om[NR_MAC]
              Frame.Slot 512.0
[Om[NR_MAC]
              Frame.Slot 640.0
[Om[NR_MAC]
              Frame.Slot 768.0
[Om[NR_MAC]
              Frame.Slot 896.0
```

[Om[NR_MAC] Frame.Slot 0.0

[0m[PHY] prach_IO = 0.0 dB

[Om[NR_MAC] Frame.Slot 128.0

[Om[NR_MAC] Frame.Slot 256.0

[Om[NR_MAC] Frame.Slot 384.0

[0m[NR_MAC] Frame.Slot 512.0

[Om[NR_MAC] Frame.Slot 640.0

[0m[NR_MAC] Frame.Slot 768.0

[Om[NR_MAC] Frame.Slot 896.0

[Om[NR_MAC] Frame.Slot 0.0

[0m[PHY] prach_IO = 0.0 dB

[Om[NR_MAC] Frame.Slot 128.0

[Om[NR_MAC] Frame.Slot 256.0

[Om[NR_MAC] Frame.Slot 384.0

[Om[NR_MAC] Frame.Slot 512.0

[Om[NR_MAC] Frame.Slot 640.0

[0m[NR_MAC] Frame.Slot 768.0

[Om[NR_MAC] Frame.Slot 896.0

[Om[NR_MAC] Frame.Slot 0.0

[0m[PHY] prach_IO = 0.0 dB

[Om[NR_MAC] Frame.Slot 128.0

[Om[NR_MAC] Frame.Slot 256.0

[Om[NR_MAC] Frame.Slot 384.0

- [Om[NR_MAC] Frame.Slot 512.0
- [Om[NR_MAC] Frame.Slot 640.0
- [0m[NR_MAC] Frame.Slot 768.0
- [Om[NR_MAC] Frame.Slot 896.0
- [Om[NR_MAC] Frame.Slot 0.0
- [0m[PHY] prach_IO = 0.0 dB
- [Om[NR_MAC] Frame.Slot 128.0
- [Om[NR_MAC] Frame.Slot 256.0
- [Om[NR_MAC] Frame.Slot 384.0
- [Om[NR_MAC] Frame.Slot 512.0
- [Om[NR_MAC] Frame.Slot 640.0
- [Om[NR_MAC] Frame.Slot 768.0
- [Om[NR_MAC] Frame.Slot 896.0
- [Om[NR_MAC] Frame.Slot 0.0
- [0m[PHY] prach_IO = 0.0 dB
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- [Om[NR_MAC] Frame.Slot 256.0
- [Om[NR_MAC] Frame.Slot 384.0
- [Om[NR_MAC] Frame.Slot 512.0
- [0m[NR_MAC] Frame.Slot 640.0
- [Om[NR_MAC] Frame.Slot 768.0

[Om[NR_MAC] Frame.Slot 896.0

[Om[NR_MAC] Frame.Slot 0.0

[0m[PHY] prach_IO = 0.0 dB

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[Om[NR_MAC] Frame.Slot 256.0

[0m[NR_MAC] Frame.Slot 384.0

[0m[NR_MAC] Frame.Slot 512.0

[Om[NR_MAC] Frame.Slot 640.0

[Om[NR_MAC] Frame.Slot 768.0

[Om[NR_MAC] Frame.Slot 896.0

[Om[NR_MAC] Frame.Slot 0.0

[0m[PHY] prach_IO = 0.0 dB

[Om[NR_MAC] Frame.Slot 128.0

[Om[NR_MAC] Frame.Slot 256.0

[Om[NR_MAC] Frame.Slot 384.0

[0m[NR_MAC] Frame.Slot 512.0

[Om[NR_MAC] Frame.Slot 640.0

[Om[NR_MAC] Frame.Slot 768.0

[Om[NR_MAC] Frame.Slot 896.0

[Om[NR_MAC] Frame.Slot 0.0

[0m[PHY] prach_IO = 0.0 dB

[Om[NR_MAC] Frame.Slot 128.0

[Om[NR_MAC] Frame.Slot 256.0

- [Om[NR_MAC] Frame.Slot 384.0
- [Om[NR_MAC] Frame.Slot 512.0
- [Om[NR_MAC] Frame.Slot 640.0
- [0m[NR_MAC] Frame.Slot 768.0
- [0m[NR_MAC] Frame.Slot 896.0
- [Om[NR_MAC] Frame.Slot 0.0
- [0m[PHY] prach_IO = 0.0 dB
- [Om[NR_MAC] Frame.Slot 128.0
- [Om[NR_MAC] Frame.Slot 256.0
- [Om[NR_MAC] Frame.Slot 384.0
- [Om[NR_MAC] Frame.Slot 512.0
- [Om[NR_MAC] Frame.Slot 640.0
- [Om[NR_MAC] Frame.Slot 768.0
- [Om[NR_MAC] Frame.Slot 896.0
- [0m[NR_MAC] Frame.Slot 0.0
- [0m[PHY] prach_IO = 0.0 dB
- [0m[NR_MAC] Frame.Slot 128.0
- [Om[NR_MAC] Frame.Slot 256.0
- [0m[NR_MAC] Frame.Slot 384.0
- [Om[NR_MAC] Frame.Slot 512.0
- [Om[NR_MAC] Frame.Slot 640.0
- [Om[NR_MAC] Frame.Slot 768.0

- [Om[NR_MAC] Frame.Slot 896.0
- [Om[NR_MAC] Frame.Slot 0.0
- [0m[PHY] prach_IO = 0.0 dB
- [Om[NR_MAC] Frame.Slot 128.0
- [Om[NR_MAC] Frame.Slot 256.0
- [Om[NR_MAC] Frame.Slot 384.0
- [0m[NR_MAC] Frame.Slot 512.0
- [Om[NR_MAC] Frame.Slot 640.0
- [Om[NR_MAC] Frame.Slot 768.0
- [Om[NR_MAC] Frame.Slot 896.0
- [Om[NR_MAC] Frame.Slot 0.0
- [0m[PHY] prach_I0 = 0.0 dB
- [0m[NR_MAC] Frame.Slot 128.0
- [Om[NR_MAC] Frame.Slot 256.0
- [Om[NR_MAC] Frame.Slot 384.0
- [Om[NR_MAC] Frame.Slot 512.0
- [Om[NR_MAC] Frame.Slot 640.0
- [Om[NR_MAC] Frame.Slot 768.0
- [Om[NR_MAC] Frame.Slot 896.0
- [Om[NR_MAC] Frame.Slot 0.0
- [0m[PHY] prach_IO = 0.0 dB
- [0m[NR_MAC] Frame.Slot 128.0

- [Om[NR_MAC] Frame.Slot 256.0
- [Om[NR_MAC] Frame.Slot 384.0
- [Om[NR_MAC] Frame.Slot 512.0
- [Om[NR_MAC] Frame.Slot 640.0
- [Om[NR_MAC] Frame.Slot 768.0
- [Om[NR_MAC] Frame.Slot 896.0
- [Om[NR_MAC] Frame.Slot 0.0
- [0m[PHY] prach_IO = 0.0 dB
- [Om[NR_MAC] Frame.Slot 128.0
- [Om[NR_MAC] Frame.Slot 256.0
- [Om[NR_MAC] Frame.Slot 384.0
- [Om[NR_MAC] Frame.Slot 512.0
- [Om[NR_MAC] Frame.Slot 640.0
- [Om[NR_MAC] Frame.Slot 768.0
- [Om[NR_MAC] Frame.Slot 896.0
- [Om[NR_MAC] Frame.Slot 0.0
- [0m[PHY] prach_IO = 0.0 dB
- [0m[NR_MAC] Frame.Slot 128.0
- [Om[NR_MAC] Frame.Slot 256.0
- [Om[NR_MAC] Frame.Slot 384.0
- [Om[NR_MAC] Frame.Slot 512.0
- [Om[NR_MAC] Frame.Slot 640.0

[Om[NR_MAC] Frame.Slot 768.0

[Om[NR_MAC] Frame.Slot 896.0

[Om[NR_MAC] Frame.Slot 0.0

 $prach_{10} = 0.0 dB$ [Om[PHY] [Om[NR_MAC] Frame.Slot 128.0

Frame.Slot 256.0 [Om[NR_MAC]

[Om[NR_MAC] Frame.Slot 384.0

[Om[NR_MAC] Frame.Slot 512.0

[Om[NR_MAC] Frame.Slot 640.0

[Om[NR_MAC] Frame.Slot 768.0

[Om[NR_MAC] Frame.Slot 896.0

Frame.Slot 0.0 [Om[NR_MAC]

[Om[PHY] $prach_{10} = 0.0 dB$ [Om[NR_MAC] Frame.Slot 128.0

[Om[NR_MAC] Frame.Slot 256.0

[Om[NR_MAC] Frame.Slot 384.0

[Om[NR_MAC] Frame.Slot 512.0

Frame.Slot 640.0 [Om[NR_MAC]

[Om[NR_MAC] Frame.Slot 768.0

[Om[NR_MAC] Frame.Slot 896.0

Frame.Slot 0.0 [Om[NR_MAC]

[Om[PHY] $prach_{10} = 0.0 dB$

Frame.Slot 128.0 [Om[NR_MAC]

- [Om[NR_MAC] Frame.Slot 256.0
- [0m[NR_MAC] Frame.Slot 384.0
- [Om[NR_MAC] Frame.Slot 512.0
- [Om[NR_MAC] Frame.Slot 640.0
- [0m[NR_MAC] Frame.Slot 768.0
- [Om[NR_MAC] Frame.Slot 896.0
- [Om[NR_MAC] Frame.Slot 0.0
- [Om[PHY] prach_IO = 0.0 dB [Om[NR_MAC] Frame.Slot 128.0
- [Om[NR_MAC] Frame.Slot 256.0
- [Om[NR_MAC] Frame.Slot 384.0
- [Om[NR_MAC] Frame.Slot 512.0
- [Om[NR_MAC] Frame.Slot 640.0
- [0m[NR_MAC] Frame.Slot 768.0
- [0m[NR_MAC] Frame.Slot 896.0
- [Om[NR_MAC] Frame.Slot 0.0
- [0m[PHY] prach_I0 = 0.0 dB
- [Om[NR_MAC] Frame.Slot 128.0
- [0m[NR_MAC] Frame.Slot 256.0
- [Om[NR_MAC] Frame.Slot 384.0
- [Om[NR_MAC] Frame.Slot 512.0
- [Om[NR_MAC] Frame.Slot 640.0

[Om[NR_MAC] Frame.Slot 768.0

[Om