ANSALDO SIGNAL

A Finmeccanica Company

UNION SWITCH & SIGNAL

UM-6800A

Microlok® II

FUNCTIONAL DESCRIPTION

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MANUAL CONTENTS

1.1. INTRODUCTION

This manual provides the following information about the Microlok II system.

- System level application and operational descriptions
- System component specifications

This manual is to be referred in conjunction with the Microlok II service manual SM6800A.

2.1. SYSTEM OVERVIEW

The Microlok II system operation is controlled by proprietary executive software running on the system hardware. The user application logic is written in a proprietary Microlok II programming language and is compiled by a proprietary compiler into a set of data tables which are interpreted by the executive software during run-time.

The high-level block diagram of the Microlok II system is shown below. The system uses diversity and self-checking concepts in which critical operations are performed in diverse ways, using diverse software operations and critical system hardware is tested with self-checking operations. Permissive outputs are allowed only if the results of diverse logic operations correspond and the self-checks reveal no failures. It uses a combination of vital and non-vital hardware, and an executive software performing critical operations on the site-specific application logic tables using dual-path processing and double storage techniques along with continuous monitoring of the hardware through the use of extensive built-in diagnostics. Any failure in any critical portion of the equipment will result in the controlled system returning to a safe state.

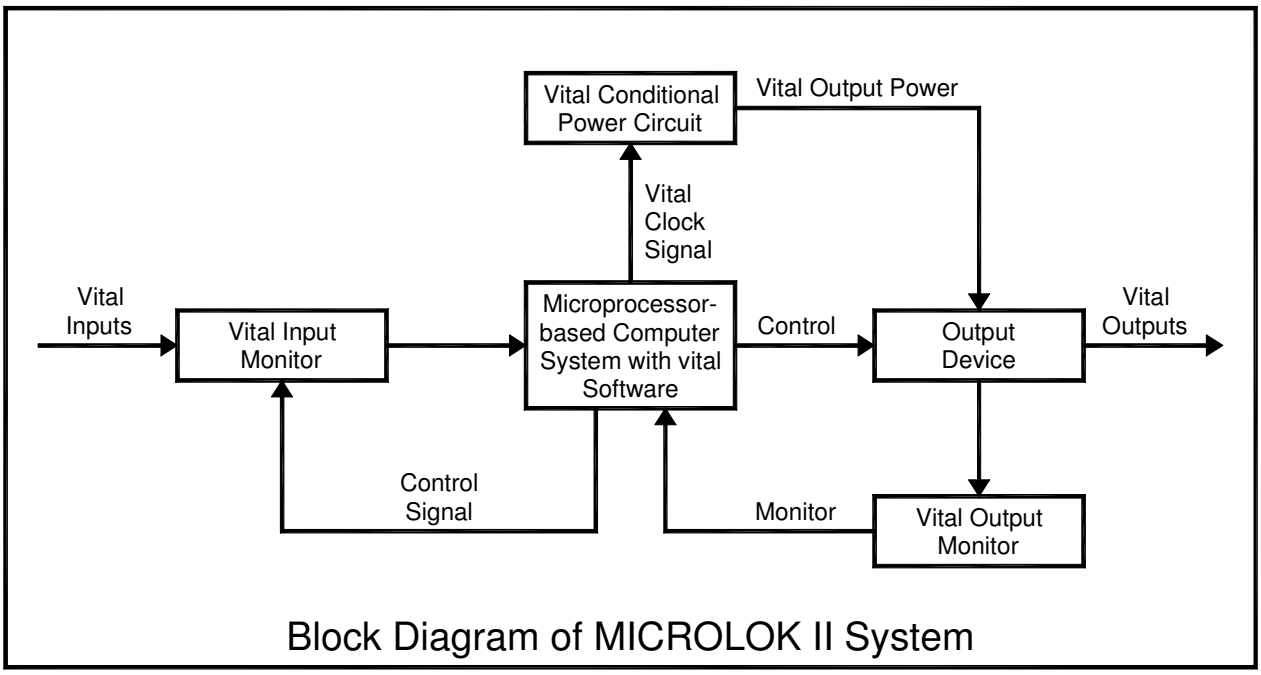

Figure-1

3.1. SYSTEM DESCRIPTION

The Microlok II interlocking system is a multi-purpose monitoring and control system, which performs the following.

- Drive Signal, Point, Crank Handle, LC Gate and Siding control relays
- Monitoring of Point position, track circuits occupancy and other field inputs
- Vital CPU for overall system monitoring, control, diagnostics and data recording
- Executive and application logic for vital interlocking functions
- Executive and application logic for non-vital control Panel & Operator VDU functions
- Serial I/O channels for communicating with MLK II to MLK II, MLK II to CAB/ Other Non-Vital application, Maintenance and Diagnostic function

4.1. MICROLOK II HARDWARE

The Microlok II system consists of modular card file-mounted equipment and external peripheral devices that are used to interface the card file circuitry to the field gears and other associated control systems. The following sections provide an overview of the hardware.

4.1.1. ENVIRONMENTAL

- The Microlok II product will operate in a standard railway environment
- The system operates in ambient temperature ranges of –40 to +70 degrees centigrade. This refers to the temperature outside the card file but inside the relevant building enclosure
- The system operates from 0 to 95% non-condensing humidity
- The system meets the required EMI specification
- The system meets the required vibration specification

4.1.2. PHYSICAL

- The card file is 16.75" wide and it can be mounted in a standard 19" rack
- Boards in the card file include a faceplate where status information will be displayed. A blank panel will be available to cover empty slots
- The system will accept power from an external battery in the range of 9.8V DC to 16.2V DC for an internal conversion to the required voltages
- The internal power converter will have a start-up voltage requirement of 11.5V DC to inhibit start-up when the battery voltage is low
- Nominal 24V input/output boards will have an input/output supply in the range of 19.6V DC to 32.4V DC

4.1.3. CARDFILE

The Microlok II card file is a G64/96 bus based card file that holds the CPU, Power Supply & Variety of I/O boards. The card file will be a user configurable. The Microlok II card file is designed to house standard 6UX220 Euro card plug-in printed circuit boards. The card file will have twenty slots.

- Slots No. 1 to 15 & 20 are used to accommodate Non-Vital or Vital I/O boards.
- Slot No. 16 & 17 are reserved for Power Supply board.
- Slot No. 18 & 19 are reserved for CPU board.

4.1.4. CPU BOARD

The CPU board is controlled by a Motorola 68332 microprocessor, which operates at a speed of 21 MHz, and includes 2K bytes of internal fast termination RAM. Most internal operations are 32 bits wide, while all outside bus cycles are 16 or 8 bits wide. The executive and application software is stored in four flash EPROMs that provide up to 8MB of memory. Flash EPROMs permit direct handling of the executive and application software using a PC connected to the CPU board front panel serial port connector. Jumpers are provided on the board to enable or disable the flash EPROMs for

programming and to select the required programming voltage. The CPU board contains the central controlling logic and diagnostic monitoring for the Microlok II system, and provides five serial data ports. The CPU connector housing has an internal EEPROM that is used to store site-specific configuration data. Even if the CPU board is replaced, the configuration data remains intact within the CPU connector's EEPROM.

- Ports 1 and 2 support an RS-485 hardware interface
- Port 3 supports an RS-423 & RS 232 interface
- Port 4 & 5 supports an RS-232 interface

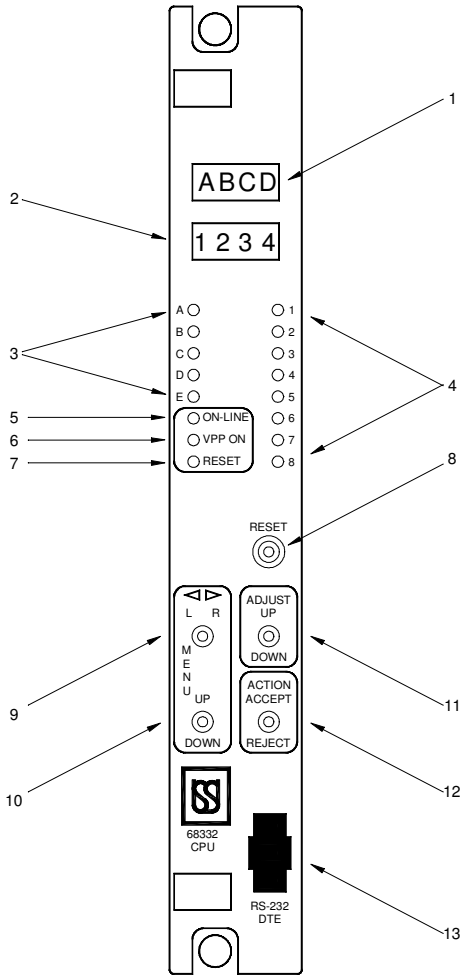

Figure – 2

Fig. 2 Ref	Label	Device	Purpose
1, 2	(None)	4-character alpha-numeric displays	On-site configuration programming menus and options.
3	**A, B, C, D, E**	Yellow LEDs	Reserved for serial link status.
4	**1, 2, 3, 4, 5, 6, 7, 8**	Red LEDs	User-defined in application software.
5	**ON LINE**	Green LED	When lit, indicates normal system operation (successful diagnostics).
6	**VPP ON**	Yellow LED	When lit, indicates FLASH +5V or +12V programming voltage enabled (via board jumper).
7	**RESET**	Green LED	When lit, indicates that the system is in reset mode.
8	**RESET**	Momentary pushbutton	When pressed, resets the CPU. Also used to place the CPU in the reset mode.
9	**MENU L-R**	3-position (return-to-center) toggle switch	Used to search main program menu items shown on displays.
10	**MENU UP-DOWN**	3-position (return-to-center) toggle switch	Used to select main program menu items shown on displays.
11	**ADJUST UP-DOWN**	3-position (return-to-center) toggle switch	Used to cycle through configuration values to be selected with **"ACTION"** switch.
12	**ACTION ACCEPT-REJECT**	3-position (return-to-center) toggle switch	Executes or cancels configuration value selected with **"ADJUST"** switch.
13	**RS-232 DTE Diagnostic Link Connector**	DB9, RS-232 Connector (DTE)	Used for connection to Maintenance PC for System monitoring diagnosis.

CPU Function

- Monitoring external inputs from vital input boards and non-vital input boards
- Processing vital external inputs and executing logic defined in the application software
- Driving vital output boards as required by the application program
- Monitoring and controlling serial communication ports (links to other controllers)
- Testing individual vital input and output channels for faults (in parallel with control of these channels) and responding to detected faults
- Monitoring system internal operation for faults and responding to detected faults
- Controlling power to vital outputs through the card file power supply and an external VCOR (fail-safe function)
- Recording system faults and routine events in user-accessible memory

- Responding to CPU board front panel switch inputs and operating the associated displays
- Interacting with a laptop PC during system diagnostic operations, application logic programming, and executive software upgrading

4.1.5. POWER SUPPLY BOARD

The Power supply board will have double width housed in the card file and it operates in the range of 9.5V to 16.5V DC producing 5V at 3amps and ±12V at 1amp that are needed for the operation of the card file circuitry. The power supply will have a start–up voltage requirement of 11.5V DC. This prevents the unit from attempting a recovery when battery voltage is low. The power supply board performs the following functions:

- Converts the external supply voltage (9.8V to 16.2V DC) to regulated ±12V and +5 for outputs to the system card file internal circuits
- Supplies energy to the VCOR relay coil under the control of the CPU board

The power supply board serves a vital role in the fail-safe design of the Microlok II system. The regulated ±12V and +5V power is distributed to all system card file boards through the card file back plane bus.

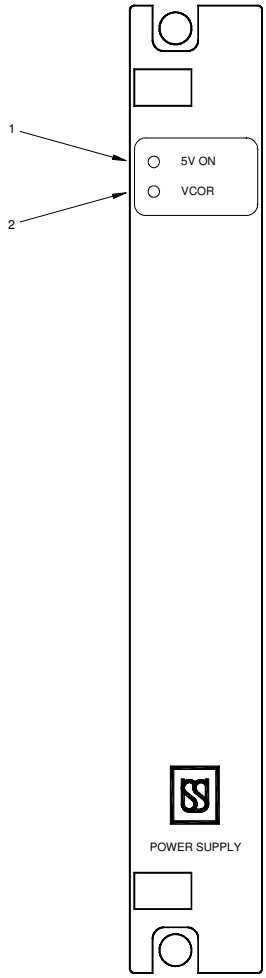

Figure - 3

Fig. 2-2 Ref	Label	Device	Purpose
1	**5V ON**	LED (green)	When lit, indicates 5V-operating power on to other Cardfile PCBs (If not lit refer to Figure-2.2.1).
2	**VCOR**	LED (green)	When lit, indicates conditional power on to VCOR relay (CPU diagnostics normal). (If not lit refer “CPS CLEAR FUNCTION” details in Figure-3.4).

4.1.6. PHYSICAL I/O

The Physical I/O characteristics have been chosen to accommodate normal railway and transit interface devices. Requirements for standard 24V DC battery supply, Vital and Non-Vital relays, lamps and LED indications have all been taken into account in determining voltage and current limits. The voltage and current ranges specified for each I/O type are based on the minimum and maximum requirements for these devices. The supply voltage

is assumed to be the maximum high voltage or minimum low voltage depending on which would cause the worse case for reliability and safety considerations.

Response times for railway and transit application have historically been specified in the 100msec to 1second range. The response times for Microlok II, based on older products, allows for fast response to state changes while allowing filtering time for reliability reasons. In addition, it must be recognized that some processing may be delayed by other system tasks. In cases where such delays can impact system safety, such as delivery of outputs within 200msec or reading of inputs within 400msec, the maximum tolerable delay time is specified in the requirements.

Non-Vital I /O Board

The Non-Vital I/O board is designed to receive non-vital inputs (controls) and generate non-vital outputs (indications). The version of the NV.IN32.OUT32 board connects each of its 32 inputs and outputs to a 96-pin connector mounted on the rear of the board. The board employs polyswitches to protect the output circuitry. A polyswitch functions like an auto circuit breaker. When the over current trip point (about 0.75 amp) is exceeded, the device switches to high impedance. The polyswitch returns to low impedance when the overload or short circuit condition is removed. Inputs on the boards are activated from a positive voltage relative to battery ground over a range of 6 to 30V DC. The non-vital I/O boards use latch ICs to buffer inputs and field effect transistors to drive outputs.

- The minimum ON threshold for a Non-Vital Input will be 4.5V DC for nominal 24V DC systems.
- The maximum OFF threshold for a Non-Vital Input will be 2V DC for nominal 24V DC systems.

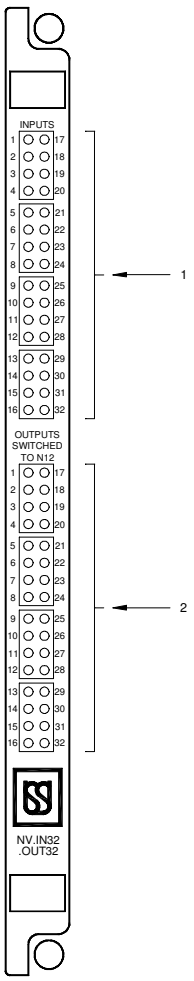

Figure – 4

Fig. 4 Ref	Label	Device	Purpose
1	**INPUTS 1-32**	Green LEDs	Monitors states of non-vital inputs 1-32. When LED is lit, respective input is on.
2	**OUTPUTS (SWITCHED TO N12) 1-32**	Yellow LEDs	Monitors states of non-vital outputs 1-32. When LED is lit, respective output is on.

Vital Output Board

Outputs are controlled by "high side" software-controlled switches. Loads should be connected from outputs to battery negative. The high side switch is used to connect battery (+) to the output. Each output is protected with a polyswitch, which acts like an auto circuit breaker. When the over current trip point is reached (approximately 0.75A), the polyswitch switches to a high impedance state. The switch resets to its low impedance state when the additional load or short is removed. A short to battery (-) will trip the

polyswitch and cause the VCOR relay to drop, but will not cause any damage. A short to battery (+) will not cause any damage, but since this condition is equivalent to a false output, the Microlok II CPU will cause the VCOR relay to drop.

- Each Vital Output PCB is having 16 outputs.
- Each output is assigned to the final relay which is driving the outdoor signalling gears such as HR, DR in case of signal & WNR, WRR in case of points.
- Since the output boards are driving outdoor gears, they are continuously monitored by the CPU and any abnormal voltage present in the output will lead to system reset / shutdown to ensure safety

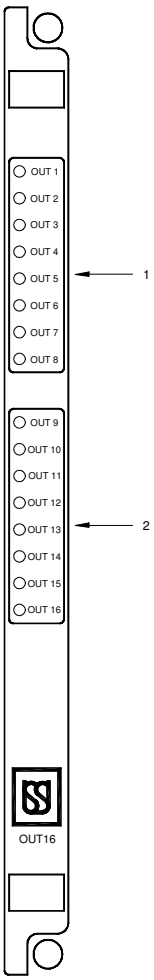

Figure – 5

Fig. 5 Ref	Label	Device	Purpose
1	**OUT1 -OUT8**	Yellow LEDs	Monitor state of vital outputs 1 through 8. When lit, indicates respective output is turned on.
2	**OUT9 -OUT16**	Yellow LEDs	Monitor state of vital outputs 9 through 16. When lit, indicates respective output is turned on.

Vital Outputs

The Vital Outputs are designed primarily to interface with vital relays. In typical railway and transit applications, most Vital relays are specified to use nominal 24V DC supply voltage.

- The minimum voltage for a Vital Output in the ON state will be 95% of I/O supply battery for 24V DC outputs.
- The maximum voltage for a Vital Output in the OFF state will be such that a Vital relay will not remain picked at the current produced. This voltage is 1.5V DC for a 24V DC output.
- The output will be capable of driving a minimum output load of 100Ω for the 24V DC outputs.

Control of outputs

Each output is controlled by the processor and monitored by a circuit providing feedback to the processor to ensure that the output is indeed what was requested by processor. Also, to check the integrity of the feedback loop, the outputs are cycled on a periodic basis. If an output is currently turned on, the processor will turn it off for an instant and verify the correct response from the monitor. Failure of these checks would result in a system shutdown and reset. See the figure-1.

Vital Input Board

There are no power connections required through the upper connector. When wiring a vital input PCB to a relay contact circuit contained in the same house of the Microlok II card file, the signal battery may be used as the energy source to activate the inputs. Terminals designated (-) may be connected to battery N24 and B24 switched over relay contacts. When wiring a vital input PCB to a relay contact circuit outside the Microlok II house, use the isolated source that is part of the power supply. This is consistent with the practice of confining signal battery to the case in which the Microlok II unit is housed.

- Each Vital Input PCB is having 16 Inputs.
- Each input is assigned to the detection of outdoor gear status such as ECRs in case of signal, WKR incase of points & TPR in case of Track.

- Since the vital inputs are dealing with the detection of outdoor gears they normally configured with double cutting arrangement.

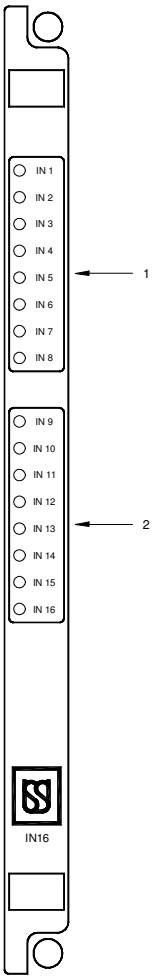

Figure – 6

Fig. 6 Ref	Label	Device	Purpose
1	**IN1 -IN8**	green LEDs	Monitor state of vital inputs 1 through 8. When lit, indicates respective input is turned on.
2	**IN9 -IN16**	green LEDs	Monitor state of vital inputs 9 through 16. When lit, indicates respective input is turned on.

Vital Inputs

Vital inputs, which are in most cases, derived from the battery supply must have the same range of inputs as the supply battery. To ensure reliable operation, the Minimum ON thresholds (the levels above which an input must read ON) were chosen to match the low ends of the battery ranges. The

only criteria for selecting the Maximum OFF thresholds (the levels below which an input must read OFF) are that they must be below the Minimum ON threshold, yet high enough above 0V to reject induced noise. The system will have the ability to access Vital Inputs even when the system is running with the Vital Outputs in an un-powered state. Since the most restrictive state for the inputs has already been defined as the de-energized state, failed inputs can safely be set to this state. This allows the system to react to the failed input without causing a Critical Error. This may cause the system to run in a downgraded state due to the OFF input state, but will cause no safety-related failures. The failed input status is available to the Application Logic such that the Application Developer may take other action as required by a particular system in the case of a failed input.

- The minimum ON threshold for inputs will be 19.6V DC for 24V DC inputs.
- The maximum OFF threshold for inputs will be 9.0V DC for 24V DC inputs.

Control of inputs

A principle similar to that used for the output circuitry is employed in the input interface circuitry. De-energizing of any input results in a more restrictive condition. All individual input interface circuits on a given board are forced to the more restrictive state through the closed loop vital input monitors. The inputs are then read and verified that they can, in fact, be forced to the more restrictive state. This is ensure that no interface circuit malfunction have occurred that could place an input in a less restrictive state. See the figure-1.

4.1.7. VITAL CUT-OFF RELAY

The vital cut-off relay (VCOR) contacts are used to control the power to all card file vital outputs. The VCOR is controlled by the CPU board. The CPU board performs continuous diagnostics, to include monitoring of all vital output and input channels at the point of interface with external circuits. This CPU responds to failure of a safety-critical diagnostic by commanding the CPS on the power supply board to remove the DC supply to the VCOR coil, thereby opening the contacts that provide battery power to the vital output boards. This fail-safe function defaults the interlocking equipment associated with the Microlok II system to the most restrictive state. PN-150B vital biased relay is used for the VCOR. This relay consisting of low voltage silver-to-silver fronts and silver-to-silver backs contacts.

4.1.8. ADDRESS SELECT PCB

The address select jumpers are used for board addressing. The jumper settings are automatically determined by the compiler after the successful

compilation of application program. This information is clearly defined and available to the user in the listing file (.mll), which is one product of compiling an application text file (.ml2). If this file is unavailable, the user can determine the jumper settings by following the instructions below. By far the best way to determine the jumper settings, however, is to use the list file. The jumper settings for each board are determined by the order in which the boards are defined in the application. The jumper settings do not depend on the order of the boards that happen to appear in the card file. If the application program and list file are both unavailable, then the order can also be found by looking at the configuration menu in the Microlok II Maintenance Tool.

- Each address select PCB consists of 6 Nos. of jumpers.
- Each slot will have its own jumper setting and each one is different from others.
- The address select PCB ensures the type of board used in the slot as defined in the application logic.
- 48 pin address select PCB is used for vital boards & 96-pin address select PCB is used for non-vital boards

4.1.9. KEYING PLUG

Each of the Microlok II card file slots includes a 12-way female keying guide next to the 96-pin connector. The guide is used to ensure installation of the proper circuit board in each card file slot after the complete card file board configuration has been determined. Each board is equipped with a corresponding 12-way male keying guide; individual keying tabs are removed at the factory in a specific pattern for the board part number. Prior to installing a board, insert keying plugs into the corresponding card file motherboard keying guide. If it becomes necessary to change the type of board installed in a given slot, the previously installed keying plugs can be removed using a knife or a pair of needle nose pliers.

5.1. SERIAL I / O

- The system will support a minimum of three kind of active ports for Application Interface processing that is RS-232, RS-423 and RS485
- All ports will provide, at minimum, Transmit (TXD) and Receive (RXD) data signals and Request To Send (RTS) and Data Carrier Detect (DCD) control signals. At least one port will provide a control input for Clear To Send (CTS)
- All control lines for all ports will be accessible such that each port can be modified to support different electrical properties without modification to the base PCB on which the port resides.

- The system will support the functions of both the master and slave of the Microlok Vital protocol.
- The system will support the functions of both the master and slave of the Genisys Non-Vital protocol.
- The Microlok and Genisys, master and slave protocols will be supported on all ports.
- The system will allow protocols of the same type to be active on more than one port.
- Only one link will be permitted to be active on a port at a given time. A Critical Error results if more than one link is assigned to the same port.

5.1.1. MICROLOK PROTOCOL

- The Microlok protocol supports from 1 to 32 Serial Stations per link.
- The Microlok protocol will be capable of handling addresses between 1 and 127.
- The Microlok protocol supports Serial Stations having from 0 to 128 input Boolean Bits and from 0 to 128 output Boolean Bits in the Application Logic. There must be at least one input or one output Boolean Bit defined for each Serial Station.
- The Stale Data Time-Out (SDTO) for the Microlok protocol will have an allowable range of 0.100 to 25.000 seconds in 100 millisecond increments. This time-out will be reset each time a valid message is received. This information is included in the Application Configuration.
- At the expiration of the SDTO, all input bits for the Serial Station will be set to 0 and the station's System Status Variable will be cleared.
- The allowable range for the Polling Interval Timer will be 0 to 2.000 seconds in 10 millisecond increments. This Non-Vital information is included in the Application Configuration.
- The allowable range for the No-Response Timer will be 30 to 5000 milliseconds in 10 millisecond increments. This Non-Vital information is included in the Application Configuration.
- A less restrictive input (1 state) will not be asserted to the Application Logic until it has been received in two consecutive messages.
- A more restrictive input (0 state) will be asserted to the Application Logic after one message has been received.
- Outputs that are more restrictive will be latched and transmitted until acknowledged by the receiver.

- When communications have not been established between the master and a Serial Station, any output messages sent between the master and that Serial Station contains all 0 values for the Application Variables.

5.1.2. GENISYS PROTOCOL

- The Genisys protocol supports from 1 to 32 Serial Stations per link. This function will be Non-Vital.
- The Genisys protocol supports addresses between 1 and 255. This function will be Non-Vital.
- The Genisys protocol supports Serial Stations having from 0 to 512 input Boolean Bits and 0 to 512 output Boolean Bits in the Application Logic. There must be at least one input or one output Boolean Bit defined for each Serial Station. This function will be Non-Vital.
- The Stale Data Time-Out (SDTO) for the Genisys link will have an allowable range of 1 to 600 seconds in 1 second increments. This time-out will be reset each time a valid message is received. This Non-Vital information will be included in the Application Configuration.
- At the expiration of the SDTO, the Serial Station's System Status Variable will be cleared. Input values will not be affected. This function will be Non-Vital.
- The allowable range for the Polling Interval Timer will be 0 to 2.000 seconds in 10 millisecond increments. This Non-Vital information will be included in the Application Configuration.
- The allowable range for the No-Response Timer will be 30 to 25000 milliseconds in 10 millisecond increments. This Non-Vital information will be included in the Application Configuration.

6.1. MICROLOK II SOFTWARE

The primary Microlok II software components are the executive software, which is actually the Microlok II operating system software, as well as the application specific user-written software. Also included in the Microlok II software architecture is self-checking diagnostics designed to support fail-safe operational requirements. The following briefly describes the major components of Microlok II software.

6.1.1. EXECUTIVE SOFTWARE

The US&S developed Executive software (Operating system) is standard for all Microlok II systems, and is responsible for the overall vital monitoring and control of the system. Executive software functionality includes vital input monitoring, decision making, and commands related to interlocking functions, monitoring vital input and output channels for intended on/off

states, processing user inputs received from laptop PC or the CPU board front panel, continuous internal and external diagnostics, recording and playback of routine event and error codes, management of serial data ports, and execution of the user developed application program software.

6.1.2. APPLICATION SOFTWARE

The Vital application program software contains the user-developed, application-specific logic for the particular Microlok II system configuration. The user develops the unique application program using software using the same US&S developed maintenance tools program used to input Executive software version upgrades. Additionally, site-specific configuration data is stored in the Cardfile-mounted EEPROM, and can be loaded using the CPU board front panel toggle switches and LED Displays. This data can be also loaded using the Maintenance tools program on a laptop PC via connection to the CPU board front panel serial port, the PC based method allows a grater range of configuration options.

7.1. MICROLOK II VITAL DIAGNOSTICS

The processor activities performing vital interlocking operations are monitored by internal diagnostics available within the Executive software that is continuously executed and controlled from the CPU board in order to detect and act upon various fault conditions. Microlok II uses diversity and self-checking concepts in which critical operations are performed in diverse ways using diverse software operations, and hardware is tested with self-checking operations. Permissive outputs are allowed only if the results of diverse logic operations correspond, and the self-checks reveal no failures. Any failure in any critical portion of the equipment results in the controlled system returning to the safe state. As discussed previously, vital software diagnostics managed by the CPU board play a key role in the fail safe operations of the Microlok II system in one particular significant respect, i.e. control of power to vital outputs through the CPS on the power supply board and the VCOR. Specifically , for the CPS to provide power to the VCOR and vital outputs, it must continuously receive a 250Hz signal from the CPU board. However, certain diagnostics tests must be passed before the processor will generate this frequency. If the CPU detects an error, or is simply unable to do anything, this 250Hz signal will no longer be generated. Once the 250Hz signal is no longer received by CPS, the DC power supply is no longer applied to the VCOR coil, thereby opening the contacts that provide power to the vital output boards. In short, this failsafe function causes the output systems controlled by Microlok II to go to most restrictive state.

8.1. SYSTEM OPERATING MODES

The Microlok II controller is a complex combination of hardware and software. when the system can not function in the Normal Operating Mode. Other system modes must be supported to allow access to those system functions that are still operational even though the entire system is not functional at that time.

Critical Errors in the Microlok II system may be caused by persistent or transient faults. After a Critical Error has occurred, the Microlok II will be reset and will perform complete system diagnostics.

The most common persistent Critical Errors are related to vital physical output processing. In order to attempt to provide some system functions in the presence of persistent Critical Errors, the unit will discontinue the vital physical output functions and, if there are no other Critical Errors encountered, continue to run in a downgraded mode. If Critical Errors continue to occur, all system application processing will be discontinued.

The Microlok II system will be capable of operating in seven different modes.

8.1.1. NORMAL MODE

In this mode, all outputs and application processing are active. All other system functions are available at user request. This will be the default mode for systems operations in the absence persistent of Critical Errors.

8.1.2. SELECTIVE SHUTDOWN MODE

This mode will be entered when persistent Critical Errors prohibit complete system operations. In this error mode, all of the Vital Physical Outputs will be disabled. In this mode, other application processing, such as logic processing, Serial Links, Vital Physical Inputs and Non-Vital I/O continues.

8.1.3. USER SELECTIVE SHUTDOWN MODE

In this mode all Vital Physical Outputs are disabled. This mode will be entered when identified as the operational mode by the Application Logic and the unit would otherwise operate in the Normal Mode as identified above. In this mode, other application processing, such as logic processing, Serial Links, Vital Physical Inputs and Non-Vital I/O continues.

8.1.4. COMPLETE SHUTDOWN MODE

In this mode, no system I/O or logic processing will be performed and all vital outputs will be in the most restrictive state. This mode will be entered when persistent Critical Errors prohibit system operations. When possible, Diagnostic Interfaces will function.

8.1.5. RESET MENU MODE

In this mode, the unit remains in the initialisation routines. No system I/O or logic processing will be performed and all vital outputs will be in the most restrictive state. This mode will be entered by a request from the System Maintainer through the Integral User Interface.

8.1.6. CONFIGURATION MODE

This mode places the unit in a special non-operational mode where the unit remains in the initialisation routines to allow for Application Configuration. No system I/O or logic processing will be performed and all vital outputs will be in the most restrictive state in this mode. This mode will be entered by request from the Application Developer.

8.1.7. BOOT MODE

This mode to allow the Generic System Software and/or the Application Image to be loaded into the system. No other system activities will take place while in this mode. This mode will be entered by request from the Application Developer.

9.1. LOGIC PROCESSING

The Boolean logic processing within Microlok II will also be of the same type of relay emulation as the Microlok and Genisys logic processors. In addition to the basic Boolean logic, the system will include table processing and block processing. The system supports Break-Before-Make execution of Boolean logic equations. All Boolean Variables used as operands in the logic equation will be Logic Triggers for the equation and a change in state of any of the operands causes the equation to be evaluated. A type of logic processing similar to a traditional computer program will also be supported. In this type of logic, the processing starts at the top of a block of statements and executes to the bottom only once each time it is triggered. This type of logic processing can be used for systems that require cyclic execution rather than relay emulation. The system supports logic blocks for numeric and Boolean processing that operate in a top down fashion when triggered. Variables used within the logic for a logic block will not automatically be Logic Triggers for the logic block. Instead, the definition for the logic blocks will include a list of Logic Triggers. Logic Blocks will only be triggered on 0->1 (zero-to-one) transitions of any of the Logic Triggers.

10.1. SYSTEM LOGS

The Microlok II system logs and reports information in three classifications. These are critical errors, warnings, and operational events. The Historical Data section of the Maintenance Tools main menu contains four tools that enable you to review the logged system information in several ways.

10.1.1. SYSTEM EVENT LOG

- The system event log records up to 5000 of the most recent critical errors, warnings, and events. When the log has reached its maximum limit, the newest errors will overwrite the oldest errors.
- A critical error will occur when the system has detected a fault which it can not continue normal operations. Hardware, diagnostic and application logic failures, among others, will cause a critical error.
- A warning will occur when the system detects some fault or condition that does not affect the system's operational mode.
- An event will be used to inform the user about certain system actions.

10.1.2. SYSTEM ERROR LOG

The system error log records up to 50 of the most recent critical system errors. When the log has reached its maximum limit, the newest errors will overwrite the oldest errors.

10.1.3. SYSTEM USER DATA LOG

The user data log records only those events that the user specifies. The user data log enables users to monitor a specifically chosen set of events. These events are assigned in the configuration section of the Tools program. The system then records in the log any state changes of the assigned events, along with the date and time that each state changes occurs. This log is capable of recording up to 90,000 of the most recent specified Boolean changes, or at least 64,000 Boolean and/or numeric changes.

10.1.4. SYSTEM MERGED EVENT LOG

The merged events log enables to view errors, warnings, and events as in the system event log. This log also provides graphic displays of parameters and events as specified in the user data log.

The merged events log, like the system events log described in above section, records the most recent system critical errors, warnings, and events. In addition, the log records all changes to parameters and events specified in the user data log. The merged event log uses both text-based and graphic data displays.

- All recent critical errors, warnings, and events appear in text mode
- All user-specified indications appear in graphic mode

11.1. SYSTEM SPECIFICATION

ENVIRONMENTAL

System Cardfile Vibration	Operating Temperature Range (All Units)	Humidity Limit
1.0grms, 0.2" displacement, 5-1000 Hz	-40°C to +70°C	95% non-condensing

SYSTEM CARDFILE HARDWARE CONFIGURATION

Cardfile Mounting	PCB Mounting	Total PCB Slots	Slot Bus Addressing	Upper PCB Interface Connectors	Remote Power Supply Connector
Std. 19" rack, Shelf or wall	Eurocard	19	Via jumpers in connector housings	96-pin male	8-way screw lock discrete wire conn.

CPU Printed Circuit Board

Microprocessor

Type	Clock Speed	Internal Bit Operations	External Bus Operations
Motorola MC68332	21 MHz	32 bits wide	16 or 8 bits wide

Executive and Application EPROMs

Capacity and Type	Total Code Space	Clock Speed	Programming Voltage
Four Intel/Micron TE28F800CV-B90 Flash Type	Up to 8 megabytes (4M x 16)	21 MHz 1 wait state	+5V and +12V

RAM (Vital Data Processing and Event/Error Logs)

Vital Data: Type	Vital Data: Capacity	Vital Data: Batt. Back-Up	Event/Error Data: Type	Event/Error Data: Capacity	Event/Error Data Batt. Back-Up
Fast Static RAM	2 banks of 64K x 16 (128K bytes)	None	Low Power Static Ram	4 banks of 512K x 16 (256K bytes)	>4hrs. @25°C

SYSTEM OPERATING POWER

Power Input to System Cardfile				
Voltage Range	Nominal Voltage	Min. Sys. Start-Up	Maximum Ripple	Current Draw
9.5 to 16.5V DC	12V DC	11.5V DC	0.5V P-P	Determined by installation (number of signal lamps, cab carrier frequency, etc.)

Cardfile Power Supply Printed Circuit Board Outputs*		
For System Cardfile PCB 5V Internal Circuits	For System Cardfile PCB 12V Internal Circuits	TO VCOR
+5V @ 3A	+12V @ 1A, -12V @ 1A	+12V into 400 ohm coil
*Not used to power vital or non-vital external devices or circuits		

Power Characteristics

Non-Vital I/O Printed Circuit Boards				
US&S Part No.	**Input and Output Voltage Range**	**Externally Available Inputs**	**Externally Available Outputs**	**Current Rating On Outputs**
N17061501	6.0 to 30.0V DC	32	32	Outputs 1-30: 0.25A (polyswitch-protected) Outputs 31, 32: 5.0A fuse*
*Suitable for lighting lamp upto 25W				

Vital Output Printed Circuit Boards				
US&S Part No.	**Voltage V_{BATT} Range**	**Load Resistance Range**	**Max. OFF Voltage**	**Min. ON Voltage**
N17060502	24V	100Ω - ∞	1.5V	V_{BATT} - 1V

Vital Input Printed Circuit Boards				
US&S Part No.	**Nom. Input Voltage**	**Min. Voltage to Ensure ON State**	**Voltage to Ensure OFF State**	**Max. Sustained Input Voltage**
N17061002	24V	16.0V	12.0V or less	62V

Mixed Vital I/O Printed Circuit Boards				
Output Specifications				
US&S Part No.	**Voltage V_{BATT} Range**	**Load Resistance Range**	**Max. OFF Voltage**	**Min. ON Voltage**
N17061602	24V	100Ω - ∞	1.5V	V_{BATT} - 1V
Input Specifications				
US&S Part No.	**Voltage V_{BATT} Range**	**Load Resistance Range**	**Max. OFF Voltage**	**Min. ON Voltage**
N17061602	24V	16.0V	12.0V or less	62V

VCOR

Type	Contacts	Coil Resist. (Ohms)	Pickup Amps	Pickup DC Volts	System Voltage
US&S PN-150B N322500-701	6FB	400	0.0132	5.3	10

NOTES