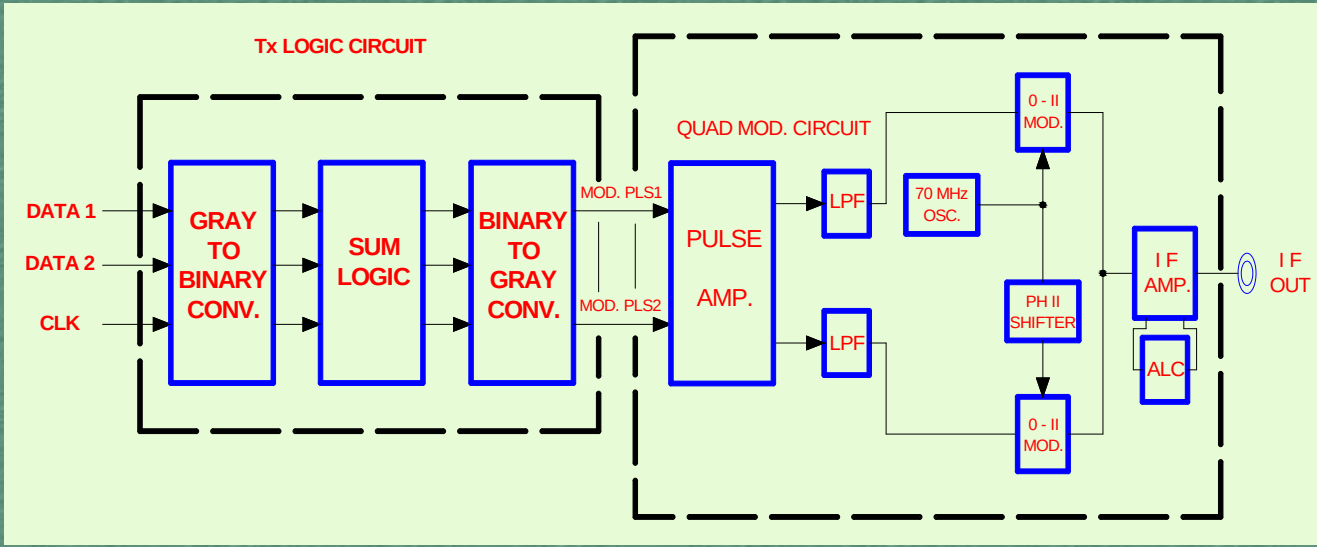
इरिसेट IRISET

TCT1

DIGITAL RADIO EQUIPMENT



Indian Railways Institute of
Signal Engineering and Telecommunications
SECUNDERABAD - 500 017

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INDIAN RAILWAYS INSTITUTE OF SIGNAL ENGINEERING & TELECOMMUNICATIONS, SECUNDERABAD - 500 017

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CHAPTER 1

INTRODUCTION TO DIGITAL MICROWAVE

1.0 Introduction

The modern communication is towards digital transmission. To digitise the analog signals, PCM techniques are used. The digital transmission medium can be microwave, optical fibre, co-axial cables etc. as shown in figure 1.1

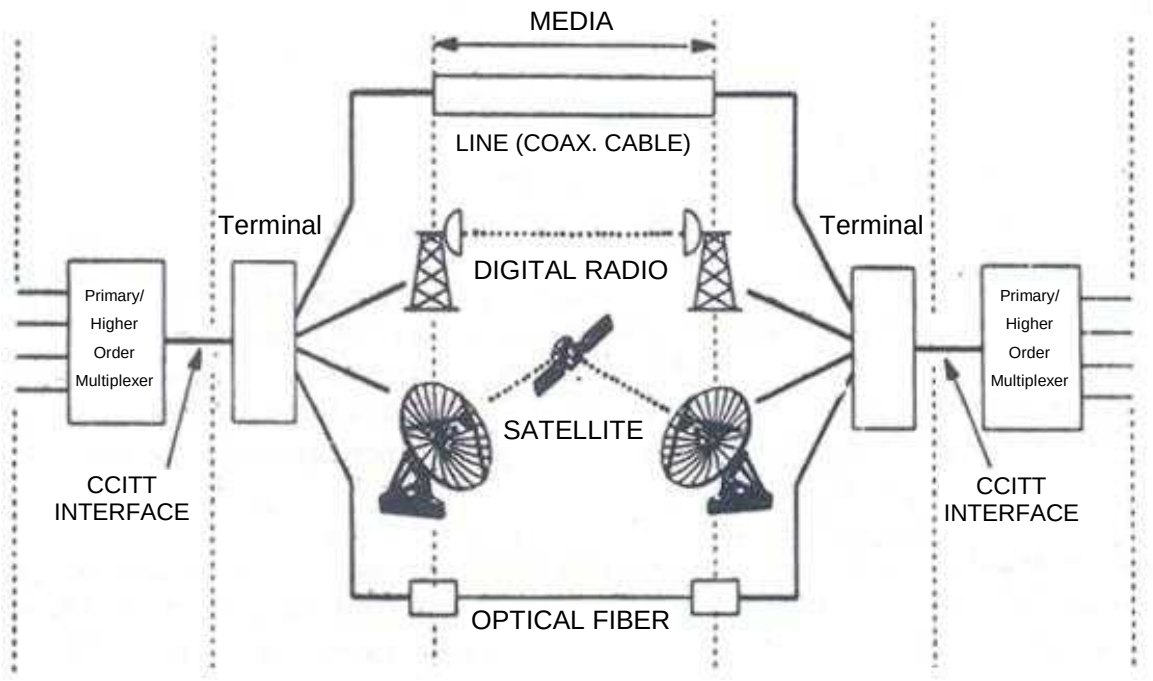

Figure 1.1 Digital Transmission System Block Diagram

The digital signals are compatible with digital logic circuits and computer systems and they are economically processed and re-routed as required. In telephony, digital transmission provides main benefits in digital switching and processing. Digital transmission also provides for error detecting and error correcting facilities by using suitable data encoding and decoding methods. This can also combine data, speech and other services into an Integrated Services Digital Network (ISDN).

1.1 Features of Digital Radio

Digital techniques are widely becoming popular for application in switching and multiplexing, thus necessitating the use of a new transmission means on radio for the medium and high capacities both for long haul applications and junctions working of inter exchanges in urban areas. Thus, an extremely rapid transition from analogue to digital radio relay systems is witnessed at present on Indian Railway also.

Radio links for direct transmission of PCM signals are of standard bit rates of 2,8,34 and 140 Mb/s. It provides a very attractive solution both technically and economically. Applicability to ISDN (Integrated Services Digital Networks) is also gaining momentum.

Some prominent features of digital radio are mentioned below: -

1. Circuit quality is independent of link length: The main advantage of digital radio is that it does not experience significant degradation in multi-hop system because repetition is by pulse regeneration instead of signal amplification.

2. Reduction in transmitter power, size, weight, power consumption and simpler antenna system: C/N (carrier to noise) ratio required for BER objective of 10^{-6} is about 18 dB in QPSK system, whereas C/N required for getting worst channel S/N of 70 dB in 120 channel FDM systems is about 50dB. This difference in C/N ratio results in saving in transmitter power, its size, weight and power consumption and simplifies antenna systems.

3. Better immunity to external interference: Digital systems are much less susceptible to interference than analog systems. For same speech quality, D/U (desired- to- undesired) ratio for digital radio can be set at a lower value than the FDM system. For example, PCM system can be operated satisfactorily at D/U ratio greater than 20 dB in co-channel. On the other hand, the FDM system requires D/U ratio greater than 50 dB to get signal-to-noise ratio (interference) of 70 dB.

4. Better circuit quality up to threshold: The quality of digital system is measured by BER instead of S/N ratio as in an analog microwave system. The performance of digital radio link remains almost constant up to a particular receive level called 'Digital Threshold'. The increase of external interference as well as the thermal noise experienced during the fading conditions has no effect on the transmission performance in digital radio until it become so large that bit errors appear. Thereafter, it falls very rapidly. The noise performance of analog FM radio in contrast deteriorates gradually but continuously with fading of received signal even before FM threshold is reached. Thus, it results in proportional deterioration of the transmission performance.

5. Total system economy: The digital radio system can offer unique features different from FDM-FM system. When the standpoint of the channel cost of voice grade circuit is evaluated, it is more profitable than the FDM-FM system because the PCM terminal equipment is less expensive and smaller than FDM ones. Digital radio permits direct interconnection with PCM MUX and also features easy maintenance.

6. More efficient for data transmission: Digital radio is more efficient for data transmission, but has less transmission capacity of voice grade channels. Analog (FDM-FM) system requires an RF channel spacing of about three times the top channel frequency, whereas 1.5 to two times the clock frequency will do in digital (TDM-PSK) system. It lends itself for transfer of various digital streams of data economically. But in telephone transmission, actual frequency spacing in MHz is more in the digital system.

7. Better speech security: It is easy to keep the privacy of the contents of a call in a digital system. In military environment, digital radio transmission is more attractive than analog because security precautions are much easier to make by on-line encryption.

8. Operational advantages: Since transmission system is digital, operations such as storage, retransmission etc. of information can be easily achieved. It is compatible with ISDN applications.

Objective:

1. In digital Radio transmission system circuit quality is _____ of link path.
   a) Independent b) dependent c) not defined d) None

2. *C/N required for a BER objective of 10^{-6} is about* _____ in QPSK system.
   a) 28 dB b) 08 dB c) 18 dB d) 38 dB

3. Small C/N ratio requirement in digital transmission systems results in saving in _____ power.
   a) Receiver b) Transmitter c) both (a) and (b) d) None

4. The quality of digital signals is measured by ----------instead of S/N ratio as in analog microwave systems.
   a) C/N ratio b) BER c) both C/N ratio and BER d) none

5. The performance of digital radio link remains almost constant up to a particular receive level called Digital threshold. (T/F)

6. The complexity of the digital radio systems lies in its modulation scheme. (T/F)

Subjective:

1. Give some of the prominent features of digital radio transmission systems.
2. How better circuit quality is achieved in digital radio transmission systems?

CHAPTER 2

DIGITAL MODULATION

2.0 Introduction

In Digital modulation, the digital information modifies the amplitude, the phase, or the frequency of the carrier in discrete steps. Figure 2.1 shows three different modulation waveforms for transmitting binary information over band pass channels. The waveform shown in Figure 2.1 (a) corresponds to discrete amplitude modulation or an amplitude shift-keying (ASK) scheme where the amplitude of the carrier is switched between two values (ON-OFF). Here for binary 1& 0, the resultant waveform consists of pulses and no pulses respectively. The waveform shown in 2.1 (b) is generated by switching the frequency of the carrier between two values corresponding to the binary information transmitted. In this method, where one carrier frequency is used to represent binary 1 and other carrier frequency is used to represent 0 (carrier frequency is changed), is called frequency shift keying (FSK).

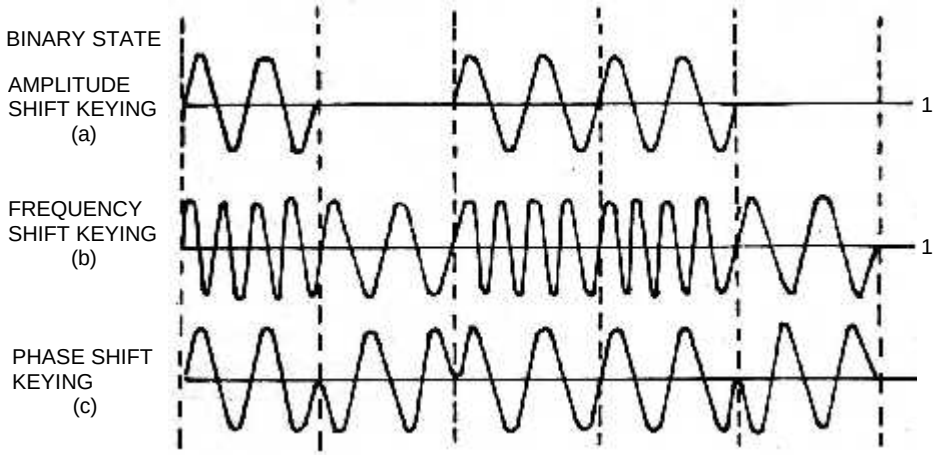

Figure 2.1 Digital Modulation Schemes: ASK, FSK & PSK

The waveform of the third method of digital modulation is shown in 2.1(c). In this type of modulation, the carrier phase is shifted between two values to represent binary 0 and 1 and hence, this method is called phase shift keying (PSK). It should be noted that both in FSK and PSK methods, the amplitude of the carrier remains constant.

2.1 BPSK Digital modulation and demodulation schemes

I-Q Definition: The sinusoidal microwave carrier can be defined in terms of its magnitude, frequency and phase relative to an arbitrary reference. In most digital radio system the frequency of the carrier is fixed so we need to consider only the phase and magnitude (or amplitude). The phase and magnitude can be represented in polar or vector co-ordinates as a discrete point in the so-called I-Q plane. I stand for in Phase (i.e. phase reference) and Q for quadrature (i.e. 90 degrees out of phase). We can then also represent this point by vectorial addition of a certain magnitude of in-phase carrier with a certain magnitude of quadrature carrier. This is the principle of I-Q modulation as shown in figure 2.2. By forcing the carrier to one of several predetermined positions in the I-Q plane, we can transmit encoded information of each position or state representing a certain bit pattern, which can be decoded at the receiver.

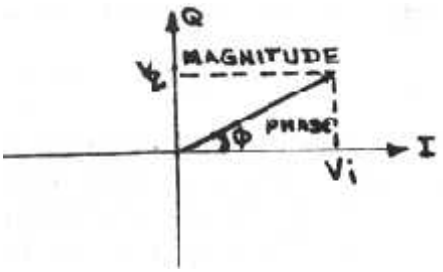

Figure 2.2 Principle of I-Q Modulation

2.2 BPSK timing and state diagram

Please refer fig.2.3. One of the simplest modulation schemes is Bi-Phase shift keying (BPSK or 2-PSK). Here the carrier magnitude is constant and to transmit either a '0' or a '1' the phase is "keyed" or switched between 0^0 and 180^0, provided the receiver has a stable phase reference to decide whether a '0' or a '1' was received and regenerate the data stream. Notice that in this simple scheme only one bit of information is associated with each state so that the carrier phase may have to be keyed at the bit rate.

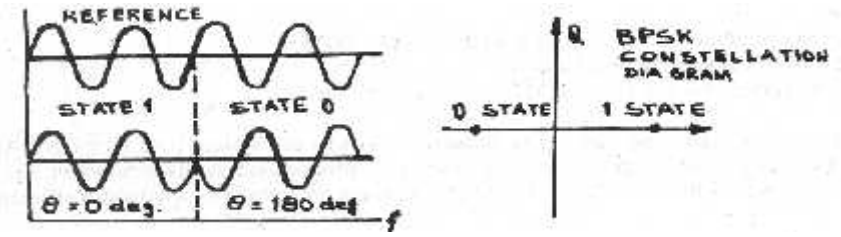

Figure 2.3 BPSK timing and state diagram

2.3 QPSK modulation

Quadrature phase shift keying (QPSK or 4-PSK) uses constant carrier magnitude but four different phase values (i.e. 45^0, 135^0, 225^0 and 315^0). Please refer fig.2.4. The modulation phase states can be generated by adding together appropriate amplitudes of in phase and quadrature carrier (V_I and V_Q) or alternatively by phase shifting the microwave carrier directly using an electronically switched phase shifter such as wave guide stubs or delay lines. Because we now have four discrete states we can transmit more information per state in this case, as you can see, 2-bits of binary data or a symbol are encoded on each of the states. As serial data is taken 2 bits at a time to form the symbol, the symbol rate is half the bit-rate. Intuitively you can probably deduce correctly that QPSK would only require half the bandwidth of BPSK for the same bit rate as its symbol-rate is half.

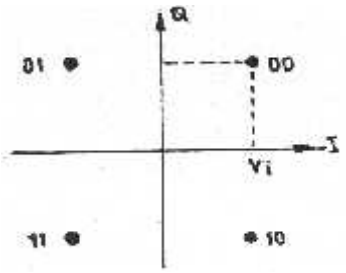

Figure 2.4 QPSK Modulation Constellation

2.5 QPSK Modulator

Figure 2.5 shows the simplified block diagram of a QPSK (4-PSK) modulator. In QPSK the incoming bit-stream is divided into two parallel streams so that one bit is fed simultaneously to both I and Q balanced modulators to construct the 2 bit symbols. The carrier output from the modulator is switched under the control of the digital bit stream. By adding together the I and Q outputs the phase state diagram is generated. Filtering has been implemented with LPF filters before the balanced modulators, thereby shaping the spectrum of the incoming pulses. Practically, some band limiting is required before modulators; otherwise the very wide spectrum will fold around dc in an I.F. modulator and overlay the desired central lobe of the spectrum.

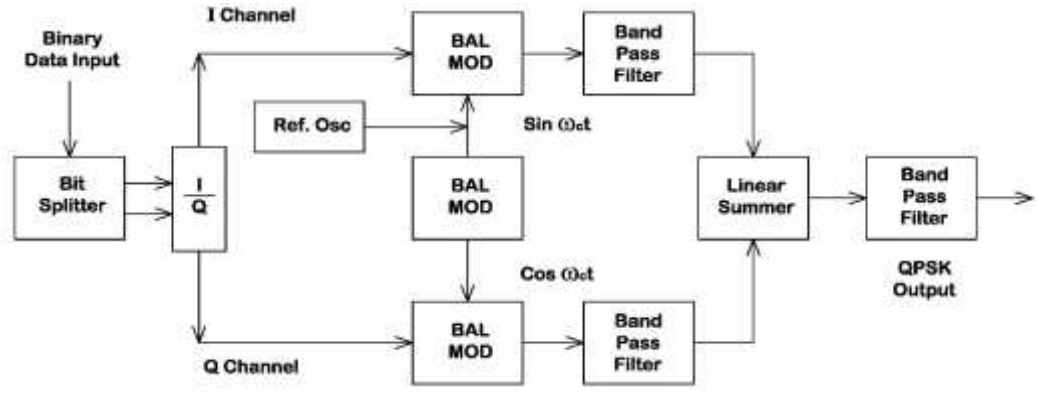

Figure 2.5 Block diagram of QPSK Modulator

2.6 QPSK Demodulator

The QPSK demodulator works in a similar way to the modulator, extracting the I and Q streams using in phase and quadrature carrier signals. The demodulator is more complicated because it must recover a carrier signal and timing signal from the incoming I.F. Please refer fig.2.6. Carrier recovery is usually implemented using a non-linear process such as frequency multiplication followed by a phase locked loop. Symbol timing is recovered from the demodulated data stream by a tuned circuit or phase-locked loop, filtering out the clock component in the data stream. The scrambler in the transmitter ensures there is always a clock component independent of the data fed to the radio input. The demodulator I and Q streams are filtered to remove unwanted I.F. signals and then passed into threshold detectors where a signal is sampled by the symbol timing clock to determine whether a '1' or '0' is present and regenerates the data stream.

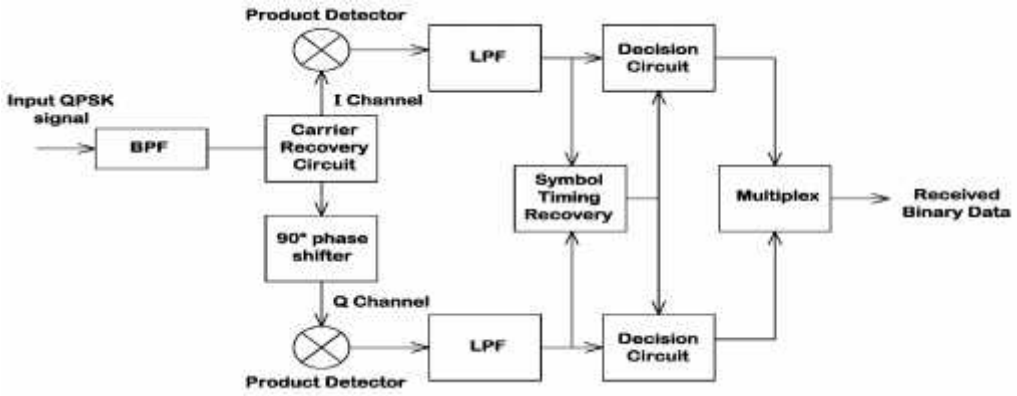

Figure 2.6 QPSK Demodulator

Objective:

1. In FSK modulation technique ---------- frequency components are transmitted to represent the binary signals.
   a) One b) Two c) Three d) Four
2. Synchronous detection is prevalent in case of ----------systems.
   a) ASK b) FSK c) PSK d) both ASK and FSK
3. The receiver complexity of digital radio transmission systems increases when ---------- modulation techniques are employed.
   a) PSK b) ASK c) FSK d) None
4. Non-synchronous detection is used in conjunction with ---------- and ---------- systems.
   a) ASK and FSK b) FSK and PSK c) ASK and PSK d) None
5. In PSK modulation technique the carrier phase is shifted between two values to represent binary 0 and 1. (T/F)
6. Carrier recovery in the demodulator is usually implemented using a non-linear process such as frequency multiplication followed by a PLL. (T/F)

Subjective:

1. Explain the principle of I-Q modulation.
2. Draw the block diagram of a QPSK modulator and explain its operation
3. Draw the block diagram of QPSK demodulator and explain its operation

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CHAPTER 3

7GHZ (34+2 Mb) NEC/BEL/ITI DIGITAL RADIO SYSTEM 770A

3.0 INTRODUCTION

The Radio equipment is a compact and fully solid state, Microwave Transmitter receiver, employing Microwave Integrated Circuits (MIC) for the RF circuit and Field Effect Transistors (FET) for the low-noise microwave amplifier.

The Digital Transmitter Receiver with Switchover Units, provide highly efficient transmission services in the 7GHz radio frequency band (7125 to 7725 MHz. CCIR Rec.385-3) which have a transmission capacity of 34 Mb/s (34 Mb/s x 1) digital signal along with 2 Mb/s way side digital signals.

3.1 Functional operation of a hot-standby terminal

The component modules arrangement of Radio Equipment along with WS/DSC Rack and NAR Rack is shown in figure 3.1.

The block and level diagram of terminal type transmitter receiver is shown in figure 3.2.

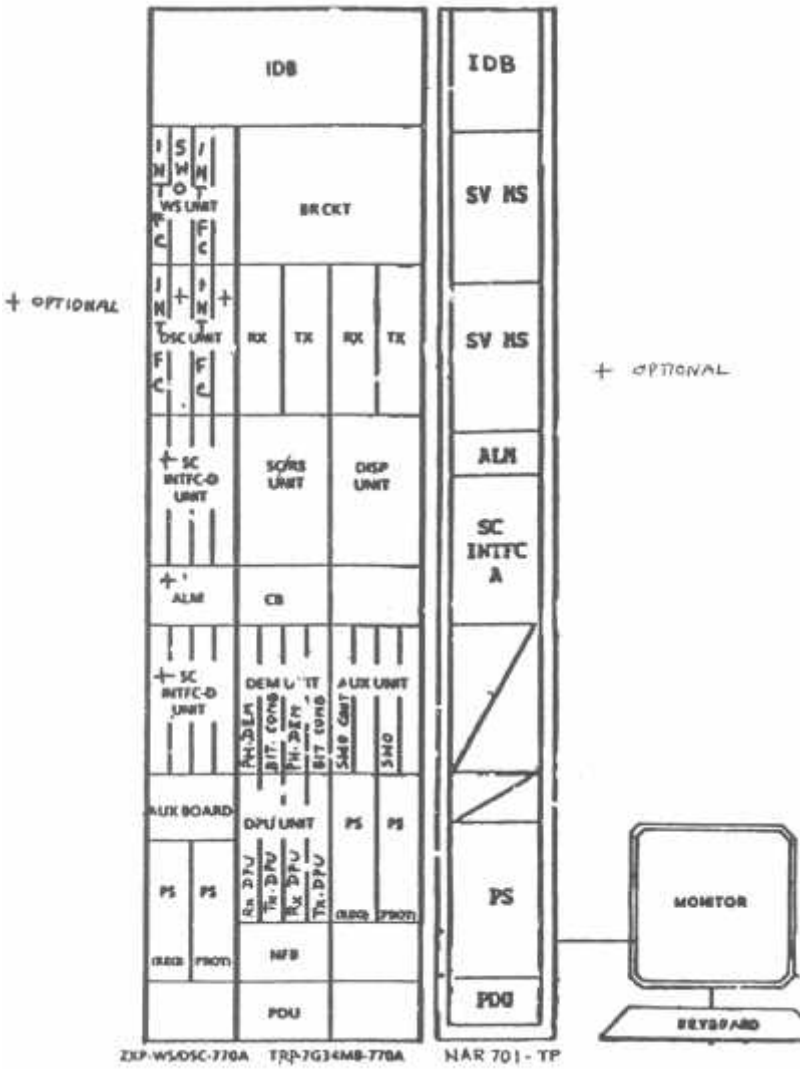
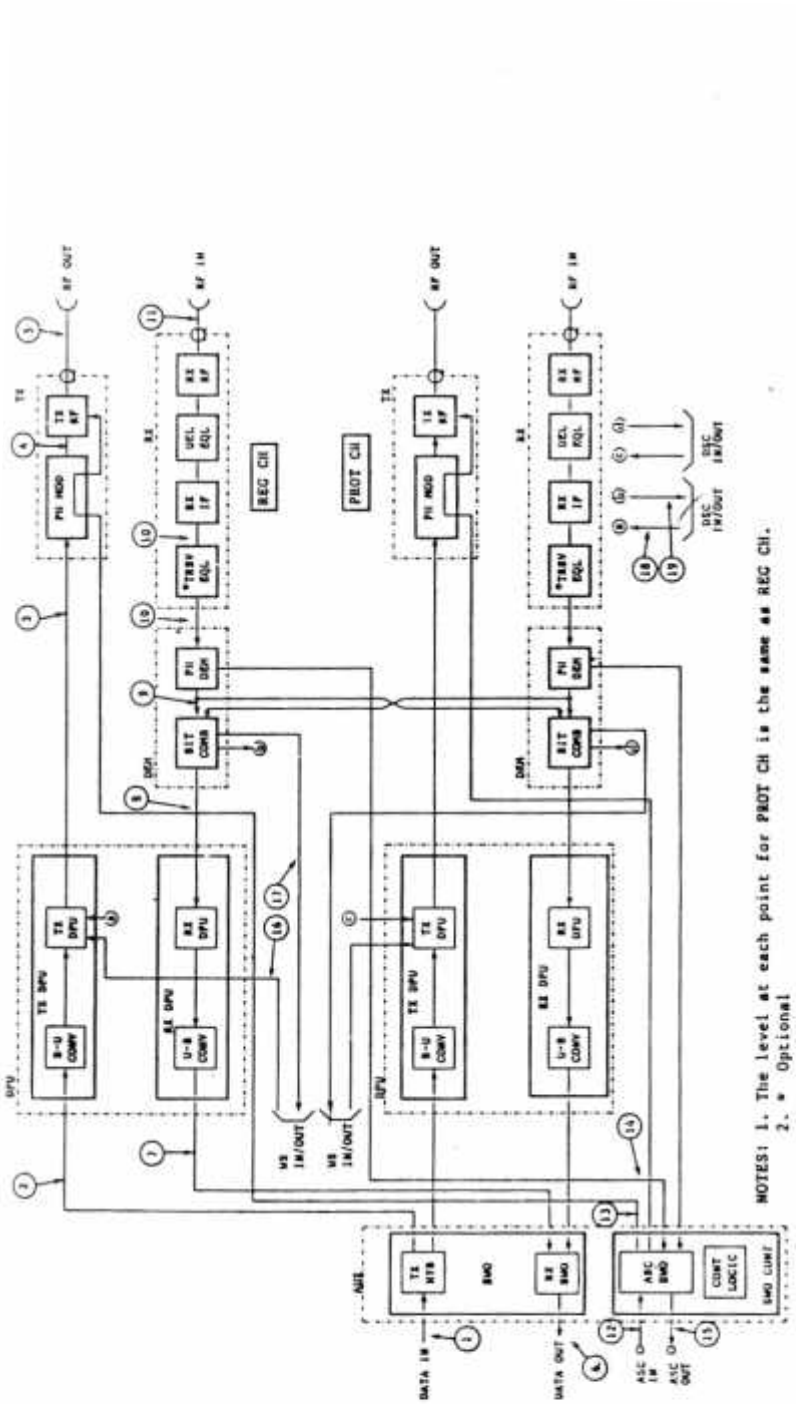


Figure 3.1 Front view of 7 GHZ (34+2 Mb) DIGITAL RADIO SYSTEMS



Point	Normal Level	Data Speed/Frequency	Impedance	Point	Normal Level	Data Speed/Frequency	Impedance
1	1.0 Vo-p ±0.1 V	34.368 Mbps	75 Ω, Unbalanced	11	-40 dBm	Assigned RX RF Frequency	50 Ω, Unbalanced
2	0.5 Vo-p ±0.05 V	34.368 Mbps	75 Ω, Unbalanced	12	-30 dBm	0.3 to 12 kHz	600 Ω, Balanced
3	0 to 2 V	19.332 Mbps	75 Ω, Unbalanced	13	-34.5 dBm	0.3 to 12 kHz	600 Ω, Balanced
4	-3 dBm	70 MHz	75 Ω, Unbalanced	14	-20 dBm	0.3 to 12 kHz	600 Ω, Balanced
5	+30 dBm	Assigned TX RF Frequency	50 Ω, Unbalanced	15	-20 dBm	1.3 to 12 kHz	600 Ω, Balanced
6	1.0 Vo-p ±0.1 V	34.368 Mbps	75 Ω, Unbalanced	16	TTL	2.4165 Mbps	-
7	1.0 Vo-p ±0.1 V	34.368 Mbps	75 Ω, Unbalanced	17	TTL	2.4165 Mbps	-
8	0 to 2 V	19.332 Mbps	75 Ω, Unbalanced	18	TTL	89.5 kbps	-
9	0 to 2 V	19.332 Mbps	75 Ω, Unbalanced	19	TTL	89.5 kbps	-
10	-3 dBm	70 MHz	75 Ω, Unbalanced	20	-	-	-

Figure 3.2 Block & Level Diagram of 7 GHz Digital Radio Equipment

3.1 Power Distribution arrangement:

No Fuse Breaker (NFB): The NFB consists of no fuse breaker and line filter. The line voltage from PDU is applied to Line Filter passed through NFB. Line filter eliminates noise components of line voltage. The output voltage of line filter is provided from terminal Z.71 of PDU to DC-DC CONV module and SC/MS UNIT.

Power Supply (PS): The PS comprises a DC-DC CONVERTOR module.

The DC-DC CONV produces a regulated +5V DC, +9V DC and -10V DC from an input power of -48V DC. The regulated +5V DC, +9V DC and -10V DC thus obtained, operate modules in the transmitter-Receiver. Each DC-DC CONV has a power turn control circuit for protecting each unit from excessive current caused by short-circuiting or from abnormal rise of the +5V, +9V and -10V output voltage. So, when an excessive current flows or an abnormal output voltage goes into modules, the corresponding power switch (circuit breaker type) of the DC-DC CONV trips to interrupt the input power. The functional diagram of power supply system is shown in figure 3.3

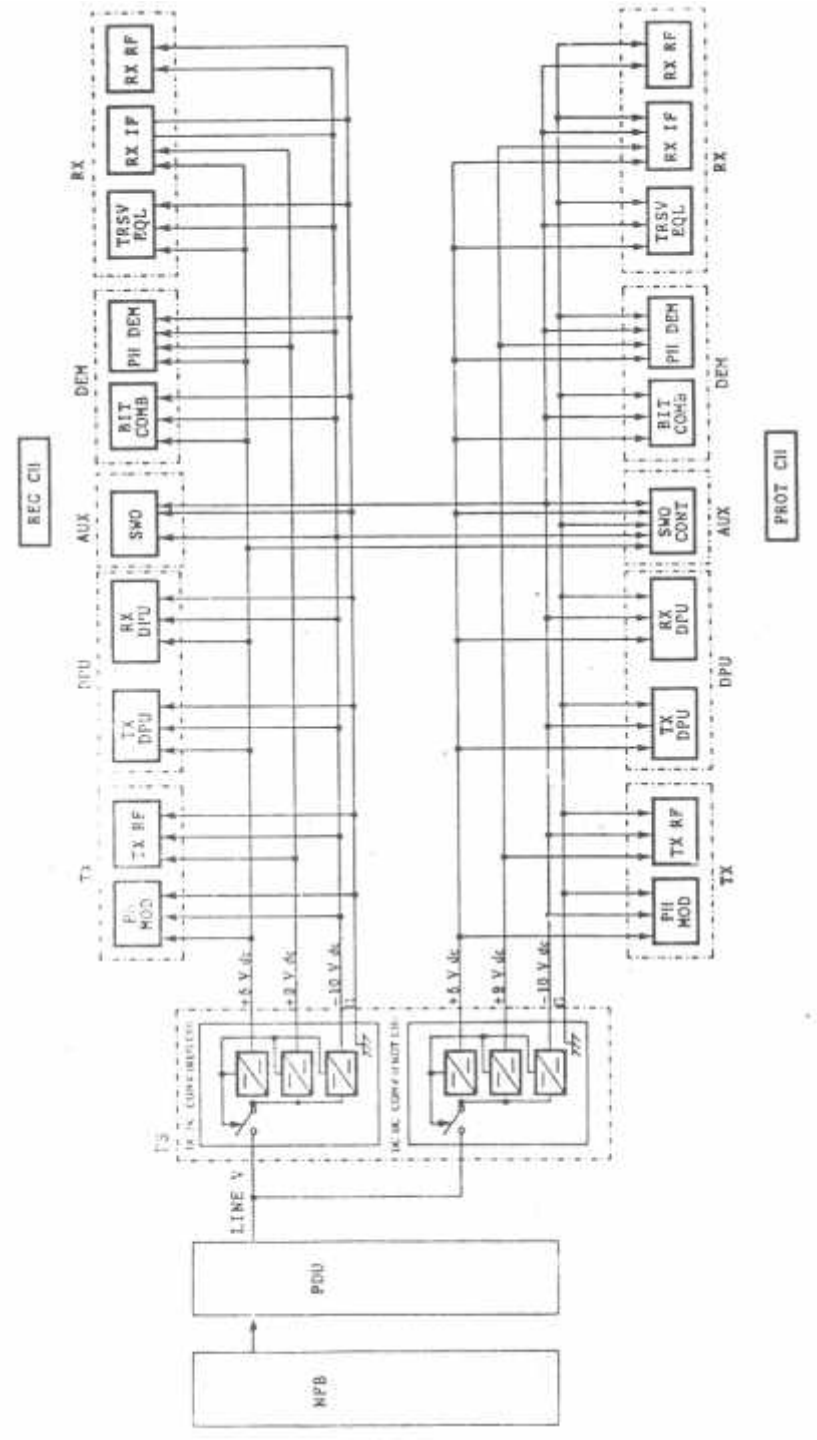


Figure 3.3 Power Supply Distribution to different modules in 7 GHz Digital Radio

3.2 Auxiliary Unit (AUX)

The AUX comprises the following two modules.

(1) Switchover (SWO)

(2) Switchover Control (SWO Cont)

The SWO consists of transmitter (TX) section and receiver (RX) section.

Switchover TX section: The HDB-3 signal (34.368 Mbps) is applied to attenuator (ATT) and its level is attenuated by approx. 3 dB. Then, the signal is delivered to the hybrid and divided into two routes respectively to be supplied to REG and PROT systems.

Switchover RX Section: The 34.368 Mbps HDB-3 input signal is applied to data switchover circuit, where one of REG and PROT is selected by the control signal. Whenever, the data switchover operates the SW OPR indicator lights. A manual signal has priority over a selection control signal from external. Whenever, the manual selection switch is in either REG or PROT position, the MANUAL indicator lights. The SWO CONT consists of ASC circuit, alarm and control circuits.

Switchover Control

a) **Alarm and Control Circuits**: The SWO CONT indicates an alarm condition and also outputs alarm and control signals to the external equipment. Alarm signals monitored in each respective module and control signals are gathered at the SWO CONT module for concentrated processing according to use.

b) **ASC (Analog Service Channel) Circuit**: The ASC signal is applied to the hybrid. Then, the signal is divided into two routes respectively to be supplied to PROT and REG systems of transmitter and applied to the attenuator. The received ASC signal is switched over by the manual switch, alarm or remote control signal.

3.3 TX DPU (B9967 A)

The TX DPU consists of Line equaliser, HDB-3 to unipolar converter, serial to parallel converter, Multiplexer, Scrambler. The functional block diagram is shown at figure 3.4.

Line Equalizer Circuit: The HDB-3 coded signal distorted by interconnecting cable is applied to the Fixed Equalization Circuit and pre-compensates that distortion. Then the signal is sent to the Equalization Circuit with automatic control circuit, which controls the frequency characteristics of the equalization and keeps the output level constant.

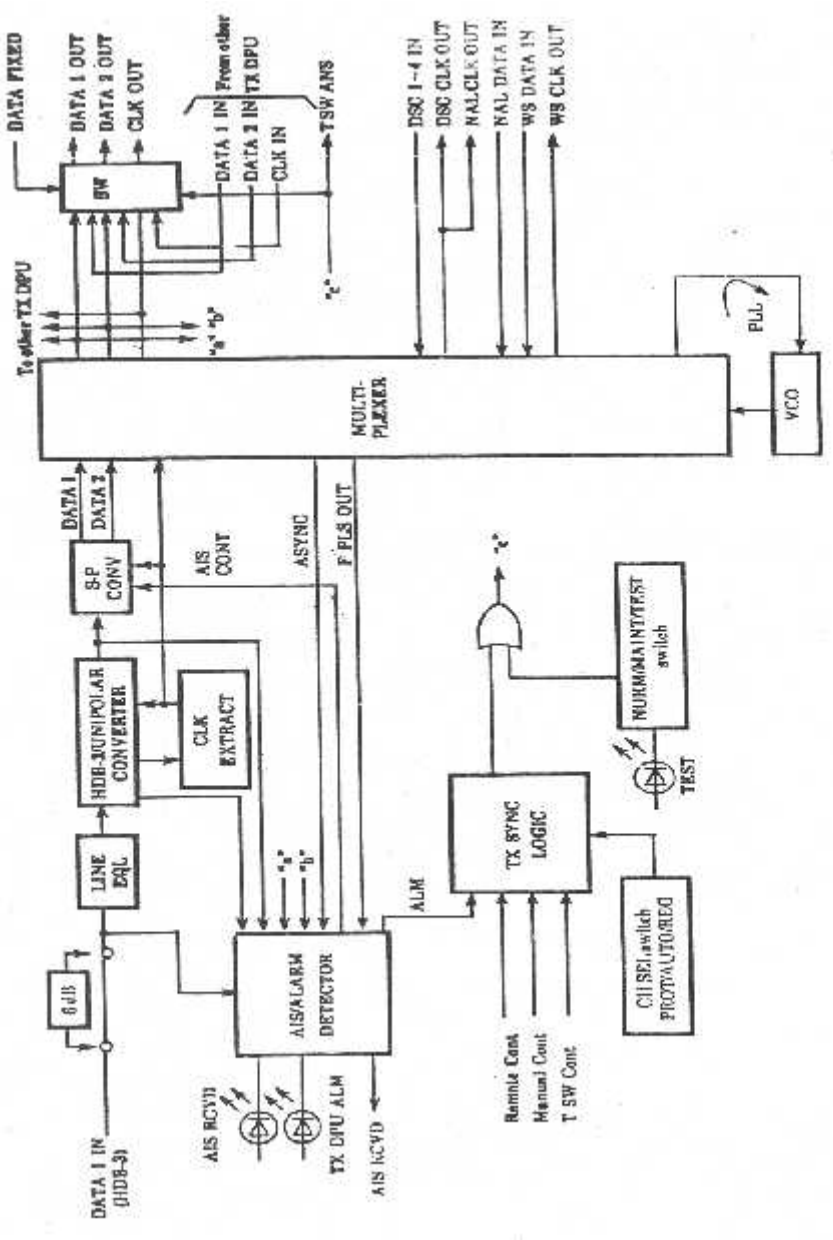


Figure 3.4 Block diagram of TX-DPU

Example of pulse waveforms

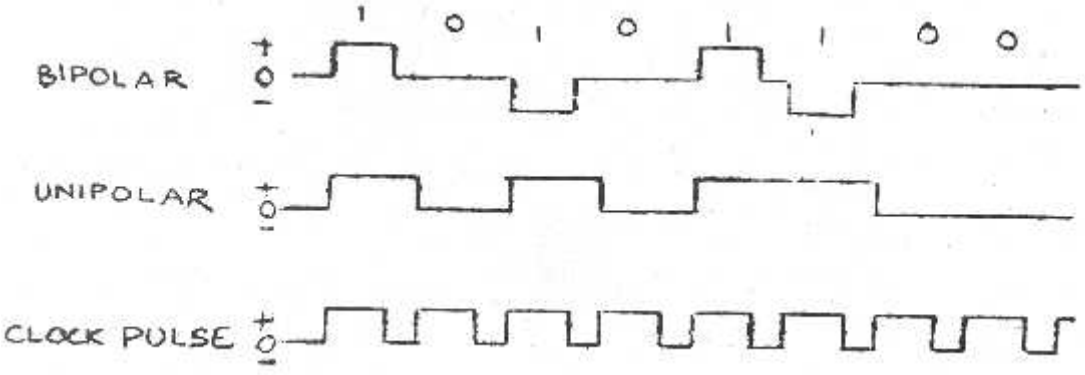


Figure 3.5 Unipolar & Bipolar Pulse Waveforms

Figure 3.6 shows a functional diagram of a HDB-3 Unipolar Converter. The input HDB-3 signal is separated into positive and negative RZ signal pulses.

Converting RZ to NRZ: The positive RZ (Return-to-Zero) signal or the negative RZ signal is converted into an NRZ (Non-return-to-zero) signal.

Removing violation pulse: The violation pulse is detected and removed from the positive NRZ signal and the negative NRZ signal.

Converting 2 to 1: The positive NRZ signal and the negative NRZ signal, which have no violation pulses, are converted to an NRZ signal of one line and then sent out.

A 34.368 MHz clock is extracted from the full-rectified signal of input bipolar stream and applied to the HDB-3 to unipolar converter.

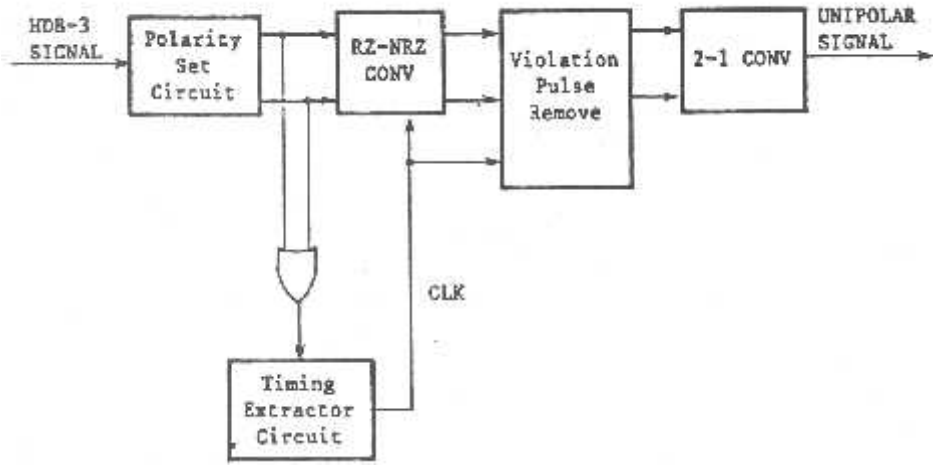


Figure 3.6 Functional diagram of a HDB-3 to unipolar Converter

Serial to Parallel Converter: The 34 Mb/s. unipolar signal is divided into two 17 Mb/s. unipolar signals in this serial to parallel converter. Figure 3.7 shows the functional block diagram of serial to parallel converter. It converts one to two data streams as shown in figure 3.8. A 34.368 Mbps signal is applied to two memories (M1 and M2) and read out from these memories by the 1/2 divided input clock and the signal from M1 memory is retimed at M3 and sent out together with the signal from M2 memory.

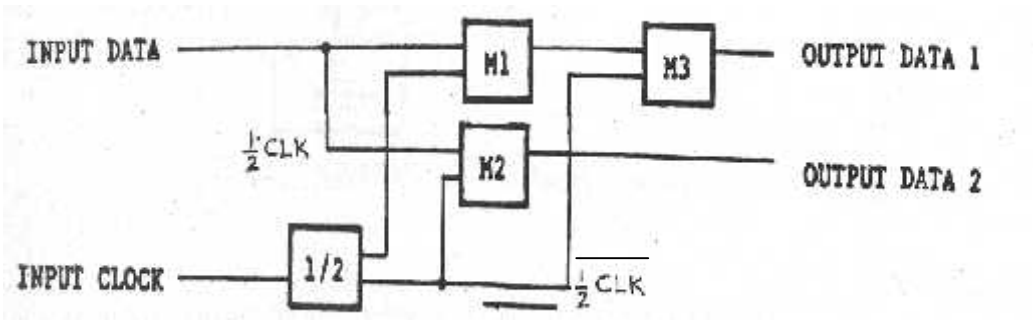


Figure 3.7 Serial to parallel converter

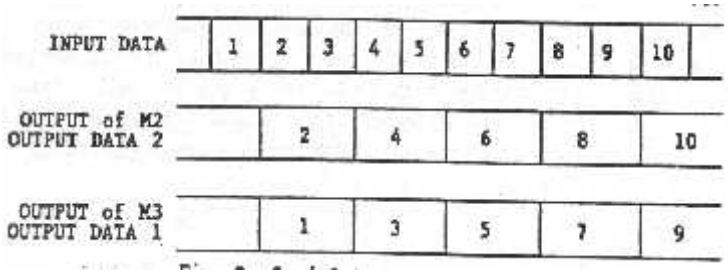


Figure 3.8 Splitting 34 Mbps data into odd & even stream

Multiplexer: The block diagram of Multiplexer is shown in figure 3.9. In this circuit, overhead bits are inserted into the two data streams. This Timing pulse generator (figure 3.10) section consists of a 432 Bits Random pattern generator, 1/2--frequency dividers and 1/6-frequency dividers, and produces the frame pattern signals inserted between time gaps of transmitted signals and the timing pulse needed in the time gap generator. The 432 Bits Random pattern generator produces scramble patterns and sub-frame pulses. The 1/2 frequency divider produces control signals for parity check, and drives the 1/6 frequency divider. The 1/6 - frequency divider outputs frame pattern signals (FS1 and FS2).

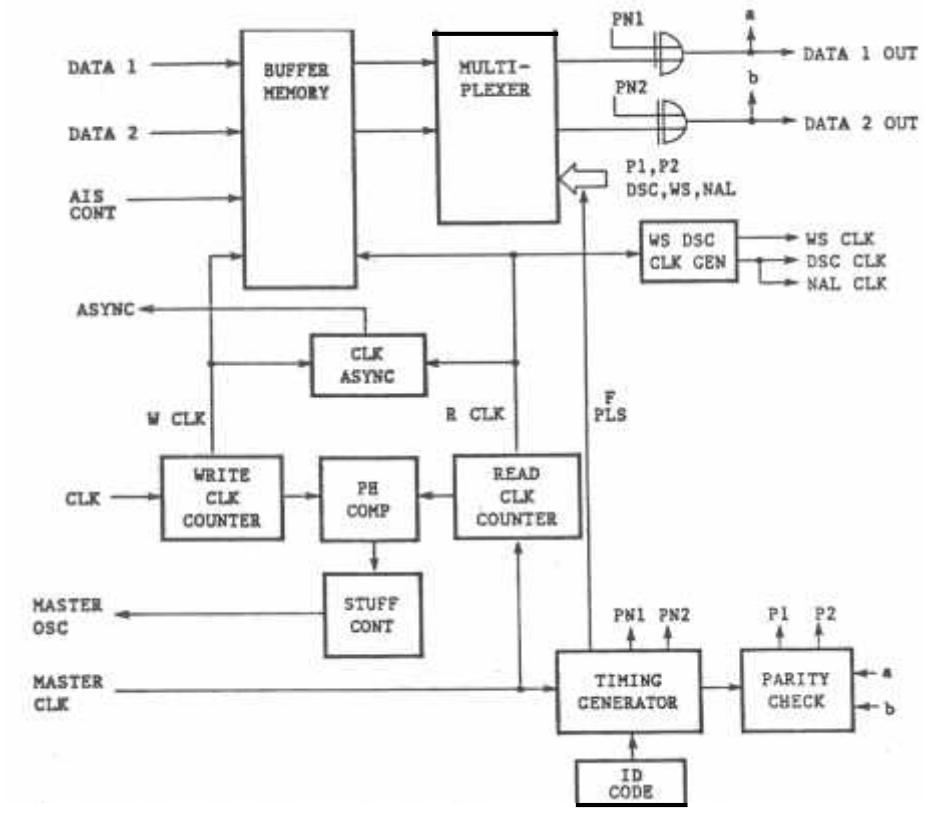


Figure 3.9 Block diagram of Multiplexing Main, WS & DSC Data

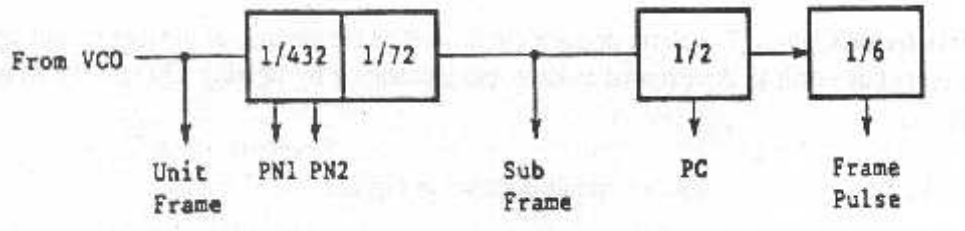


Figure 3.10 Timing signal generation for TX-DPU Process

Write/Read Clock Counters: The signal stream from the B-U CONV circuit that is written in the Elastic Memory is read out with a clock signal from VCO having the time gap at the ratio of 9 bits to 1 bit. The frequency of the signal stream read out is Fvco. The time gap of one bit is inserted for 8 bits signal. The signal stream having time gap is sent out to the selector where frame pattern, parity check and DSC signals are inserted at the location of time gap. When input signal from B-U CONV is not supplied *, the content of the Elastic Memory is controlled logic “0” and “1” by alarm signal from B-U CONV. And 1010 repeated pattern is transmitted to radio path.

Note: * for example, input HDB-3 signal lost or AIS signal received.

Stuff Control Circuit: This circuit monitors the phase difference between the Master clock and extracted clock signal from an input HDB-3 data stream, sends the stuff information to the Multiplexer and controls the stuff rate.

Buffer Memory: This memory consists of an 8-bit elastic memory and functions to let the write clock to write DATA in and the read clock to read DATA out. By this memory, the input signal transmitted by f_L (17.184 MHz) frequency is converted to Data lines transmitted by f_H (19.332 MHz) frequency.

Multiplexer: This circuit multiplexes the Digital Service Channel, Wayside signal, switchover control (NAL data), Frame Pulse and Parity Check Bit to the corresponding time slot in Data signal produced by the buffer memory.

Scrambler: Pseudo - random pattern scrambling is adopted to control the mark ratio and thereby obtain optimum frequency spectrum and stable phase demodulation operation regardless of variations in mark ratio of the incoming signal.

The Scrambler consists of Module-2 arithmetic circuit. The scramble pattern is a 432 bits random pattern produced at the Timing Pulse Generator. The scrambled signal stream is sent out to the 4 PH MOD.

Parity Counter: By using the pulses supplied from the timing pulse generator, this counter calculates Data in Module-2 at every other bit for the original Data signals simultaneously for 2 data streams and multiplexes the result to the parity bit.

ID Code Selection: A frame pattern signal is selected by switch on the front module, then generated in the timing generator and sent to the Multiplexer. The multiplexed frame pattern signals are used for channel identification at the receiving side. ID code is added to identify the corresponding receiver only and is added to D2 stream.

Alarm Detector Circuit: The alarm detector circuit detects the absence of input or output signal and informs this result to the external module and indicates it by lighting LED on the front of module. The block diagram of alarm detector circuit is shown in figure 3.11.

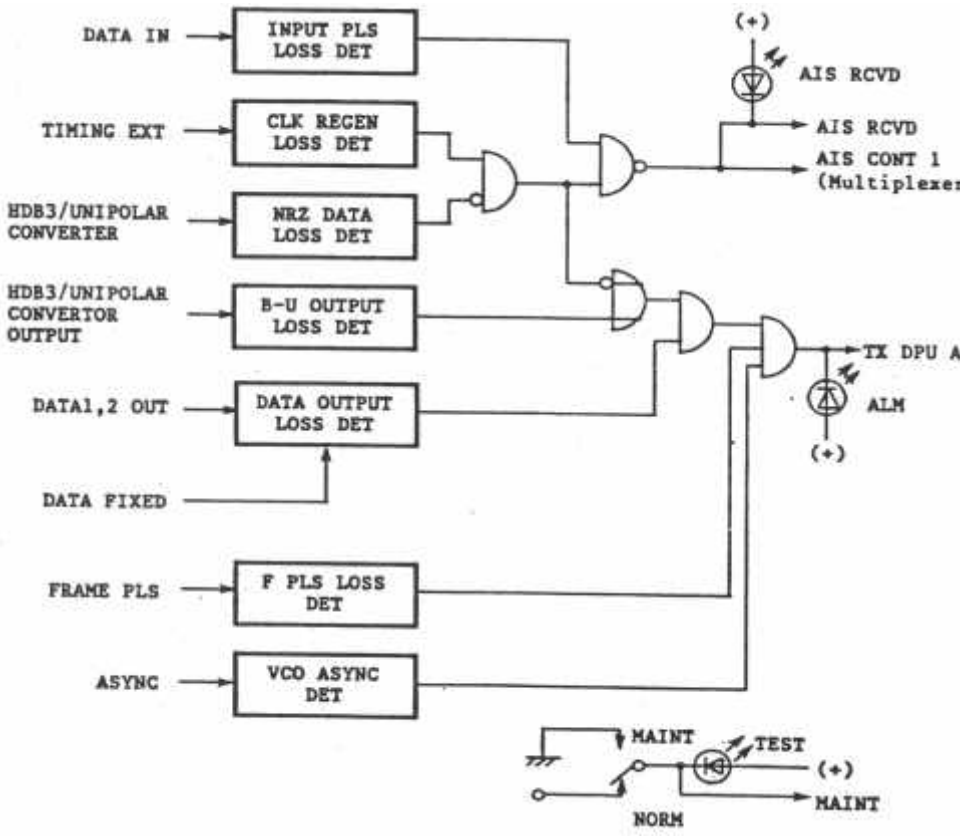


Figure3.11Block diagram of Alarm Detector

3.4 Transmitter (TX) (C0035-A): The TX consists of phase modulator (PH MOD) B9945A and Transmitter RF circuit (TX RF) C 0060A. The functional block diagram is shown at figure 3.12.

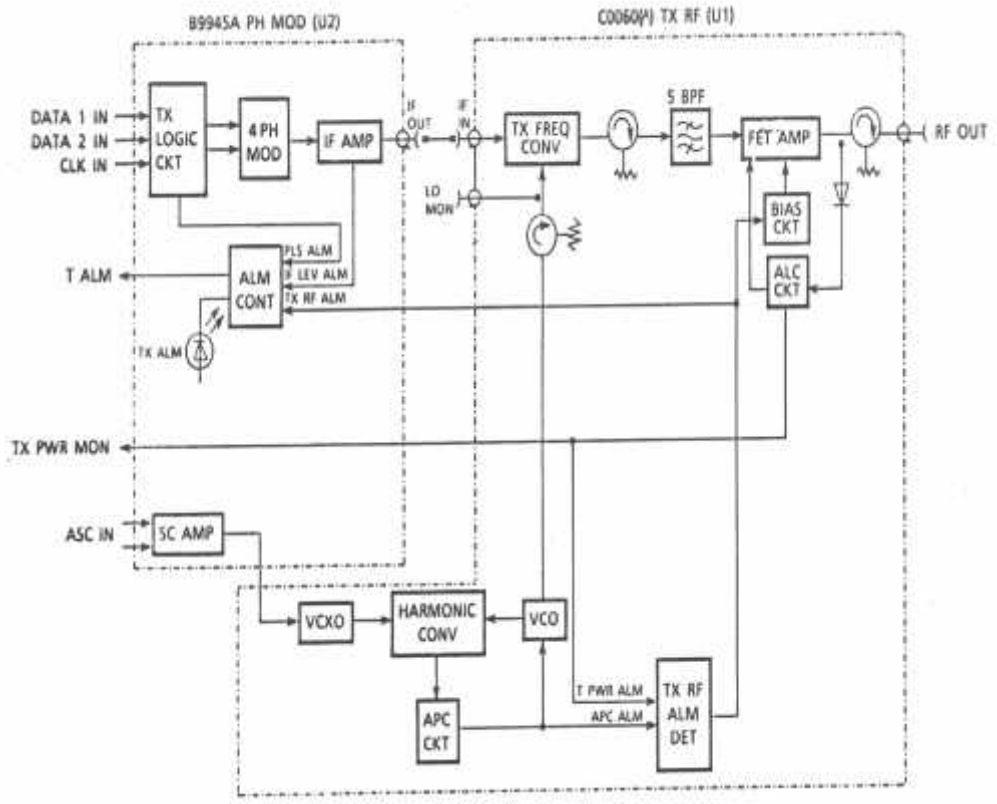


Figure 3.12 Block diagram of Transmitter

Phase Modulator (PH MOD) B9945A (Figure 3.13)

The PH MOD contains a TX LOGIC circuit, a QUAD MOD circuit and SC AMP circuit.

A 70 MHz IF carrier is generated at the 70 MHz oscillator and split into two carriers (LO1 and LO2) for each 0- π modulator. The phase difference between the two 70 MHz carriers has π /2 radians. In each 0- π modulator, the phase of the 70 MHz carrier is modulated to a 0- phase or π -phase by input pulse streams. The output of the two 0- π modulators is then combined for four -phase assignments onto a 70 MHz IF carrier. The 4-phase, phase modulated IF signal thus obtained is amplified by IF amplifier and sent to the TX RF module at an output level of -3 dBm. To obtain stable IF output level, the IF output level is regulated to -3 dBm by changing the impedance of PIN diode connected in series in the IF AMP with an ALC (Automatic level control) voltage from the ALC circuit. The PH MOD has an alarm detection circuit for monitoring output data streams of the TX LOGIC circuit, IF output signal level of the QUAD MOD circuit and alarm information from the TX RF module. Normally, a "1" (about 0V) appears but in an alarm condition, the TX ALM indicator lights red and a "0" (about -8V) appear.

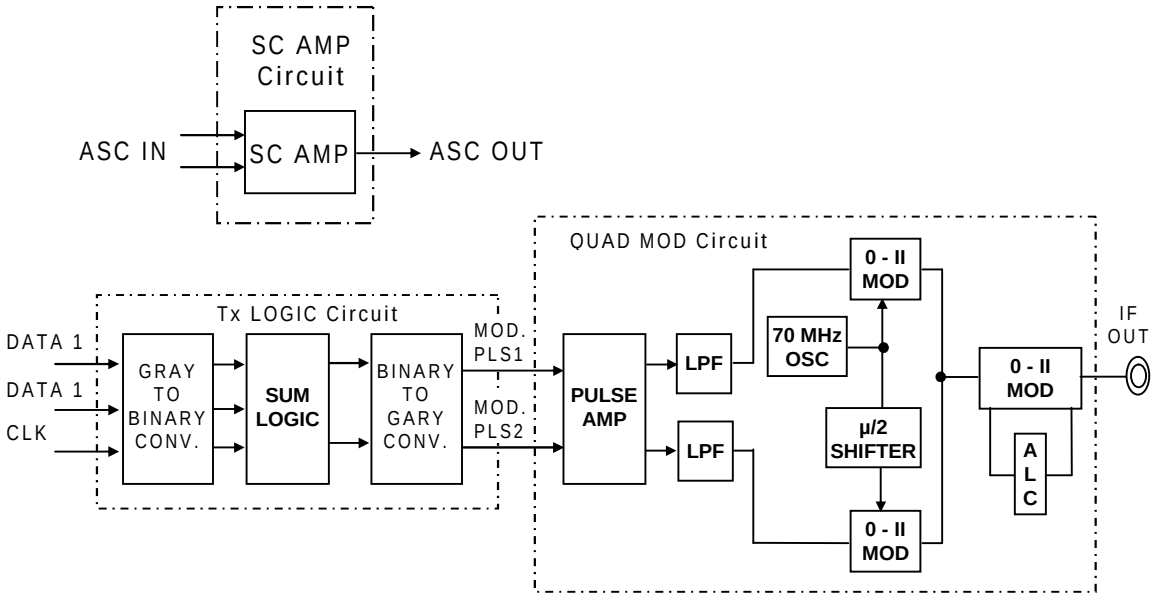


Figure 3.13 Block diagram of Phase Modulator

SC AMP circuit: The SC AMP circuit amplifies the analog service channel (ASC) signal and applies it to the TX local oscillator in the TX RF module where frequency modulates the RF signal with the applied SC signal.

Transmitter RF circuit (TX RF) C0060A (Figure 3.14)

The TX RF produces a 7 GHz band transmitting frequency signal by mixing a 7 GHz band local oscillator signal with a 70 MHz IF signal, and amplifies it with Field Effect Transistors (FET).

The TX RF consists of: -

1) Transmitter Frequency Converter (TX FREQ CONV) Section
2) FET Amplifier (FET AMP) Section; and
3) Transmitter Local Oscillator (TX LO) Section

Transmitter Frequency Converter (TX FREQ CONV) Section: It consists of a mixer (X31), an IF attenuator (R32 to R34) and a C1457A 5-stage Band pass Filter (C1487A 5 BPF, U1). The IF input signal is fed to the IF IN terminal and applied to the mixer (X31) through an IF attenuator (R32 to R34), and also a local frequency signal from TX LO section is applied to the mixer. The Mixer (single balanced type) consists of a GaAs schottky barrier diode (X31), strip line and slot line. The input IF signal passes through a micro-strip slot transition. The local signal also is converted into the slot line with a 1/4--wavelength line and applied to diode X31. These signals are mixed by each diode to produce an RF signal. The RF signal thus produced is applied to FET AMP section through an isolator (W3) and 5 BPF (U1). The 5 BPF is of Chebyshev type and has an attenuation of more than 40 dB at the outside of F_O ± 70 MHz. Therefore, this 5 BPF passes only the desired frequency signal from TX FREQ CONV section while eliminating all other frequencies.

Part of the TX LO output is coupled by a directional coupler, appearing at the LO MON terminal for monitoring the oscillating frequency without interrupting TX LO output.

FET AMP Section

It has a three stage FET amplifier sub module (U2 to U4) with input and output matching circuits (MSC2 to MSC6), an isolator (W4), an automatic level control (ALC) circuit (IC301), IC302 and TR301) and an FET bias circuit.

An RF input signal from 5 BPF (U1) is applied through an impedance matching circuit (MSC2) to the first stage FET AMP sub module (U2).

The first stage FET AMP sub module (U2), consisting of a 3-stage FET transistor and a PIN diode attenuator, amplifies the input RF signal by the 3-stage FET transistor and provides a constant output power level at RF OUT terminal by adjusting the internal impedance of PIN diode using the control voltage from ALC circuit.

The RF input thus amplified and ALC controlled at the first stage FET AMP sub module (U2) is amplified by the second stage FET AMP sub module (U3) that is composed of a 3 - stage FET transistor and the third stage FET AMP sub module (U4) that has one FET transistor to a suitable level.

The output power of the third stage FET AMP sub module (U4) appears at the RF OUT terminal through isolator (W4) and MSC6. The output isolator (W4) improves the VSWR of the output of this module.

Part of the output power of the third stage FET AMP sub module (U4) is coupled to the detector X41 that converts it into a dc component. The dc component thus obtained is sent to the ALC circuit for monitoring the voltage.

The ALC circuit consists of a 3 - stage ALC amplifier (IC301 and IC302), DC amplifier (TR301) and AUTO / MAN jack (Z 301).

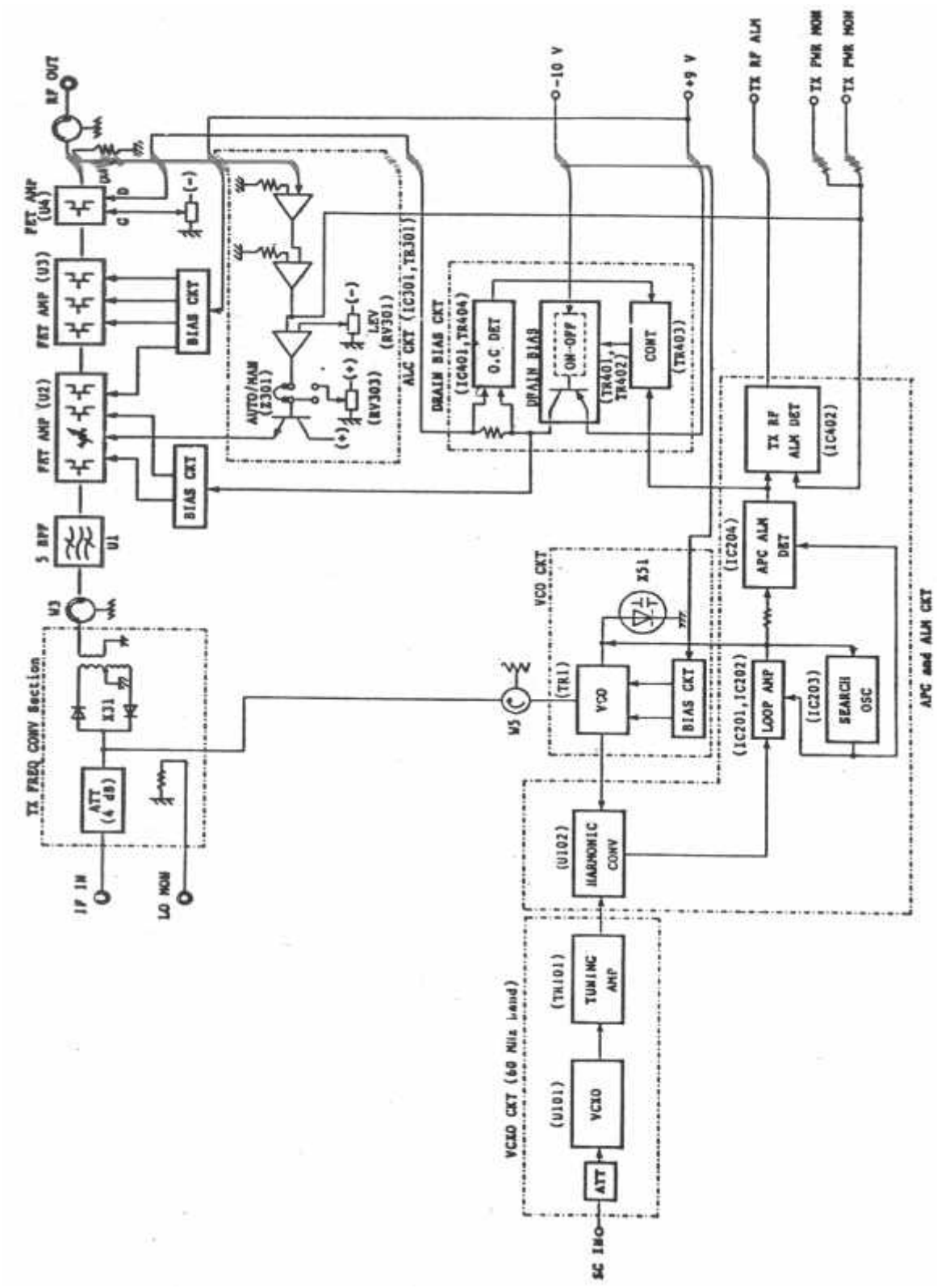


Figure 3.14 Block diagram of Transmitter RF circuit

DC monitoring voltage sent from the detector (X41) in the FET AMP is amplified by 3 - stage ALC amplifier (IC301 and IC 302) to obtain a DC voltage proportional to the RF output power. The DC voltage is applied through a contact AUTO of the AUTO / MAN. Jack (Z301) to the DC amplifier (TR301).

The DC amplifier amplifies the DC voltage to the value required for ALC operation. The output DC voltage (ALC voltage) of the DC amplifier is fed back to the first stage FET AMP sub module (U2) with PIN diode attenuator. The ALC voltage decreases (approaches +9 Volts at point “VA” on the FET AMP (U2) when the RF output power decreases, and loss of the PIN diode attenuator increases to prevent the decrease of the RF output power, or vice versa. The RF output power of the FET AMP, therefore, remains constant.

The ALC loop circuit can be opened or closed by the AUTO / MAN. Jack (Z301). The LEV control (RV301) controls the level at RF OUT terminal when ALC loop circuit is formed (the AUTO / MAN jack is set to AUTO). Normally, the AUTO / MAN jack is set to AUTO. When the jack is set to MAN, the RF output power is manually controlled by control RV303.

FET Bias Circuit

1) For first stage and second stage FET AMPS (U2 and U3)

A positive voltage of approx. 8 volts is supplied to FET transistors in the U2 and U3 through resistors R402 to R407. These FET transistors are controlled to provide a constant drain current by the self-bias voltage method.

2) For 3rd stage FET AMP (U4)

The gate bias circuit for FET transistor in the U4 has a voltage stabilizer (X303) with gate voltage adjuster (RV401). A stabilized -10 volts is applied to Zener diode X303 and regulated to -5.1volts. This voltage is supplied to voltage adjuster (RV401).

The negative voltage at the slider of the variable resistor RV401 is applied to the gate of FET transistor in the U4. The drain bias circuit for FET transistor in the U4 consists of TR401 to TR404 and IC401. A positive voltage of 9 volts is supplied to the FET through a high frequency cut-off filter (L502 and C502) and transistor TR402 of drain bias circuit. A protection circuit (TR401 and TR402) is provided in order to control a drain voltage to the FET transistor to prevent the FET damage; a gate bias is applied at first before transistor TR402 conducts to supply a drain voltage.

TR401 is conducted by -10V, applied to the emitter and -9.3V applied to its base. The conducted TR1 supplies +8.3 V at the base of TR402 through R408 to conduct TR402 and supplies a bias voltage to the drain terminal of FET.

An over-current detection circuit (TR404 and IC401) monitors the drain current through R401, and conducts TR403 when the drain current reaches three or four times the normal level. When TR403 conducts, +8.9V appears at the base of TR402 causing TR402 to cut off, the FET stops supplying the drain bias voltage to protect itself from damage due to over-current. Similarly, when trouble occurs in the APC circuit of TX LO section, the APC alarm signal turns TR403 ON and TR402 OFF so as to stop supplying the drain bias voltage and stops the FET operation.

TX LO Section: It section consists of a voltage controlled oscillator (VCO) using dielectric resonator, voltage controlled crystal oscillator (VCXO), automatic phase control circuit and alarm circuit (APC and ALM CKT).

The VCO circuit consists of a transistor oscillator (TR1) with a Varactor diode (X51) to close the feedback loop. The transistor oscillator contains a transistor (TR1) and a dielectric resonator, which consists of a suspended strip line, and also a Varactor diode (X51) is coupled to the dielectric resonator. This VCO directly generates a 7GHz band RF frequency and the output signal is sent to the mixer circuit through an isolator (W5). A portion of the VCO output signal is fed to the APC circuit and the control voltage from the APC circuit is applied to the Varactor diode (X51). This loop (APC loop) phase locks the VCO frequency with the built in voltage controlled crystal oscillator. Part of the VCO output signal appears at the FREQ MON terminal for monitoring the oscillating frequency without interrupting the local signal. The bias circuit (BIAS CKT) determines the base-to-emitter voltage of transistor TR1. Voltage Controlled Crystal Oscillator (VCXO) Circuit contains a 60-MHz band crystal oscillator (U101) having a Varactor diode to insert the service channel (SC) signal into the transmitting circuit and a 60-MHz band-tuning amplifier.

The 60-MHz band crystal oscillator (U101) directly generates a 60-MHz band signal frequency equal to 1/N (N is a natural number which makes the VCXO frequency nearly equal to 60 MHz) of the VCO frequency and functions as an FM modulator by which the 60-MHz band signal frequency is modulated with SC signal applied to the terminal SC IN.

The tuning amplifier amplifies the 60-MHz band signal to a required level for driving the phase detector (HARMONIC CONV). The output circuit of the tuning amplifier (C105, C106, L101 and L102) tunes with the oscillation frequency of 60-MHz band crystal oscillator and rejects undesired waves such as spurious.

APC Loop Section, that is, the phase lock loop (APC LOOP) circuit consists of a phase detector (HARMONIC CONV; U102), APC LOOP amplifier (LOOP AMP: IC 201 and IC202), search oscillator (IC203) and VCO. The closed loop frequency response of this APC loop is in a low pass mode, when the difference between the VCO frequency and the multiplied crystal oscillator frequency is less than the cut-off frequency of the APC loop. The beat frequency between both frequencies is amplified and applied to the VCO. The VCO output signal is modulated with this beat frequency. The output amplitude of the APC LOOP AMP increases when the beat frequency becomes low according to the open loop frequency response.

As a result, the waveform of the beat signal is distorted and the dc component is generated by this distortion so that both frequencies become coincident. Consequently, the VCO frequency is pulled into the multiplied crystal oscillator frequency. Therefore, the pull-in frequency range is rather narrow. However, after this loop is pulled in once, phase lock condition can be held up to the saturation value of the APC LOOP AMP output voltage because of high dc gain.

The search oscillator (IC203) provides an effect of expanding the pull-in range by swinging the VCO frequency. So, the search oscillator oscillates when the frequency of VCO is unlocked, and stops oscillating when locked. Thus, the frequency difference becomes very close to zero and then the feedback operation of the APC LOOP causes the VCO to

synchronize or lock with the signal from the crystal oscillator. Once in lock, the VCO frequency is completely controlled by the crystal oscillator. The alarm circuit (IC203, IC204 and IC402) monitors the oscillation frequency of VCO and the RF output power, and issues TX RF alarm signal from terminal when either of them exceeds the specified value. When the APC loop is in the unlock state, the search oscillator oscillates and the search signal issues. Diode (X204) detects this search signal and converts into a dc voltage, drives IC203, IC204 and IC402 of alarm circuit and sends out the APC alarm signal as the TX RF alarm. The TX output is cut-off when APC loop is in the unlock state to prevent adjacent channel interference.

IC 204 - 1/2 and IC204-2/2 monitor the control voltage from the APC LOOP AMP to the VCO, and sends out the APC alarm signal as the TX RF alarm when the monitored signal exceeds the specified value. The monitoring signal (a dc voltage) of the RF output power is picked up from the second stage ALC amplifier output of the ALC circuit through resistor R307 and applied to IC402. When the RF output power decreases below the specified value, IC402 operates and sends out the RF output power alarm as the TX RF alarm.

3.5 Receiver (RX) C0091A (Figure 3.15)

The receiver (RX) consists of a RXRF circuit (C 0102A) and a RX IF circuit (B 9957 A).It converts a 7 GHz band receiving RF signal into a 70 MHz IF signal and amplifies the 70 MHz IF signal to the required level.

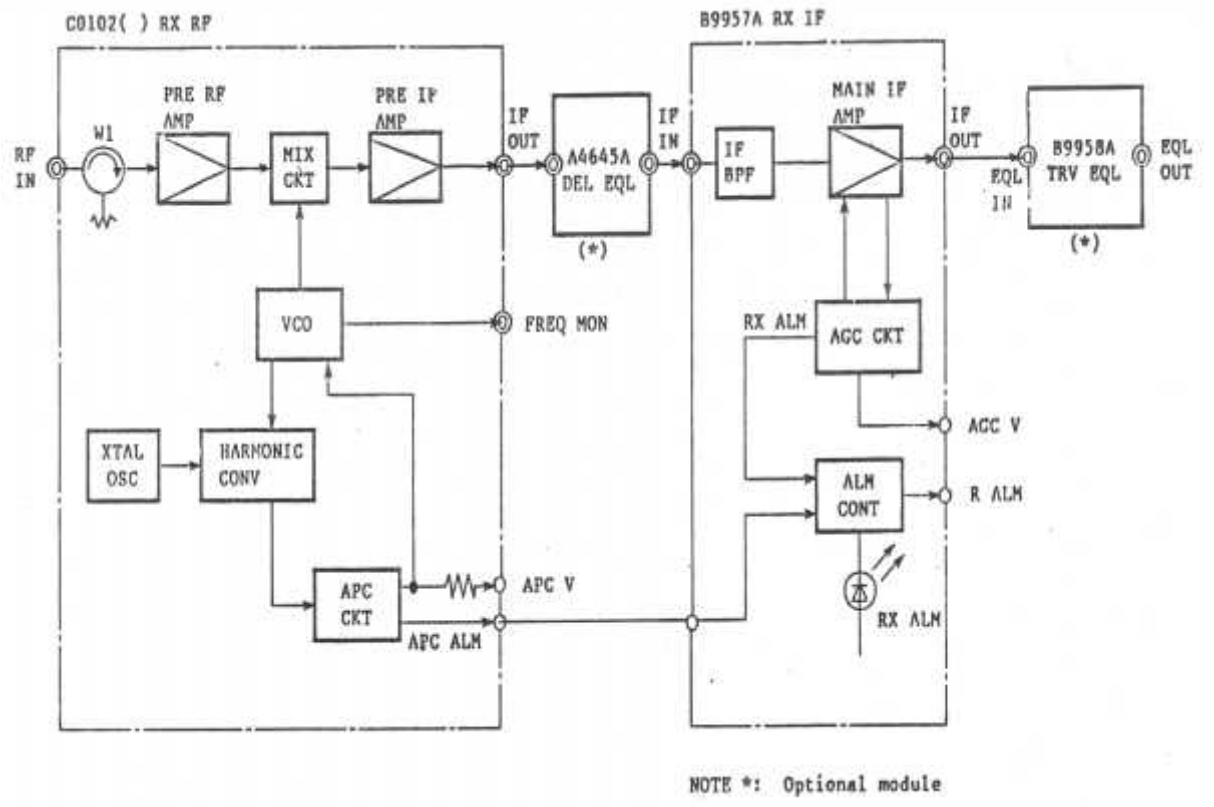


Figure 3.15 Block diagram of Receiver

The RX RF consists of: (Figure 3.16)

1) Receiver Frequency Converter (RX FREQ CONV) Section; and
2) Receiver Local Oscillator (RX LO) section.

The RX FREQ CONV section consists of a pre-RF amplifier, FET bias circuits, mixer Circuit and IF amplifier.

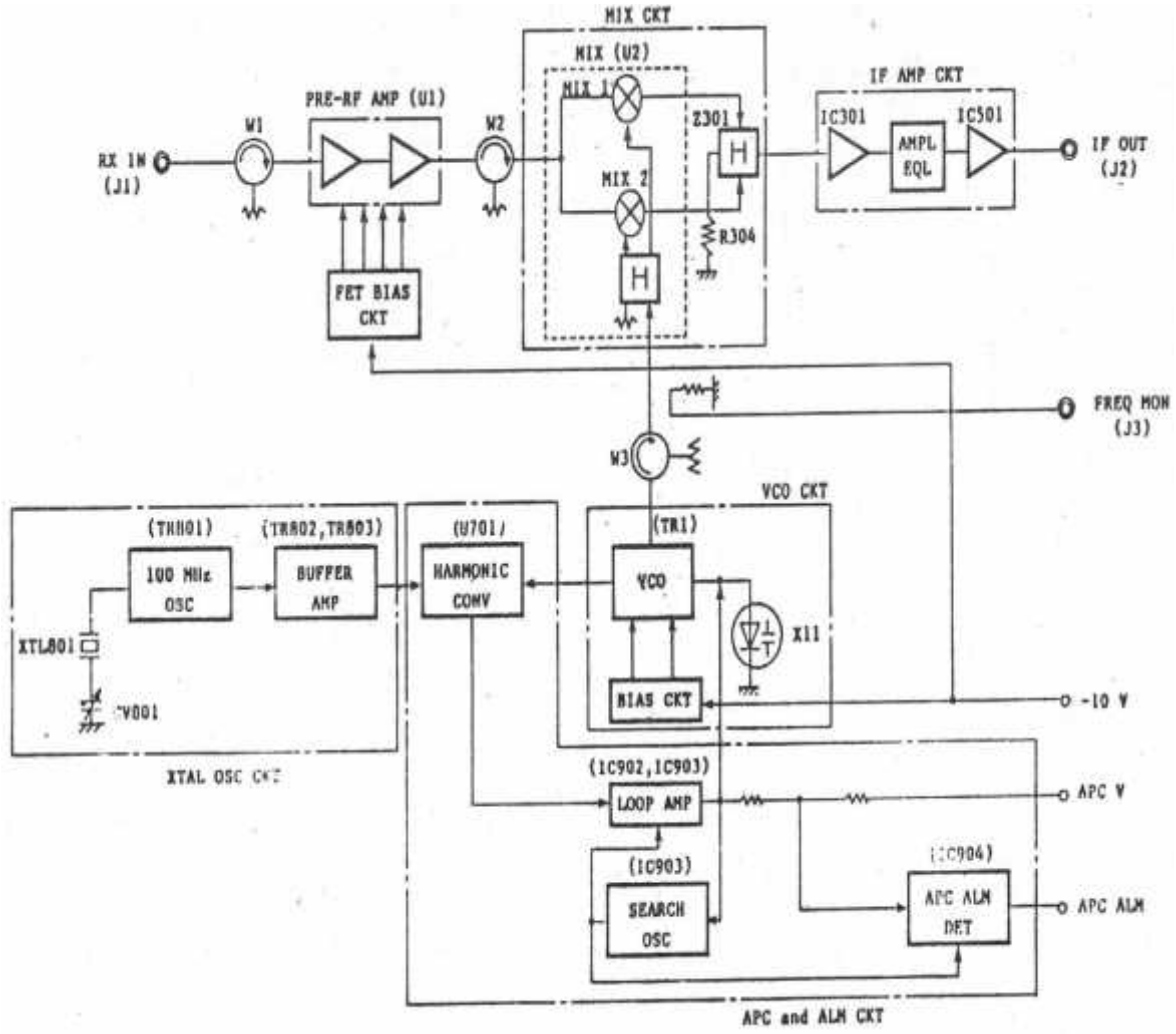


Figure 3.16 Block diagram of Receiver RF Section

The Pre-RF amplifier amplifies the RF input signal and the mixer converts it to output an IF signal with a local frequency signal from the receiver local oscillator, suppressing image-side spurious and noise without using a BPF. The Pre-IF amplifier and the IF amplifier amplify the IF signal.

Pre-RF Amplifier: The RF input signal is fed to the input terminal RF IN and applied through an isolator (W1) to the Pre-RF amplifier (U1). The Pre-RF amplifier is a 2-stage, low noise amplifier, which is formed by GaAs FET transistors. The isolators W1 and W2 improve the VSWR of input and output of the Pre-RF amplifier respectively.

The FET bias circuit (TR101 and TR102) has two bias stabilizers and protection circuits for the GaAs FET transistors in the Pre-RF amplifier (U1). The voltage fed to the power terminal is applied to the FET bias circuit and regulated, to be used for gates G1, G2 and sources S1, S2 respectively. Thus, the source drain voltage is about -3 volts, the gate drain voltage is about source drain volts and the drain electrode is grounded. The gate bias voltage is controlled to make the source drain voltage of about -3 volts, and thus obtain the constant drain voltage.

The MIXER circuit contains sub module U2, a wideband image cancel balanced mixer with 4 Silicon Schottky barrier diodes, RF hybrid and IF hybrid (Z301). Here, a local frequency signal from the VCO passes through the RF hybrid (formed by micro-strips) where it is split into two. One for MIX 1 and another one (with phase delayed relatively by 90^0) for MIX 2. These local frequency signals are mixed in each balanced mixer with an RF input signal and an image signal in phase from the Pre-RF amplifier. Thus, these balanced mixers (MIX 1 and MIX 2) produce an IF signal and an IF image signal with a constant phase difference. The IF signals from MIX 1 and MIX 2 are applied to an IF hybrid (Z301) with a phase difference of 90^0. Also the IF image signals from MIX 1 and MIX 2 have a phase difference of 90^0 in the opposite direction to the IF signal. Here, when the local frequency is 70 MHz above the RF input frequency, the IF signals appearing at output terminal 2 of the IF hybrid become in phase and the image signals at that terminal cancel, but no IF signal appears at output terminal 6 and image IF signals, which are in phase, are absorbed in the resistor R304 connected to the terminal. Thus, the output IF signal appears at the output terminal 2 of IF hybrid.

However, when the local frequency is 70 MHz below the RF input frequency, the IF signals appear in phase at output terminal 6 of IF hybrid and the IF image signals in phase appear at output terminal 2 and then are absorbed in the resistor R304 as described above.

The IF amplifier consists of two amplifiers and an amplitude equalizer and the IF signal from the mixer is amplified by the IF amplifier to the required level at the IF OUT terminal. The amplitude equalizer equalizes amplitude to frequency response.

The RX LO section consists of a voltage controlled oscillator (VCO) using dielectric resonator, crystal controlled oscillator, automatic phase control circuit and alarm circuit (APC and ALM CKT). The VCO circuit consists of a transistor oscillator (TR1) having a Varactor diode (XII) to close the feedback loop. The transistor oscillator contains a transistor (TR1) and a dielectric resonator, which consists of a suspended strip line. Also, a Varactor diode (XII) is coupled to the dielectric resonator.

This VCO directly generates a 7 GHz band RF frequency and the output signal is sent to the mixer circuit through an isolator (W3). A portion of the VCO output signal is fed to the APC circuit and the control voltage from the APC circuit is applied to the Varactor diode (X 11). This loop (APC loop) phase locks the VCO frequency with the built in crystal controlled oscillator. Part of the VCO output signal appears at the FREQ MON terminal for monitoring the oscillating frequency without interrupting the local signal. The bias circuit (BIAS CKT) determines the base to emitter voltage of transistor TR1.

The crystal controlled oscillator circuit contains a 100 MHz band crystal oscillator (TR801) with quartz crystal (XTL 801) and two stage buffer amplifier (TR 802 and TR 803). The 100 MHz band crystal oscillator generates a frequency equal to (1/ 74 or 1/ 76) of the VCO frequency and the buffer amplifier amplifies it to a value suitable for driving the phase detector (HARMONIC CONV).

The phase lock loop (APC LOOP) circuit consists of a phase detector (HARMONIC CONV; U701), APC loop amplifier (LOOP AMP; IC902 and IC903) and VCO. The closed loop frequency response of this APC loop is in the low pass mode, when the difference between the VCO frequency and the multiplied crystal oscillator frequency is less than the cut-off frequency of the APC loop, the beat frequency between both frequencies is amplified and applied to the VCO. The VCO output signal is modulated with this beat frequency. The output amplitude of the APC LOOP AMP increases when the beat frequency becomes low according to the open loop frequency response.

As a result, the waveform of the beat signal is distorted and the dc component is generated by this distortion so that the both frequencies become coincident. Consequently, the VCO frequency is pulled into the multiplied crystal oscillator frequency. Therefore, the pull in frequency range is rather narrow. However, after this loop is pulled in once, phase lock condition can be held up to the saturation value of the APC LOOP AMP output voltage because of high dc gain.

The search oscillator provides the effect of expanding the pull in range by swinging the VCO frequency. Thus, the frequency difference becomes very close to zero and then the feedback operation of the APC LOOP causes the VCO to synchronize or lock with the signal from the crystal oscillator. Once in lock, the VCO frequency is completely controlled by the crystal oscillator. The APC ALARM circuit contains a search oscillator (SEARCH OSC; IC903) and APC alarm detector (APC ALM DET; IC904).The SEARCH OSC operates when the APC loop is in the lock off condition and the output signal is fed to the APC ALM DET. The output voltage at the APC ALM terminal is -10 volts when APC normal and zero volts in lock off condition.

Receiver IF Circuit (RX IF) B 9957-A (Figure 3.17)

The converted 70 MHz IF signal is fed to the RX IF circuit through a delay equalizer which equalizes, on a hop basis, the system delay caused by filtering in the transmitter receiver and the RF branching circuit.

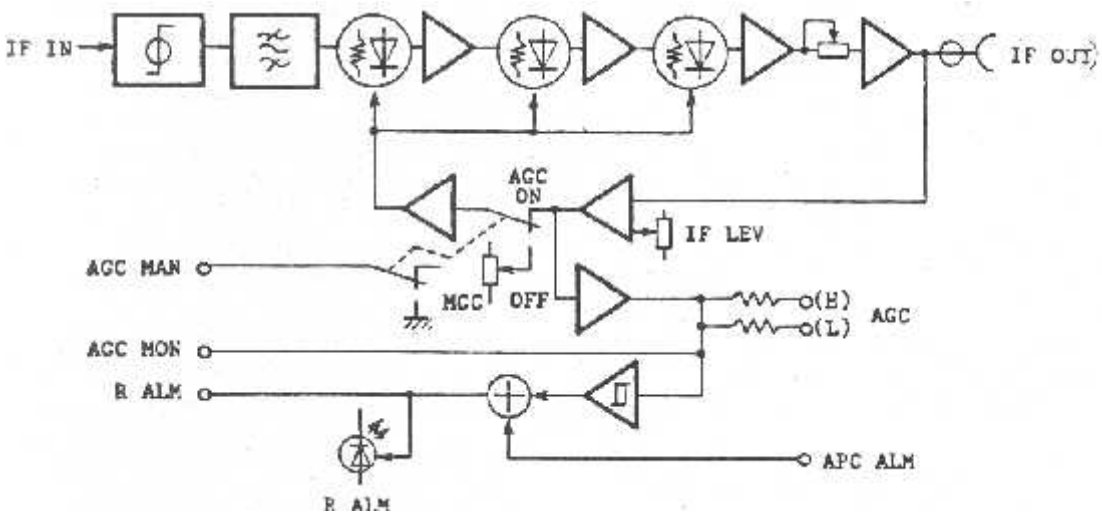


Figure 3.17 Block diagram of Receiver IF section

A4645A DEL EQL (Optional): The DEL EQL is an optional IF delay equalizer. The DEL EQL is used for equalization of reflected delay developed in the branching circuit of the Transmitter Receiver. The DEL EQL is used depending on system requirement.

It is pre-mounted at the factory according to the delay characteristics developed. It is completely factory adjusted and this needs no adjustment on site.

The RX IF comprises:

1) B 5015F IF Band pass Filter (for B9957A type) or
   B 5015G IF Band pass Filter (for B9957B type)
2) Main IF Amplifier (MAIN IF AMP) Section; and
3) Alarm Circuit.

The B5015 (F) IF BPF has a 5 stage IF band pass filter, U1 amplitude equalizer and IF delay equalizer. The BPF circuit consists of a Chebyshev type 5- stage band pass filter with sharp cut-off characteristics. It passes only the desired IF signal, and eliminates all other frequencies.

The IF amplitude equalizer following the IF band pass filter equalizes the IF amplitude-to-frequency response. The two stage IF delay equalizer equalizes the IF delay developed in the IF band pass filter.

The MAIN IF AMP section consists of a main IF amplifier (MAIN IF AMP), an AGC circuit and an alarm circuit. The MAIN IF AMP is a wideband amplifier (TR101 and IC101 to IC104) with PIN diodes. It has a high dynamic AGC range of about 55 dB which keeps the IF output level of -3 dBm within $\pm$ 0.5 dB. This amplifier operates as a vario-loser whose gain is controlled by PIN diode. Here, an IF signal from the IF BPF (U1) terminal is amplified by the 5 - stage amplifier (TR101 and IC101 to IC104) and branched at the output of the fifth stage amplifier (IC104). The IF output level is regulated to -3 dBm by changing the impedance of the PIN diode, connected in series to the output of a transistor, with AGC voltage from the dc amplifier (AGC AMP, IC107).
The AGC circuit consists of an AGC amplifier (IC105) and an AGC MGC switch (S101). The AGC AMP (IC105) has an IF buffer amplifier, detector and dc amplifiers. Hence, the IF output signal of the 4-stage IF amplifier (IC101 to IC104) branches to the IF buffer amplifier in the AGC amplifier (amplifies it to the appropriate level). The amplified IF signal is detected by the detector and provides a dc voltage proportional to the IF signal level. This dc voltage is amplified by the dc amplifiers and applied through AGC contact of the AGC MGC switch (S101) to the dc amplifier.

The output dc voltage (AGC voltage) of the dc amplifier is fed back to the 4-stage IF amplifier (IC101 to IC104) with PIN diodes. The AGC voltage decreases (approaches ground potential) when the IF signal level increases and the gain of the IF amplifier decreases to prevent any increase of the IF signal level, or vice versa; thus keeping the output level of the MAIN IF AMP remains constant. A portion of the AGC voltage amplified by the dc amplifier in IC appears at the AGC V MON terminal to monitor the AGC voltage. The AGC loop circuit

can be opened or closed by the AGC - MGC switch (S101). The IF LEV control (RV102) controls the level at the IF OUT terminal when an AGC loop circuit is formed (the AGC - MGC switch in AGC). Normally, the AGC - MGC switch is set to AGC. When the AGC - MGC switch is set to MGC, for maintenance, terminal Z1-b20 grounds to issue a maintenance signal, and the gain of the MAIN IF AMP is manually controlled by MGC LEV control (RV103).

Alarm Circuit

	Alarm operation condition		
1) IF output level low	0 to -2V	ALM	RX ALM LED (X119) is lighted. Terminal Z1-c20 is TTL low level.
2) APC ALM (Z101-1):	-8 to -10V	NORM	RX ALM LED (X119) is unlighted. Terminal Z1-c20 is TTL high level.

Transversal Equalizer (TRSV EQL) B9958-A (Optional) (Figure 3.18)

This module automatically compensates both amplitude and delay distortion which are caused by selective fading in the microwave propagation path. This is achieved by monitoring and suppressing inter- symbol interference at the 4 phase demodulator.

The TRANSV EQL module consists of a transversal filter circuit, a control signal generator (CONT SIG GEN), and an IF amplifier (IF AMP). The input of the module is 70 MHz with a nominal level of - 3 dBm and an impedance of 75 ohms, unbalanced.

The IF signal from the RX IF module, is fed to the IF IN jack.

a. The transversal filter circuit (variable band pass-filter) has four delay line units with 3 taps (Signal outlet), eight multipliers which control tap weights, two signal adders and a directional coupler (quadratic hybrid). The delay time of each of the delay line units is 1/fc (fc: Clock Frequency) second.

In normal (undistorted) conditions the IF signal passing through the route shown by the thick line, shares the majority of the signal component. When the IF signal is distorted by selective fading in the transmission path, the upper part of the circuit eliminates the in-phase distortion and the lower part compensates for distortion caused by quadrature components. The tap weights are controlled with signals from the control signal generator.

b. The control signal generator supplies four (4) control signals to the multipliers of the transversal filter. These control signals are generated by data signals and error signals of each P and Q channel from the PH DEM module. The control signals are reset with a reset signal detected during carrier synchronization loss, over maximum level error, at the PH DEM module. The equalized IF signal from the transversal filter circuit goes to the IF amplifier, where the attenuated IF signal is amplified to - 3 dBm at an impedance of 75 ohms, unbalanced.

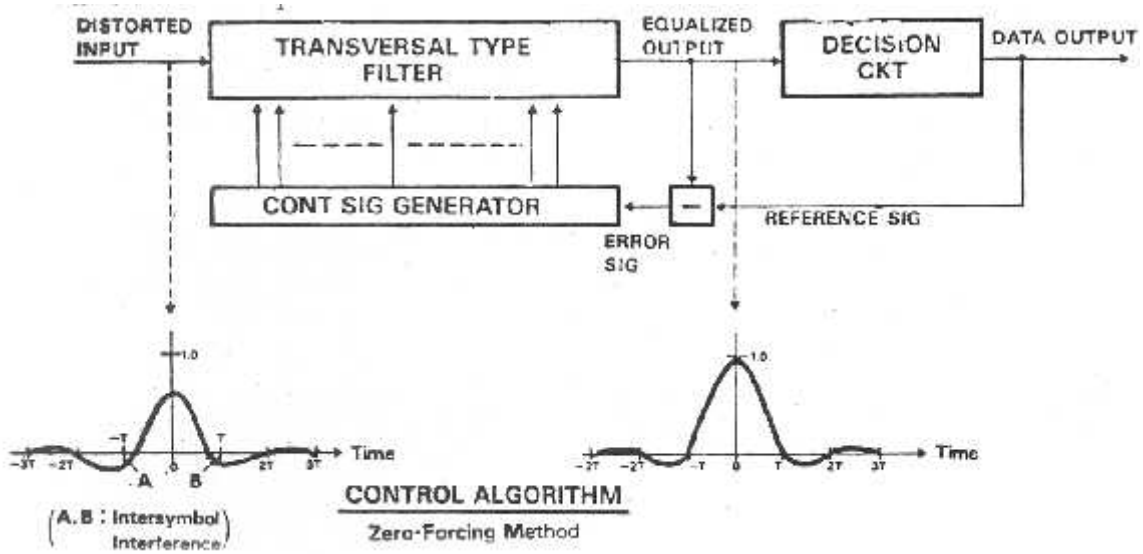


Figure 3.18 Block diagram of Equalization

Demodulator (DEM) D2799-A (Figure 3.19)

The DEM comprises the 4 phase Demodulator (PH DEM) D2668-A and the Bit combiner (BIT COMB) B 9961-A. The received IF signal is applied to the PH DEM and converted to two binary coded pulse streams. The converted pulse streams from the PH DEM are sent to the RX DPU through the BIT COMB.

(1) Carrier Recovery & 4 PSK Demodulator: The modulated signal input from IF IN is branched into two. One of the branched signals is mixed with the VCO signal and the other is mixed with π/2 phase shifted VCO signal. As a result, the output corresponding to the phase difference between the input signal and the VCO signal is obtained.

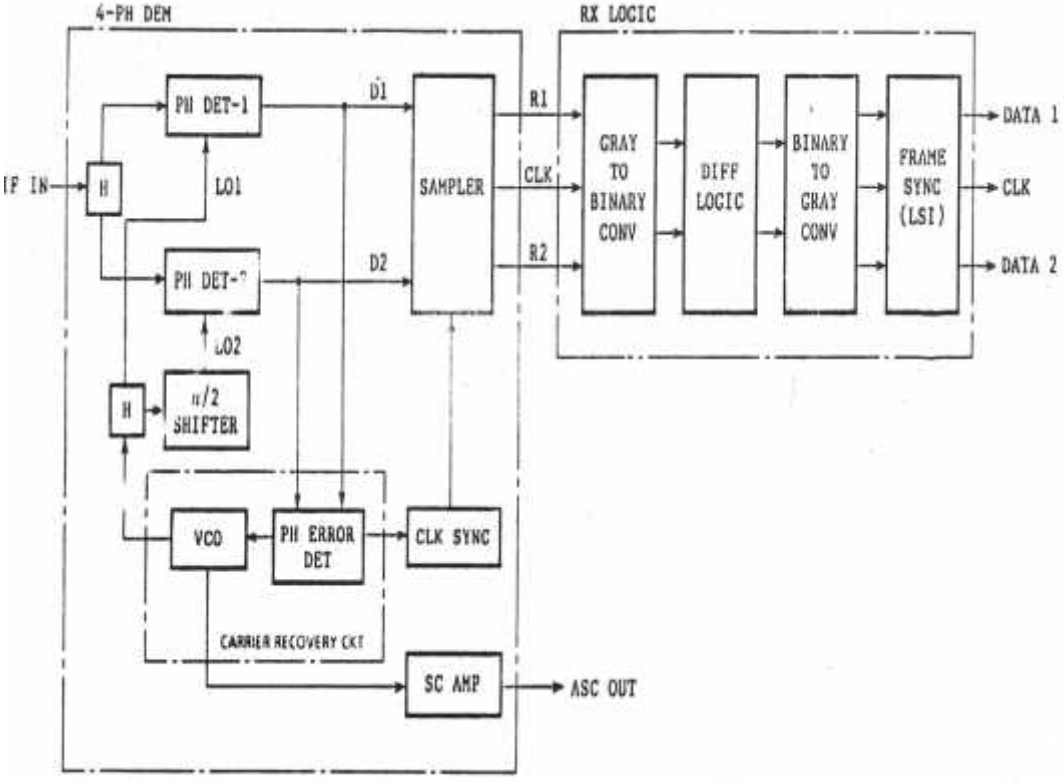


Figure 3.19 Block diagram of Demodulator

The signals P and Q are split and applied to an amplifier and a full wave rectifier respectively. The outputs from the amplifier and the full wave rectifier are each applied to a decision circuit and converted into pulse wave signals. These are logically processed by an error signal detector, which generates an APC signal and an ALC signal. The APC signal is applied to the 70 MHz VCO to synchronize the input signal with the output signal by controlling the oscillation frequency of the VCO. The ALC signal controls attenuation of the attenuator to keep the IF signal input to the PH DET constant. As a result of coherent detection by using the recovered carrier the base band signal is demodulated.

(2) SC AMP: The SC signal is FM-modulated to a carrier signal and transmitted. Therefore, at the carrier recovery circuit (Costas loop) described in (1), an SC signal is demodulated from the control signal for the VCO. The demodulated SC signal is amplified and the output has a balanced 600 ohms impedance.

(3) CLK SYNC & Pulse Regeneration: The demodulated base band signal is fully rectified and input to the CLK SYNC. The CLK SYNC circuit has a VCO and regenerates a clock. The demodulated base band signal is instantaneously detected with this clock and reshaped as the pulse signal.

(4) Differential Decoding Circuit and Descrambler Circuit: The circuit outputs correctly sequenced data from the digital signals by logic operation. This logic operation is called differential decoding and corresponds to the reverse operation of differential encoding performed in the modulation section. The descrambler circuit consists of Modulo-2 arithmetic circuit and shift resistor. The data signal is descrambled by PN pattern produced at the self-data signal timing.

(5) Transmission Quality Monitoring and Channel Discrimination Circuit: The recovered digital signals from the differential decoding circuit are sent to the frame synchronization LSI. The function of this LSI is to provide frame synchronizing, and also to provide transmission quality monitoring.

Transmission quality in the frame synchronizing LSI is monitored using a parity check after frame synchronization has been established by a one bit shift hunting method. Here, the parity check is performed by parity check counter which counts parity bits on the received data stream, at the F SYNC also generates parity bits in the same way as the transmitting side, and compares the bit numbers with that of the F SYNC at specific intervals, and parity error pulse (P PLS ERR) is generated if the comparison is detected in error. The BER detector counts P PLS ERR signal and generates BER alarm signal according to a threshold level setting. The BER threshold level can be set for a high BER detector of any one 3×10^{-4}, 3×10^{-5}, or 3×10^{-6} and for a low BER detector of any one 3×10^{-3}, 3×10^{-4}, 3×10^{-5}, 3×10^{-6} or 3×10^{-7}. Channel discrimination is obtained by selecting the frame synchronization bit for frame synchronization function (“ID CODE SELECT” function) at both the TX and RX end.

(6) WS/DSC drop and insert: The WS/DSC signals can be extracted and/or added from/to the main signal streams freely in the LSI circuit.

Bit Combiner (BIT COMB) B9961-A (Figure 3.20)

It corrects the delay timing of each input data stream in the regular and protection channels, and accomplishes hitless switching by triggering the four (4) switching mode signals so as to select one of the two data signals. Furthermore, it monitors the circuit quality and channel identification by the frame synchronization. Type A has drop and insert functions for the DSC signals and WS signal.

CIRCUIT OPERATION PRINCIPLES: The B9961A BIT COMB consists of a PROT/REG data selector, delay adjustor-1, delay adjustor-2, data line selector, and switching logic circuit in LSI, frame synchronizer and alarm control circuit.

Delay Adjuster 1: The functional diagram of the delay adjustor 1 is shown in figure 3.21. The flip-flop circuit shifts the data after retiming. Then, the data is delayed by 7 bits delay in the 7 bits shifter.

Delay Adjuster 2: The functional diagram of the delay adjuster 2 is shown in figure 3.22. The data is adjusted until the fixed delay matches to the 0 to 0.5 bits of the protection channel data by means of the timing adjustment (Coarse).

According to delay difference between REG and PROT, 4-bit shifted data is determined to use or not to use (Ex. DATA in PROT lags behind those in REG).

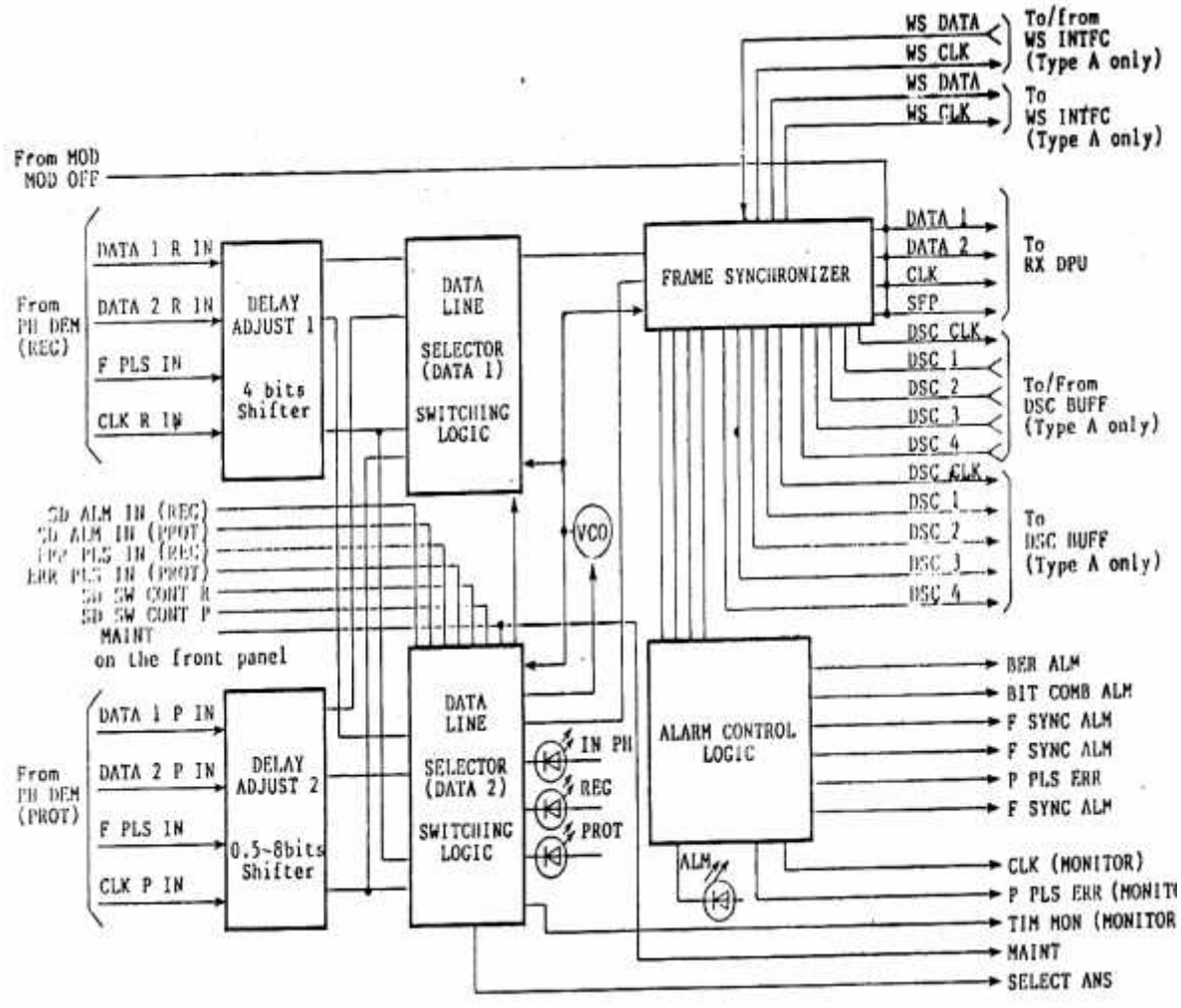


Figure 3.20 Block diagram of bit-combiner

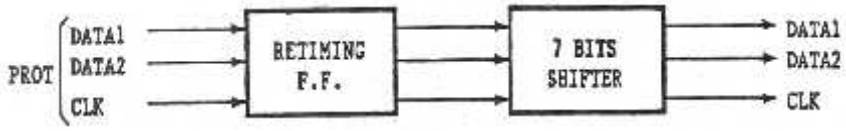


Figure 3.21 Block diagram of delay adjustor-1

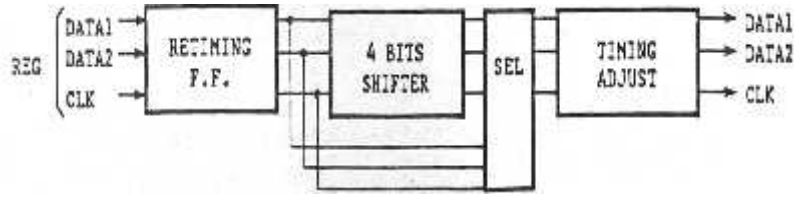


Figure 3.22 Block diagram of delay adjustor-2

Data Line Selector: The data line selector receives the data and clock inputs concurrently from the delay adjustors 1 and 2 and selects either of them to accept an output by the switching control signal from LS1.

Switching Logic: The functional diagram of the switching logic in LSI is shown in figure 3.23. The switching logic has a logic function to give a switching signal priority over three other switching signals among the four (4) incoming switching signals. The order of priority is as follows:

1) Manual control signal from the REG-AUTO-PROT switch on the front side of the BIT COMB module
2) Remote control signal from external supervisory equipment
3) R ALM signal from the SWO CONT module, and
4) Error pulse from the PH DEM module.

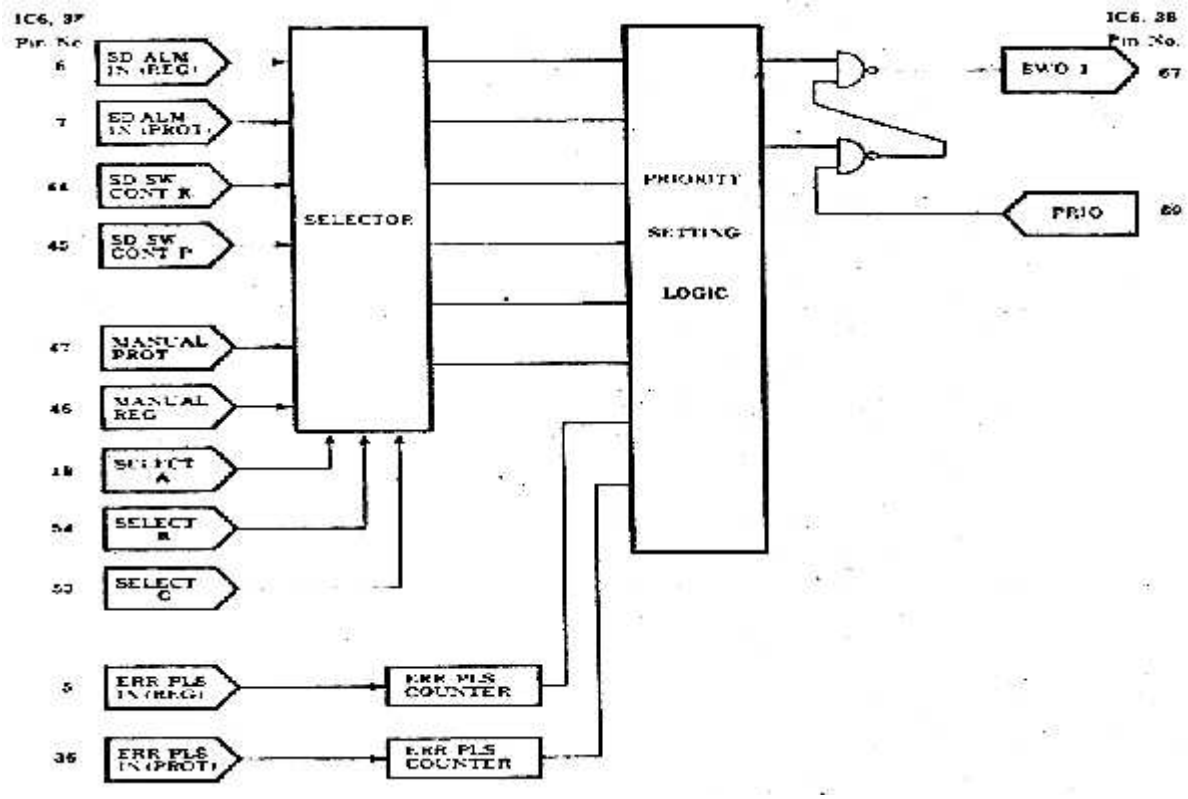


Figure 3.23 Functional diagram of switching logic

Frame Synchronizer: The functional diagram of the frame synchronizer is shown in figure 3.24. The circuit takes the frame synchronization of Data lines selected by the Data line selector and conducts the monitoring of circuit quality by parity check bit and Type A takes the dropping and insertion of the DSC signal.

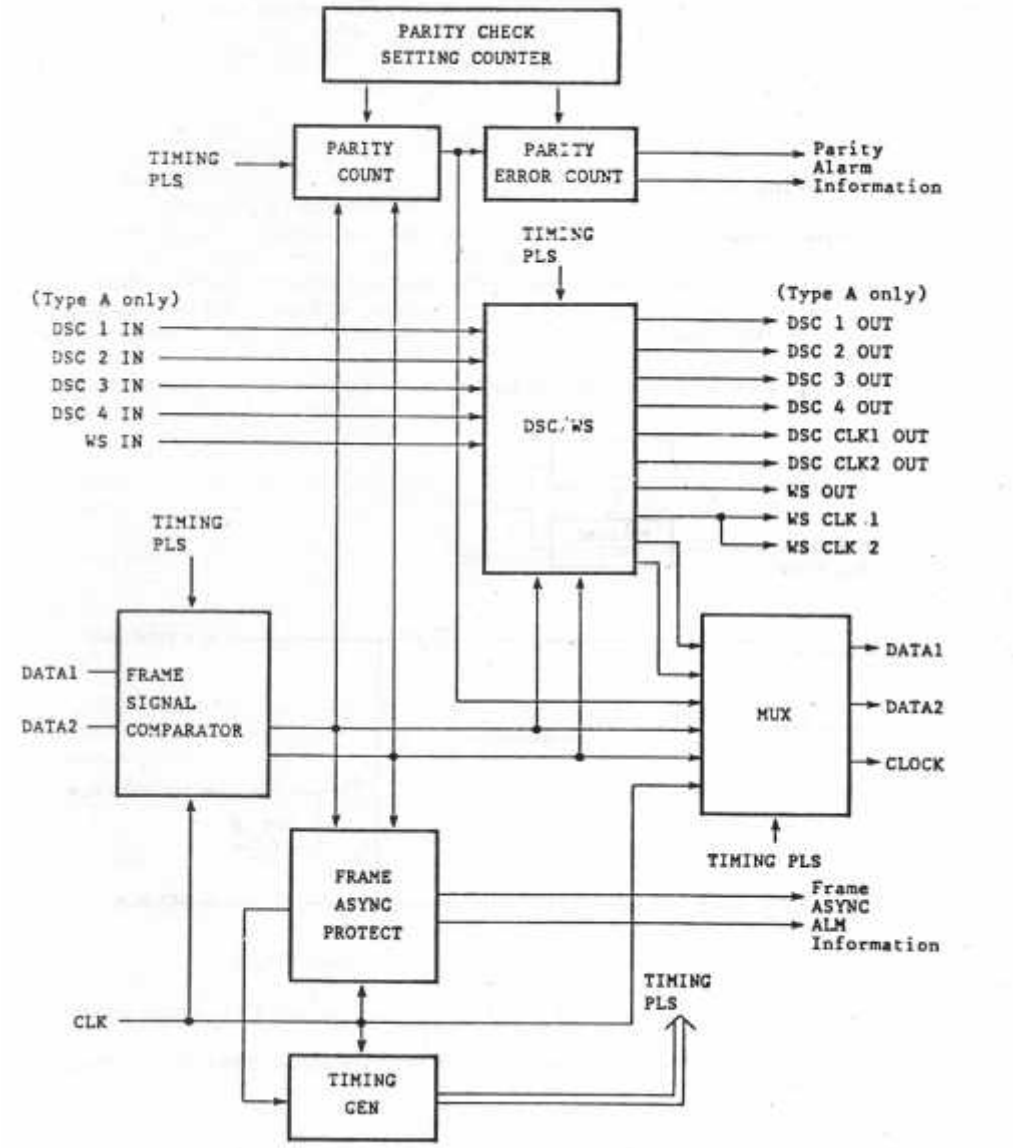


Figure3.24 Block diagram of frame synchronizer

ALM Control Circuit: The functional diagram of the alarm control circuit is shown in figure 3.25. The PLS LOSS DET operates when the DATA 1 and 2 signals of the F SYNC output are failed. The BIT CLK SYNC ALM is sent when the VCO (Voltage control oscillator) is asynchronized. The F SYNC ALM is sent when the frame is asynchronized.

The BER ALM is sent when the parity error is increased more than specified value.
The BIT COMB ALM is sent out and ALM LED is lighted with above four (4) alarms.

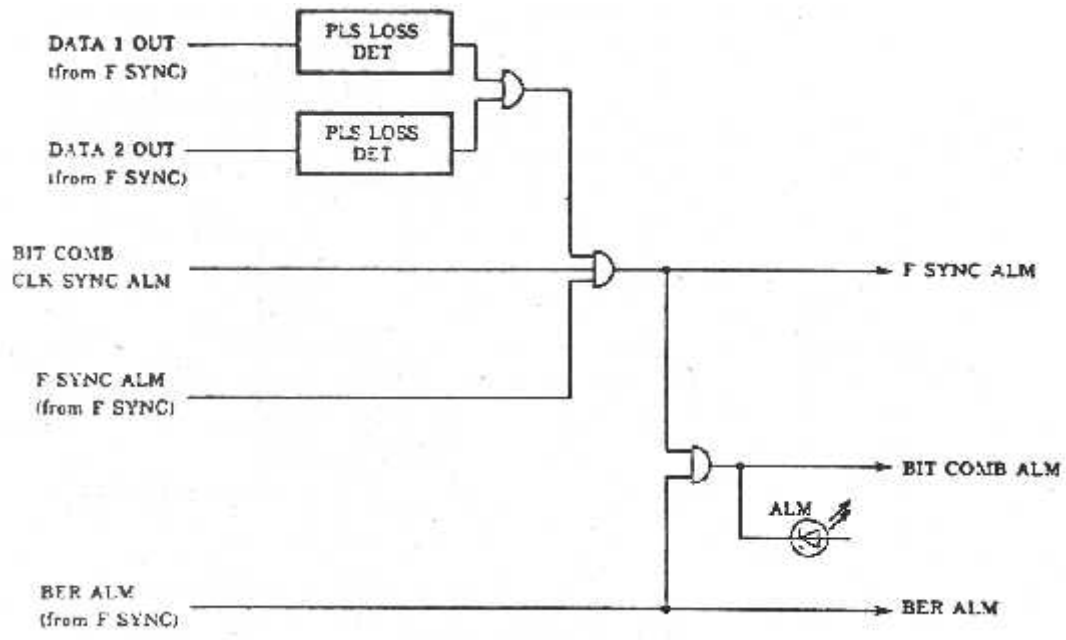


Figure 3.25 Block diagram of ALM& Control Circuit

3.6 RX DPU B9968-A (Figure 3.26)

The RX DPU consists of demultiplexer, parallel to serial converter, unipolar to HDB-3 converter. Its functions are reverse to the B-U Converter operation of transmitting end to feed an original HDB-3 signal to SWO Module.

Demultiplexer (Figure 3.27)

The demultiplexer descrembles input data stream with a random pattern, and extracts all bits inserted into the data stream. The original signal, same as that of the transmitting end is reproduced and sent to the parallel - serial converter.

Comparator: This phase compares 1/8-division frequencies of the Read clock (17.184 MHz) and write clock (19.332 MHz) and inputs the result to APC (Automatic phase comparator) of VCO.

Buffer Memory: The signal descrambled is written in the elastic memory by an input clock having time gaps at the ratio of 9 bits to 1 bit. At this time, the overhead bits (Frame pulse, DSC, parity bit) are not written in the elastic memory; therefore, the signal written in memory has gaps. These gaps are smoothed by PLL (Phase locked loop) and an original signal, the same as that of the transmitting end is reproduced and sent to the U-B CONV.

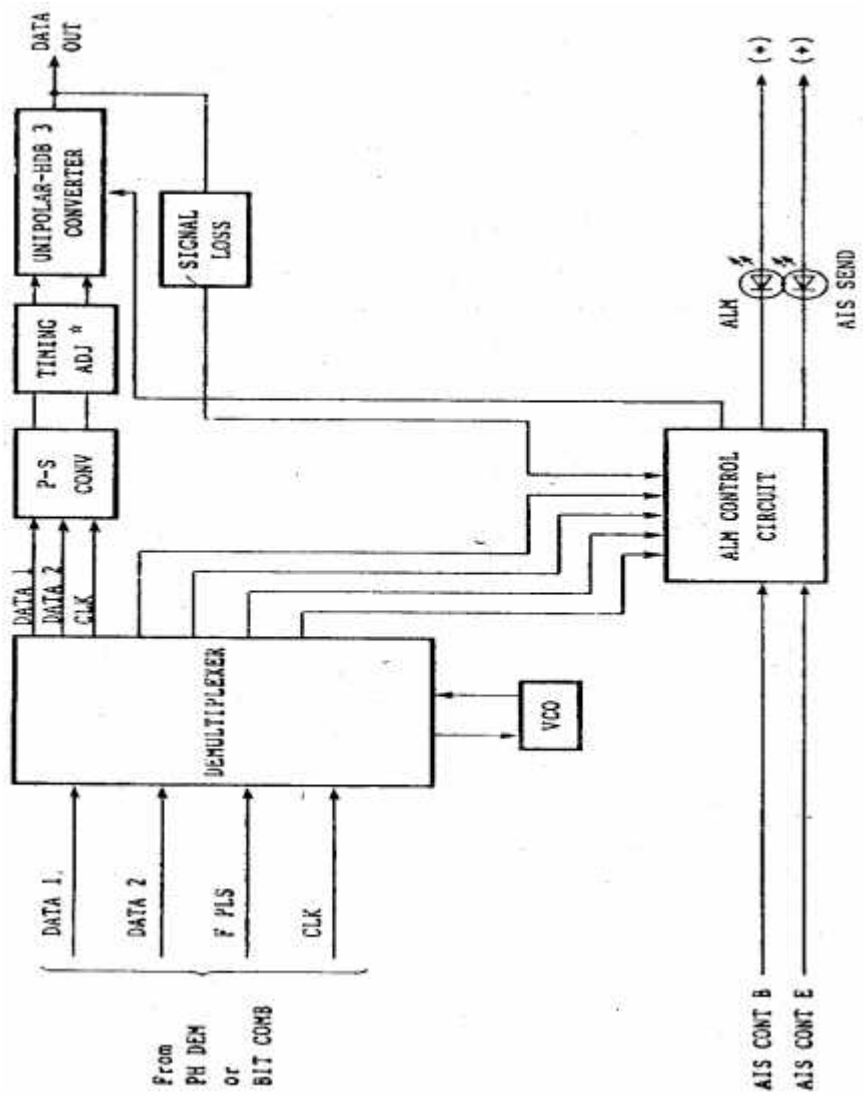


Figure 3.26 Block diagram of RX-DPU

AIS DET: This detects that the input signal becomes the radio systems AIS signal (1, 0, 1, 0) and outputs the low level (less than 0 $\pm$ 0.2 V) to the AIS receiving signal.

Parallel Serial Converter Circuit (Figure 3.28 and 3.29)

The converter reshapes the timing of input DATA 1 and DATA 2 to ease the parallel to serial conversion by input clock signals. The converter selects alternately the contents of DATA 1 and DATA 2 with clock pulses at the selector circuit consisting of OR circuits.

As a result, parallel to serial conversion is performed so that information of DATA 1 precedes and that of DATA 2 follows the serial stream. However, since the serial converted data streams have a difference in width of one bit, the phase ambiguity is eliminated and retiming takes place by a clock pulse generated by multiplying the input clock. The streams are then output as data streams whose one bit width is arranged.

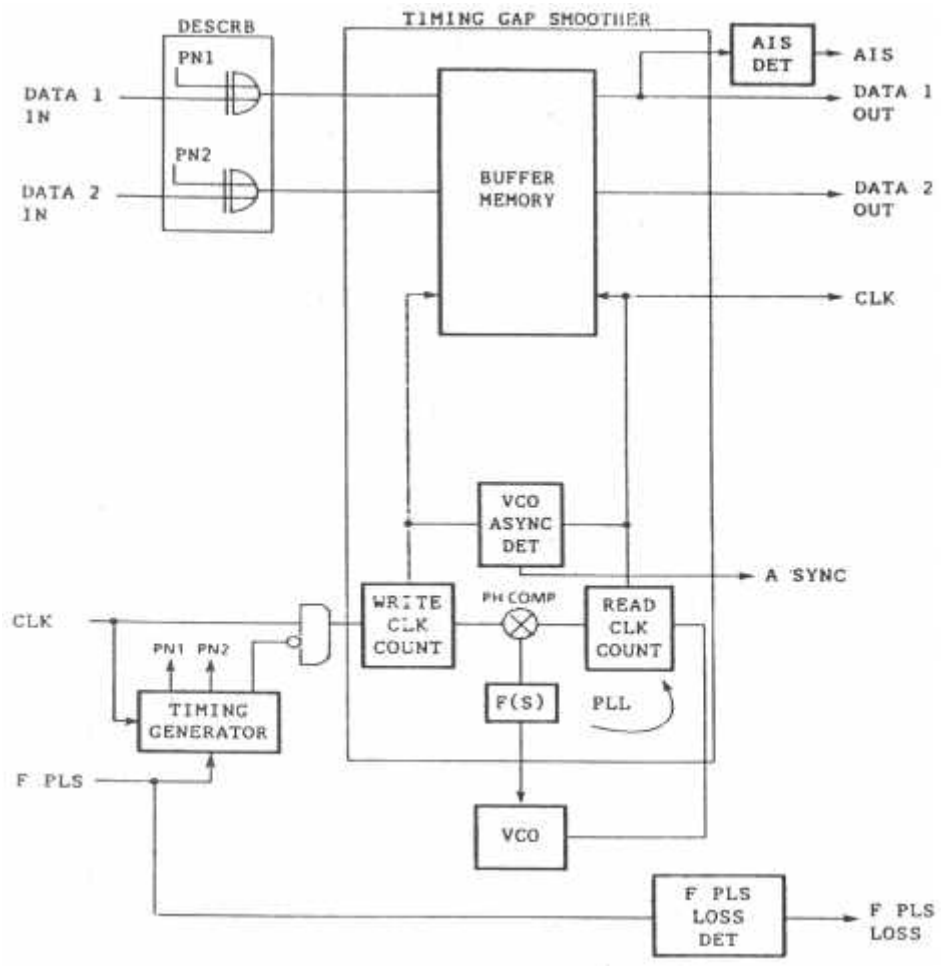


Figure 3.27 Block diagram of De-multiplexer in RX-DPU

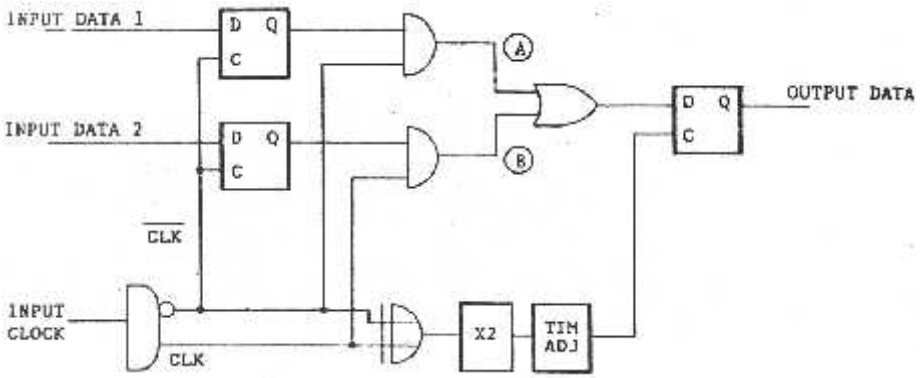


Figure 3.28 Parallel to serial converter

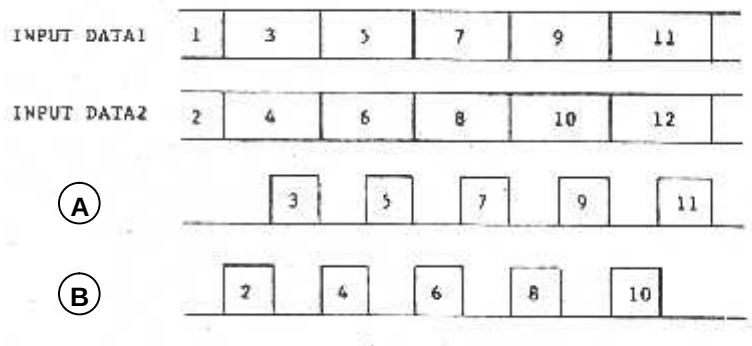


Figure 3.29 Odd & Even streams merging to get 34 Mbps data

Delay Adjuster: The block diagram of the delay adjuster is shown in figure 3.30. The input data shall be adjusted until the fixed delay matches 0 to 0.5 bits by means of timing adjustment (fine). Then, the data is adjusted until the fixed delay matches $\pm$ 2 bits by means of timing adjustment (Coarse).

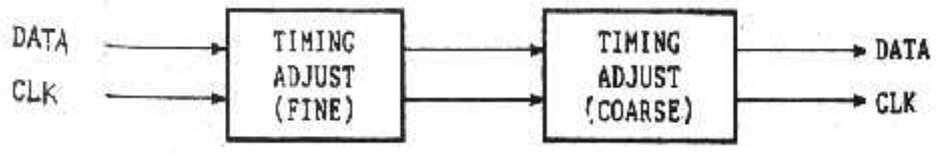


Figure 3.30 Block diagram of delay adjustor

Unipolar - HDB-3 Converter: The block diagram and timing chart of this function are shown in figures 3.31 and 3.32.

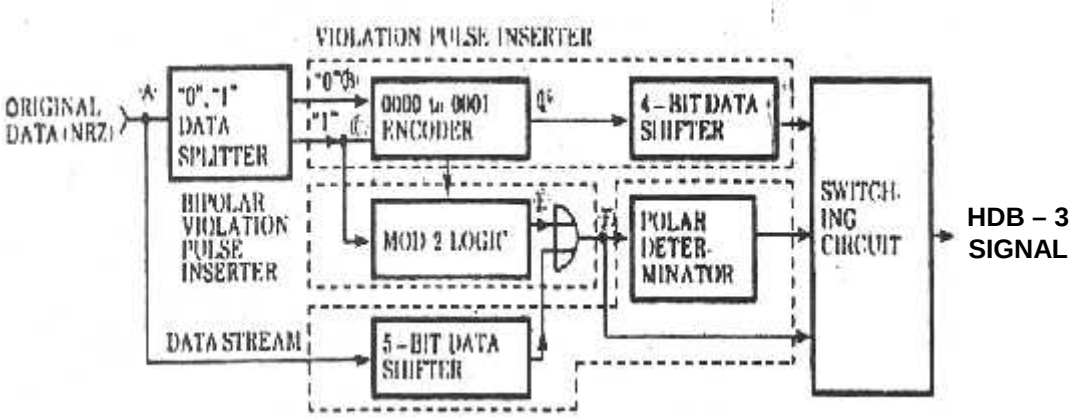


Figure 3.31Block diagram of Uni-polar to HDB3 converter

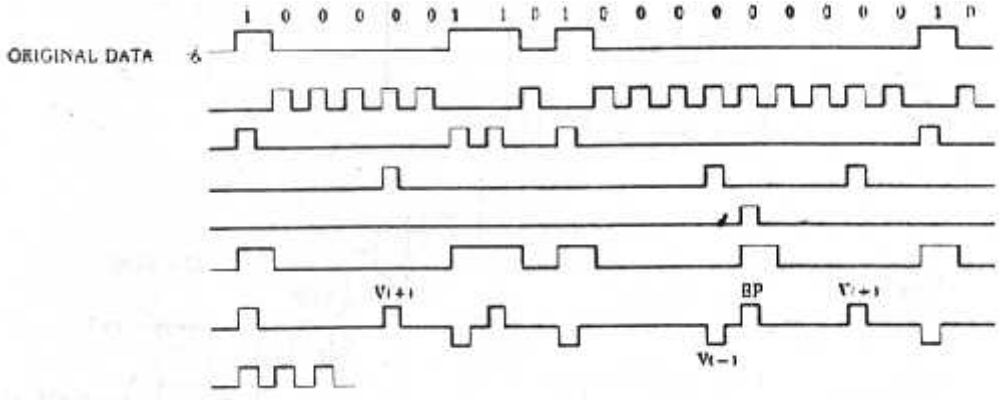


Figure 3.32 Waveforms associated with unipolar to HDB3 conversion

An input data stream with NRZ signal is fed to the data splitter circuit which divides the input data into the “0” position signal and the “1” position signal. The “0” position signal is applied to the “0000 to 0001” encoder which converts the 4-bit continuous input 0 (“0000”) sequence into “0001”. Part of the output encoded data is then applied as the reset input to the MOD 2 logic circuit where the split “1” position signal from the data splitter circuit is processed sequentially. The MOD 2 logic circuit detects whether the number of “1”s included in the violation pulse interval is odd or even. Here, when an even number is detected, the bipolar violation pulse is inserted.

On the other hand, the data stream is applied to the 5-bit shifter where insertion timing coincides with bipolar violation pulse, and thus the bipolar violation timing pulse is inserted into the main data signal. The output data from the “0000 to 0001” encoder is applied to the switching circuit through the 4-bit shifter, and is used as a trigger of the violation pulses.

The data stream of the main signal is also applied to the polar detection circuit as well as the switching circuit. The polar determinate circuit supplies the decided polar information of the main signal to the switching circuit. Thus, the unipolar data signal is converted to the HDB-3 data signal.

Alarm Control Circuit: The block diagram of the Alarm Control Circuit is shown in figure 3.33. OR LOGIC activates the RX DPU ALM from the input pulse cut-off, output pulse cut-off and clock Async detection. AIS SEND is activated by OR LOGIC of CONT signal (AIS CONT IN) from the outside and by the detection information from the demultiplexer. At the same time, it is also input to the unipolar/HDB-3 converter and sets the RX DPU output signals to all “1”. Also, when AIS OFF CONT signal is received from the outside, AIS SEND is inhibited.

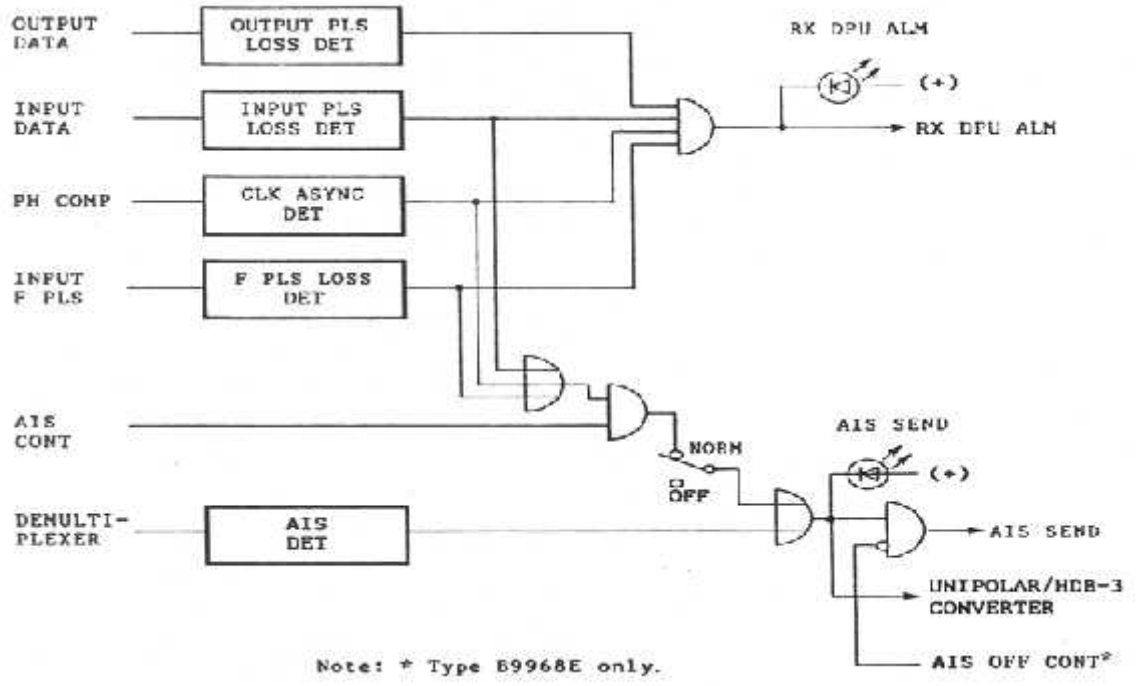


Figure 3.33 Block diagram of Alarm Circuit

3.7 Branching Circuit (BR CKT): The BR-7G-770B BR CKT has two applications according to the applicable system requirements as described below.

1+1 Hot standby System (C0130T) (Figure 3.34)

The transmitting signals from transmitters TX1 and TX2 enter the coaxial switch. Normally, the coaxial switch selects a transmitting signal from TX1 (regular channel) and terminates signal from TX2 (protection channel). A control signal (+9V) from the TR equipment passes through relay contact on the RELAY BOARD and is applied to the coaxial switch, and when the control signal reverses absolutely the polarity with relay contact, the coaxial switch

selects then a transmitting signal from TX2. The transmitting signal is sent to a band pass filter (TX BPF) which is tuned to the respective transmitting frequency and suppresses the undesired components of the signal. The signal is then passed to the duplexer and sent to the antenna through the wave-guide. If the power supply (+5 V) for the RELAY BOARD interrupts, the relay on the RELAY BOARD is released and the coaxial switch selects the transmitting signal from TX1.

The received signal from the antenna enters the RX BPF through the duplexer and isolator. The band pass filter of the RX BPF, tuned to f1', selects the desired input frequency and rejects undesired input frequencies. The received signal F1' selected at the RX BPF is sent to the hybrid which delivers the signal to the RX1 (regular channel) and to the RX2 (protection channel).

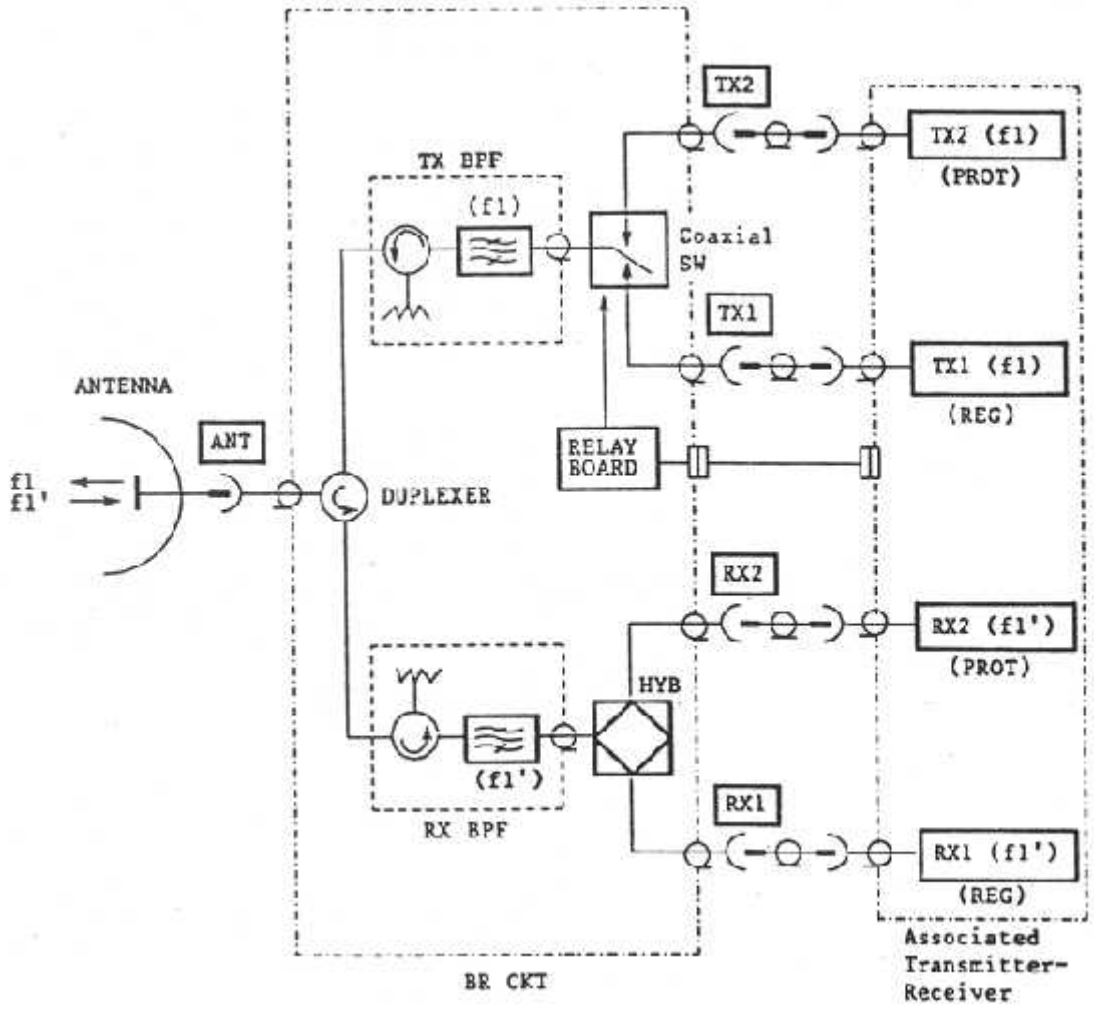


Figure 3.34 1+1 hot standby without diversity

1+1 Hot standby with Space Diversity System (C0168S) (Figure 3.35)

The transmitting signals from transmitters TX1 and TX2 enter the coaxial switch. Normally, the coaxial switch selects a transmitting signal from TX1 (regular channel) and terminates signal from TX2 (protection channel). A control signal (+9 V) from the TR equipment passes through relay contact on the RELAY BOARD and is applied to the coaxial switch, and when the control signal reverses absolutely the polarity with relay contact, the coaxial switch selects then a transmitting signal from TX2. The transmitting signal is sent to a band pass

filter (TX BPF), which is tuned to the respective transmitting frequency and suppresses the undesired components of the signal. The signal is then passed to the duplexer and sent to the antenna through the wave-guide. If the power supply (+5-V) for the RELAY BOARD interrupts, the relay on the RELAY BOARD is released and the coaxial switch selects the transmitting signal from TX1.

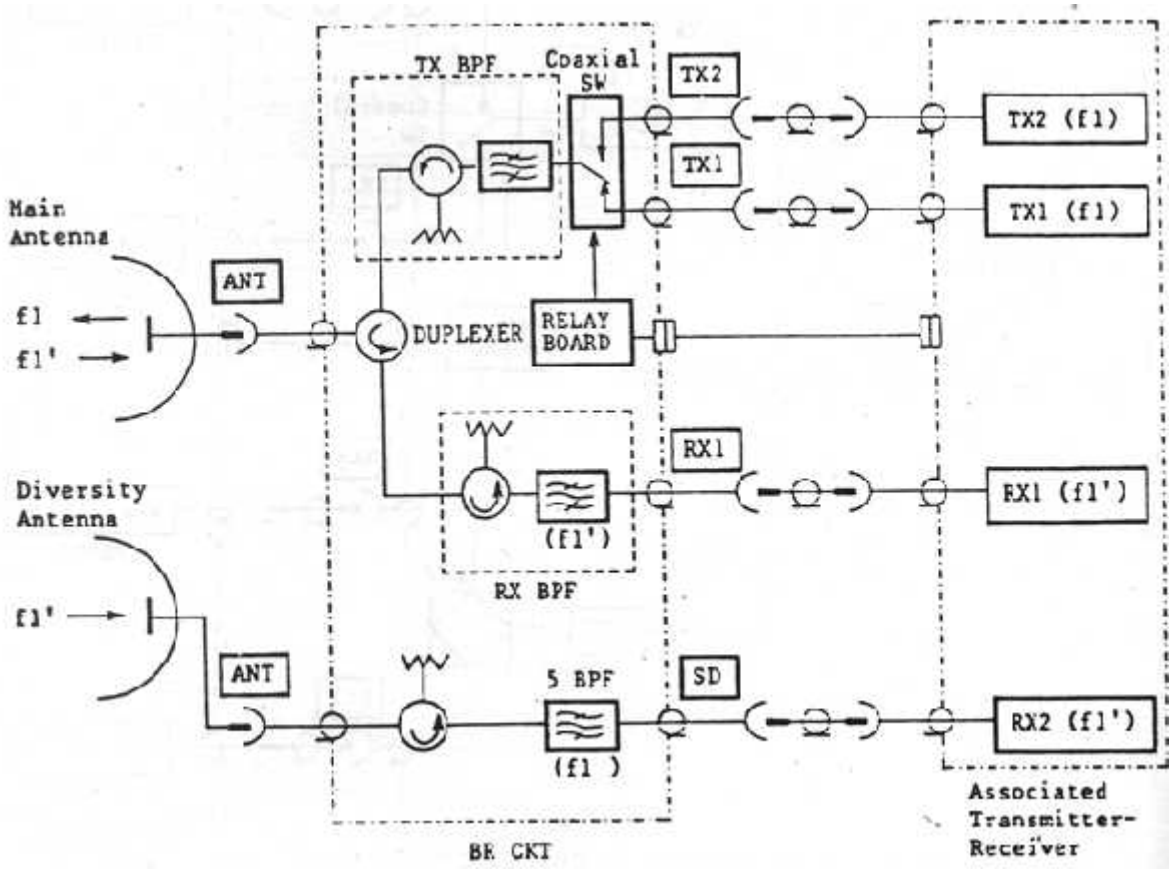


Figure 3.35 1+1 Hot-standby with Space Diversity

The received signal from the MAIN antenna enters the RX BPF through the duplexer and isolator. The band pass filter of the RX BPF, tuned to f1', selects the desired input frequency and rejects undesired input frequencies. The received signal f1' selected at the RX BPF is sent to the MAIN RX. The received signal from the SD antenna enters the 5 BPF through the isolator. The 5BPF, tuned to f1', selects the desired input frequency and rejects undesired input frequencies f1'. The signal passes through the 5 BPF is sent to the SD RX.

3.8 Digital Service Channel Interface (OPTIONAL) (Figure 3.36 & 37)

Transmission of the digital service channel is available by Digital Service Channel Interface (DSC INTFC) equipped in ZXP-WS/DSC-770 WS/DSC interface equipment. A DSC INTFC can transmit up to 4 channels of 72 Kb/s data signals.

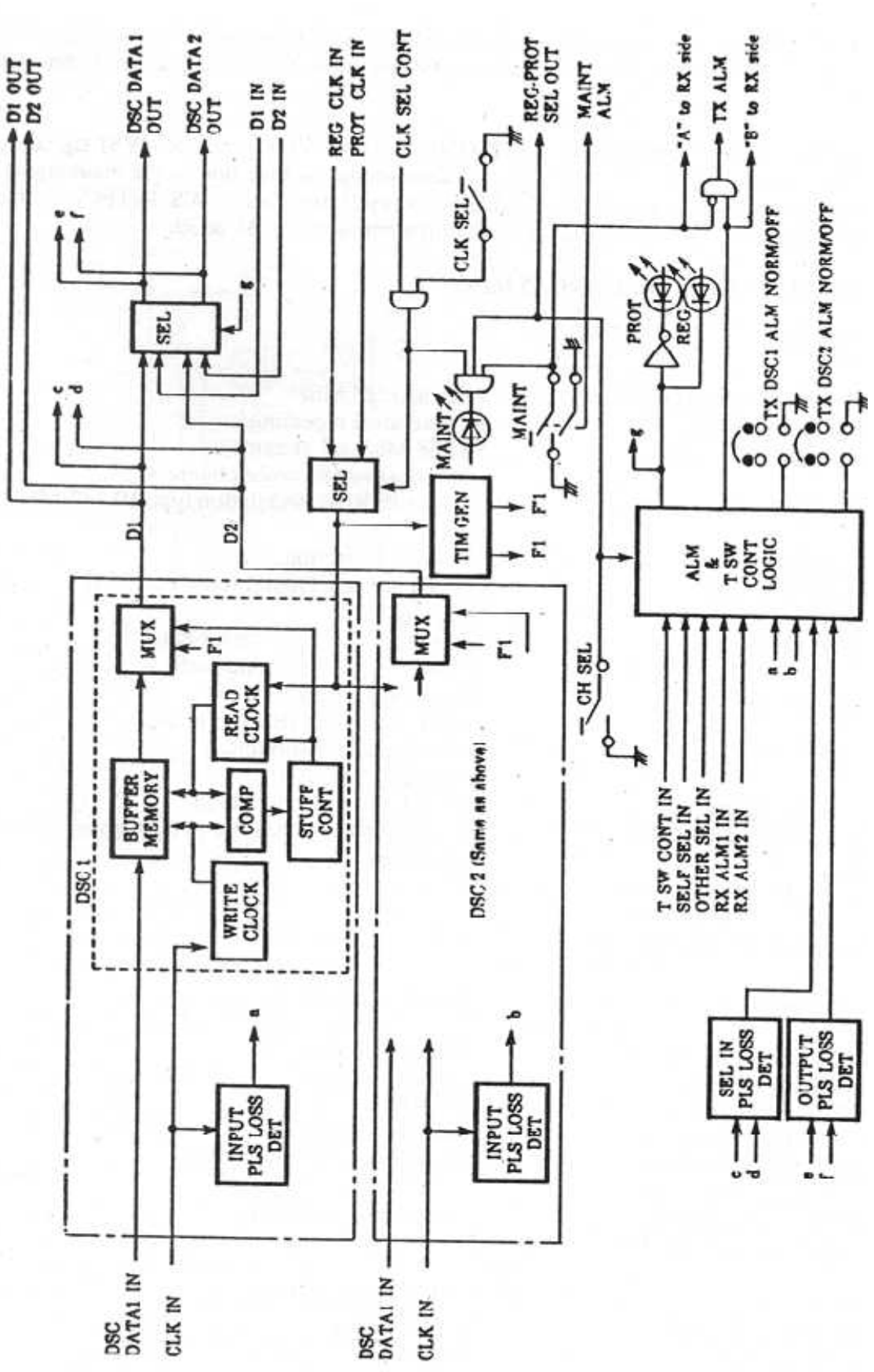


Figure 3.36 Block diagram of showing DSC Integration

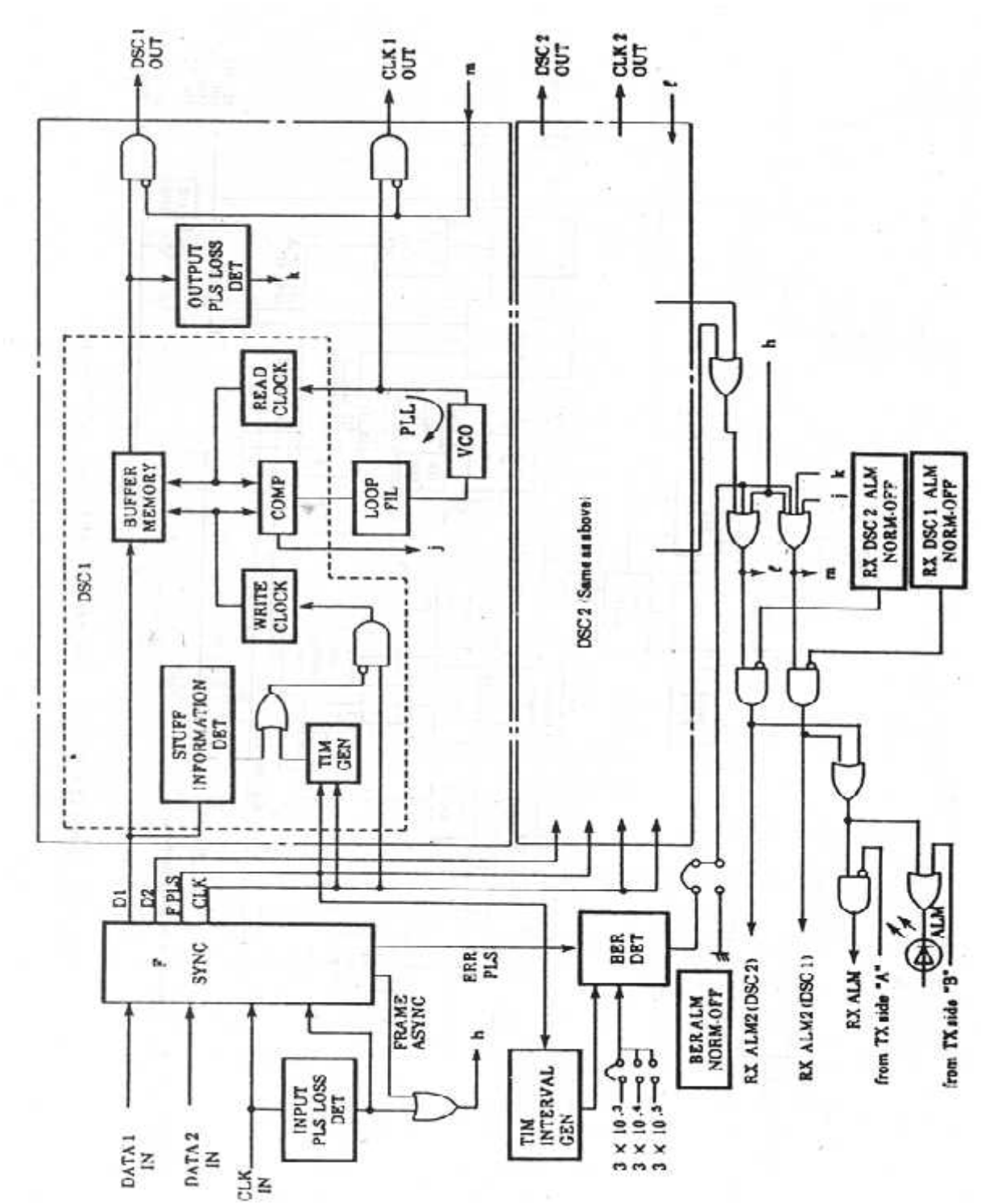


Figure 3.37 Block diagram showing DSC segregation

3.9 Wayside Signal Transmission (OPTIONAL) (Figure 3.38 & 3.39)

A 2.048 Mb/s. wayside (WS) signal equivalent to 30 telephone channels can be transmitted through the bit insertion to the main signal. Drop and insertion of wayside signal is available by wayside interface (WS INTFC) Unit equipped in ZXP-WS/DSC-770 WS/DSC Interface Equipment.

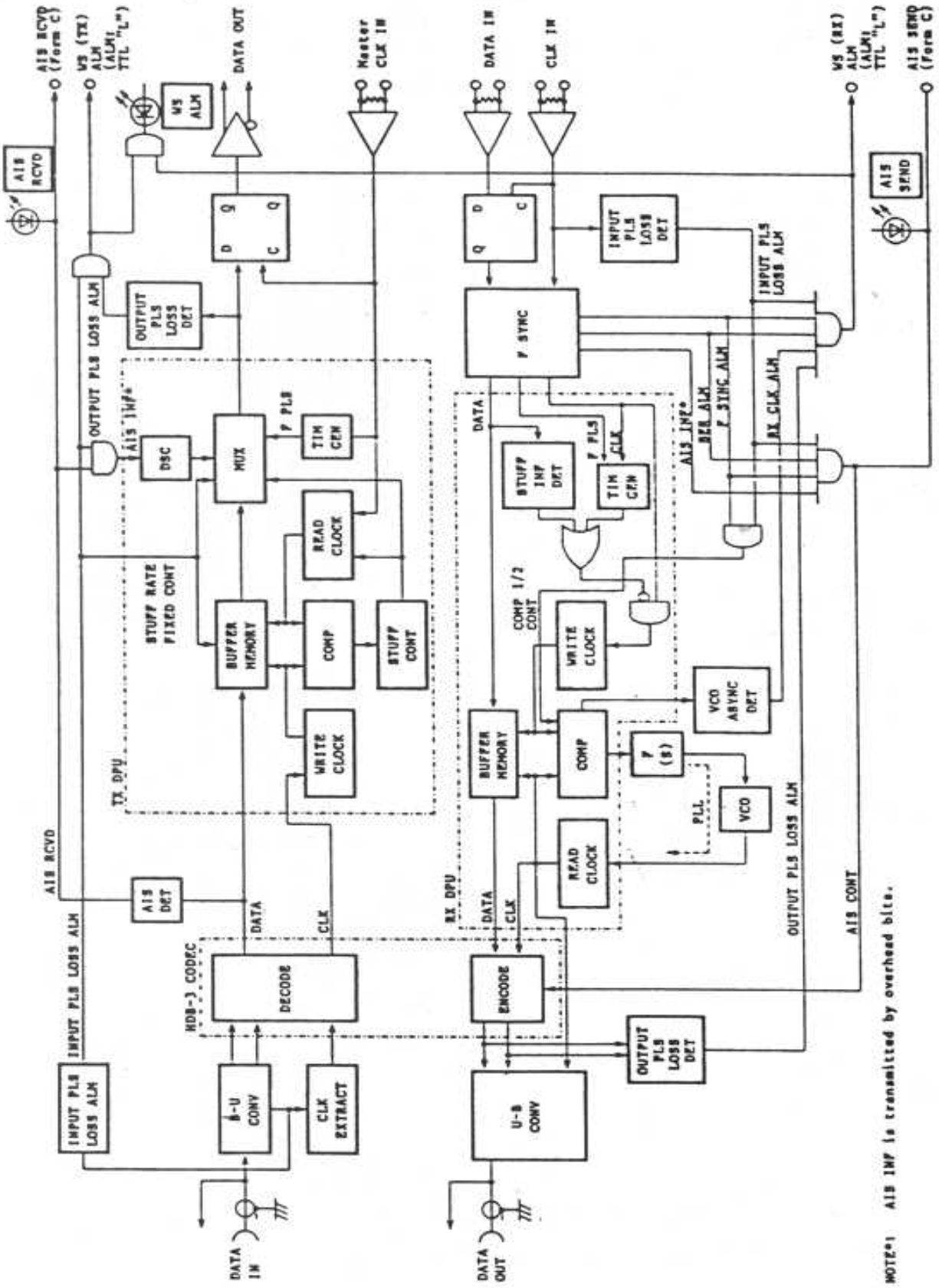


Figure 3.38 Block diagram showing WS Interface

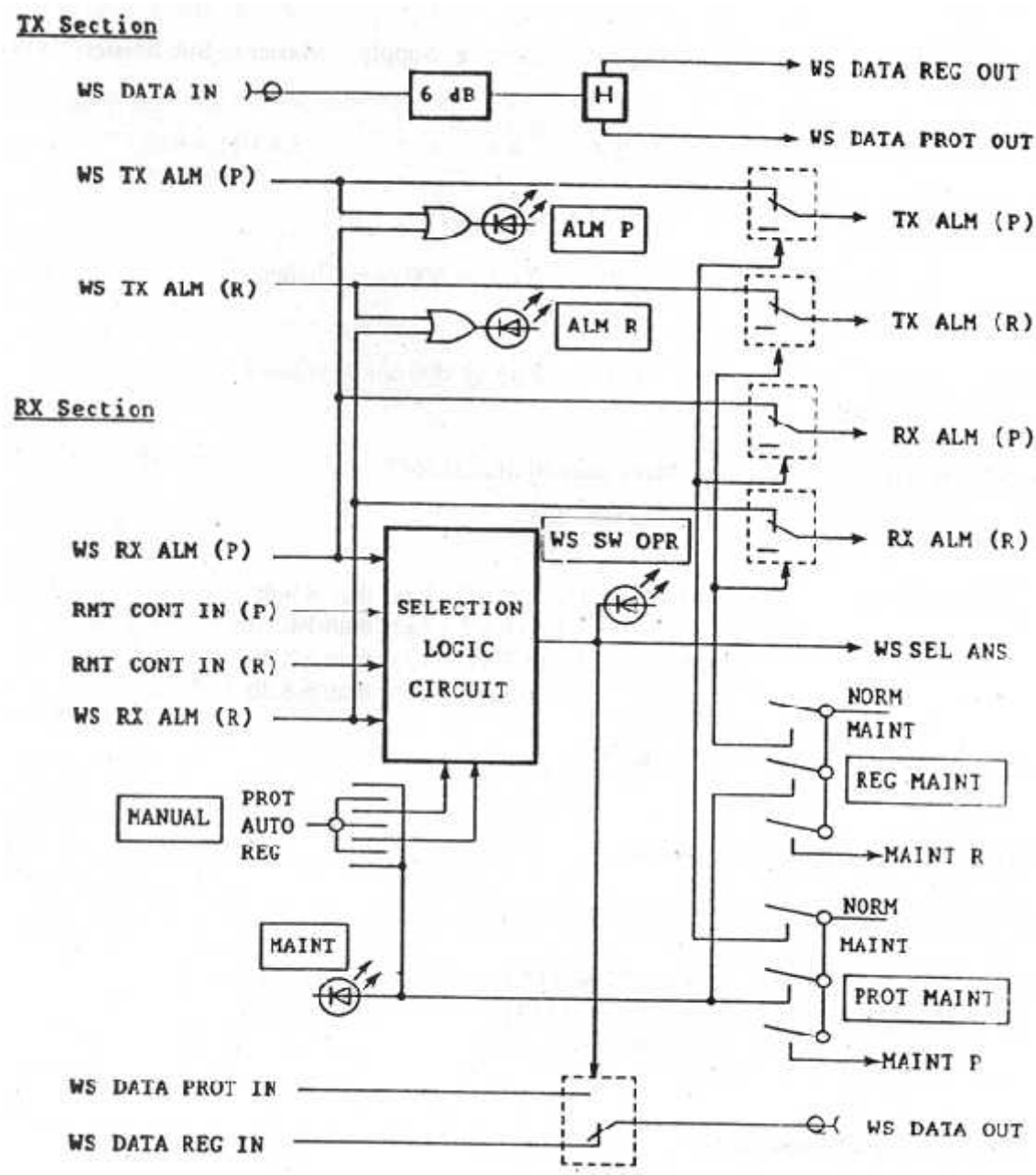


Figure 3.39 Alarm function on WS Interface Module

3.10 PERFORMANCE SPECIFICATIONS

GENERAL

1. Operation Frequency Band	: 7125 to 7725 MHz
2 Repeating Type	: Regenerative repeating
3. Transmission capacity	: 34.368 Mb/s x 1 stream (Equivalent to 480 voice channels)
4. Modulation	: 4-phase PSK IF modulation type 19.332 Mb/s rate
5. Demodulation	: Coherent Detection.
6. Service Channel	: Analogue (standard), Digital (Optional) (ZXP-WS/DSC-770)
7. Service Channels	: Analog 3 CH (0.3 to 12 KHz) Digital 4CH (As optional)

8. Type of switch : Relay switching (RF), Hitless switching (Bit combiner)
9. Wayside signal : 2.048 Mb/s. X 1 (optional), (ZXP-WS/DSC-770)
10. Power Source : - 48V DC (- 36 to - 75V.DC)
11. Power Consumption : Approx. 144W (1+ 1 system)
12. Ambient temperature : 0^0C to +50^0C.

Transmitter - Receiver

1. TX output power : +30 dBm + 1.0 dB
   - 1.5 dB.
2. TX frequency stability : Within $\pm$ 20 ppm
3. RX noise figure : Less than 4.0 dB
4. RX IF frequency : 70 MHz
5. RX AGC range : More than 50 dB
6. RX Level to the bit Error rate of 1 X 10^{-6} : Lower than -79.5 dBm.
7. RX Level to the bit Error rate of 1 X 10^{-3} : Lower than - 83.5 dBm.

Size of Rack : {2100 x 2400 x 250} mm
TX - RX. Freq. difference : 151.614 MHz
Adjacent Channel. Freq. difference : 34 MHz

Input/ Output Data Interface (Main Signal)

1. Line code : HDB-3 (high density bi polar -3)
2. Line bit rate : 34.368 Mb/s $\pm$ 20 ppm
3. Signal level : CCITT Rec.G703, 1.0 V_O - p
4. Impedance : 75 ohms. Unbalanced

Analog Service Channel : Omnibus OW 0.3 - 3.4 | Remote supply. 4.3 - 7.4 | Master to Sub Master 8.4 - 11.4 KHz.

1. Frequency band : 0.3 to 12 KHz (3 CH)
2. Signal input level (from SC RS Unit) : - 30 dBm $\pm$ 2 dB @ 600 ohms balanced
3. Signal output level (To SC RS Unit) : - 20 dBm $\pm$ 2 dB @ 600 ohms balanced.
4. S/N (Weighted) : > 50 dB/CH for 1

Branching Circuit

1. Insertion loss : HS/HS Type TX to RX1 : Less than 8.9dB
   TX to RX2 : Less than 14.3 dB
   : HS/SD Type TX to RX1 : Less than 6.8 dB
   TX to RX2 : Less than 6.8 dB
2. Output flange at antenna port : IEC PDR70

Digital Service Channel (Optional)

(Interface to/from SC REP D2 and/or SV REP D2)

1. Bit rate : 89.5 Kb/s ± 50 PPM per CH (Up to 4 CH)
2. Input/Output level : 2 Vp-p nominal (TTL)
3. Impedance : 130 Ohms balanced.
4. Line Code : NRZ

Wayside Signal (Optional)

1. Line Code : HDB-3/NRZ
2. Line Bit Rate : 2.4165 Mb/2 ± 50 PPM
3. Signal Level : CCITT Rec. G703, $2.37V_{0\text{-}P}$
4. Impedance : 130 Ohms balanced

3.11 NETWORK MANAGEMENT SYSTEM (NMS)

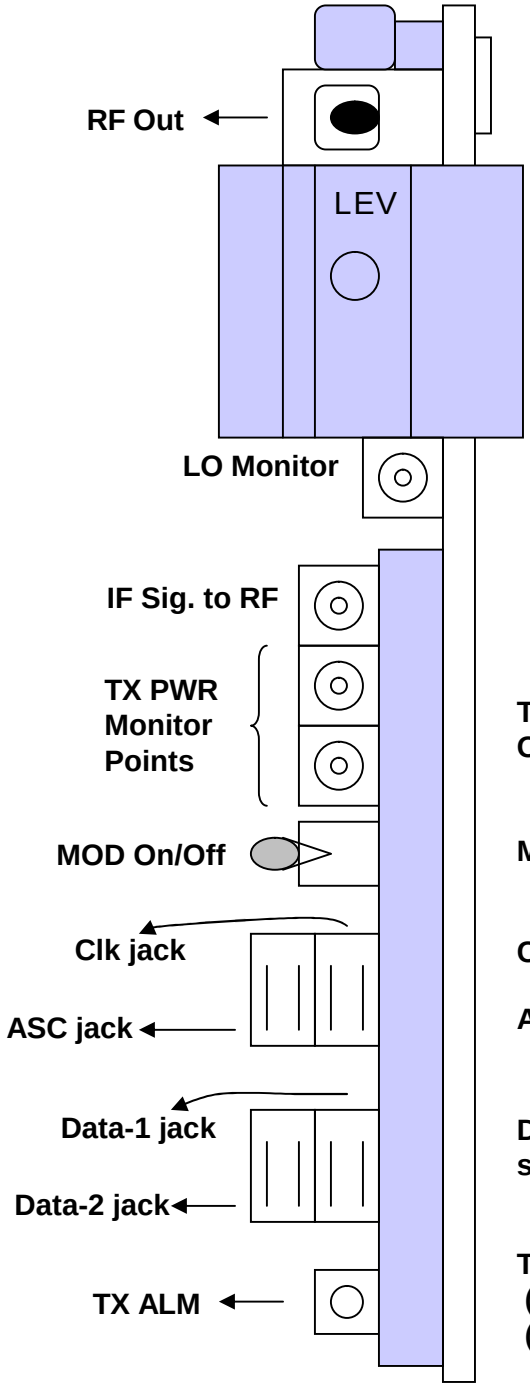
A network management system is a computer based control system which can supervise, monitor, maintain and control the performance of a given network, on-line, in real time, from one or more network control centres.

The master station controls all the remote stations and is equipped with PC-AT based computer system. The host computer communicates with the NSV interface card in the NSV 700 series supervisory master unit (SV - MS) through RS232C link at 9600 baud using high level data link control (HDLC) protocol. HDLC is a synchronous protocol. Hence a synchronous communication controller card is plugged in one of the slots of the PC-AT machine. The synchronous controller card has two ports one with 9 pins and the other with 25 pins. 9-pin port is used for the diagnostics of the card. 25 pin port is used for communication with the NSV Interface module.

The tek emulation terminal is connected to the computer through RS232 link at 9600 baud, which is used as man machine interface and displays the entire data pertaining to the network. A printer is also connected to the computer for data logging purposes, using electronics parallel interface.

DMW Radio Equipment Alarms
&
Troubleshooting

TX Module



LEV Control enables adjustment of RF Output Power

TX PWR Monitor points enable monitoring of TX Power Output (calibrated to dc voltage 1 V to 2.5 V)

MOD On/Off switch allows/disallows modulation

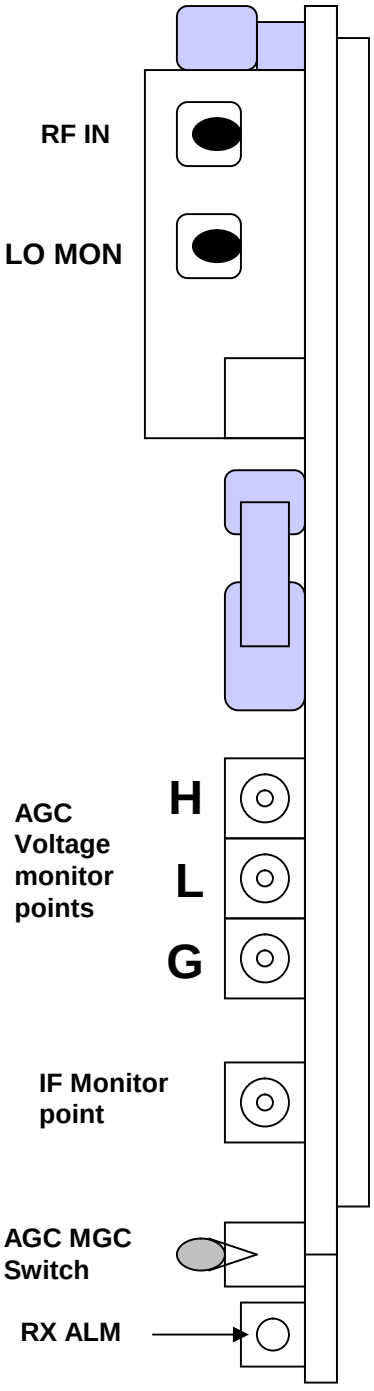
Clk. Jack enables monitoring of clock input signal

ASC Jack enables monitoring of ASC input signal

Data-1 & 2 jacks enable monitoring of odd / even streams at the input of TX Module

TX ALM indicator lights red when
(a) TX output power drops more than 3 dB below normal
(b) 19.332 Mbps data inputs lost

RX Module



AGC Voltage monitor points HG used to monitor high-level signal -30 to -70 dBm

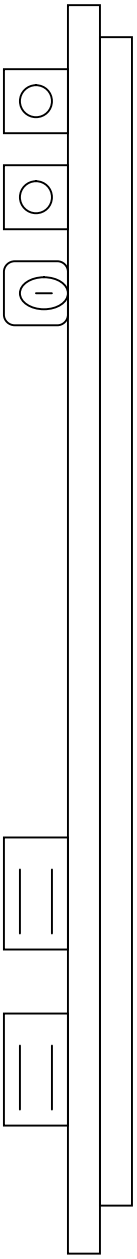
LG points used to monitor low-level signal -70 to -90 dBm

AGC-MGC switch controls AGC bias circuit. The switch in AGC position forms AGC loop. The switch in MGC position disconnects AGC loop.

RX ALM indicator lights red when –

- **RX RF input level drops below pre-determined level**
- **RX IF module output signal is lost**

TX DPU Module



TX-DPU ALM — **TX-DPU ALM indicator lights red when output pulse of TX-DPU is lost or input clock of TX-DPU is lost or clock synchronization is lost**

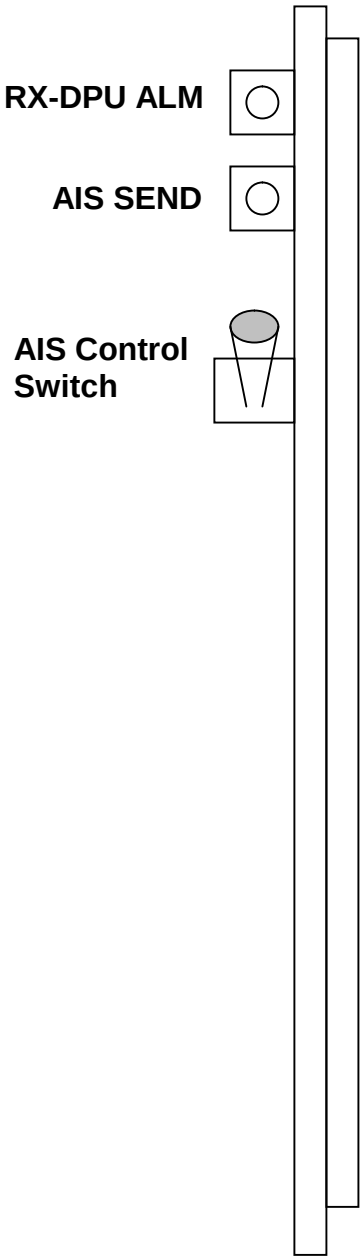
AIS RCVD — **AIS RCVD lights amber when input signal from MUX is 'all 1 s' bit stream**

ID Code Selection — **ID code selection switch selects frame pattern for channel identification. (To set as same at TX & RX)**

-6 dB Plug — **Close –6 db plug when SWO module is not provided. Also, while doing BER measurements with Test sequence, close this plug or else SWO will do**

NORM Plug — **Close NORM plug when SWO module is provided**

RX DPU Module



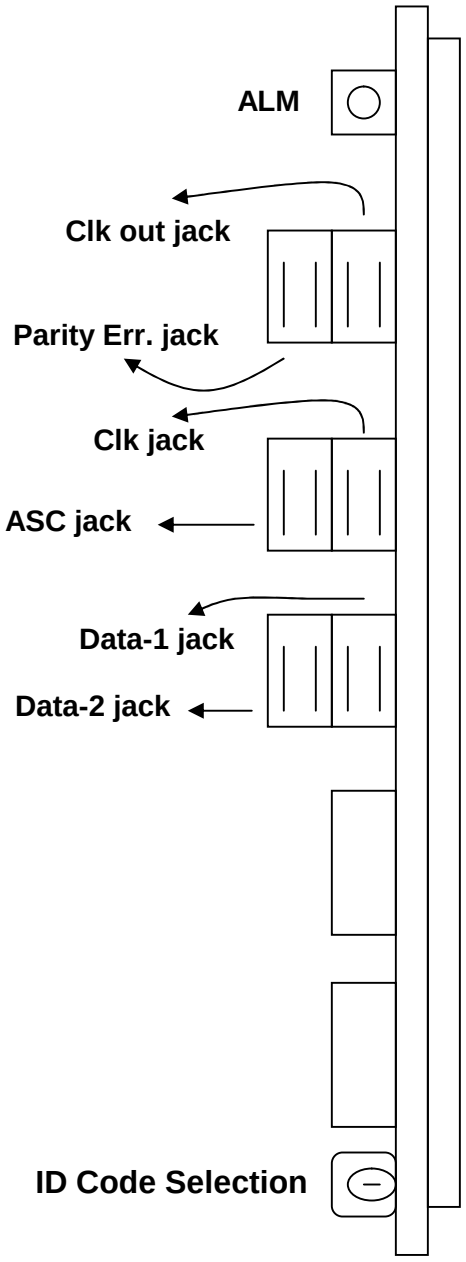
RX-DPU ALM indicator lights red when input or output pulse of RX-DPU is lost or clock synchronization is lost

AIS SEND indicator lights amber when –

- **Input signal from MUX is 'all 1 s' bit stream**
- **Failure of radio equipment**
- **Frame synchronization is lost**
- **BER is worse than 1X 10^{-4}**
- **ID code not coinciding**
- **Clock synchronization is lost**

AIS control switch is normally set to NORM position. It is set to OFF position when BER measurement is carried out

PH DEM Module



ALM indicator lights red when –

- **Output of PH-DEM is lost**
- **Frame sync. is lost**
- **Carrier sync. is lost**
- **BER worse than $1X10^{-4}$**

Clk. Jack enables monitoring of clock output signal

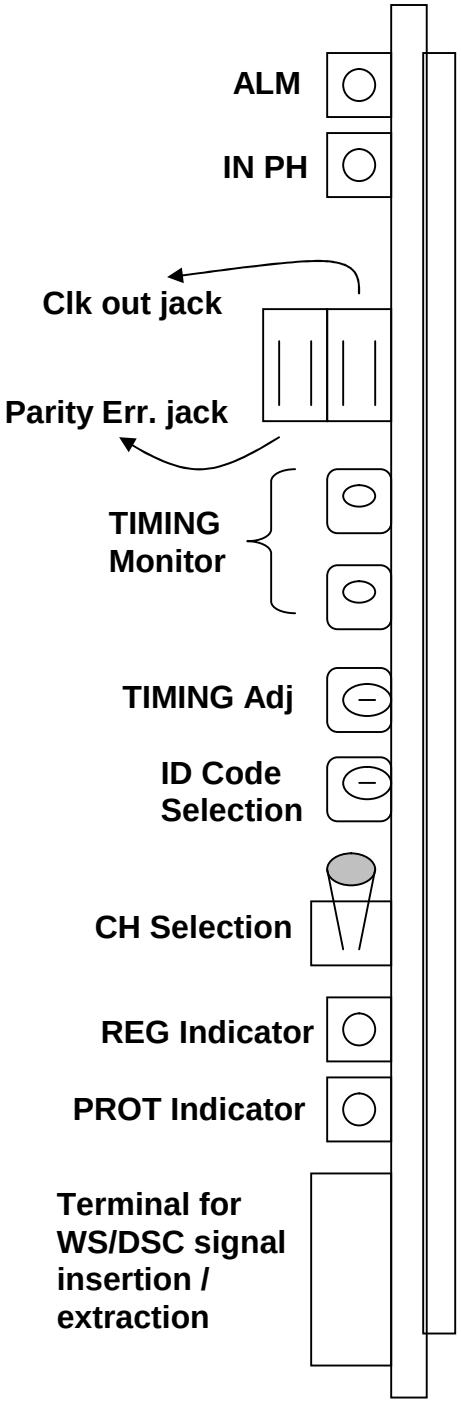
Parity Err. Jack together with Clk-out jack enables monitoring of parity error

Clk. Jack enables monitoring of clock output signal

ASC Jack enables monitoring of ASC output signal

Data-1 & 2 jacks enable monitoring of odd / even streams at the output of PH-DEM

BIT Combiner Module



ALM indicator lights red when
- **(a) Output pulse of BIT-COMB is lost**
- **(b) Frame sync is lost**
- **(c) BER is worse than $1X10^{-4}$**

IN PH indicator lights green when timing difference

Parity Err. Jack together with Clk-out jack enables monitoring of parity error

TIMING Monitor: Monitoring point for clock signal

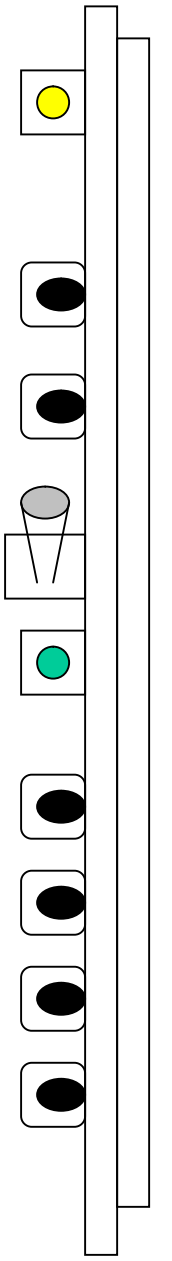
TIMING Adj: Control to adjust timing difference between REG & PROT

CH Sel. Switch: 3 position switch REG/AUTO/PROT

REG Indicator: Lights green when REG is chosen

PROT Indicator: Lights green when PROT is chosen

SWO Module



Manual indicator: Yellow indication when MANUAL switch is set to REG or PROT position

Data-in port: 34 Mbps data-in (main traffic) through push-type connector & coaxial cable

Data-out port: 34 Mbps data-out (main traffic) through push-type connector & coaxial cable

MANUAL Switch: 3-Position switch to select REG / PROT / AUTO

SW OPR Indicator: Lights green when Receive signal is chosen from PROT channel

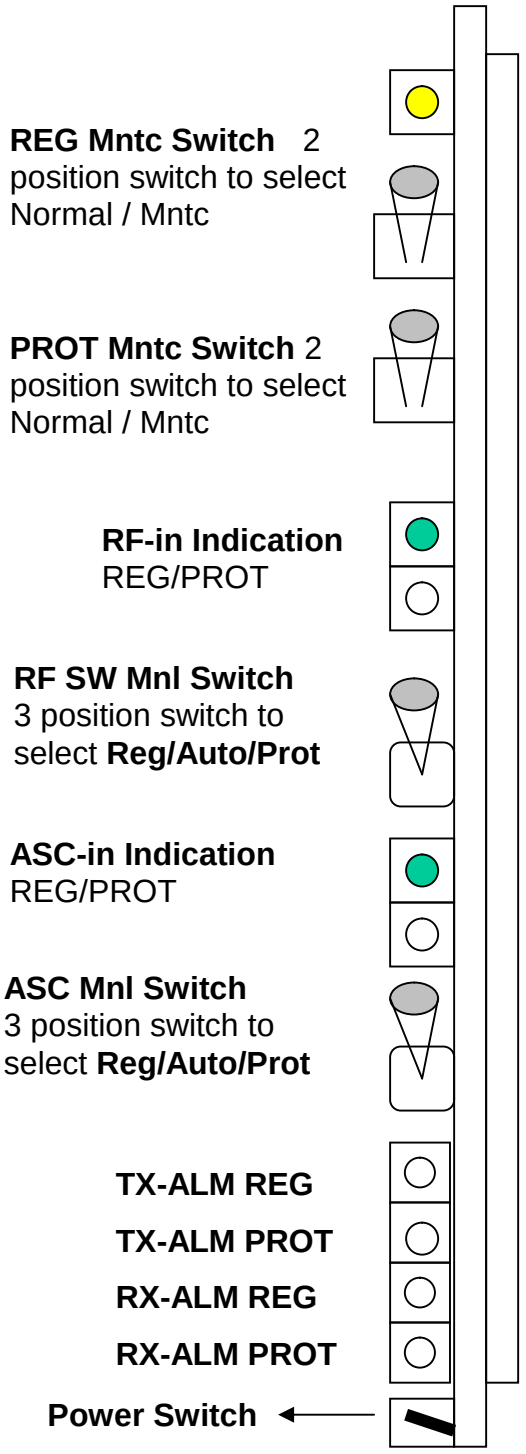
REG Data-in port: To send incoming data to TX-DPU of REG

PROT Data-in port: To send incoming data to TX-DPU of PROT

REG Data-out port: Takes data from RX-DPU of REG

PROT Data-in port: Takes data from RX-DPU of PROT

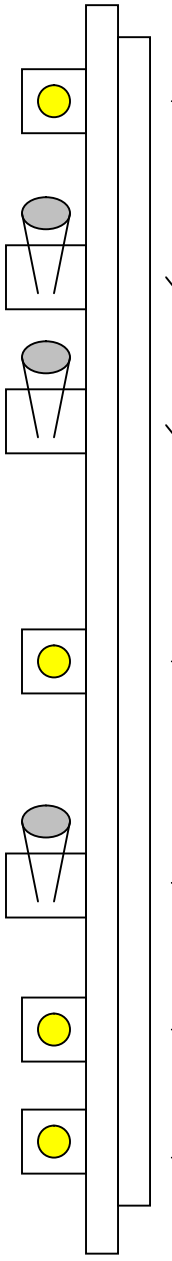
SWO Control Module



Mntc. indicator: Yellow indication when -

- REG Mntc switch is set to Mntc. Position or
- PROT Mntc switch is set to Mntc. Position
- ASC MNL switch is set to REG or PROT position
- RF SW MNL switch is set to REG or PROT position
- Mntc signal is applied from any of RX-DPU, Bit combiner, TX, RX or SWO module

WS SWO Module



Maintenance Indicator: Lights yellow when-

- REG Mntc or PROT Mntc switch is set to maintenance position

REG Mntc. Switch: 2 position switch for WS-REG path - NORM for normal working and MNTC for maintenance mode

PROT Mntc. Switch: 2 position switch for WS-PROT path NORM for normal working and MNTC for maintenance mode

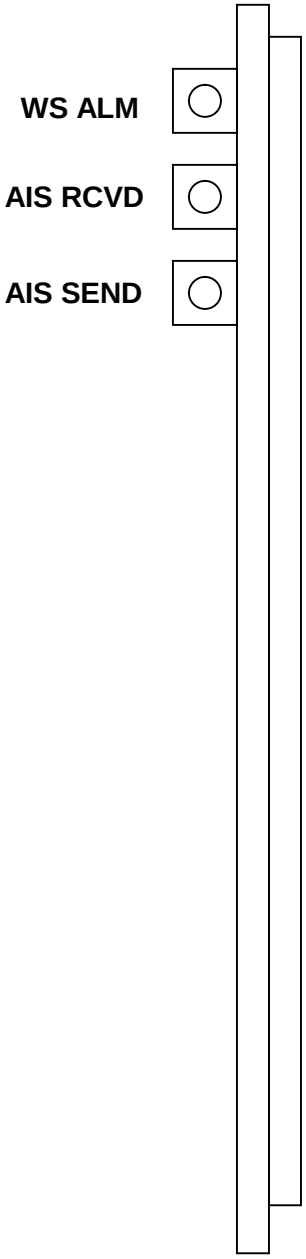
WS SWO OPR: Lights yellow when WS reception is from PROT

MANUAL Switch: 3 position switch REG/AUTO/PROT

ALARM Indication for REG: Lights red in case of TX alarm issued or RX alarm received on WS REG

ALARM Indication for PROT: Lights red in case of TX alarm issued or RX alarm received on WS PROT

WS INTFC Module



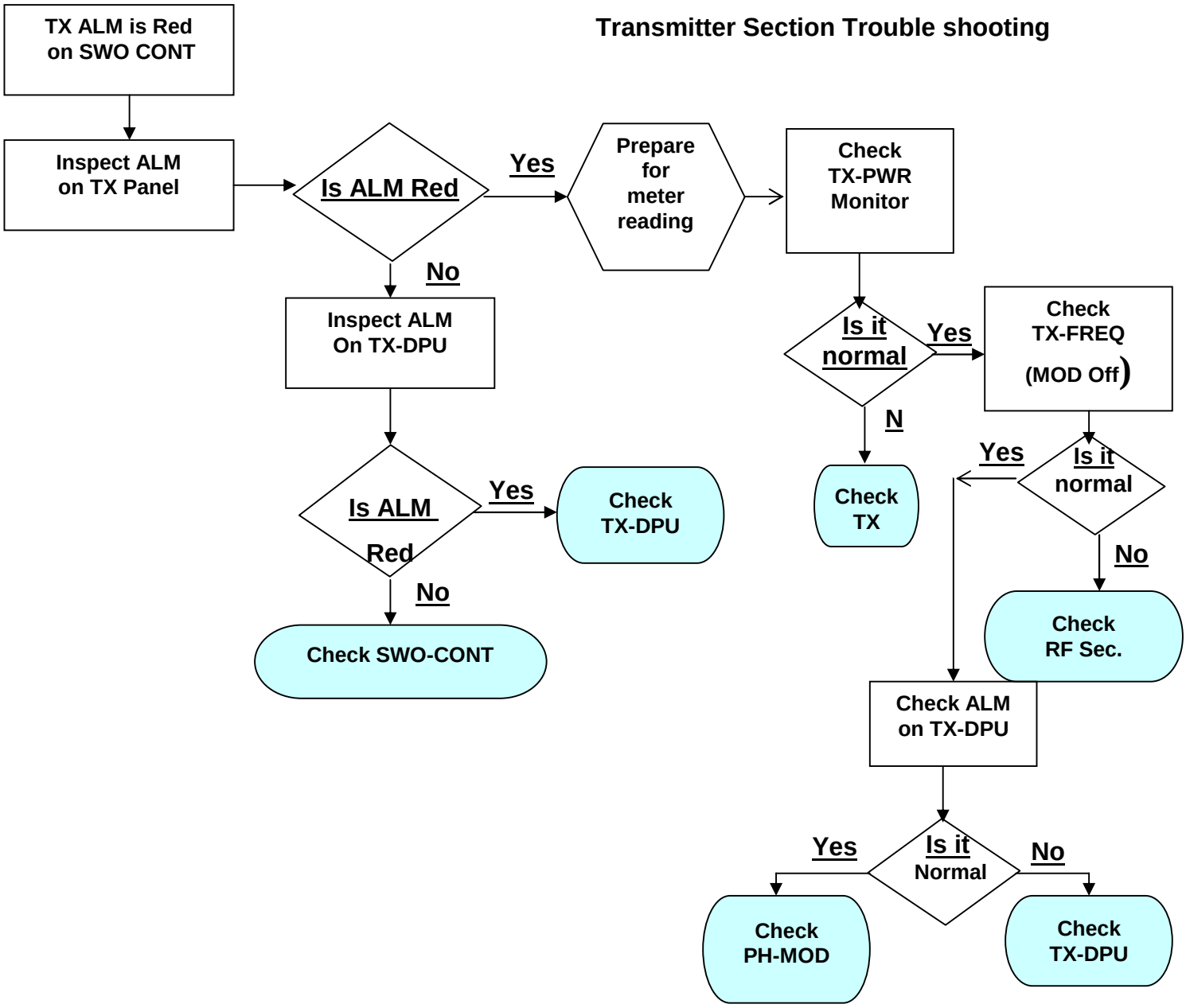
WS ALM indicator lights red when-

- **WS - TX Data input is lost**
- **WS- TX Data output is lost**
- **WS- Clock input is lost**
- **WS- Clock output is lost**
- **Frame Sync. Is lost**
- **BER is worse than 1 X 10^{-5}**

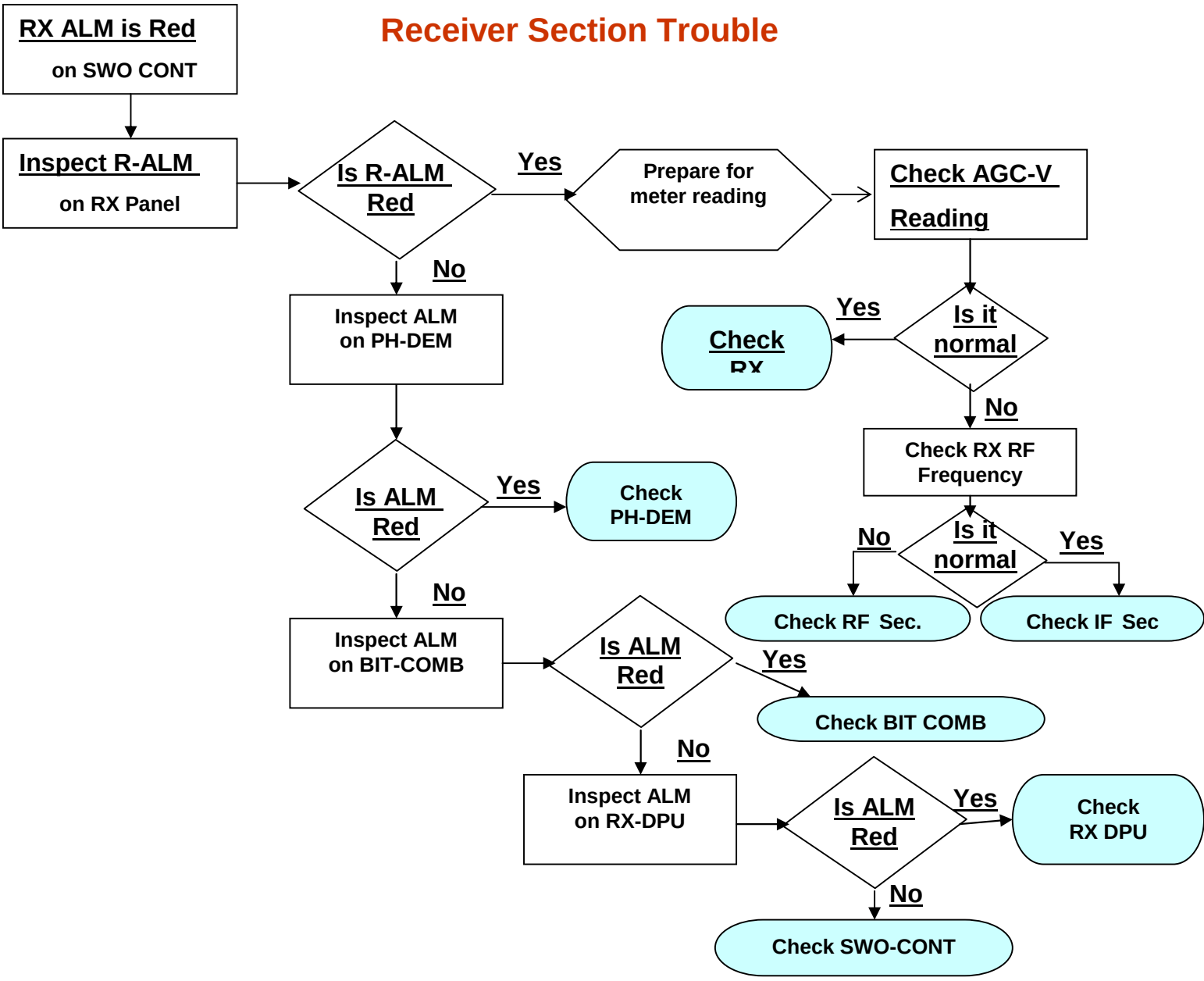
AIS RCVD lights amber when input signal from DI-MUX is ‘all 1 s’ bit stream

AIS SEND lights amber when output signal sent to DI-MUX is ‘all 1 s’ bit stream

Transmitter Section Trouble shooting

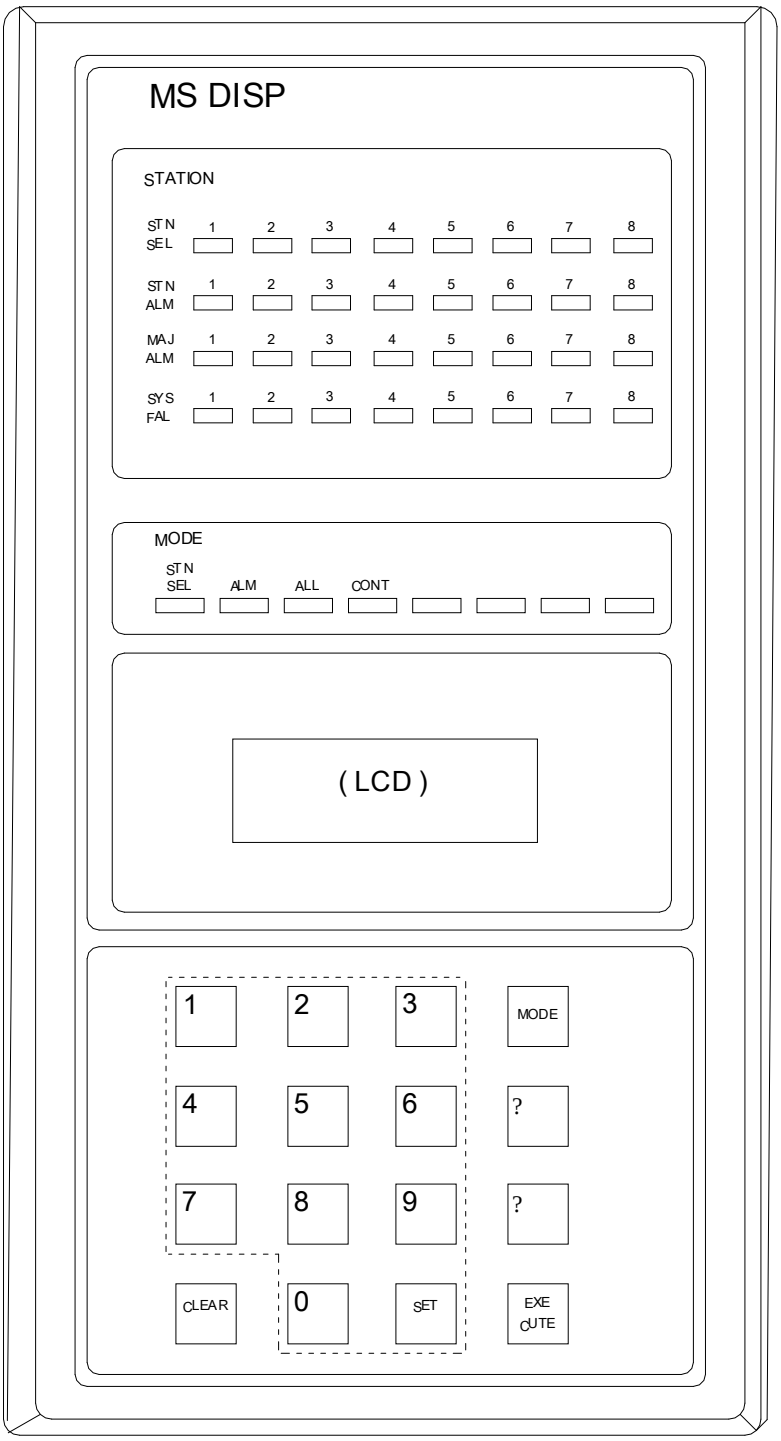


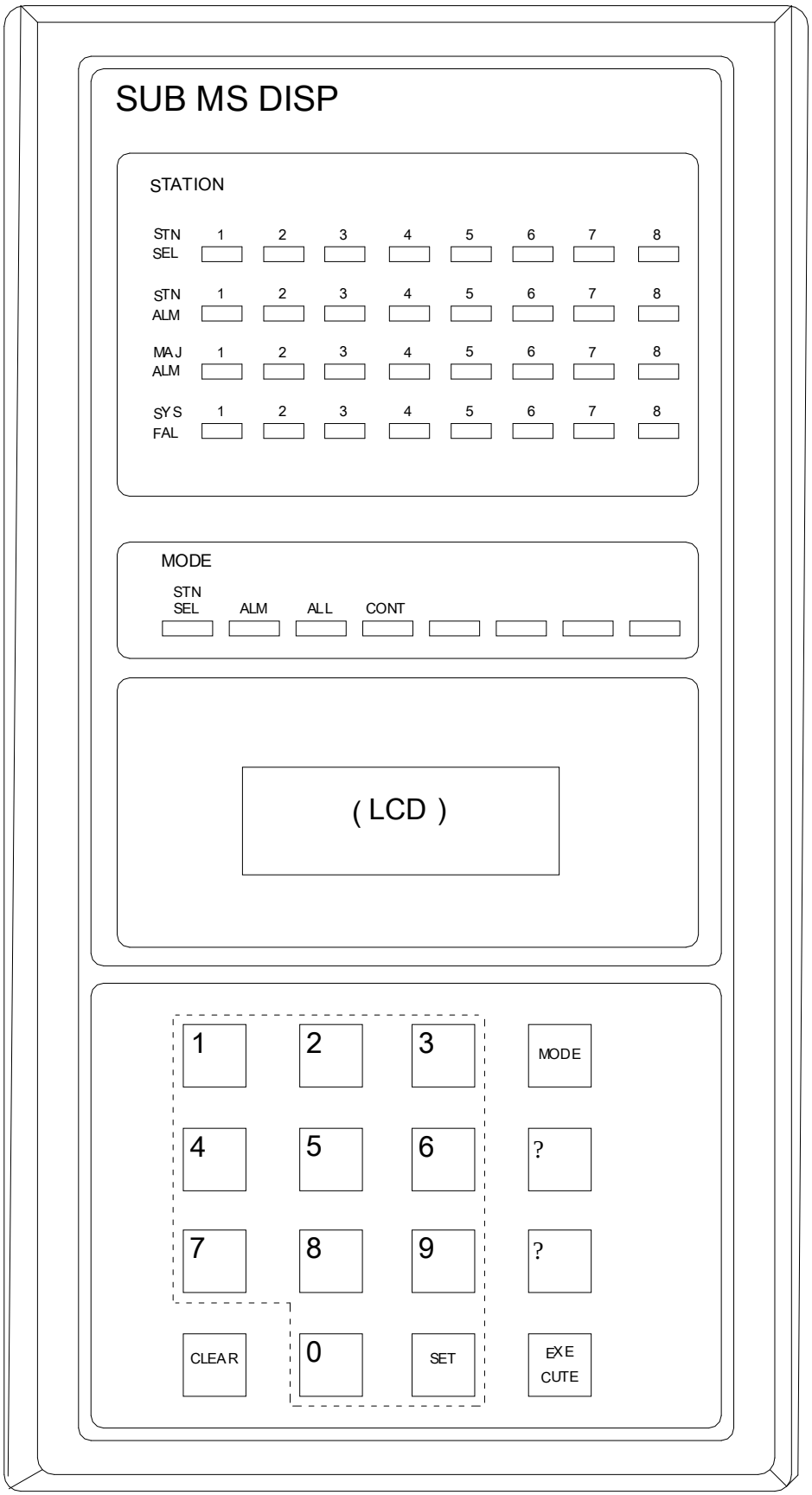
Receiver Section Trouble

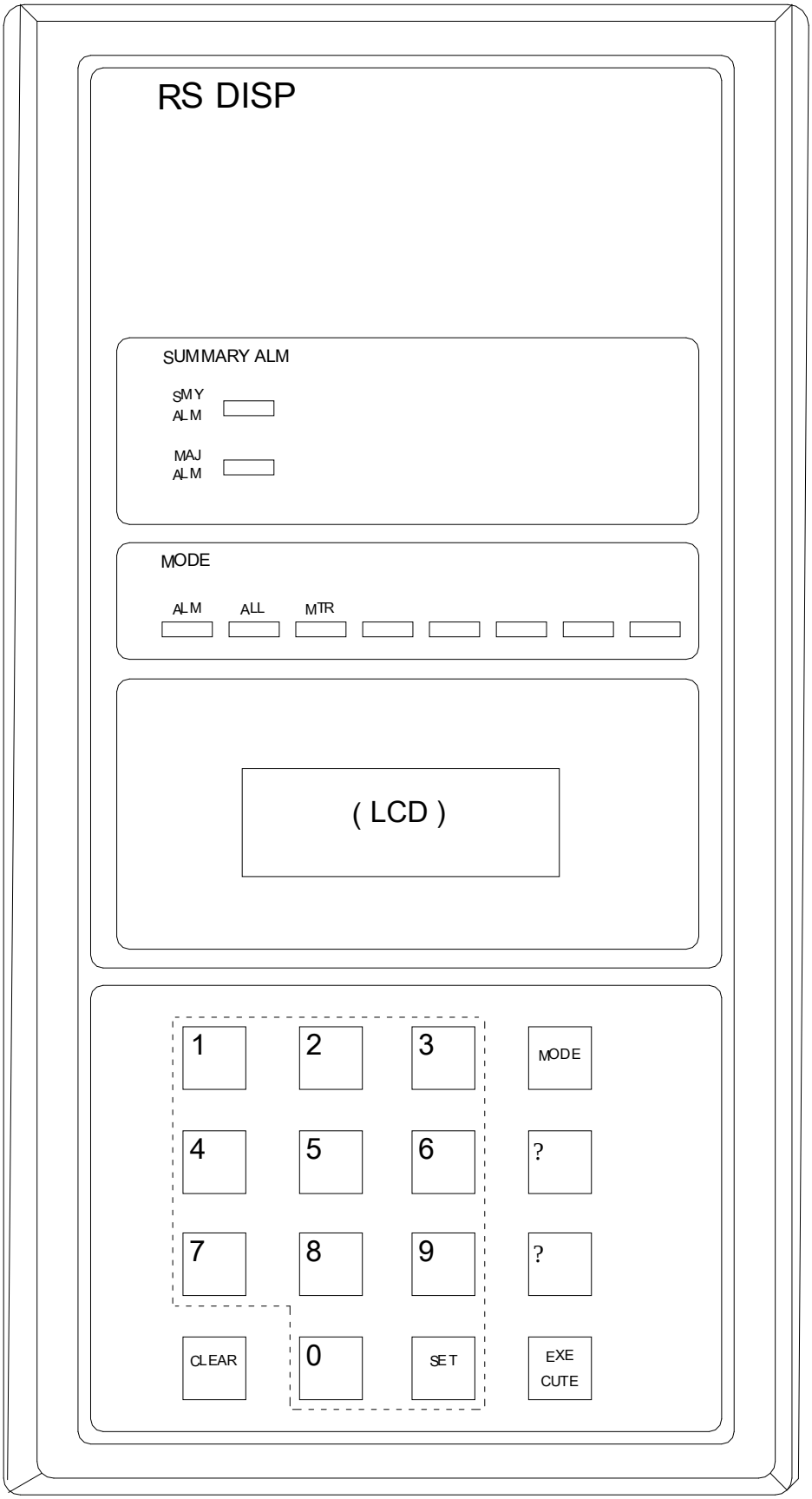


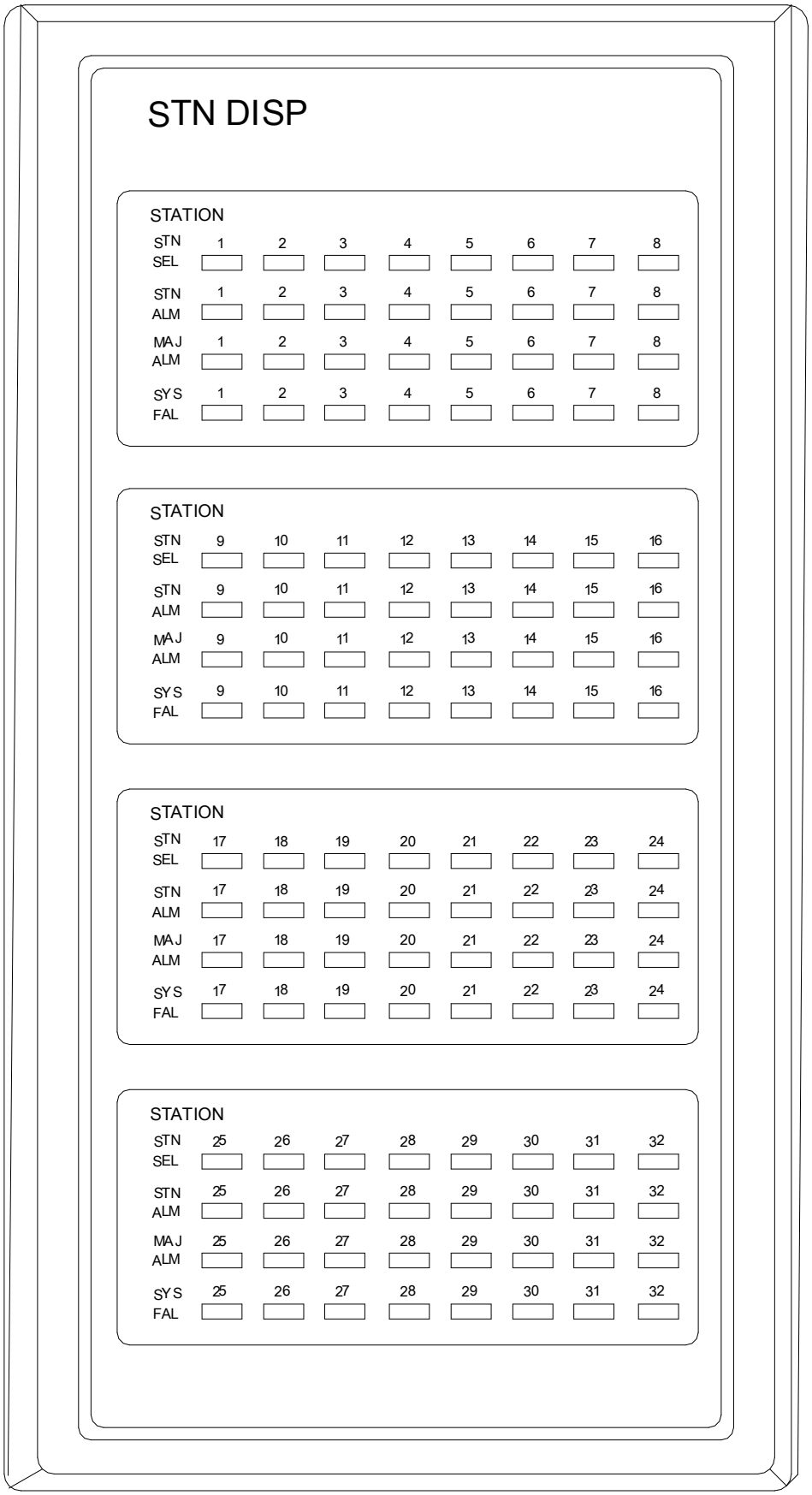
DISPLAY SYSTEM

Display system of NEC Equipment is configured as:
MS DISP
SUB MS DISP
RS DISP
STN DISP




SUB MS DISP
STATION
STN SEL 1 2 3 4 5 6 7 8
STN ALM 1 2 3 4 5 6 7 8
MAJ ALM 1 2 3 4 5 6 7 8
SYS FAL 1 2 3 4 5 6 7 8
MODE
STN SEL
ALM
ALL
CONT
(LCD)
1
2
3
MODE
4
5
6
?
7
8
9
?
CLEAR
0
SET
EXE CUTE


RS DISP
SUMMARY ALM
SMY ALM
MAJ ALM
MODE
ALM
ALL
MTR
(LCD)
1
2
3
MODE
4
5
6
?
7
8
9
?
CLEAR
0
SET
EXE CUTE


STN DISP
STATION
STN SEL 1 2 3 4 5 6 7 8
STN ALM 1 2 3 4 5 6 7 8
MAJ ALM 1 2 3 4 5 6 7 8
SYS FAL 1 2 3 4 5 6 7 8
STATION
STN SEL 9 10 11 12 13 14 15 16
STN ALM 9 10 11 12 13 14 15 16
MAJ ALM 9 10 11 12 13 14 15 16
SYS FAL 9 10 11 12 13 14 15 16
STATION
STN SEL 17 18 19 20 21 22 23 24
STN ALM 17 18 19 20 21 22 23 24
MAJ ALM 17 18 19 20 21 22 23 24
SYS FAL 17 18 19 20 21 22 23 24
STATION
STN SEL 25 26 27 28 29 30 31 32
STN ALM 25 26 27 28 29 30 31 32
MAJ ALM 25 26 27 28 29 30 31 32
SYS FAL 25 26 27 28 29 30 31 32

Objective:

1. NEC Digital Radio equipment is designed to work in the frequency band
   ---------- to ----------
   a) 7125 MHz to 7725 MHz b) 7125 KHz to 7725 KHz
   c) 7125 GHz to 7725 GHz d) 7125 Hz to 7725 Hz
2. The AUX unit of NEC digital radio equipment comprises of ---------- and---------- Modules
3. a) SWO and SWO CONT b) TX DPU and RX DPU c) WS SWO and WS INTF d) PH DEM and BIT COMB
4. The data selector switch in the RX section of the SWO module of NEC digital radio equipment selects one the two ---------- signals coming from the REG and PROT equipments on receiving the control signal.
   a) 2 Mbps b) 34 Mbps c) DSC d) ASC
5. The ---------- module of NEC digital radio equipment consists of alarm & control circuits and ASC circuit.
   a) SWO CONT b) SWO c) WS SWO d) WS INTF
6. The SWO module of NEC digital radio equipment consists of a transmitting section and receiving section. (T/F)
7. The ASC signal to the REG and PROT equipments of NEC digital radio equipment is supplied by SWO CONT module. (T/F)
8. A 432 bit Random pattern generator produces scramble patterns and sub-frame pulses. (T/F)
9. A frame pattern signal, called ID Code, is selected by a switch on the front module of TX DPU unit of NEC digital radio equipment. (T/F)
10. The TX alarm indicator on the front face of the TX module of NEC digital radio equipment lights red when the alarm output is about – 8 V. (T/F)
11. The Analog Service Channels frequency modulates the RF signal in the TX RF module of NEC digital radio equipment. (T/F)
12. The isolators employed at the input and output of the Pre-RF amplifier circuit of NEC digital radio equipment improves the VSWR. (T/F)
13. The amplitude equalizer employed in IF amplifier section of NEC digital radio equipment equalizes amplitude to frequency response, (T/F)
14. The delay equalizer employed in NEC digital radio equipment is used for equalization of reflected delay developed in the branching circuit of the Transmitter-Receiver. (T/F)
15. Transversal equalizer module in NEC digital radio equipment compensates both amplitude and delay distortion which are caused by selective fading. (T/F)
16. BIT COMB module of NEC digital radio equipment monitors the circuit quality and channel identification by the frame synchronization. (T/F)

17. The RF signal coming from the antenna is applied to the REG and PROT equipments of NEC digital radio equipment through an RF hybrid in the branching circuit. (T/F)
18. The number of Analog service channels provided in of NEC digital radio equipment is three. (T/F)
19. The number of Digital service channels optionally provided in of NEC digital radio equipment is four. (T/F)
20. The input power supply variation to NEC digital radio equipment can be form – 36 to –75 V DC. (T/F)
21. Power consumption for a 1+1 hot standby system of NEC digital radio equipment is 144 Watts. (T/F)
22. The TX frequency stability of NEC digital radio equipment is ± 20 ppm. (T/F)
23. Analog service channel having frequency band 4.3 to 7.4 KHz is used for remote supervisory circuit in NEC digital radio equipment. (T/F)
24. The line bit rate of DSC channel in NEC digital radio equipment is 89.5 Kbps. (T/F)
25. Selective and voice calling facility on EOW is available in NEC digital radio equipment. (T/F)
26. A master station display unit of NEC digital radio equipment is capable of monitoring and controlling 32 stations in the link including the master station. (T/F)
27. A sub-master station display unit of NEC digital radio equipment is capable of monitoring and controlling 8 stations in the link including the sub-master station. (T/F)
28. An RS display unit of NEC digital radio equipment is capable of monitoring the station itself only. (T/F)

Subjective:

1. Briefly explain the function of AUX units in NEC digital radio equipment.
2. Explain the function of TX DPU unit of NEC digital radio equipment.
3. Draw the block diagram of multiplexer section of TX DPU.
4. What is the function of Buffer memory and ID code selector of TX DPU unit in NEC digital radio equipment?
5. What is the function of Scrambler and Stuff control circuit in TX DPU of NEC digital radio equipment?
6. Briefly explain the function of PH MOD unit of NEC digital radio equipment.
7. Briefly explain the function of DEL EQL unit of NEC digital radio equipment
8. Explain the function of TRSV EQL circuit in RX IF section of NEC digital radio equipment
9. Explain the function of PH DEM unit of NEC digital radio equipment.
10. Explain the function of BIT COMB unit of NEC digital radio equipment.
11. Classify the display system of NEC digital radio equipment and give their usage.

CHAPTER 4

18 GHz DIGITAL RADIO SYSTEM

4.0 Introduction

Why and how the need was felt for the use of 18 GHz Digital Radio System on Indian Railways?

In early sixties 25 KV AC Electrification was started in Railways and Telecom. Facilities were transferred to U/G cable. During maintenance, the following problems were encountered on cable system.

- Frequent incidents of theft, cable cut leading to more number of joints, poor quality work etc., made the joints prone to water ingress.
- Fault localisation further made difficult, opening a joint by wrong suspicion.
- Quick restoration by providing interruption cables and permanent restoration at a later date - resulted - in entire system becoming noisier day by day.
- Frequent failure of ringing.
- Long delays in locating low insulation faults
- Theft of emergency sockets made system further weak.
- P&T Dept. not having sufficient cables for permanent restoration and continuance of interruption for a long time.

Therefore, a new system was thought of, with basic features of

- Not to provide any equipment in block section
- Most of the equipments must be concentrated at one location - free from miscreants.
- Adequate protection to equipment room.

A solution thought was a radio relay system with repeater/Drop-insert at all Rly.Stations.

But, the UHF in 400 MHz or 900 MHz was ruled out due to **-**

- Lack of adequate number of frequencies to overcome the problem of over reach.
- Basic instability of UHF equipment for a multi-hop system having more than 6 hops on account of the inherent noise in the equipment of this range.
- The difficulties of providing security for the block circuits even if adequate frequencies are available to cater for overreach on account of diffraction/ducting.
- poor availability of frequencies in 4, 5 & 7 GHz bands
- 11 to13 GHz band monopolised by P&T Dept.

Hence, 15-18 GHz band was the only leftover option.

- Equipments were also readily available in 18 GHz
- **The main drawback was attenuation caused by rain**

How arrived at the decision to use 18 GHz system?

- Found from a report of CCIR that a system can be engineered taking into account the maximum possible attenuation due to rain likely to be encountered in the area in question.
- As the path length may be about 10 Km the major part of the normal fade margin can be set off against the requirement of rain attenuation.
- Path being small, multi-path fading need not be taken into account for calculation.
- Similar system was approved for Canadian National Railway. Canadian Mountain Police was already using a similar system with 18 hops.
- Radio Repeaters being of re-generative type will give an error free output and there is no accumulation of noise from hop to hop.
- Even if the digital receiver operates at an input level marginally above the threshold level, a satisfactory BER is obtained thus allowing engineering links with reduced fade margin.
- In Digital Multiplexing, the number of channels, loaded does not affect the performance.
- In Digital Multiplexing, increasing the V.F. levels on individual channels does not increase the loading of the system and hence the noise.

4.2 18 GHz DIGITAL MICROWAVE RADIO (HARRIS MAKE)

General Description

Overview: The Farinon Urbanet 18GHz Digital Microwave Radio is a complete system for business, industrial, and common carrier light density communication in the 18.36 - to 19.16 GHz band. The radio is compact, light, simple to install and operate, and easy to maintain.

SYSTEM CONFIGURATION

Main Configuration Options: The Urbanet 18GHz radio is available in three main protection configurations: (1) Expandable non-protected (NP), (2) Non-expandable non-protected (NP), and (3) Monitored-hot-standby protected (MHS).

Expandable and Non-expandable Radios: The expandable non-protected radio can be reconfigured, even after installation, to a protected radio. The non-expandable non-protected radio cannot be reconfigured to a protected radio. All non-protected radios, however, whether expandable or non-expandable, can be converted from standard-power to high-power output.

Transmission rate and power options: Transmission rate and output power options are available for each of the three configurations. Transmission rate options are: (1) FCC/DOC (4 X T1, 6.312 Mb/s), and (2) CCIR (4 X E1, 8.448 Mb/s). Output power options are: (1) Standard-power output and (2) High-power output.

Conversion of Expandable Radios: The Urbanet 18GHz expandable non-protected radio can be reconfigured, even after installation, for protected and/or high-power-output operation. MHS standard-power-output radios can be reconfigured for high-power-output operation.

The conversions are:

1. NP standard-power to NP high-power
2. MHS standard-power to MHS high-power
3. NP to MHS standard-power
4. NP high-power to MHS high-power
5. NP standard power to MHS high power.

Other Optional Equipment and Software

Available optional equipment includes the Farinon Digital Versatile Service Channel (DVS) assembly, the Farinon Digital Versatile Alarm (DVA) assembly and Remote System Control and Alarm Network surveillance software (FARSCAN), and a Farinon Fuse and Alarm Panel can be installed to operate with the Urbanet 18GHz.

4.3 TECHNICAL SPECIFICATIONS

General Characteristics

1. Frequency Range	:	18.58 to 19.16 GHz
2. Nominal bit rate	:	4XT1 (6.312 Mb/s) & 4XE1 (8.448 Mb/s).
3. Channel capacity	:	96 (at 4 XT1) & 120 (at 4XE1)
4. RF Channel Bandwidth	:	10 MHz (FCC 4XT1 or CCIR 4XE1) 5 MHz (DOC 4XT1)
5. System Configurations	:	Non-protected Expandable, Non-protected Non-expandable and Monitored Hot-Standby Protected (MHS).
6. Operating environment		
Ambient Temp Range	:	-30^0 C to + 55^0C (Out door RF Assembly)
	:	0^0C to + 40^0C (Indoor MUX/Modem assy.)
Storage	:	-40^0 C to 65^0 C
Humidity All weather operation		
(Outdoor RF assay)	:	95% at 40^0 C (Indoor MUX assy.)
7. Altitude	:	4500 meters (15,000 feet) AMSL.

Transmitter Characteristics

1. RF Power Output (at antenna port)			
Non-protected assemblies	:	Standard Power	+15 dBm
		High Power	+23 dBm
MHS Assemblies	:	Standard Power	+14 dBm
		High Power	+23 dBm
2. Frequency Stability	:	+30 ppm (+ 0.003)	
		(-30^0 C to $+55^0$ C)	
3. Type of Modulation	:	4-level Frequency-Shift Keyed (4-FSK)	
		Direct modulation (bipolar, digital base band)	

RECEIVER CHARACTERISTICS

		US FCC	CAN DOC	CCIR
1. Emission Designator	:	6M40F7W	5MOOF7W	8MOF7W
2. Receiver Threshold	:			
BER = 1×10^{-6}		-83 dBm	-83 dBm	-82 dBm
BER = 1×10^{-3}		-86 dBm	-86 dBm	-85 dBm
		(4T1)	(4T1)	(4E1)

4.4 18 GHz Digital Radio Equipment - (WEBFIL Make)

Features

1. Direct RF Modulation
2. Digital Transmission at following CEPT rates:
   1 x E1 (30 Ch)
   2 x E1 (60 Ch)
   4 x E1 (120 Ch)
   1 x E2 (120 Ch)
3. Flexible transmission rate selection by Personality Card.
4. Built-in Higher Order MUX.
5. Tuneable DRO for RF Channel Selection
6. User Programmable Scrambling for Communication security
7. In-built test and diagnostic facilities for routine maintenance.
8. Built-in Supervisory and Local/Remote Loop-back test facilities.
9. Digital Express Order wire Channel with DTMF station selection.
10. VLSI and MIC Technology of minimal power consumption.
11. Weatherproof RF units mountable at the Antenna rear, needing no wave-guide; contribute to system gain and economics.
12. Modem and changeover units separable from RF unit by 300 metres and interconnected by inexpensive cables.
13. Centralised Network monitoring
14. Simple installation procedure with inexpensive tools
15. Forward Error Correction Coding for higher reliability and data integrity (Optional).
16. Complies with all relevant CCITT recommendations.

4.4.1SYSTEM OPTIONS

1. CEPT Bit rate Options:
   a) 1 x 2 Mb/s; b) 2 x 2 Mb/s; c) 4 x 2 Mb/s; d) 1 x 8 Mb/s
2. Monitored Hot Standby (Single frequency) or Frequency Diversity (using a pair of frequencies) configuration.
3. Additional PCM voice channel for Omnibus Order wire Communications.
4. DMC Net for Radio Network data management from a designated Master Terminal.
5. FEC for enhanced System Gain
6. RF mounting - Indoor or Outdoor.

4.4.2 SPECIFICATIONS

G e n e r a l

Operating Frequency	:	17.7 - 19.7 GHz
Modulation type	:	BPSK
RF Connector	:	SMA
Digital Capacity	:	2.048 Mb/s. 2x2.048 Mb/s.
	:	4x2.048 Mb/s. 8.448 Mb/s.
Standard Voice Channel Capacity	:	30, 60,120
Digital Interface	:	CEPT-1 (2.048 Mbit/s)
Digital Input/Output Connections	:	75 BNC Connectors.
Digital Line Code	:	HDB3
Modem & RF Unit Interface		
Connector Type	:	Coaxial Type Connector
Recommended Coaxial Cable	:	RG-6 (Belden 9248 or its equivalent)
Maximum separation	:	300 metres

Transmitter

Power Output (at RF Unit antenna port)	:	+20 dBm (100 mW)
Frequency Stability	:	±0.02%
Frequency Source	:	Dielectric Resonator Oscillator.

Receiver

T y p e	:	Dual Conversion
Sensitivity at 10^{-6} BER	:	2.048 M bits/s : -86 dBm
(at RF Unit antenna port)		2 x 2.048 M bits/s : -83.5 dBm
		4 x 2.048 M bits/s or
		8.448 M bits/s. : -81 dBm
Un-faded BER	:	10^{-10} or better
Un-faded BER with FEC	:	10^{-12} or better
Max. Input signal level at 10^{-6} BER	:	-15 dBm

System Gain

At 10^{-6} BER (Guaranteed value at RF Unit antenna Port)

2.048 Mbit/s	:	106 dB
2x2.048 Mbit/s	:	103.5 dB
4x2.048 Mbit/s or		
8.448 Mbit/s	:	101 dB
Forward Error Correction gain		
(If equipped with this option)	:	3 dB

Additional Branching Losses (For protected terminals)	On Line	Standby
MHSB Transmitter	2.5 dB	2.5 dB
MHSB Receiver	2.5 dB	15.5 dB

Order wire & Data Channel

General

Station Addressing	:	Up to 800 Stations
Order wire Ports		
Customer Port Interface		
Telephone Connector	:	RJ-11 (modular jack)
VF Bandwidth	:	300-3400 Hz
Signalling	:	Dual Tone Multiple Freq. (DTMF)
Analog Alarm & Expansion Port		
Interface	:	600 ohms balanced
Frequency	:	300-3400 Hz.
Level	:	0 dBm

Power Requirements

S o u r c e	:	-48 VDC, positive ground
Allowable Input Range	:	-41 to -56 VDC
Power Consumption (Typical)		
Non-Protected	:	40 watts.
Monitored-Hot-Standby		
(Protected)	:	90 watts

Environmental

Altitude	:	Up to 4500 meters.
Temperature Range		
RF Unit/Antenna (Requires	:	-30^0 C to $+55^0$ C
50 MHz Channel Bandwidth)		
M o d e m	:	0^0 C to $+50^0$C
Relative Humidity		
RF Unit	:	Up to 100 %(All weather operation)
Modem	:	95% at + 40^0 C.

Objective:

1. In 18 GHz digital radio system MUX equipments used at all stations are all Drop/Insert type. (T/F)
2. The path length in 18 GHz digital radio system is about 10 Km. (T/F)
3. Since the radio repeaters are of re-generative type in 18 GHz digital radio systems there is no accumulation of noise from hop to hop. (T/F)
4. Even if the digital receiver in 18 GHz system operates at an input level marginally above the threshold level, a satisfactory BER is obtained. (T/F)
5. The main drawback in 18 GHz digital radio systems is the attenuation caused by rain. (T/F)
6. The frequency range of 18 GHz Harris make is 18.58 to 19.16 GHz. (T/F)
7. Channel transmission capacity of Harris 18 GHz digital radio equipment is ----------
   a) 120 b) 30 c) 24 d) 480
8. RF channel bandwidth of Harris 18 GHz digital radio equipment is ---------- MHz
   a) 100 MHz b) 200 MHz c) 1 MHz d) 10 MHz
9. RF output power at antenna port of Harris 18 GHZ digital radio equipment is ---------- for Non-protected assemblies.
   a) + 23 dBm b) + 13 dBm c) + 33 dBm d) + 43 dBm
10. RF output power at antenna port of Harris 18 GHZ digital radio equipment is ---------- for MHS assemblies.
    a) + 23 dBm b) + 13 dBm c) + 33 dBm d) + 43 dBm
11. The type of modulation used in HARRIS 18 GHz digital radio equipment is ----------
    a) 4-FSK b) 4-PSK c) 8-FSK d) 8-PSK
12. The frequency stability of transmitter of Harris 18 GHz digital radio equipment is
    a) ±30 ppm b) ±20 ppm c) ±10 ppm d) ±40 ppm

Subjective:

1. Why and how the need was felt for the use of 18 GHz digital radio systems on Indian Railways?
2. What problems were encountered on cable systems, which paved the way for 18 GHz systems?
3. How it was arrived at the decision to use 18 GHz?

CHAPTER 5

DIGITAL MICROWAVE MEASUREMENTS

5.0 List of Test Equipments

1. Digital Multimeter
2. M.W. Power Meter
3. M.W. Frequency Counter
4. Spectrum Analyzer
5. M.W. Signal Generator
6. Digital Transmission Analyzer & Jitter Generator
7. Digital Storage Oscilloscope
8. Constellation Analyzer/Vector Analyzer
9. Network Analyzer
10. Carrier/Noise Test Set
11. Various accessories for the above.
12. Digital Radio Test System (Fading Simulator & Spectrum Analyzer, Power Meter, R.F. Source Freq. Counter, etc.)

5.1 Power Supply Voltages

Connect the digital multimeter between earth and the test points designated by the Manufacturer, which are to be compared with the standard readings. The A.C. ripple should be observed on the Oscilloscope, which should be less than 0.2% of the supply voltage.

5.2 Transmitter Output Power

Measure the transmitter output power via the directional coupler or built-in RF Mon. on a MW Power Meter, with appropriate calibration factor and compare with the standard reading.

5.3 Transmitter Output Frequency and RLO Frequency

Measure the transmitter's un-modulated output frequency after disconnecting base band data on a frequency Counter, connected via directional coupler at RF Mon Test Point.
RLO frequency is to be checked at the monitoring point provided on the RLO Unit.

5.4 Calibration of AGC level against input receive level

The AGC meter readings of the Receiver are relative indications of the received carrier level and can be used to determine the received signal level, under traffic-carrying conditions. An RF Signal Generator is connected to the input of the Receiver to simulate a received signal. The frequency of the Generator is set to the center frequency of the Receiver under test and its level is precisely adjusted to the nominal input signal level.

Varying the Generator's output level in steps and noting the AGC readings draw AGC calibration curve.

5.5 Study of Spectrums (Figure 5.1)

Spectrum Analyser is an oscilloscope design to perform signal analysis in the frequency domain and used to study elements such as, Amplifiers, Oscillators, Mixers, Filters and Modulators. It is of two types: -

i) Swept Toned for Telecom. Measurements
ii) Real-time Analyser for Geological Applications
(It does not provide phase information about a signal)

Connect the Spectrum Analyser via directional coupler or at RF Mon. Test Point. Without BB input, adjust Spectrum Analyser to display the transmitter carrier. After reconnecting the data from a Pattern Generator as required (HDB3, 2^{23} - 1), adjust the Spectrum Analyser sweep-width to display the modulated output spectrum. Compare the displayed spectrum against the regulation mask and confirm the symmetrical shape of the spectrum. The first side-lobe peak level relative to the carrier peak level should be at least -25 dBc (dB referred to carrier level). Spurious emission from the transmitter, which are any individual unwanted emissions present at the output shall not exceed -79 dBW within the frequency group in which the transmitter lies and at any other frequency shall not exceed -96 dBW.

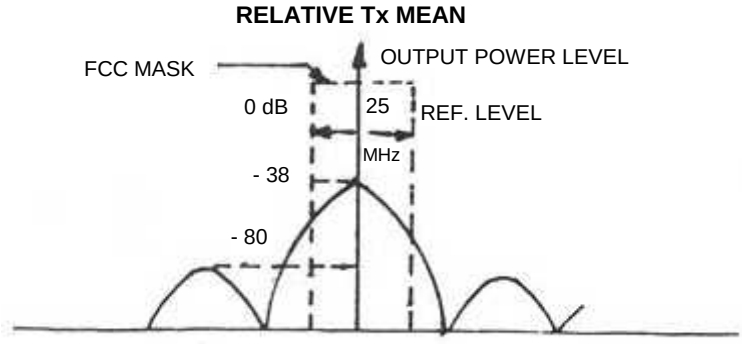


Figure 5.1 Frequency Spectrum illustrations

5.6 Analogue Service Channel Deviation

The deviation of the analog service channels is checked by 'Bessel Zero' method. To set the desired system deviation requires the use of a modulating source and a Spectrum Analyser to monitor the Carrier Frequency Component.

5.7 C/N versus BER Measurement

There are two methods of making C/N Vs BER Measurements:

i) The traditional method of fade simulation (Varying C)
ii) The method of additive noise (Varying N)

(i) Fade Simulation Method (Figure 5.2)

An attenuator is connected at the MW input of the receiver, so that the incoming signal can be attenuated into the receiver noise. A Power Meter is used to check the effective C/N ratio in the IF Section. To simulate the filter, which may exist after the IF stage and before the demodulator, which can introduce noise, the noise level measurement is made after inserting the appropriate filter into the Power Meter.

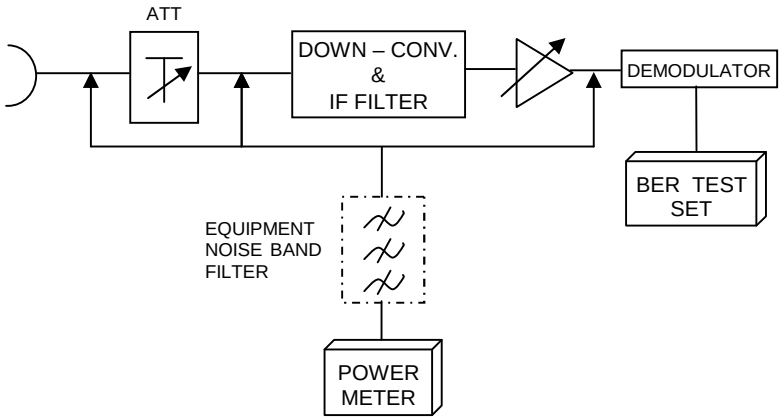


Figure 5.2 BER Test by Fade-simulation

Advantages

It tests the overall system implementation margin due to impairments in Modem and Path.
It tests the transmitter power, antenna gains and receiver AGC action.
It is simple and cheap by using only an Attenuator.

Disadvantages

The inaccessibility of the attenuator and hence, time consuming.

The inaccuracy of the attenuator affects the repeatability of the measurement.

Propagation effects may cause a variation in carrier power received.

Additive Noise Testing Method (Figure 5.3): In this, the digital radio receiver operates at normal unattenuated received signal levels. The IF signal in the receiver path is connected through the (HP3-A) carrier/noise test set, which is set to the appropriate system bandwidth. By the Test Set adding the noise, C/N is accurately known and the BER is checked using a Pattern Generator at the transmitter end and an Error Detector at the output of the demodulator.

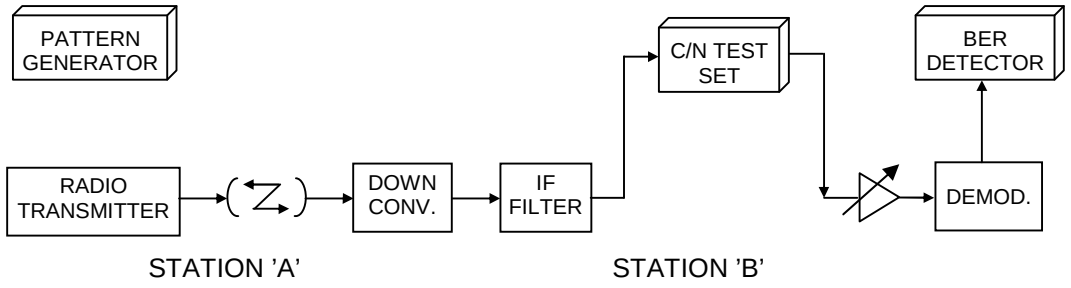


Figure 5.3 BER Test by Additive Noise Method

Automatic measurements are also possible with HPIB facility.

As per CCITT Standard, for a C/N of 13.5 dB, a minimum of 1 X 10^{-4} BER must be obtained.

Advantage

As the carrier varies due to propagation conditions, the Test equipment injects into the IF, a noise power that tracks the carrier to keep a constant C/N over the measurement period. The long measurement time (days) required for determining low background BER can be reduced by using a C/N test, in which an interfering signal is added to produce a controlled amount of eye closure. The increased BER is then easily measured and the true background BER can be estimated.

5.8 BER (DTA) Measurement

BER is the ratio of the number of impaired bits to the actually transmitted number of bits over a period of time.

Digital Transmission Analyser

The Digital Transmission Analyser is basically a Pattern Generator and Digital Error Detector packed into one Unit. It may also contain built-in Jitter Generator. Digital Transmission Analyser, DTA is one of the versatile Instruments for Digital Transmission. It is used for the measurement of BER, Jitter, etc. DTA can be used when the transmission media is Optical Fibre or Digital UHF or digital Microwave or Coaxial Cable.

The DTA can be used for 2MB, 8MB or 34MB. The DTA can calculate and display the following parameters:-

1. No. of unavailable seconds (UVS)
2. Unavailable seconds % (UVS %)
3. No. of errored seconds (ES)
4. Errored Seconds % (ES %)
5. No. of heavily or severely errored seconds (SES)
6. Heavily/Severely errored seconds % (SES %)
7. No. of degraded minutes (DM)
8. Degraded Minutes % (DM %)
9. No. of seconds with Fault Indication (SFI)
   A Fault Indication (SFI) is obtained on detection of AIS, signal loss for at least 1mS, or detection of a Sync search).

(10) Errored seconds % related to 64 Kbit/s rate (S64%) etc.

The other measurements such as Peak-to-peak jitter are possible using the DTA, with the built-in Jitter Generator.

The DTA generates different data patterns, which can be selected from the front panel. The length of pattern can be set ($2^{15} – 1$, $2^{23} - 1$). The line code (HDB3/CMI etc.), the bit rate (2Mb, 8Mb, and 34 Mb) etc., can also be set easily. An accurate clock frequency output is also available. The DTA can receive all the combination of for analysis. Measurements such as, Error count, Error ratio, Error seconds, Error free seconds, % unavailability, % errored seconds, % severely errored seconds, % degraded minutes can be easily seen and a hard copy is obtained from the built-in printer with timings. Flags such as, Power Loss, Data Loss, Clock Loss, AIS are also provided.

Procedure

1) At Station A, connect the DTA data output to the DATA IN of Radio Transmitter after setting the appropriate bit rate, line code and pseudo-random pattern length.
2) At Station B, connect the other DTA's data input to the DATA OUT of Radio Receiver after setting as per the generator at Stn. A.
3) The selected readings are displayed digitally as well as print out is given.

5.9 Jitter Measurements

The CCITT definition of Jitter is "Short term variations of the significant instants of a digital signal from their ideal positions in time". Jitter can also be considered as spurious modulation of the digital signal clock.

Causes

Jitter can be caused during line transmission of the signal (line jitter), or during channel multiplexing/de multiplexing (multiplexing jitter).

- Line jitter is mainly due to the differential jitter introduced by the repeater clock recovery circuits.
- Multiplexing jitter is due to multiplexing of quasi-synchronous signals (justification jitter, delay time jitter, residual jitter).

Equipment response of Jitter: Telecommunications equipment must accept a minimum level of jitter at the input junction, without inducing errors.

- In the absence of any jitter of an external origin at input, the equipment must produce output jitter on its junction, which does not exceed a specified value.
- A specified amplitude/frequency relation (jitter transfer function) must be observed, between the jitter present at input of the equipment, and resultant output jitter.

Jitter can be increased, filtered and amplified along the transmission link, by the different items of system equipment.

Effects of Jitter

Excessive jitter amplitude introduces errors in the digital data transmitted, thus degrading communication quality.

Jitter amplitude is expressed in Units of time (seconds), phase (radians or degrees) or digit periods (Unit Interval (UI)). UI is the nominal time allowed for the transmission of one digit and is the widely used unit. A UI is thus numerically equal to the reciprocal of the digit rate and is easily convertible to other units.

Ex. 0.25 UI (P-P) on a 2Mbit digital signal is equivalent to 0.122 Sec. or $\pi/2$ radians.

Jitter on the symbol timing clock, which is used to sample the demodulator I and Q signals is also a source of errors in digital radio, which leads to eye-closure at the sampling instant leading to an equivalent C/N margin. The Jitter is mostly due to the unwanted phase modulation of the digital signal and the Jitter can be observed on a Digital Storage Oscilloscope also.

5.10 Maximum Tolerable Input Jitter (MTIJ) (Figure5.4 & 5.5)

This is tested by applying increasing Jitter to an input data-stream and determining the onset of bit errors.

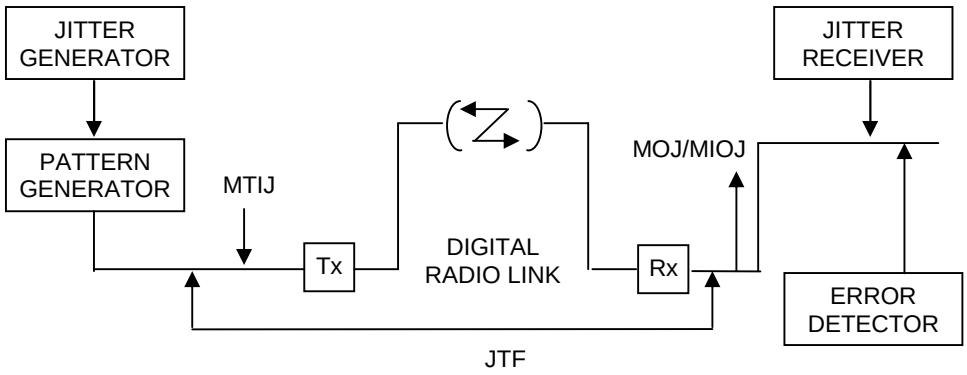
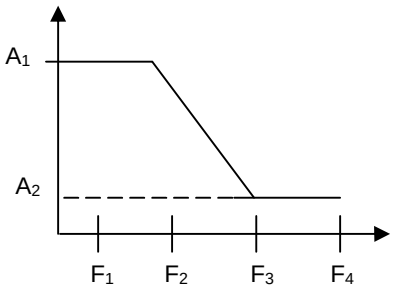


Figure 5.4 MTIJ Test set-up



A1 (U1 – PP)	1.5	1.5
A2 (U1 – PP)	0.2	0.15
F1 (Hz)	20	100
F2 (KHz)	2.4	1.0
F3 (KHz)	18	10
F4 (KHz)	100	8.0
PRBS	$2^{15} - 1$	$2^{23} - 1$
(Freq)		

Figure 5.5 MTIJ Test Results

The actual tolerance of the equipment must be above the mask.

Maximum Output Jitter (MOJ): It is the level of output jitter with a jittered input signal.

Maximum Intrinsic Output Jitter (MIOJ): It is the level of output jitter with a jitter free input signal. Usually the measurement for the above two is done measuring the output Jitter in each of a number of Freq. and comparing the results with the standard CCITT values.

Ex: 34 Mbit 0.1 - 800 KHz -- 1.5 UI (P-P)
10 - 800 KHz -- 0.15 UI (P-P)

5.11 Jitter Transfer Function (JTF) (Figure 5.6 & Figure 5.7)

It is a measure of how the jitter is attenuated by passing through the system, a necessary specification to prevent jitter accumulation in the network.

Jitter Gain = $20 \log_{10}$ (Output Jitter/Input Jitter)

The Jitter gain calculated for a number of frequencies across the bandwidth, is used to construct the JTF, CCTI specifications takes the form of a mask.

Figure 5.6 JTF concept

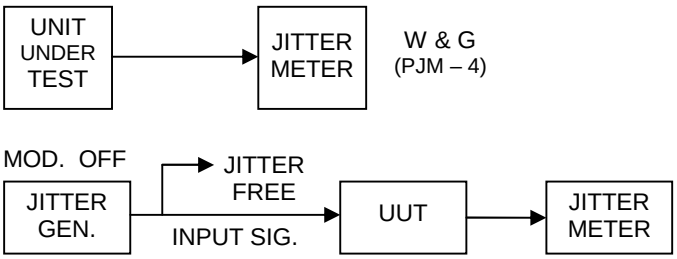


Figure 5.7 JTF Test set-up

5.12 ERRORS

An Error is a bit inversion in the binary sequence during transmission. In contrast to Jitter, which can be eliminated, the number of errors contained in the message sent can be on the increase between one end of the transmission link and the other. It is, therefore, important to ensure that no component element of the system perturbs the complete link.

<table>
<tr><td rowspan="4">Total time</td><td rowspan="3">Availability Time</td><td>Acceptable quality</td></tr>
<tr><td>Degraded quality</td></tr>
<tr><td>Unacceptable quality</td></tr>
<tr><td colspan="2">Unavailability time</td></tr>
</table>

Causes

Errors are principally due to thermal noise in repeaters, cross talk between the balanced pairs of the same cable and the repeater clock recovery circuit in the presence of signal jitter.

5.13 Transmission Quality

A direct relation exists between the number of errors present in a digital transmission, and the quality of the resultant communication. However, the impact of isolated errors is not the same as that of error bursts. CCITT recently attempted to characterize transmission quality by the error rate (ratio of the number of error bits to the total number of bits), referenced to time.

This has produced the following classification: -

- Acceptable quality: error rate less than 10^{-6} in one minute.
- Degraded quality: error rate between 10^{-6} and 10^{-3} in one minute (degraded minute)
- Unacceptable quality: error rate exceeding 10^{-3} in a scan period of one second (unacceptable second).
- Unacceptable quality for 10 or more consecutive seconds, communication state “unobtainable".

Diagram is demonstrating sub-division of total communication observation time is presented above. The quality parameters thus defined are valid for cable transmission in particular. They appear less appropriate for carriers.

5.14 Eye Diagrams

It is useful for deciding the threshold level for repeaters and also to judge the quality of the received signal. The larger the eye opening the better is the quality. The eye diagram can be observed on a Digital Storage Oscilloscope. A storage CRT can retain the display much longer on the phosphor screen than the ordinary CRT. The storage CRT has multiple targets and two electron guns viz., Flood Gun and Writing Gun.

Facility is provided usually in the demodulator/regenerator sections in the receiver of the Digital M.W. radio equipment for in-service monitoring of the eye diagram on a DSO.

5.15 Constellation Analyser (Figure 5.8)

It is a special purpose high-performance dual-channel sampling oscilloscope designed for digital radio measurements. By displaying the value of Q and I eye diagrams at the sampling instants and super-imposing these samples, we get the so-called Constellation Diagram. It can display the radio constellation or either I/Q eye-diagrams. The amplitude and phase distortions caused by individual impairments uniquely deform the constellation pattern thus enabling the user to recognize the problems immediately.

The impairments can be such as: -

1) Interference 2) Low C/N 3) Without Lock 4) Phase Jitter

5) Amplitude Imbalance 6) Misadjusted Modulator Levels, etc.

To make the constellation measurement in-service, the radio must be equipped with suitable monitor points in the demodulator, providing the post demodulation I and Q streams and clock. The Analyser can also display I and Q 'eye reduction' as a bar chart.

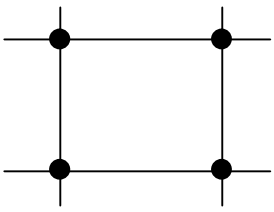


Figure 5.8 QPSK Constellation

Display	mV/div
I	1.47
Q	1.42
Closure	
I	14.0%
Q	13.8%
Lock	0.0
Quad	0.0
Non-linear	
RMS	0.2%
AM	0.8%
PM	0.1%

MV/div: Gives scaling between inter-section of the graticule and used to measure any amplitude variations between the I or Q signal states or variations between I & Q signals.

Closure: Evaluates the RMS size of Constellation Cluster percentage of cluster separation, which is a measure of Jitter and ISI levels for I and Q signals.

Lock (Angle Error): It is a measure of any joint phase misalignment of the I and Q signals from the received carrier.

Quad (Angle Error): Measures any deviation from 90 (quadrature) between the I and Q signals.

Non-Lin: Evaluates any non-linear contribution to poor performance.

RMS - Total non-linearity

AM - AM – AM contribution

PM - AM - PM "

Vector Analyser: Like Constellation Analyser, it also displays eye and constellation diagrams and also has two extra modes, vector and 3-D rotation.

5.16 Network Analyser: Individual component testing is easy with network Analyser.

(i) Using fade simulator and network analyzer, the transversal equalizer's notch response ('Signature Curve') can be easily measured and adjusted. Usually, for a BER of 1×10^{-6}, the transversal equalizer must be able to adjust for a notch depth of 27 dB at 70 MHz.

(ii) The wave guide filter's response as well as other filter can also be checked.

(iii) Using network analyzer, the VSWR can be measured indirectly, but easily.

Network Analyzers are instruments that measure transfer and/or impedance functions of linear networks through Sine Wave Testing.

Capabilities: Transfer functions - Magnitude/phase insertion loss/gain, attenuation, S-Parameters (Ratios of reflected and transmitted travelling waves measured at the network ports), electrical length, group delay, deviation from linear phase.

5.17 Definitions

$$\text{Bit Error Rate (BER)} = \frac{\text{No. of error bits}}{\text{Total No. of bits sent}}$$

Error Interval (EI) = Total of intervals in total measurement time (T) in which more than one error occurs in interval t (0.01, 0.1 or 1s)

Error-free interval (EFI):- Ratio of time intervals in which no error occurs.

$$= \frac{\text{Total Meas. Time (T) - Error interval (EI) X Interval Time (t) x 100\%}}{\text{Total measurement time (T)}}$$

$$\text{Error seconds (ES)} = \frac{\text{Time in which more than one error occurs x 100\%}}{\text{Total measurement time.}}$$

$$\text{Error-free seconds (EFS)} = \frac{\text{Sum of no. error time (seconds) x 100\%}}{\text{Total measurement time (T)}}$$

Severely Errored Seconds (SES):-One-second interval having a bit error ratio worse than 10^{-3}.

Degraded Minutes: - One-minute interval having a bit error ratio worse than 10^{-6}.

Objective:

1. The AC ripple should be less than 0.2% of the supply voltage when observed on an Oscilloscope. (T/F)
2. Spectrum analyzer is an instrument to perform signal analysis in the frequency domain. (T/F)
3. Line jitter is mainly due to differential jitter introduced by the repeater clock recovery circuits. (T/F)
4. Multiplexing jitter is due to multiplexing of quasi-synchronous signals (T/F)
5. Telecommunication equipments must accept a minimum level of jitter at the input without inducing errors. (T/F)
6. Excessive jitter amplitude introduces errors in the digital data transmission. (T/F)
7. Jitter amplitude is expressed in Unit intervals. (T/F)
8. A Unit interval is numerically equal to the reciprocal of the digit rate. (T/F)
9. An Error is a bit inversion in the binary sequence during the transmission. (T/F)

SUBJECTIVE

1. List the various tests that are conducted for maintenance of digital radio systems and their periodicity.
2. What are the various causes of Jitter in digital radio transmission systems?
3. Define Jitter tolerance and Jitter transfer. Draw the masks of Jitter transfer function and Jitter tolerance.
4. Define the following
   i) Error
   ii) BER
   iii) JITTER
   iv) ES
   v) SES
   vi) DM