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I R I S E T

DIGITAL ELECTRONICS LABORATORY

EXPERIMENT NO. DE- 1

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Experiment No. DE-1

Study of Digital ICs and Their Properties

Objective: The main aim of this lab sheet is

- to introduce to you the two **most popular digital IC families,** that you may most likely come across with during your working in railways, **and their specific characteristics**.
- to give you information on how to handle and use these ICs and
- to instruct you about the **dos** & **don'ts** while handling the digital trainer kits that you are going to use while performing experiments in the lab.

I. Important Instructions to Trainees before Handling Trainer Kits

1) Before beginning any experiment first carefully read the experiment sheet given to you
2) Then verify whether the given kit is the one meant for the present experiment. If not ask for the proper one.
3) Handle the **Kits** and the **patch cords** with maximum care
4) **IMPORTANT:** Don't remove any ICs from the trainer kits.
5) **Don't touch the ICs in the kits with your hands**. Many ICs are static sensitive and can be damaged when you touch them because your body becomes charged with static electricity, from your clothes for example.

II. Introduction to Digital ICs

Before going into the details of digital ICs let us know some important terms related to them.

a) Terminology used with Logic Circuits

V_{CC} : *The voltage applied to the power pin(s). In most cases the voltage the device needs to operate at.*

V_{IH} : [Voltage Input High] *The minimum positive voltage applied to the input which will be accepted by the device as a logic high*.

V_{IL} : [Voltage Input Low] *The maximum positive voltage applied to the input which will be accepted by the device as a logic low.*

V_{OL} : [Voltage Output Low] *The maximum positive voltage from an output which the device considers will be accepted as the maximum positive low level.*

V_{OH} : [Voltage Output High] *The maximum positive voltage from an output which the device considers will be accepted as the minimum positive high level.*

V_T : [Threshold Voltage] *The voltage applied to a device which is "transition-Operated", which cause the device to switch. May also be listed as a '+' or '-' value.*

1) Sinking and Sourcing Currents

IC outputs are often said to **'sink'** or **'source'** current. The terms refer to the direction of the current at the IC's output.

(a) **Sourcing Current** : *It is the current supplied (sourcing) by a logic device when its output is in high state*

If an IC is **sourcing a current** means the current is flowing **out of the output**. This means that a device connected between the IC output and the negative supply (0V) will be switched **on when the output is high (+Vs)**.

(b) **Sinking Current** : *It is the max. current accepted(sinking) by a logic device when its output is in low state*

If an IC is **sinking a current** means the current is flowing **into the output**. This means that a device connected between the positive supply (+Vs) and the IC output will be switched **on when the output is low (0V)**.

2) **Propagation Delay** : *Propagation delay is the minute time lapse that takes place in logic devices between the instances of application of input signals and occurrence of changes in the output signals*.

3) **Fanout** : *The number of other logic devices inputs that can be driven by the output of a logic device.*

b) Popular Logic Families

All standard digital functions like logic gates, flip flops, counters etc., are introduced into the market in the form of ICs. These ICs are produced in different logic families by different manufacturers. Here we will discuss only two very popular logic families and their properties. These logic families are TTL and CMOS.

TTL - Transistor Transistor Logic family

CMOS - Complementary MOSFET logic family

TTL Family Devices

This logic family devices are very popular and are being used almost in every digital system. These devices are faster but consume more power than CMOS devices.

CMOS Family Devices

This logic family devices are also very popular and are main competitors to TTL devices. CMOS ICs consume much less power than TTL and operate with voltages from 3V to 15 V . CMOS, though, is much more susceptible to damage from static electricity. Hence, it is **essential** to use **grounding strap**. CMOS comes in two series, with corresponding numbering schemes:

1) **40 XX - metal gate CMOS**
2) **74CXX - silicon gate CMOS**

Metal gate CMOS (40XX) has a rated working voltage of 3 - 15 V but can be used down to 2V.

Silicon gate CMOS (74CXX) logic has a working voltage range of 2 -6V but can be used at less than 1V. For microwatt power applications the lowest possible voltage is used. (This subfamily is pin compatible with corresponding TTL ICs and that is why it uses TTL numbering scheme).

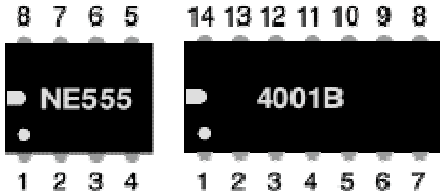
The properties of the devices belonging to these two logic families are very different and are required to be known by every electronic engineer. The following table gives various parameters of both logic types.

Device Parameter	Logic Family	
	TTL	**CMOS**
IC Numbering	**Commercial:** 74, 74L, 74S, 74LS, 74AH, 74AC, 74ACT **Military:** 54, 54L, 54H, 54S, 54LS, 54AH etc	4000 , 74HC, 74C & 74HCT
Operating Voltage	+5VDC ± 0.25V(comm.) +5VDC ± 0.5V(military)	+3 to +15 V DC (Conventional) +3 to +18V DC(4000B series) +2 to +6V DC (74HC) +5V DC (74C, 74HCT)
Operating Temperature	0º C to +70º C(comm.) -55º C to +125º C(milit)	-55º C to +125º
Fan out	10 TTL inputs	50 CMOS inputs

Sinking Current	16 mA	1mA
Sourcing Current	2 mA	1mA
Propagation Delay (Operating Speed)	10 nS	30nS
Signal Logic Levels	a) V_{IL} : 0 to 0.8V b) V_{IH} : 2 to 5V c) V_{OL} : 0 to 0.4V d) V_{OH} : 2.4 to 5V	V_{IL} : < 25% of Vcc V_{IH} : 75% of Vcc to Vcc V_{OL} : 0 to max 4% of Vcc V_{OH} : > 94%
Power Dissipation	10 mW	Very low, few µW (but at high freq., ≥1MHz, a few mW**)**
Sub-families	74L XX -- low-power TTL (1/10 the speed, 1/10 the power of "regular" TTL) 74HXX -- high-speed TTL (twice as fast, twice as much power) 74SXX -- Schottky TTL (for high-frequency uses) 74LSXX -- combination of low-power & Schottky, same speed as regular TTL, but at 1/5 the power consumption	4000B - Improved design 74HC - High Speed CMOS 74C - TTL compatible pinout 74HCT - do

III. Important Information Needed Before Using Integrated Circuits (ICs)

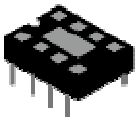
a) Pin numbering on ICs



The pins are numbered anti-clockwise around the IC (chip) starting near the notch or dot. The diagram shows the numbering for 8-pin and 14-pin ICs, but the principle is the same for all sizes.

b) IC holders (DIL sockets)

ICs (chips) are easily damaged by heat when soldering and their short pins cannot be protected with a heat sink. Instead we use an IC holder, strictly called a DIL socket (DIL = Dual In-Line), which can be safely soldered onto the circuit board. The IC is pushed into the holder when all soldering is complete.



Commercially produced circuit boards often have ICs soldered directly to the board without an IC holder, usually this is done by a machine which is able to work very quickly. Please don't attempt to do this yourself because you are likely to destroy the IC and it will be difficult to remove without damage by de-soldering.

c) What to do with the Unused Input Pins in TTL & CMOS ICs ?

When working with CMOS ICs(4000seires) any of the unused input pins must not be left open but they must be connected to Ground or V_{DD} as required in the circuit.

In case of TTL ICs (74xx/54xx series) **floating(unconnected) inputs** behave as if they are connected to **Logic Highs**. Hence, it is essential to connect all unused inputs to Low.

d) Datasheets

Datasheets are available for most ICs giving detailed information about their ratings, functions, pin out diagrams, timing plots and internal logic circuits. In some cases example circuits are shown. The large amount of information with symbols and abbreviations can make datasheets seem overwhelming to a beginner, but they are worth reading as you become more confident because they contain a great deal of useful information for more experienced users designing and testing circuits.

Review Questions

1. What precaution is to be taken before touching pins of ICs?
2. Which logic family you prefer if you need less power consumption?
3. If one input each of a TTL and a CMOS OR gates is left open in a circuit what would be their output levels ?
4. Specify $V_{IL(MAX)}$, $V_{IH(MIN)}$, $V_{OL(MAX)}$, $V_{OH(MIN)}$ values for TTL devices

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Experiment No. DE-2

BASIC LOGIC GATES

Objective

To study the logic operations of Basic gates, and Universal gates and to verify their Truth Tables.

Introduction

The basis for any digital system, irrespective of its size, is only three fundamental operations which are repeatedly used. These fundamental operations are: OR, AND and NOT logic operations. The circuits which offer these operations are called as **basic gates** or basic logic circuits. A Gate is a circuit with two or more inputs but only one output. Gates are digital (2 state) circuits because the input and output signals are either **low** or **high** voltages only. Gates are called logic circuits because they can be analyzed with Boolean Algebra. Different combinations of basic gates lead to some more gates. All these gates including basic gates are commonly called as **Logic Gates** which are divided into the following three categories,

1) Basic Gates - OR, AND & NOT gates.
2) Universal Gates - NAND & NOR gates.
3) Parity Gates - Exclusive-OR & Exclusive-NOR gates

Equipment Required

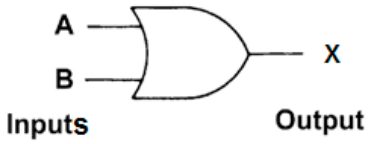
1) Basic Logic Gates Trainer kit.
2) Set of patch cords

Procedure of Experiment

1) Connect power adapter to the kit as well as to AC mains and switch on power
2) Connect the two logic input switches on the trainer kit to the OR circuit A and B points with patch cords
3) Feed logic inputs in a sequence as given in truth table.
4) Verify the output of OR with the help of LED connected to it.
5) Record the outputs and then compare them with the expected ones.
6) Repeat the same steps for all other gate circuits.

1) BASIC GATES

(a) OR Gate



X = A + B

OR Gate Symbol Logic Equation

Inputs		Obtained Output	Expected Output
A	B	X = A+B	
0	0		0
0	1		1
1	0		1
1	1		1

Truth Table-1

(b) AND Gate

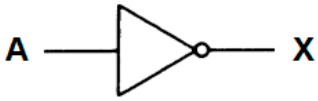
X = A.B

AND gate symbol Logic Equation

Inputs		Obtained Output	Expected Output
A	B	X = A . B	
0	0		0
0	1		0
1	0		0
1	1		1

Truth Table-2

(c) NOT Gate



$X = \overline{A}$

NOT gate symbol Logic Equation

Inputs	Obtained Output	Expected Output
A	$X = \overline{A}$	
0		1
1		0

TruthTable-3

2) UNIVERSAL GATES

(a) NAND Gate

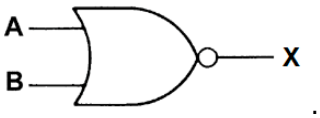
$X = \overline{A.B}$

NAND gate symbol Logic Equation

Inputs		Obtained Output	Expected Output
A	B	$X = \overline{A.B}$	
0	0		1
0	1		1
1	0		1
1	1		0

Truth Table-4

(b) NOR Gate



$X = \overline{A+B}$

NOR gate symbol Logic Equation

Inputs		Obtained Output	Expected Output
A	B	X = A+B	
0	0		1
0	1		0
1	0		0
1	1		0

Truth Table-5

Review Questions

1) Which gates are called as Basic Logic gates and why?

2) What is the advantage with Universal gates?

3) Draw in the below space the circuit used for AND gate on the trainer kit.

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Experiment No. DE-3

DEMORGAN'S THEOREMS & UNIVERSAL GATES

Objective

To Verify DeMorgan's Theorems and Functions of Universal Gates

Introduction

Augustus De Morgan, an English mathematician, discovered two important theorems known as **De Morgan's Theorems or laws.** He was the first person to acclaim George Boole's great achievement, the **Boolean Algebra**. Most mathematicians ignored Boolean Algebra when it first appeared and some even ridiculed it. But Augustus De Morgan realized that it offered profound insights into logic mathematics. De Morgan had actually paved the way for Boolean Algebra by discovering De Morgan's theorems.

DEMORGAN'S THEOREMS

1) $\overline{A + B} = \overline{A} \cdot \overline{B}$

2) $\overline{A \cdot B} = \overline{A} + \overline{B}$

Devices Available on the Trainer Kit

1)	7400	Quad Nand Gate	1 No
2)	7402	Quad Nor Gate	1 No
3)	7404	Hex Inverter	1 No

4) LOGIC Inputs Switches 4 Nos

5) LED Driver with 7404 4 Nos

1) Verification of DeMorgan's First Law

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

The left hand side term in this equation is the Boolean equation of NOR gate. According to this law the logic outputs of the following two gates are same for the same inputs. The logic equivalent for this theorem is the below given figure.

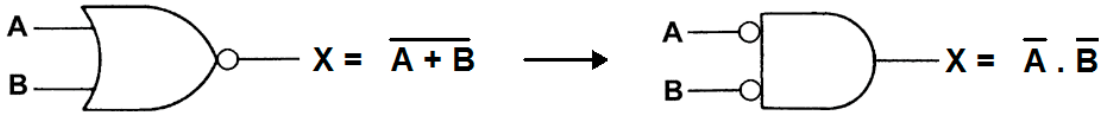

Fig. 1- DeMorgan's 1st Law

Now let us verify or prove correctness of this theorem. Follow the procedure given below.

Procedure:

1) Connect two logic switches to the inputs of one of the NOR gates
2) Connect output of NOR gate to LED driver.
3) Feed logic inputs to NOR gate and record its outputs as per its truth table (Table-1)
4) Now connect two NOT gates to the inputs of a AND gate as shown in fig.1
5) Feed logic inputs to A,B terminals as given in Table-2
6) Record in Table-2, all output values of AND gate for each input combination
7) Compare the outputs in both the tables and these two should be same.

INPUTS		OUTPUT
A	B	$X = \overline{A + B}$
0	0	
0	1	
1	0	
1	1	

Table-1

INPUTS		OUTPUT
A	B	$X = \overline{A} \cdot \overline{B}$
0	0	
0	1	
1	0	
1	1	

Table-2

2) Verification of DeMorgan's Second Law

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

The left hand side term in this equation is the Boolean equation of NAND gate. According to this law the logic outputs of the following two gates are same for the same inputs. The logic equivalent for this theorem is the below given figure.

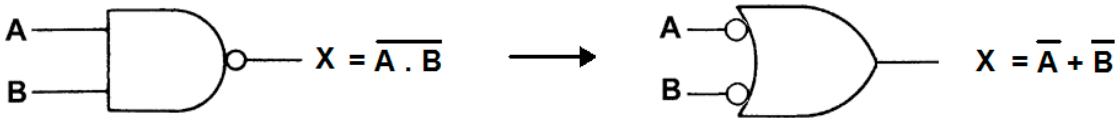

Fig.2- DeMorgan's 2nd Law

Let us verify this equation two to find out the correctness of the theorem. Follow the below given procedure.

Procedure:

1) Connect Two logic switches to the inputs of one of the NAND gates
2) Connect output of NAND gate to LED driver.
3) Feed logic inputs to NAND as shown in Table-3 and record its outputs
4) Now connect two NOT gates to the inputs of an OR gate as shown in fig.2
5) Feed logic inputs to A,B terminals as given in Table-4
6) Record in Table-4, all output values of OR gate for each input combination
7) Compare the outputs in both the tables and these two should be same.

INPUTS		OUTPUT
A	B	$X = \overline{A \cdot B}$
0	0	
0	1	
1	0	
1	1	

Table-3

INPUTS		OUTPUT
A	B	$X = \overline{A} + \overline{B}$
0	0	
0	1	
1	0	
1	1	

Table-4

3) Verification of Universal Gate Functions

1) Make connections as shown in fig.3 for using a NOR gate for inverter
2) Verify its function by feeding logic inputs
3) Now connect two NOR gates as shown in fig.4 for availing OR function
4) Verify its function by feeding logic inputs

5) Connect three NOR gates as in fig. 5 and verify for AND function
6) Did you get all Basic logic functions successfully from only NOR gates?
7) Now replace NOR with NAND in the below figures and verify their logic functions

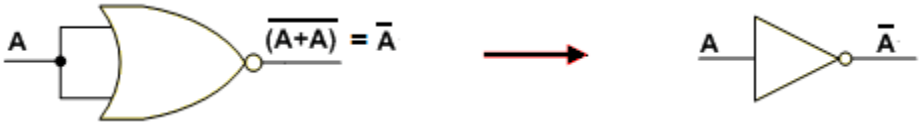

Fig.3 - Implementing an Inverter Using only NOR Gate

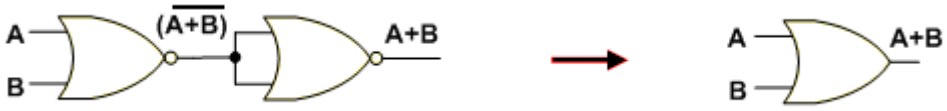

Fig.4 - Implementing OR Using only NOR Gates

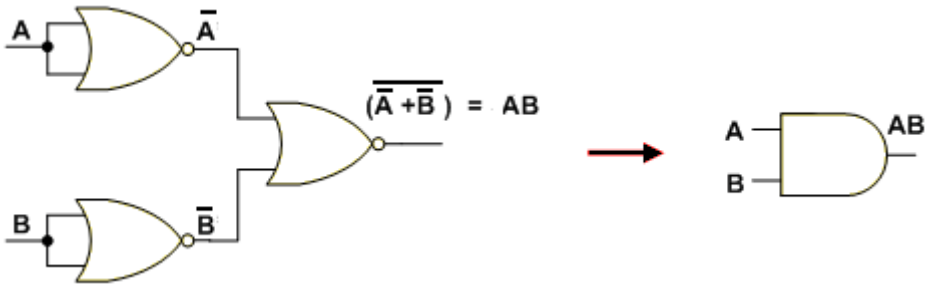

Fig.5 - Implementing AND Using only NOR Gates

Review Questions

1) What did you understand from the DeMorgan's theorems and universal gates?

2) Write the equivalent logic terms for the following using DeMorgan's Theorems

a) $\overline{A+B+C}$ =

b) $\overline{A.B.C.D}$ =

c) $\overline{(A+B)} \cdot \overline{(C+D)}$ =

d) $\overline{(A.B)} + \overline{(C.D)}$ =

e) $\overline{A + \overline{BC}}$ =

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Experiment No. DE-4

FLIP FLOPS

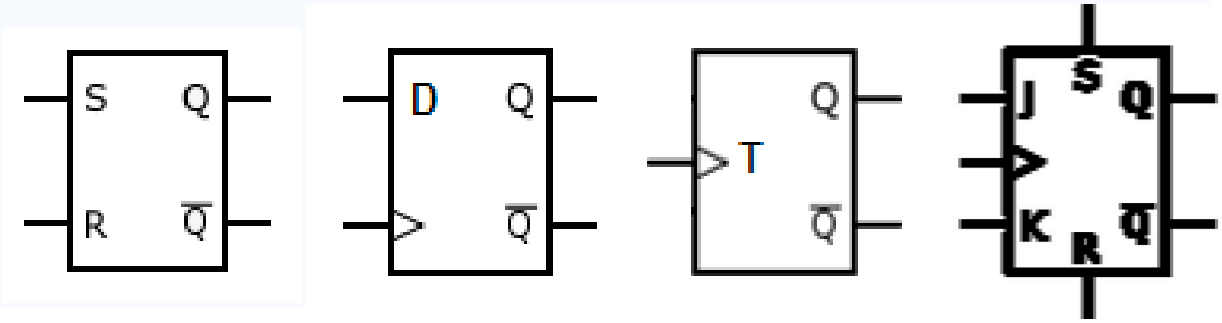
Objective of Experiment

To study the functioning of SR, D, T and JK Flip Flops.

Introduction

In digital electronics, a **flip-flop** is a very vital device and it forms the basic building block for number of sequential logic devices like registers, counters etc. A **flip-flop** is a device that has **two stable output states**. This means, it is a **bistable** device whose function is similar to that of a bistable multivibrator. Due to this property it can be used as a **basic memory element** or **storage cell** which is capable of storing a single bit of data, a 0 or a 1

A flip-flop is usually controlled by **one** or **two input signals** and/or a **clock** (or gate) **signal**. It has two outputs named **Q**, the normal output and $\overline{Q}$, its complement. The two stable states of the flip flop are known as **Set** and **Reset**. When Q is High it is called **Set** state and when Q is Low it is called **Reset** state. The symbols of different types of flip flops are shown below. The **arrow marked** input line is the **clock input** in these symbols.



SR- Flip Flop D- Flip Flop T- Flip Flop JK – Flip Flop

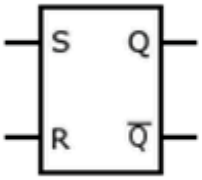
Logic Symbols of Flip Flops

SR Flip Flop

SR Flip Flop is the simplest and basic form among all the flip flops. It has two input lines, S (Set) and R (Reset) as shown in figure above. As their names indicate, these inputs are used one at a time either to SET or to RESET the flip flop, respectively. But very important is, **both the inputs should not be high simultaneously** which leads to **illegal operation** of the SR flip flop. Here in the kit there is no SR flip flop. But we can avail SR function from either IC 7474, D flip flop or IC7476, JK flip flop.

1) Procedure to study SR Flip Flop Operation (using IC7474 or IC7476)

a) Select two logic switches and keep them in High state
b) Connect the two switches outlets to the $\overline{S}$ and $\overline{R}$ erminals of D or JK Flip Flop
c) Also connect the Q and $\overline{Q}$ outputs of the flip flop to two LED drivers
d) Connect power supply adapter and switch ON the trainer kit.
e) Now using logic switches feed logic inputs as given in table-1 and
f) Record the flip flop output states in the same table for each input state.
g) The table will let you know the logic function of SR Flip Flop



S.No	$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	Name of State
1	**1**	**1**			
2	**0**	**1**			
3	**1**	**0**			
4	**0**	**0**			

Symbol of SR-Flip Flop

Table-1 - Truth Table of SR- Flip Flop

Review Question-1: What the last input condition in the table is called as and why so?

Answer:

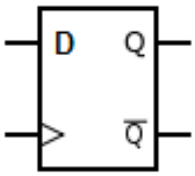
D Flip Flop

In a D Flip Flop the Q output always assumes the state or value available on its D input at the time of application of a clock pulse. For this reason, It is called the **D** flip-flop since the output takes the value of the **D** input or ***Data*** input. Generally, D flip flops are designed to trigger the output changes at one of the clock edges (a rising or falling edge). The D flip-flop can be interpreted as a **basic memory or storage cell.**

2) Procedure to study D Flip Flop Operation

a) Connect one logic switch outlet to the D terminal on D Flip Flop (IC 7474)
b) Connect clock output of pulser (Below yellow terminal) to clock terminal of flip flop
c) Connect the Q and $\overline{Q}$ outputs of D flip flop to two LED drivers
d) Now feed logic inputs on D input , as given in table-2 , using logic switch

e) Apply clock pulse by pressing push button of pulser
f) Record the flip flop output levels in the table for every input state.
g) The values in the table show the functioning of the D Flip Flop



Symbol of D-Flip Flop

S.No	Clock	D	Q	$\overline{Q}$	Name of State
1	**Low**	**X**			
2	**High**	**1**			
3	**High**	**0**			

Table-2 - Truth Table of D- Flip Flop

Review Question-2: Mention the input levels to be fed on SR lines of the given D Flip Flop while using as D Flip Flop

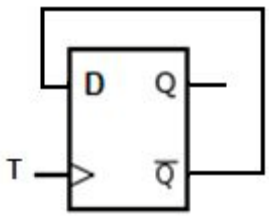
Answer:

T Flip Flop

A T- Flip Flop (Toggle Flip Flop) is one more type of flip flop which **inverses** or **toggles** its output state on the application of every input clock pulse. T- flip flop are used for designing binary counters.

3) Procedure to study T Flip Flop Operation

a) Make interconnection between **D** and $\overline{Q}$ as shown in the below figure, on IC 7474, to convert the D flip flop into a T Flip Flop
b) After making this connection the clock input lead acts like T input of a T flip flop
c) Connect this T lead to the push button pulser and apply clock pulses one by one at a slow rate and observe the changes on **Q** output.
d) It **toggles** with every clock pulse applied
e) This is nothing but a T flip flop operation



D- Flip Flop operated as T- Flip Flop

S.No	T	Q	$\overline{Q}$	Name of State
1	_⊓_			
2	_⊓_			
3	_⊓_			
4	_⊓_			

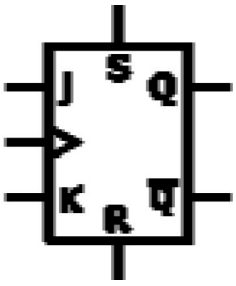
Table-3 - Truth Table of T- Flip Flop

JK Flip Flop

A JK Flip Flop is considered as the most versatile and very useful flip flop among all flip flops because it offers the functions of both an SR flip flop and a T-flip flop. It replaces the unwanted **illegal input condition** of SR flip flop with a useful **toggle mode**. Like the SR flip-flop, it has two data inputs, J (set) and K (reset), and a clock input. Using J and K inputs it can either be set or reset or remain in a previous state thus offering an SR function. When both J and K are in **High** state it works like a T flip flop. With a slight alteration it can also give the function of a D flip flop. Therefore, a JK flip-flop is a universal flip-flop, because it can be configured to work as an SR flip-flop, a D flip-flop, or a T flip-flop.

4) Procedure to study JK Flip Flop Function

a) Connect two logic switch outlets to the J& K terminals on JK Flip Flop (IC 7476)
b) Connect clock output of pulser (yellow or green) to clock terminal of flip flop
c) Connect the Q and $\overline{Q}$ outputs of JK flip flop to two LED drivers
d) Now feed logic inputs on JK terminals in the same sequence as given in table-3
e) Apply clock pulse by pressing the push button of pulser
f) Record the flip flop output states in the table for every input state.
g) Observe on which edge of clock pulse the output is changing
h) The values in the table show the actual functioning of a JK Flip Flop
i) Identify different modes of operation of JK flip flop in the table and record them in the last column



JK-Flip Flop Symbol

S.No	Clock	J	K	Q	$\overline{Q}$	Name of State
1	**Low**	**X**	**X**			
2	**High**	**X**	**X**			
3	_⊓_	**0**	**0**			
4	_⊓_	**0**	**1**			
5	_⊓_	**1**	**0**			
6	_⊓_	**1**	**1**			
7	_⊓_	**1**	**1**			
8	_⊓_	**1**	**1**			

Table-4 - Truth Table of JK- Flip Flop

Review Question-3:

a) What should be the levels on SR inputs while using as JK flip flop?
b) Mention whether the given JK flip flop is a positive edge or negative edge triggered.

Answer:

Review Question-4:

How do you convert the JK flip flop into a T flip flop? Show with a diagram the connection details for the same, in the below given space.

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4-BIT ADDER / SUBTRACTOR

Objective

To study 4-bit BINARY addition and subtraction using adder IC7483.

Introduction

A binary adder/subtractor is a digital circuit which performs the arithmetic operations of **addition** and **subtraction**. This circuit is similar to the ALU unit of CPU in a computer, which can perform all arithmetic and logic operations.

For adding any two multi-bit binary numbers we need as many single bit adders as the bit length of these multi-bit numbers. In the addition process if there is any carry at any bit place it should be added along with the next place bits of the numbers. This makes us to use all full adders for every bit place except in the first bit place where an half adder is sufficient. But if a full adder is used at this place also, the adder assembly becomes flexible and can be used for adding higher bit numbers by cascading two or more such adders. A circuit of a 4 bit adder by using four full adders is shown in fig.1 below.

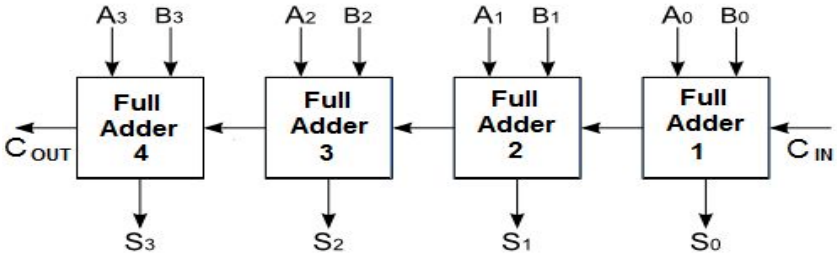

Fig.1 - A 4 bit Adder

Description of 4 bit Adder/Subtractor (Trainer Kit) Circuit

A 4-bit adder- cum- subtractor can be designed using the IC7483 which is only a 4-bit arithmetic adder, but not a subtractor. It comprises of 4 single-bit adders built from four full adders. The terminals A_3 A_2 A_1 A_0 and B_3 B_2 B_1 B_0 are for feeding the first and second 4 bit numbers, respectively, which are to be summed up. The output is available from the 4 sum bits and one carry out bit. While performing addition its carry input (C_{in}) is to be connected to a **Low**. This same IC7483 can also be used for **arithmetic subtraction by using 2s compliment method of addition**. For this we need a circuit arrangement as shown below in fig.2. In subtraction the second input value B which happens to be a negative value must be converted to its 2s compliment form and then added with first number A. The EX-OR gates convert each bit of B into **1s compliment** and then a **'1'** (C_{in} = High) is added to this to produce the **2s compliment of B** which is added to A by 7483 to produce the difference of A minus B. This same circuit is used for either addition or subtraction by using **mode select line** which is connected to one input lead of each EX-OR gate (**M lead** in the fig.2). That is, when **M is Low addition** and when **M is High subtraction** is performed by the same circuit. Thus, this circuit of 4-bit adder/subtractor can be used to add or subtract two nibbles(4 -bit values) at a time.

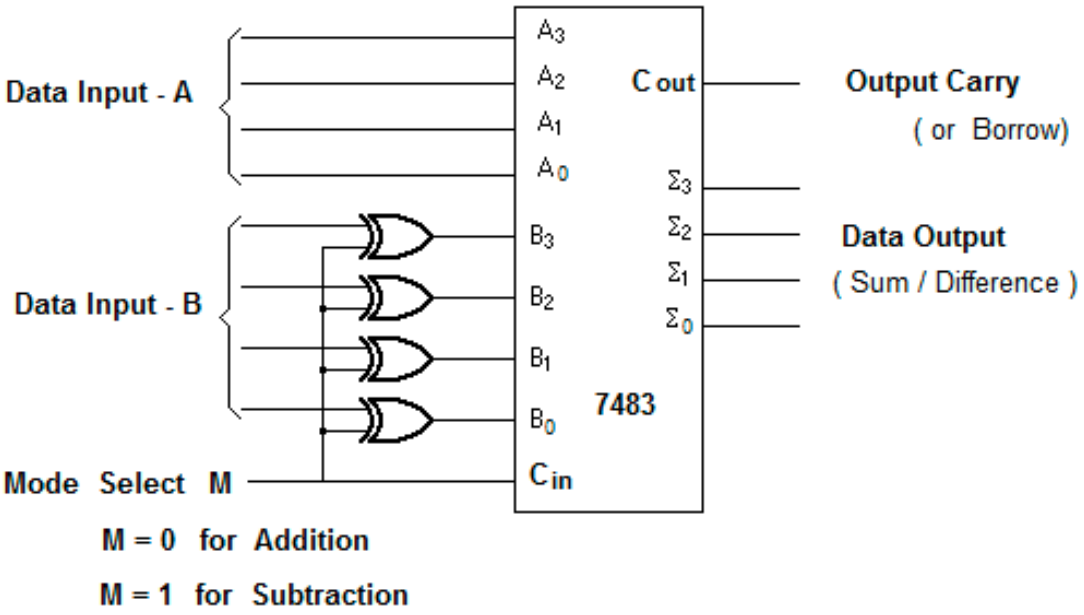

Fig.2 - Adder/ Subtractor Circuit

Equipment Required

1) 4-bit binary full adder/ subtractor trainer kit
2) Its power adopter and
3) Patch cords.

ADDITION

Procedure

1) Connect power adapter one end to kit and other end to the AC mains
2) Switch ON the experimental kit
3) Connect C_{IN} to low for binary addition
4) Feed 4 bit binary inputs using logic switches on A_3 A_2 A_1 A_0 and B_3 B_2 B_1 B_0 terminals.
5) The sum of these two nibbles should appear at terminals $\mathbf{S_3}$ $\mathbf{S_2}$ $\mathbf{S_1}$ $\mathbf{S_0}$, where

$$\mathbf{S_3\ S_2\ S_1\ S_0} = A_3\ A_2\ A_1\ A_0 + B_3\ B_2\ B_1\ B_0$$

6) Record your results in table-1

Table For Addition

C_{IN}	A3	A2	A1	A0	B3	B2	B1	B0	C_{OUT}	S3	S2	S1	S0
0	0	0	0	0	0	0	0	0		0	0	0	0
0	0	0	0	1	0	0	0	1		0	0	1	0
0													
0													
0													
0													
0													
0													
0	1	1	1	1	1	1	1	1					

Table-1

SUBTRACTION

Procedure

1) Connect C_{IN} to High for binary subtraction
2) Feed 4 bit binary inputs using logic switches on A_3 A_2 A_1 A_0 and B_3 B_2 B_1 B_0 terminals.
3) The difference of these two nibbles should appear at terminals $\mathbf{S_3}$ $\mathbf{S_2}$ $\mathbf{S_1}$ $\mathbf{S_0}$, where

$$\mathbf{D_3\ D_2\ D_1\ D_0} = A_3\ A_2\ A_1\ A_0 - B_3\ B_2\ B_1\ B_0$$

4) Record your results in table-2

Table For Subtraction

C_{IN}	A3	A2	A1	A0	B3	B2	B1	B0	B_{OUT}	D3	D2	D1	D0
1	0	0	0	0	0	0	0	0		**0**	**0**	0	0
1	0	0	1	1	0	0	0	1		**0**	**0**	1	0
1													
1													
1													
1													
1													
1													
1													
1	1	1	1	1	1	1	1	1					

Table-2

Review Questions

1) How the adder 7483 is able to perform subtraction in this experiment? Explain briefly.

2) How do you perform an 8 bit addition using 7483 s ?

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Experiment No. DE-6

UNIVERSAL SHIFT REGISTER

Introduction

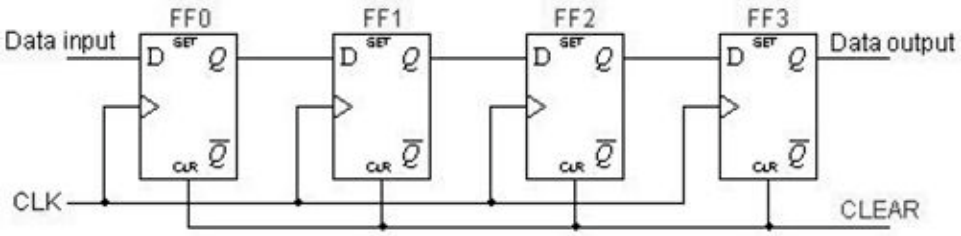
Shift registers are sequential logic circuits meant for storage of digital data, like the memory registers. But, in addition to this the stored data can be shifted one bit at a time in any direction in shift registers. There are different types in shift registers, like **shift right, shift left** and **parallel load**.

- In right/left shift registers the data is fed to the input of first/last flip flop and then it is shifted into the register by single bit wise with every clock pulse applied.
- In parallel shift registers all the bits of input data are applied to the input lines at a time. Then by applying a single clock pulse all these bits are loaded into the register simultaneously. Even if the data changes at the inputs it is not recognized until the next clock pulse is applied.

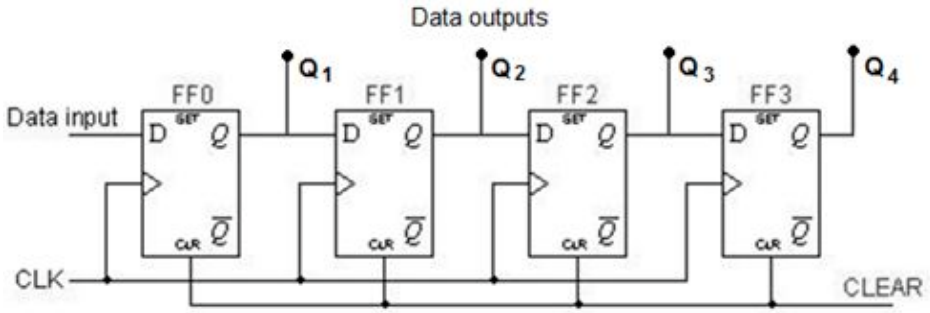
The basic types of shift registers are:

1) Serial In - Serial Out, (SISO)
2) Serial In - Parallel Out, (SIPO)
3) Parallel In - Serial Out, (PISO)
4) Parallel In - Parallel Out, (PIPO) and
5) Bidirectional shift registers.

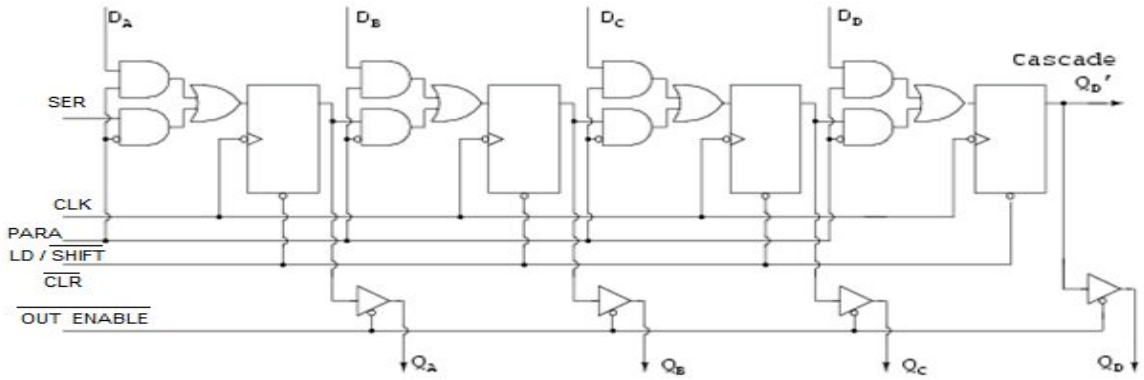
The diagrams in fig.1 show the construction of a serial-in serial -out , serial-in parallel-out and parallel in parallel out shift registers using flip flops.



Serial - In Serial - Out Shift Register (SISO)



Serial - In Parallel - Out Shift Register (SIPO)



Parallel - In / Parallel-Out shift Register (IC 74LS395)

Fig.1- Types of Shift Registers

74194 - Universal Shift Register

74194 is a 4 bit bidirectional shift register with both parallel loading and serial loading capability. It means data can be loaded into this register either in **parallel mode** or in **serial mode** with both **shift right** and **shift left** functions. Because of this it is called a universal shift register. The universal shift register IC 74194 has four distinct modes of operation. These are

1) **Parallel Load**
2) **Serial load with Shift Right** (data shifted from Q_0 towards Q_3)
3) **Serial load with Shift Left** (data shifted from Q_3 towards Q_0)
4) **Inhibit** (does nothing)

For selecting these modes of operation two **mode-select pins,** S_0 and S_1 are provided on the IC. The required bit inputs on these two pins for selecting different modes is shown in table-1. 74194 is a 4 bit shift register provided in a 16-pin DIP package. Its outputs are

Q_0 to Q_3. The parallel inputs are applied to D_0 to D_3 pins. In serial mode **Shift right** and **Shift left** inputs are fed to SR and SL pins, respectively.

S.No	S_0	S_1	Mode of Operation
1	**0**	**0**	Inhibit Mode
2	**0**	**1**	Shift Right (Serial Loading)
3	**1**	**0**	Shift Left (Serial Loading)
4	**1**	**1**	Parallel Load

Table-1 - Mode Selection in 74194

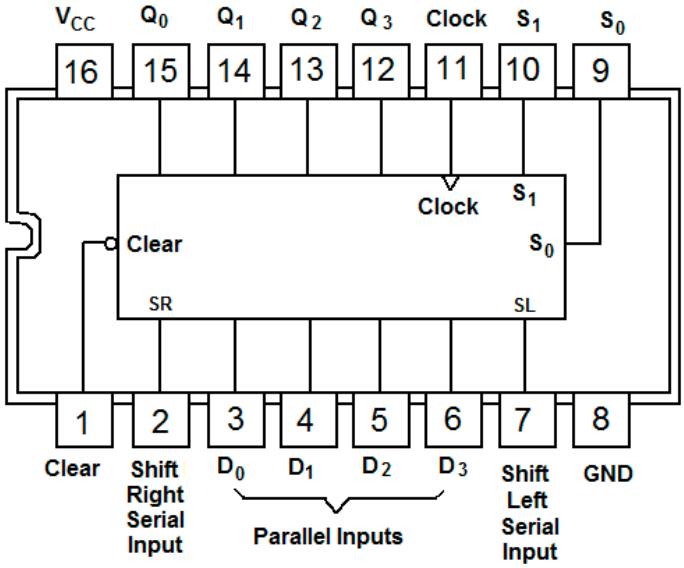


Fig.3 – IC 74194 Pin-out Diagram

EXPERIMENTAL PROCEDURE

1) Connect power adapter to the universal shift register kit
2) Connect yellow terminal (clock output) of pulser to the yellow terminal (clock input) on 74194.
3) Switch on the power to kit.
4) Select **inhibit mode** (S0=0,S1=0) using mode control input switches on the kit
5) Clear the outputs with **master reset switch**
6) Feed any 4-bit parallel input and/or the two serial inputs, then apply a clock pulse
7) Observe what happens. No change should take place in the output bits of 74194

Serial Loading

a) Shift Right

1) Select shift right mode through S0 and S1
2) Clear the outputs Q_0 - Q_3 to 0 using **master reset switch**
3) Feed **shift right input** (pin 2) as given in table-2, using the switch provided on it
4) Apply a clock pulse by pressing and releasing the push button in the pulser circuit
5) Observe the change in outputs and record it the in table -2
6) Then change the logic-1 on shift right input to **logic-0**
7) Apply one clock pulse and observe what happens
8) The logic-1 at Q0 shifts to Q1 and the logic-0 on serial input enters on to Q0 .
9) Similarly apply one more clock pulse and record the changes in the table
10) Load any 4 bit data into the shift register by feeding a single bit input each time and record in the table

Conclusion: The Logic-1(High) bit fed with the first clock pulse keeps on

_____ with each clock pulse applied

S.No	Clock pulse	Shift Right Input	Q0	Q1	Q3	Q4
1	1st _⊓_	1				
2	2nd _⊓_	0				
3	3rd _⊓_	0				
4	4th _⊓_	0				

Table-2

b) Shift Left

1) Select shift left mode through S0 and S1
2) Clear the outputs Q_0 to Q_3 to 0
3) Feed logic-1 to shift left input pin (pin 7) using the switch provided on it
4) Apply a clock pulse by depressing push button in the pulser circuit
5) Record the outputs in table -3.
6) Then change the logic-1 on shift left input to logic-0
7) Keeping logic-0 input slowly apply three more clock pulses and observe outputs
8) The Logic-1(High) bit fed with the first clock pulse keeps on shifting left with each clock pulse applied
9) Record the outputs in the table
10) Similarly try to load any 4 bit data into the shift register by feeding single bit at a time

Conclusion: The Logic-1(High) bit fed with the first clock pulse keeps on

_____ with each clock pulse applied

S.No	Clock pulse	Shift Left Input	Q0	Q1	Q3	Q4
1	1st _⊓_	1				
2	2nd _⊓_	0				
3	3rd _⊓_	0				
4	4th _⊓_	0				

Table-3

Parallel Loading

1) Select Parallel load mode through S0 and S1
2) Connect any 4 bit input to D0 to D3 pins
3) Apply a clock pulse by pressing the push button in the pulser circuit
4) Observe the outputs. They should be same as the 4-bit input fed.

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SYNCHRONOUS BINARY COUNTER

Objective To study a 4 Bit Synchronous Binary Counter

Introduction

A Binary Counter is one of the most used digital devices. Binary counters are mainly of two types. One is **Ripple or asynchronous counter,** slow in counting, and the other is **Synchronous counter**, faster and can be used in high frequency applications.

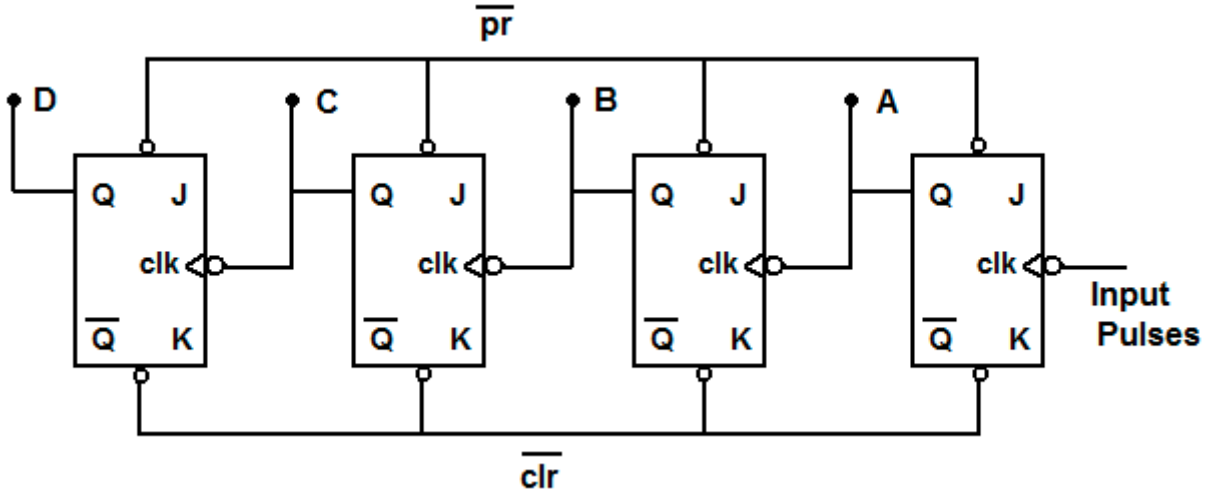

Fig.1 - 4-bit Ripple Counter

A binary counter is designed by cascading either T-flip flops or JK flip flops as shown in the fig.1. The maximum counting capacity (modulus) of a counter depends upon the number of flip flops (or bits) cascaded. Suppose if we have a 4 bit counter which uses four flip flops, the maximum no. of clock pulses that can be counted by

it is $2^4 = 16$. i.e. from 0000 to 1111. Because there are 16 different output states for this counter it is also called as **Modulus -16** counter. **The modulus of a counter is the number of output states it has**.

By making some changes in the design we can produce a counter with any desired modulus, for example a Decade counter which is capable of counting maximum 10 clock pulses only. Hence, it is also called **modulus- 10** counter.

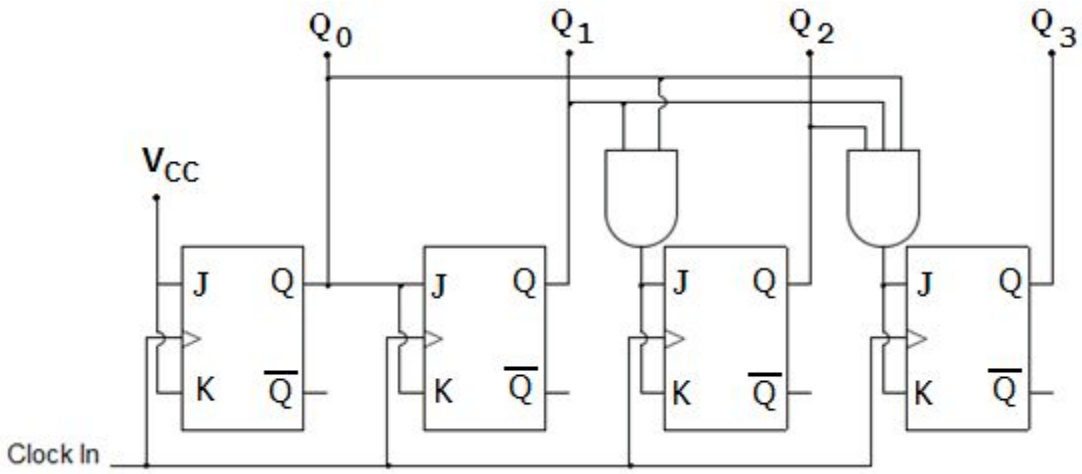

Fig.2 - A 4 bit Synchronous Counter

In this experiment we are going to study the working of a 4-bit synchronous counter using IC 74LS161. This counter has three modes of working

1) Preset mode
2) Count mode
3) Inhibit count mode

These modes are selected as shown in the table-1

MODE	MR (Clear)	CLK	CEP	CET	P_E (Load)
To Clear Outputs	0	X	X	X	X
1) Preset	1	_⊓_	1	1	0
2) Count	1	_⊓_	1	1	1
3) Inhibit counting	1	x	0	x	x
	1	x	x	0	x

Table-1

x - means anything (low or high or a pulse)

EXPERIMENTAL PROCEDURE

1) Connect the power adapter to the trainer and switch on.
2) Connect all the outputs, Q_0, Q_1, Q_2, Q_3 and T_C to logic outputs using patch cords.
3) Clear the counter outputs Q_0, Q_1, Q_2, Q_3 and T_C by connecting MR to Low
4) For **COUNT MODE** connect input switches MR, CEP, CET, P_E to high and clock to mono pulse generator and feed a clock pulse with push button.
5) By applying clock pulses slowly see that the outputs of the counter progress from 0000 through 1111 sequentially.
6) While the counting is progressing, carefully monitor status of T_C.
7) After each clock pulse, record the outputs Q_0, Q_1, Q_2, Q_3 and T_C in table-2 below
8) In **PRESET or parallel load mode** any required initial count value can be loaded into the counter. For doing this connect **MR to high** and the parallel inputs P_0 , P_1, P_2 and P_3 to logic input switches for the required value, say 1001.
9) Connect P_E to low and then apply a clock pulse by pressing push button of pulse generator.
10) Now observe that the input 1001 at P_0 thru P_3 is loaded onto the outputs Q_0 thru Q_3. Try to load different values in Preset mode.

CLK Pulse	**Q_0**	**Q_1**	**Q_2**	**Q_3**	**T_C**
0	**0**	**0**	**0**	**0**	**0**
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					

12					
13					
14					
15					
16					
17					
18					
19					
20					

Table-2

Review Questions

1) When did the T_C change during the counting? And what is the purpose of it ?
2) Observe what happens if each one of MR, CEP, CET, P_E is connected to low and a clock pulse is applied?
3) What is the advantage of a synchronous counter over a binary counter ?
4) Are you successful in loading different preset values in parallel mode?

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Experiment No. DE-8

DECADE COUNTER

Objective

To study the operation of Decade Counter using IC 7490

Description:

A decade counter is designed using four flip flops. That means it is a 4 bit binary counter but with a modulus of 10 only. Generally it is meant for counting in the decimal order, thus resulting in BCD output values. Because of this it is also called as a BCD counter. In every electronic test and measuring equipment, wherein the measured values are to be displayed numerically, the usage of decade counters is compulsory.

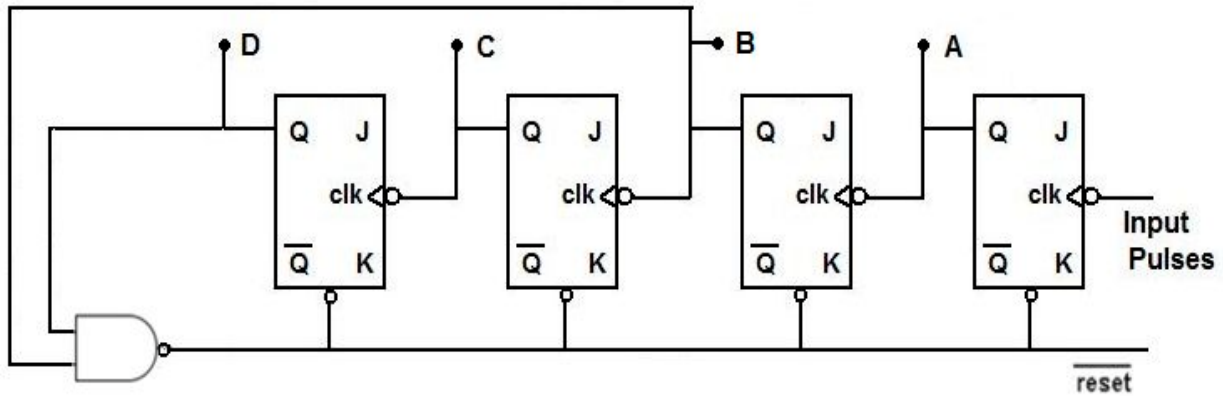

Fig.1 – A decade Counter made of JK Flip Flops

In fig.1 a schematic of a decade counter using four JK flip flops and one NAND gate is shown. It is a ripple counter where the clock pulses are applied to the 1st flip flop A only. The output of every flip flop is connected to the clock input of next flip flop. On application of clock pulses to the counter its count value increments from 0000 through 1001, that is after 9 clock pulses. When a 10th clock pulse is applied the output of the counter would be 1010 but as the high bits of B and D flip flops outputs are connected to the NAND, the counter gets reset immediately. Thus, with 10th pulse the counter is reset to initial value 0000.

Decade Counter - IC 7490

7490- Decade counter consists of 4 flip flops connected as a divided by 2 counter with A_{IN} and A_{OUT} and a divided by 5 counter with BDin and B,C, D outputs. Clock input is applied to A_{IN} and A_{OUT} is connected to BD_{IN} to give a mod-10 counter with outputs A,B,C and D. D_{OUT} is the most significant bit and A_{OUT} is the least significant bit. The flip flops are triggered with the negative edge of the clock transition.

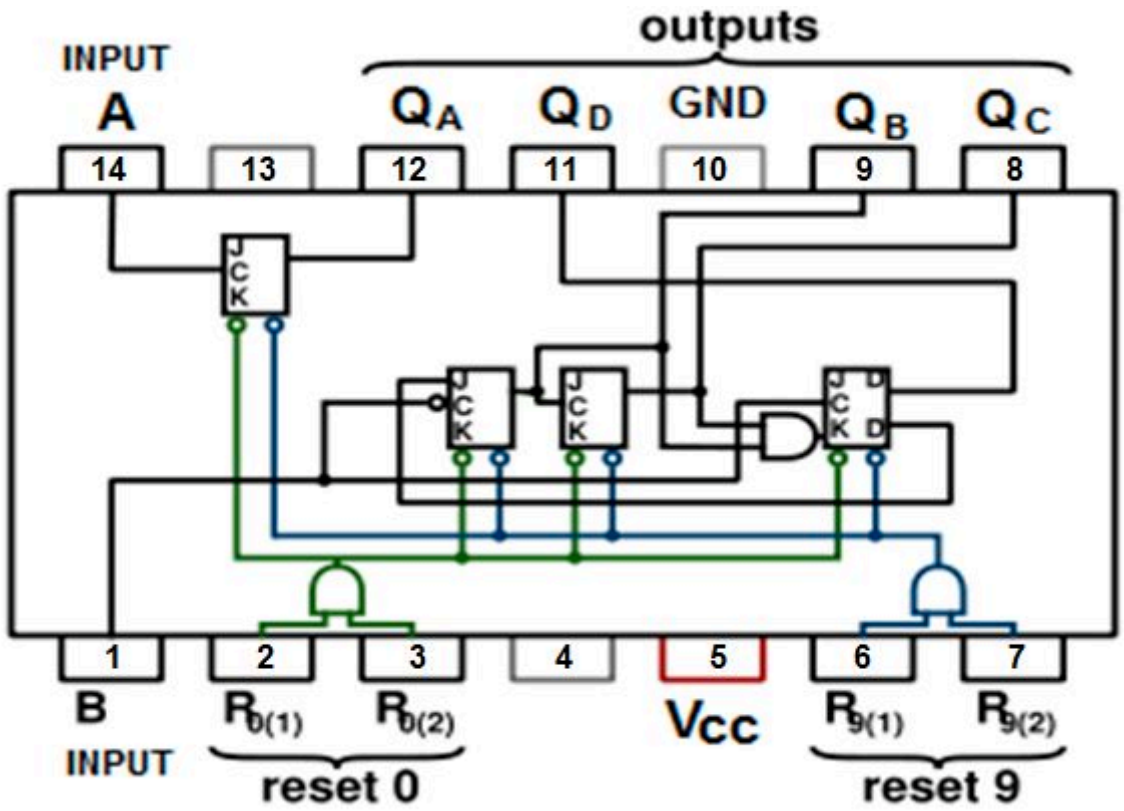

Fig.2 - Pin out and Internal Logic Circuit of IC7490

There are four reset inputs provided on 7490. These are R_{01} & R_{02}, to reset counter to 0 and R_{91} & R_{92} to preset counter to 9. During counting these reset inputs R_{01}, R_{02}, R_{91} & R_{92} should be set in any one of the combinations shown in table-1, on the next page.

S.No.	R_{01}	R_{02}	R_{91}	R_{92}	Mode
1	1	1	1	1	**Count Disable**
2	0	x	0	x	**Count Enable**
3	x	0	x	0	

Table -1

The counter can be **reset to '0'** or **preset to 9** by setting R_{01}, R_{02}, R_{91} & R_{92} as shown below in table-2.

	R_{01}	R_{02}	R_{91}	R_{92}
Reset to 0	1	1	0	0
Preset to 9	0	0	1	1

Table -2

Components Available On Trainer Kit

The trainer consists of the following components

1) Decade counter using IC 7490.
2) Binary to Seven Segment decoder/ driver using IC 7447.
3) 7- Segment common anode type LED display (FND 542)
4) Bounceless pulser.
5) Built in 5 Volts Power supply.

PROCEDURE

1) Connect power adapter to the trainer kit and switch on the power.
2) Reset the counter using R_{01} & R_{02} as per setting given for Reset to **' 0 '** state.
3) Observe the reading on the LED display.
4) Now Preset the counter to **' 9 '** using R_{91} & R_{92} as per the settings given for preset to '9' state
5) Observe the reading on the LED display.
6) Set input to **count enable mode** using R_{01}, R_{02}, R_{91} & R_{92} (connect to low)
7) Connect bounceless pulser output A_{OUT} to clock input A_{IN} of counter (Blue to Blue)
8) Apply clock pulses by pressing and releasing push button of pulser
9) Observe the count sequence on the LED display.
10) Record the findings in the below given table-3.

lock pulse No	R_{01} & R_{02}	R_{91} & R_{92}	Outputs				Display on 7- segment LED
			D	C	B	A	
Preset to 9	00	11					**9**
Reset to 0	11	00					**0**
0	00	00	0	0	0	0	
1	00	00					
2	00	00					
3	00	00					
4	00	00					
5	00	00					
6	00	00					
7	00	00					
8	00	00					
9	00	00					
10	00	00					

Table -3

Review Questions

1) What will be the display on 7-segment LED if all the four reset inputs are high?
2) Do you agree that the outputs from 7490 are only BCD values?
3) What is the need for providing **'preset to 9'** inputs?

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Experiment No. DE- 9

BCD TO 7 - SEGMENT DECODER

OBJECTIVE

Study of BCD to 7-Segement decoder and 7-segment LED display.

INTRODUCTION

In electronic systems and instruments wherever numerical values are to be displayed the 7-segment LED devices are used. The inputs to these display devices must be available in 7-segment form but not in binary. Hence there must be a separate device which can convert the binary codes (ie., the 4 bit BCD codes) used to represent each numerical value in decimal system into 7-segment codes. The IC 7447 does exactly this.

DESCRIPTION

The IC 7447 is a 16 pin device. Its pin-out diagram is shown in fig.1. IC 7447 is called as BCD to 7 Segment Decoder / display Driver. The pin details of 7447 are as below:

- It has four input pins A, B, C, D (shown as A_0, A_1, A_2, A_3 on the kit) for feeding the BCD value of the digit to be displayed.
- It has 7 output pins a , b, c, d, e, f & g which are to be connected to the corresponding pins on a 7-segment LED display.
- There are 3 additional pins LT, RBI and BI / RBO.
- **LT- Lamp Test**. If a low is applied to this pin all segments of LED should glow.
- **RBI - Ripple Blanking Input**. A low on this pin blanks displaying of zero (0).
- **BI / RBO – Blanking Input** & **Ripple Blanking Output**. This pin acts as **input** (BI) as well as **output** (RBO).

NOTE: The main functions **LT, RBI** and **BI/RBO** can be verified in experiment **DE-13**

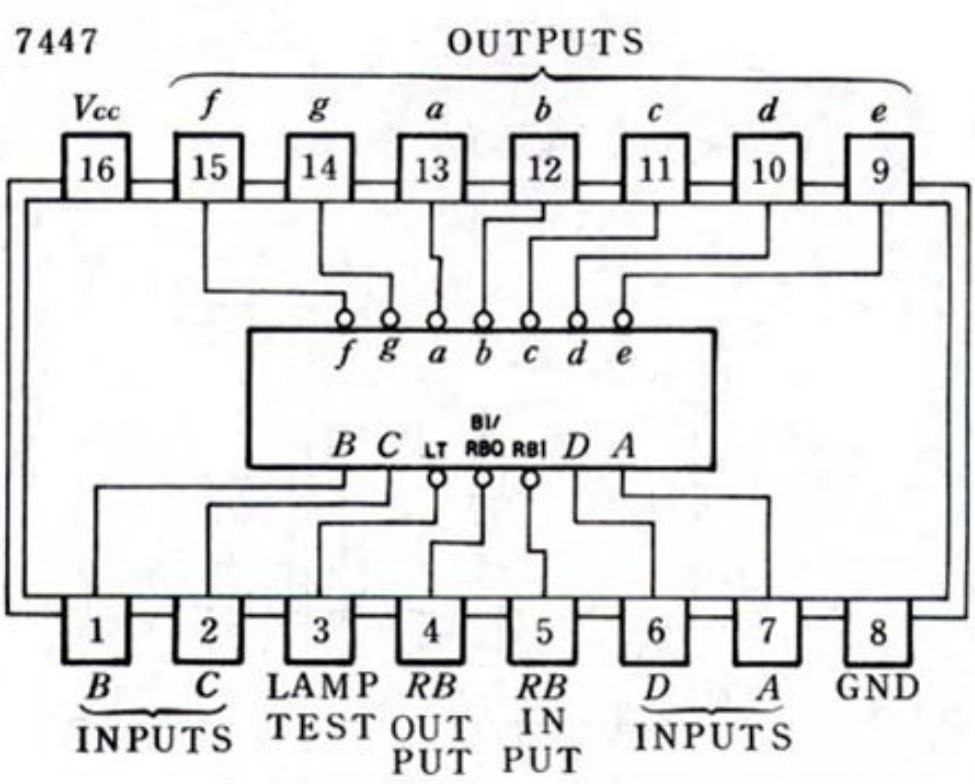


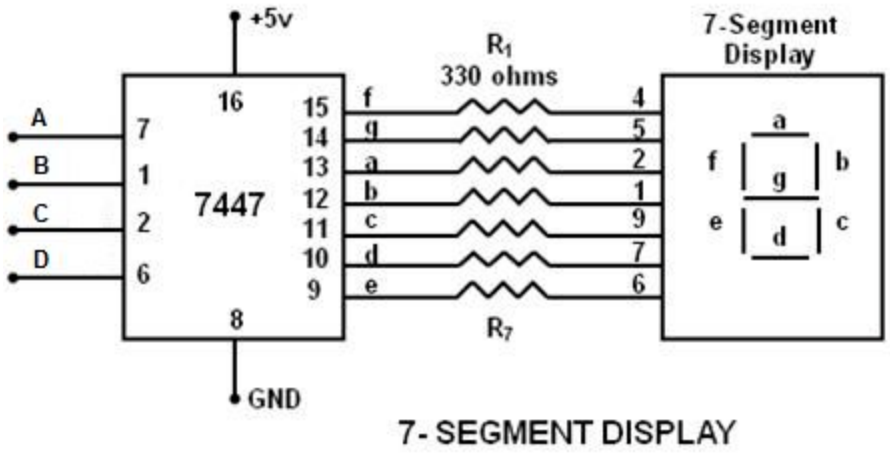
Fig.1 – Pin-out of IC 7447

The BCD input connected on A, B, C, D pins is converted into 7-segment form and outputted through a , b, c, d, e, f & g pins to drive a common anode type 7 segment LED display (LTS – 542 is used in the kit) . Each output lead of 7447 is connected to the corresponding segment of LED display through a current limiting resistor of 330Ω . Whenever the output from 7447 is low the LED connected to that segment lights. For displaying every decimal digit different segments are required to be lit.

The features offered by this device are the following.

FEATURES

1. It has all Open- Collector Outputs.
2. Can Drive LED Segments Directly.
3. Lamp Test Provision.
4. Cascadable Zero – suppression capability. (Means unwanted zeros suppression on the display)



7- SEGMENT DISPLAY

Fig.2 - Connecting 7447 to 7-segment Display

COMPONENTS AVAILABLE IN THE KIT

1) IC 7447
2) 7 - Segment display (CA) - LT542
3) 4 Input logic switches with indicators
4) Built in fixed DC source of +5V.

EXPERIMENTAL PROCEDURE

1. Connect the AC power adapter to the kit
2. Switch ON power to the kit
3. Using the toggle switches, feed 4 bit binary inputs in sequence as given in table-1
4. The BCD input value is indicated by the LEDs connected to the switches
5. A logic 1 is represented by a glow and a logic 0 by no glow.
6. Observe the corresponding decimal number on the 7 - Segment Display.
7. Change the input switches of A_1, A_2, A_3 & A_4 through all the 16 combinations
8. Record in table-1 the LED display output patterns for non-BCD inputs.

S.No.	Binary input	Displayed Digit	Remarks
1	0000	0	
2	0001	1	

3	0010	2	**4 bit BCD values**
4	0011	3	
5	0100	4	
6	0101	5	
7	0110	6	
8	0111	7	
9	1000	8	
10	1001	9	
11	1010		**Non-BCD 4 bit values**
12	1011		
13	1100		
14	1101		
15	1110		
16	1111		

Table-1

Review Questions

1) What is the output signal level required on 7-segment output lines of 7447 to glow the LED segments?

2) What is the function of LT?

3) What is the purpose of RBI and RBO?

4) What type of LED display is used in the kit?

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EVEN/ODD PARITY CHECKER/ GENERATOR

Objective

To study the Even/Odd Parity Checker/Generator using IC 74180.

Introduction

In data transmission systems characters in text messages and numerical data are represented by ASCII codes or some fixed-bit size binary codes. These binary codes are unique for every character. If any single bit in this code changes during transmission then the interpreted character would be different from the transmitted one. This results in errors and in turn may lead to conveying a wrong message or data altogether. To overcome this problem PARITY of bit 1s (the count of number of 1s) in the character code is checked as a measure of the correctness of the data. Parity value may come in ODD numbers like 1,3,5,7,9 or in EVEN numbers like 0,2,4,6,8. And based on this the parity of a byte is called either an **Odd Parity** or **Even Parity**.

First, one **parity scheme** is chosen before the transmission of data. Then each byte or block of received data is checked for the chosen parity. If the parity is satisfied, the byte is accepted as **correct data** otherwise **wrong data**.

Parity Schemes

There are two types of parity schemes:

1) Odd Parity

The stream of data is broken up into **blocks of bits**, and the number of 1 (**High**) bits in each data block is counted. If the **count is not an odd value, then a 1 (High) bit is added to the data block as the " parity bit** " otherwise a 0 (Low) bit is added as the " parity bit. "

2) Even Parity

In Even Parity the required parity bit, to be added to the data bits, will be just opposite to the parity bit which is used in case of odd parity scheme.

Description of 74180

For understanding this parity concept, the experimental kit with IC 74180 is used in this experiment. IC 74180 can be used for both checking and generating parity for 8 bit data. The details of IC 74180 are as given below:

I_0 to I_7 : *8 input lines, for feeding data bits*

P_E & P_O : *Parity enable/ cascading inputs*

ΣE & ΣO : *Even and Odd parity outputs*

The 74180 can be used for both

1) ***Checking the parity*** of input data and also for
2) ***Generating the required parity bit*** which satisfies the overall parity when it is combined with the data bits.

Procedure

I. Parity Checking :

1) Connect P_E to HIGH and P_O to LOW, to select Parity Check Mode
2) Feed any 8 bit data using the 8 switches on input lines **I_0 to I_7**
3) Note down the parity of input data in the table-1 given below
4) Observe the parity output levels shown by LEDs
5) Record these also in the table-1 given below
6) Now, look at your recording in the table-1
7) **Depending on the parity of the input data bits the respective parity output is made HIGH**.
8) Is the same thing you got ? If YES, your results are **CORRECT**.

Parity of 8 bit Input Data	Parity Checker Mode		Parity Check Bits	
	P_E	P_O	ΣE	ΣO
Even	1	0		
Odd	1	0		
Even	1	0		
Odd	1	0		

Table-1

II. Parity Generation :

1) Connect P_E to LOW and P_O to HIGH, to select Parity Generator Mode
2) Feed any 8 bit data with Even and Odd parities alternately, as shown in the table using switches
3) Observe the parity output bits shown by LEDs
4) Record these in the table-2 given below
5) Now check the parity of 9 bits (8 bit input + **ΣE** bit) and record in the table-2
6) Similarly, check the parity of 9 bits (8 bit input + **ΣO** bit) and record it
7) Now, look at your recording in the table-2
8) Does the parity of 9 bits satisfy any required parity ?
9) If YES, your results are **CORRECT** otherwise wrong

Parity of 8- bit Input Data	**Parity Generator Mode**		**Generated Parity Bits**		**Parity of 9- bits Including ΣE**	**Parity of 9- bits Including ΣO**
	P_E	**P_O**	**ΣE**	**ΣO**		
Even	0	1				
Odd	0	1				
Even	0	1				
Odd	0	1				

Table-2

Review Questions

1) What are the modes wherein you can operate 74180 and how do you select these modes?
2) What will you do if it is required to check the parity of more than 8 bit data ? Show with a sketch how to make a **16 bit parity checker / generator** using 74180s.

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Experiment No. DE-11

DECIMAL TO BINARY ENCODER

Objective

To study a Decimal to Binary (BCD) Encoder

Description

An encoder is a device which converts information from one format or code to another format or code. An Encoder has multiple input lines, like a multiplexer. It also has multiple output lines but less in number than the input lines. The general relation between the input and output lines is:

*If there are **'n'** output lines on an encoder, its input lines may be **2^n** or less.*

Encoders are available to encode either a **decimal** or **hexadecimal** input to a **binary** or **BCD** output code.

Decimal To Binary Encoder

A decimal to binary encoder is a device which converts a **decimal input** to a **binary output.** The figure and table-1 given on the next page show the **logic symbol** and the **truth table** of a **decimal to binary encoder**, respectively. There are 9 decimal input lines which are shown as 1, 2, 3,…and 9. The binary output lines are four Q_0 to Q_3. This device is implemented through combinational logic. Number of logic gates are used in the circuit which is shown on the trainer kit provided with this experiment.

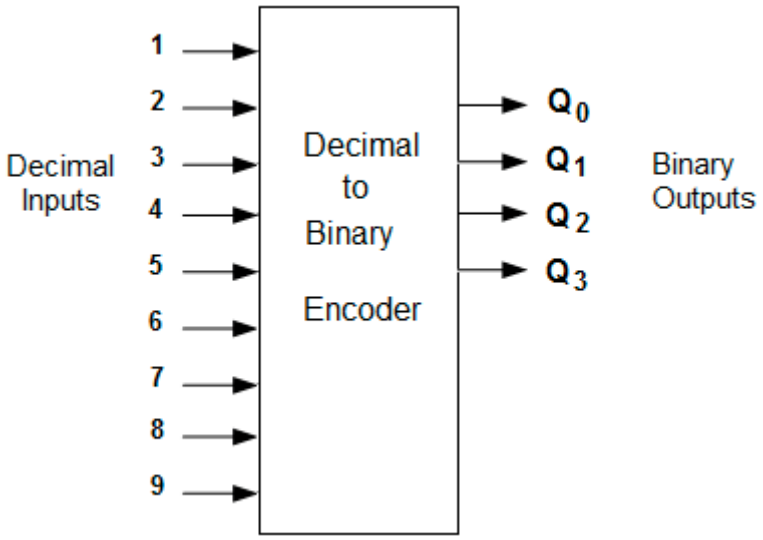

Fig. - Logic Symbol of Decimal to Binary Encoder

S No	DECIMAL INPUTS										BINARY OUTPUTS			
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	Q_3	Q_2	Q_1	Q_0
1	✓	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	✓	0	0	0	0	0	0	0	0	0	0	0	1
3	0	0	✓	0	0	0	0	0	0	0	0	0	1	0
4	0	0	0	✓	0	0	0	0	0	0	0	0	1	1
5	0	0	0	0	✓	0	0	0	0	0	0	1	0	0
6	0	0	0	0	0	✓	0	0	0	0	0	1	0	1
7	0	0	0	0	0	0	✓	0	0	0	0	1	1	0
8	0	0	0	0	0	0	0	✓	0	0	0	1	1	1
9	0	0	0	0	0	0	0	0	✓	0	1	0	0	0
10	0	0	0	0	0	0	0	0	0	✓	1	0	0	1

Table-1 - Truth table of Decimal to Binary Encoder

In the experimental kit provided for performing this experiment the following items are present

1) There are 9 input switches each representing 9 decimal digits from 1 to 9.
2) These 9 switches are connected to 9 LEDs.
3) When these switches are in 0 position the LEDs glow and in 1 position LEDs go OFF

4) If any one of these switches is changed from 0 to 1 its value is encoded or translated into 4 bit binary by the **encoder** circuit and fed to 4 output LEDs.
5) Each switch represents one decimal digit sequentially, starting from 1 on top to 9 in the bottom.
6) The decimal 0 input is automatically available when all switches are in 0 position.

Procedure

1) Connect the AC power adapter and switch on the kit
2) Keep all switches in 0 position
3) Observe the 9 input LEDs and 4 output LEDs
4) All input LEDs should glow and output LEDs should be OFF
5) Change the 1st switch on top to position - 1
6) Observe the status of 4 output LEDs
7) Record the status of these LEDs in the table-2 below (Glow = 1 and No-glow = 0)
8) Put back 1st switch to 0 position
9) Then change 2nd to 1 position
10) Observe the output on the 4 LEDs and record it in the table-2
11) Put back 2nd switch to 0 and change 3rd switch to 1
12) Record the LED output in the table-2
13) Repeat this processes for all the switches one by one
14) After completing for all switches, examine the output binary codes in the table-2
15) These codes should be the BCD codes of decimal digits

Decimal Input (Switch operated)	**Binary Output** (Output LEDs status)
0 (all switches off)	
1	
2	
3	
4	
5	
6	
7	
8	
9	

Table -2

Review Questions

1) Why there is no input switch in the kit to represent the decimal digit 0 ?
2) What ICs are used in the circuit of this kit ? Write their numbers and functions.
3) Mention some applications of Decimal to Binary Encoder

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Experiment No. DE-12

BINARY (BCD) TO DECIMAL DECODER

Objective

To study a Binary to Decimal decoder circuit using 7442 IC.

Introduction

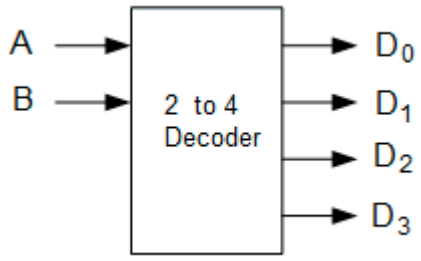
A **Decoder** is the exact opposite of an "Encoder" which was studied about in the last practical session. The decoder is basically, a combinational logic circuit that **converts a binary data,** fed on its input lines, into an **equivalent decimal value** represented by one of its number of discrete output lines. **Binary Decoders** have input bit sizes of 2-bit, 3-bit, 4-bit etc., depending upon the number of data input lines. An **"n-bit"** decoder has $\mathbf{2^n}$ output lines. Typical combinations of decoders include, 2-to-4, 3-to-8 and 4-to-16 line configurations. Binary Decoders are available to "decode" a Binary or BCD input into a Decimal output value. The relation between the input and output lines of decoder is:

If there are 'n' input lines on a decoder, its output lines will be $\boldsymbol{2^n}$***.***

A decoder is the most extensively used device in memory chips, multiplexers & demultiplexers, microprocessors etc. In memory chips decoders are used as M**emory Address Decoders** for selecting the individual memory registers, one at a time.

For understanding the actual logic of a decoder let us look at a 2 to 4 line decoder which is shown below in Fig.1 which shows the logic symbol and the truth table of a 2 to 4 line binary decoder. In fig.2 the actual circuit diagram using combinational logic for implementing the 2 to 4 line binary decoder is shown.

A 2-to-4 line Binary Decoder



A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Fig.1

In this simple example of a 2-to-4 line binary decoder, the binary inputs A and B determine which output line from D_0 to D_3 is "HIGH" or at logic level "1" while the remaining outputs are held "LOW" or at logic "0". Therefore, which output line is "HIGH" identifies the binary code present at the input lines. In other words it "decodes" the binary input fed on its input lines A and B.

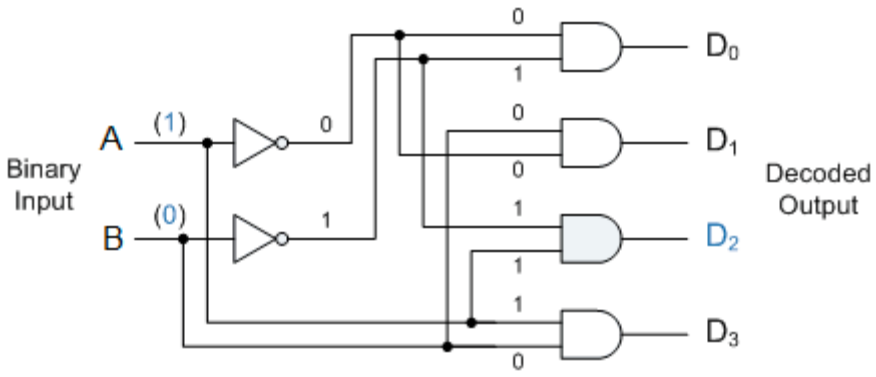


Fig.2 Circuit of a 2 to 4 Decoder

Trainer Kit Description

The IC 7442 is a BCD to Decimal decoder. Its function is to decode a 4-bit BCD number to one-of-ten decimal outputs. Actually a 4 bit decoder can accommodate 24 or 16 outputs. But 7442 being a BCD decoder there are only 10 output lines representing the decimal digits 0, 1, 2, …, 9. The 4 binary/ BCD inputs are labeled as A, B, C and D, and 10 decimal outputs as 0, 1, 2,------8, and 9.

Components on the kit

1) IC 7442
2) Four toggle switches to feed BCD vales
3) Ten LED indicators to indicate the status of decimal outputs.

Experimental Procedure

1) Switch ON the experimental board by connecting power cord to the AC mains.
2) Keep all the four input switches A, B, C, D in 0 position.

3) Verify the output value with the help of LEDs
4) This should indicate decimal 0
5) Now feed all BCD values one after the other in sequential order
6) Verify the corresponding output values through LED indicators
7) Record both inputs and outputs in the table given below

Binary (BCD) Input on A B C D				**Decimal Output On LEDs**
D	**C**	**B**	**A**	
0	**0**	**0**	**0**	**0**

Review Questions

1) Feed the 4-bit binary values beyond BCD codes using ABCD inputs to 7442 and note down your observation on output LEDs.

2) What is the difference between a general 4 bit binary decoder and this 7442 decoder.

3) Mention a few applications of a BCD to decimal decoder.

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3- DIGIT DECADE COUNTER

Objective

a) To construct and study the operation of 3-digit decade counter using three 7490 decade counting units.
b) To verify the functions of LT, RBI and BI / RBO pins of IC 7447, the display driver.

Introduction

It is already observed in the previous experiment DE -8 that how a decade counter is used for counting clock pulses in decimal order. Now, In this practical session we study how a full fledged multi digit counter is designed with the help of 7490s and 7447s. For constructing a 3 digit decimal counter the devices used are

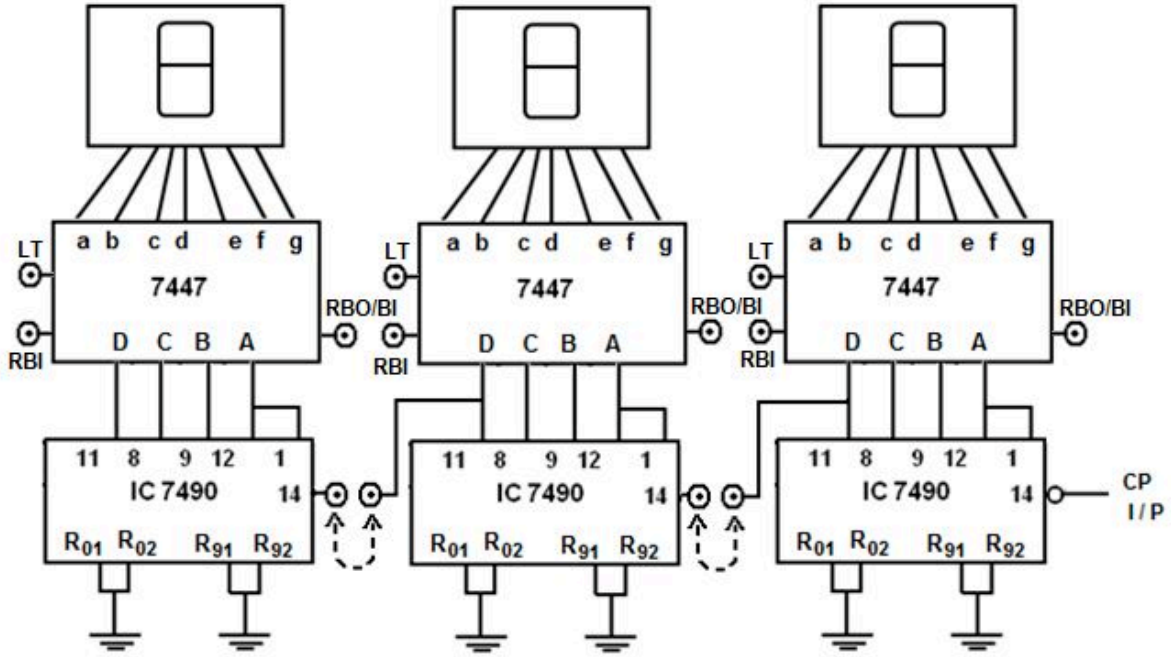
1) Decade counter IC 7490s 3Nos
2) BCD to Seven Segment decoder/driver IC 7447 3Nos
3) 7 Segment common anode type LED display (LT 542) 3Nos

These devices are to be interconnected as shown in the below given figure for constructing a 3 digit decimal counter. This is the same like what we have seen in the experiment DE-8. But the only change is the same circuit is triplicated by providing three independent single digit decade counters. With help of these three independent counters there is a flexibility to have either

1) 3 single digit counters or
2) A 2-digit counter or
3) A 3-digit counter

just by cascading the individual units. The cascading is done by connecting the output D of previous stage (pin 11) to the clock input of next stage (pin 14) on 7490 ICs.

a) Construction & Study of 3 Digit Counter



Procedure

1) Switch ON the experimental board by connecting power cord to AC mains.
2) Connect the clock generator output to CP I/P (clock input) terminal of LS digit counter. (Red to Red)
3) Reset the count to 000 by pushing the Set/Reset switch to RESET and then back to SET.
4) Feed clock pulses to counter input by changing the Start/Stop Switch of clock generator to START position.
5) Observe the counting on the display.
6) Now, cascade the individual counting units by shorting adjacent yellow terminals
7) Observe the counting on the display
8) Notice that the counting proceeds from 000 towards 999 and then repeats.

Review Questions-1

1) Name some applications of decade counters which you have seen.

2) Interconnect first two stages of counters and observe what would be the value on the display if a clock pulse is applied after a display of 99.

3) During which edge of the clock pulse the 7490 triggers and counts ?

b) Verification of LT, RBI and BI / RBO Functions of IC 7447

The functions of the pins LT, RBI & BI / RBO of 7447 are as shown in the table below.

S.No	LT	RBI	BI/ RBO	Function
1	0	1	1	Lamp test . All 7-segments are lit
2	1	0	1	Digit 0 (Zero) is not displayed (blanked). But digits 1-9 are displayed
3	1	1	0 (As BI input)	All digits 0-9 are blanked.
4	1	1	RBO signal (output)	RBO signal = High, when there is a display of a digit RBO signal = Low, when the display is blank.

Table-1

Procedure

LT-Lamp Test

1) Connect **Low** input to the LT terminal of any one of the digit driver, 7447.
2) Observe what happens. All the 7-segments should glow.
3) This is a test to know whether all segments are lighting or not

BI- Blanking Input

4) Disconnect the low on LT and connect it to the BI terminal of any digit driver
5) Apply clock input pulses to the respective 7490. Observe what happens
6) Nothing is displayed on the LED display. This means the display is blanked.

RBI & RBO Cascading for Blanking Leading- Zeroes

7) Disconnect **low** from BI and connect the low to the RBI pin of MS digit (100s digit) driver IC 7447.
8) And connect the same 7447 RBO terminal to the RBI terminal of next digit on the right.
9) Now cascade all the three 7490s using connecting wires
10) Apply clock pulses to the extreme right (units) position decade counter, 7490.
11) Observe what happens.
12) The leading zeros are blanked on the display while counting is taking place.
13) Now disconnect the low given to the RBI input of 100s (MSD) digit driver.
14) Apply clock pulses and observe the counting.
15) Now the leading zeroes are displayed during counting
16) From these steps the functions of LT, RBI & BI/RBO should be clear to you now.

Review Questions-2

1) What is the function of LT in 7447?
2) What is the difference between BI & RBI functions in 7447?
3) The display on the counter should show the values from 1-99, not from 0-99. How do you get this?

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Experiment No. DE-14

16 LINE DIGITAL MULTIPLEXER & DEMULTIPLEXER

Objective

To study a 16 line Digital Multiplexer and Demultliplexer

Introduction

*A digital **Multiplexer** is a device which facilitates connectivity between many inputs and a single output selectively.* That is, only any one input line at a time can be connected to the output line, by an input selection logic. The below given Fig.1 explains the logic of the multiplexer in a simple manner.

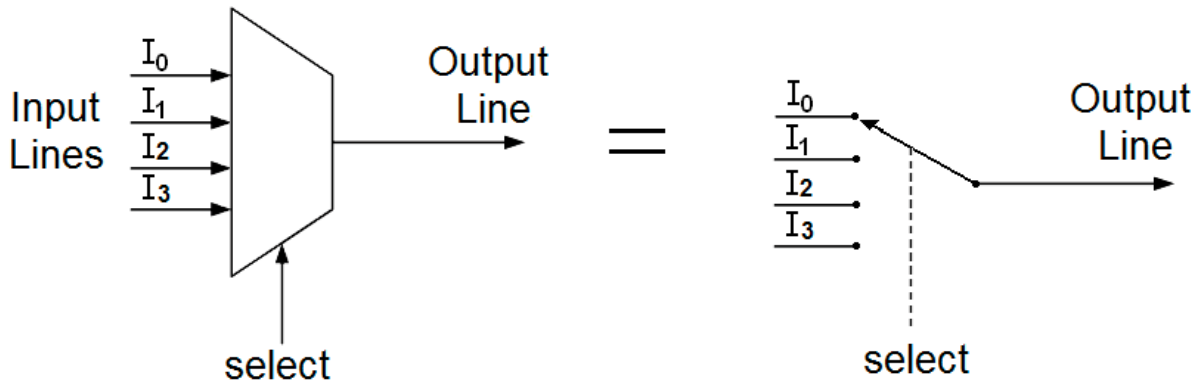

Fig.1 - The Logic of a Multiplexer

In other words it can be stated that "*a **Multiplexer** (or **mux**) is a device that performs **multiplexing**, which means it selects data on one of many input lines and sends it onto a single output line*". For selecting the required data input line it is provided with a selection

logic. A multiplexer of 2^n inputs has **n select bits**, which are used to select which input line to send data to the output.

Description of Mux & Demux Experimental Kit

In this kit the following devices are used.

1) IC 74150 16-to-1 line Multiplexer
2) IC 74154 1-to-16 Demultliplexer.
3) IC 7493 4-bit binary(mod-16) counter. (used as scan signal generator)
4) IC 7400 Quad NAND gate(used as bounce less pulser)
5) IC 7404 Hex Inverter

MULTIPLEXER

The Multiplexer IC 74150 is also known as DATA SELECTOR. The input data bits are D0 to D15. Only one of these is connected to the output at a time. Which one is connected depends on the address placed on the select lines A0- A3. The addresses of the input lines are generated sequentially by applying clock pulses from a pulser to the 4-bit binary counter IC 7493.

a) Experimental Procedure for Multiplexer

1) Power on the unit by connecting AC adapter
2) Connect multiplexer output to the adjacent LED monitor.
3) Ensure that the 4 LEDs on the outputs of Scan Signal Generator are OFF. If not by pressing the push button of bounce less pulser bring them to OFF
4) Now change the switch connected to the input line D_0 between 0 and 1 positions 2 to 3 times
5) You will find the LED monitor is also changing with the changes on switch
6) This means presently the input line D_0 is selected by placing its address on address lines (A_0-A_3) of multiplexer
7) Now feed one clock pulse using the push button of pulser
8) Observe the address on select lines changes to 0001
9) Change the switch on D_0
10) Observe for any changes on output LED. But no change in LED status
11) Now, change the switch on D_1 for 2 or 3 times
12) The output monitor LED changes now along with the switch changes
13) This means input D_1 is connected to the output of the multiplexer
14) Change other switches and observe
15) But you find that none of them is connected to the output
16) Similarly select all other input lines one by one and verify the connectivity with the output line

Review Questions

1) Can a multiplexer be used for implementing different Boolean equations ? If yes show how?
2) Mention some applications of Multiplexer ?
3) Why scan signal generator is required in the kit ?.

DEMULTIPLEXER

*A **Demultiplexer** (or **demux**) performs just opposite operation of a multiplexer. It takes data from a single input line and sends it to a selected line among many output-lines.*

Demultiplexer IC 74154 is used as the counter part of 74150 multiplexer. It has single input line which can be connected to any one of the 16 output lines by selection address. In this kit both these Mux and Demuxs are interconnected as shown in Fig.2 below. Common selection addresses supplied by the counter 7493 so that any input line on the multiplexer is connected to the same numbered output line on the demultiplexer.

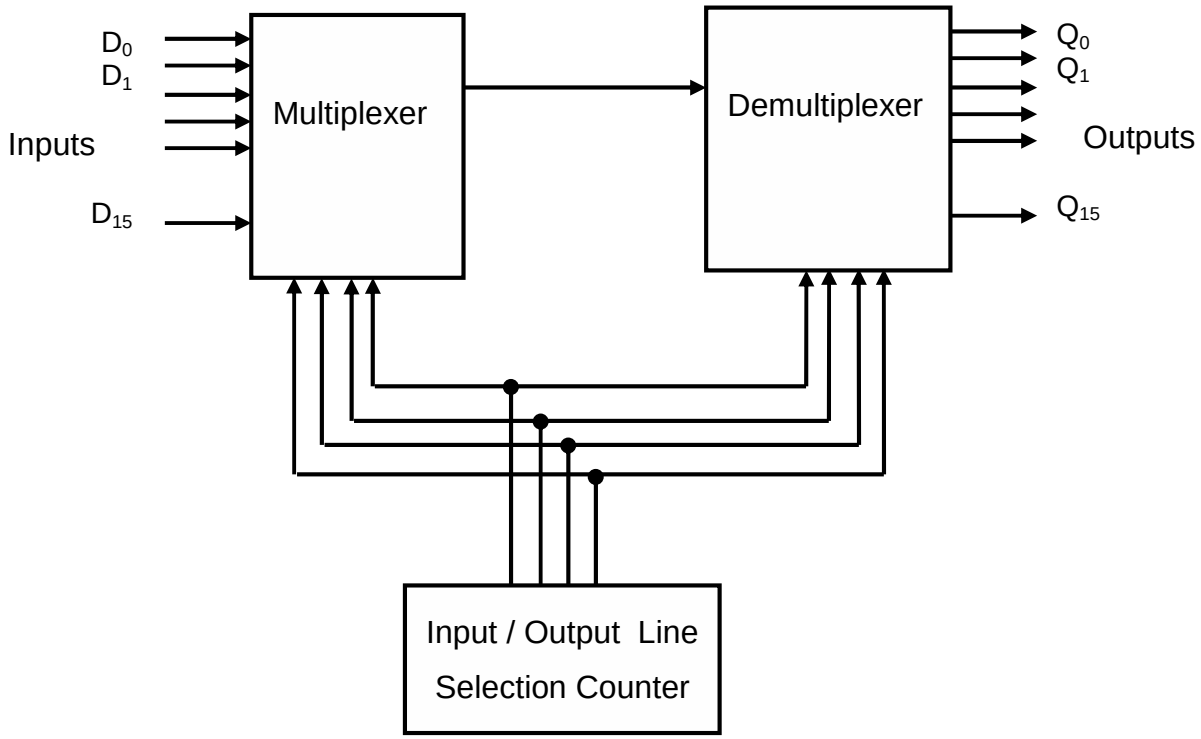

Fig.2 - Mux and Demux Interconnection

b) Experimental Procedure for Demultiplexer

1) Connect multiplexer output to the input of demultiplexer
2) Place the address 0000 on the select lines of both mux and demux
3) Change switch on D_0 from 0 to 1 and from 1 to 0 for 2 or 3 times
4) Observe onto which output line of demultliplexer this data is reaching
5) Give one clock pulse using push button of pulser for selecting next data line
6) Feed logic 0 and 1 using input switches and find out which input is reaching onto the same output line of demultiplexer
7) Continue the same procedure for checking the connectivity between the mux and demux
8) Finally you will find out that same numbered input and output lines are interconnected in every step of line selection using select lines

Summary

Based on their logic functions we can define mux and demux as below

- *A multiplexer is equivalent to a **multiple-input, single-output switch**, and*
- *A demultiplexer, to a **single-input, multiple-output switch.***

Review Questions

1) What is the main difference between a Multiplexer and a Demultiplexer ?
2) Name some of the applications of Demultiplexer ?
3) In the combined circuit of mux & demux given in the kit , is it possible to connect any data input of multiplexer to any output line of demultiplexer ? If not possible, what changes are required in the circuit ?.