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विद्युत सिगनल प्रयोगशाला
प्रयोग नं: ई एस एल 33

IRISET

ELECTRICAL SIGNALLING LABORATORY

EXPERIMENT NO.: ESL – 33

नाम
Name   :   _ _ _ _ _ _ _ _ _ _ _ _ _ _

अनुक्रमांक   प्राप्त अंक
Roll No   :   _ _ _ _ _ _ _ _ _ _ _ _ _ _   Marks Awarded   :

पाठ्यक्रम
Course   :   _ _ _ _ _ _ _ _ _ _ _ _ _

दिनांक   अनुदेशक का अधाक्षर
Date   :   _ _ _ _ _ _ _ _ _ _ _ _ _ _   Instructor Initial   :

HANDS-ON PRACTICE ON MICROLOK-II EI

Application Software & Maintenance Tool

AIM: Study on MICROLOK-II EI system Application Software and its uploading using Maintenance tool - - Hands-on Practice.

Introduction:

- MLK II EI requires relays, only for field Inputs and Outputs.

- All other relays used in Relay Interlocking system are represented by Non vital input, output bits and Boolean bits in MLK II Application Logic.
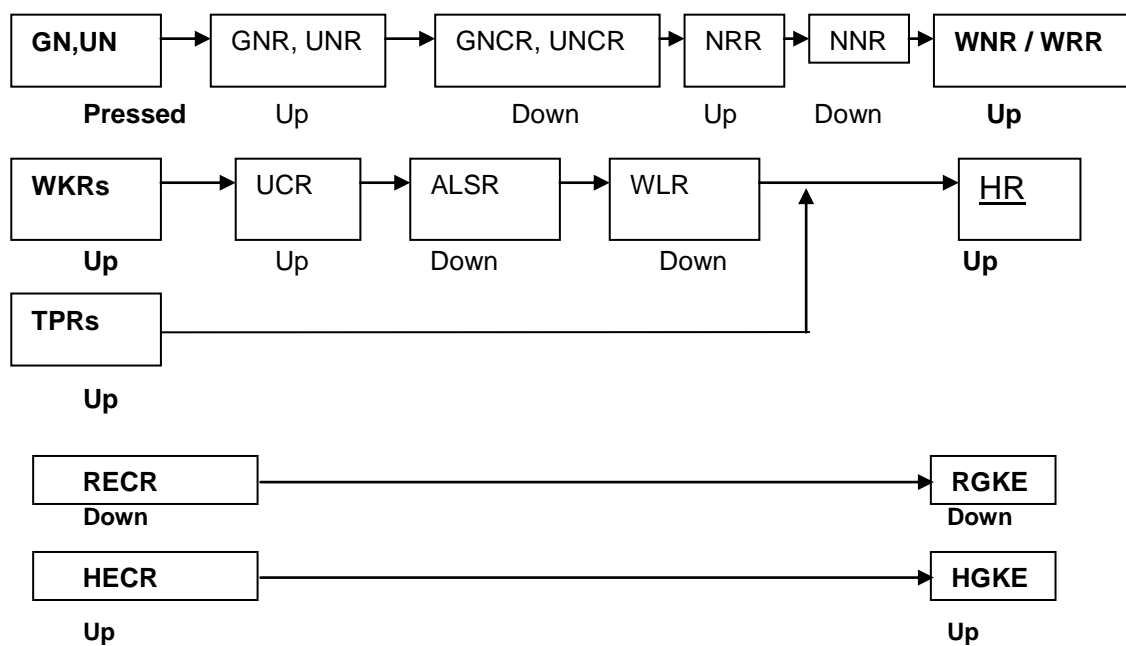
Application Program Design

- Application Program is nothing but another form of Interlocking Circuit.

- The design is based on Signal Interlocking Plan, Route Control Chart & Front Plate Drawing (Indication panel).

- Application Program is written in form of equations called Boolean equations.

- All the relays used in conventional circuits are called as BITs when referred to Application Program.

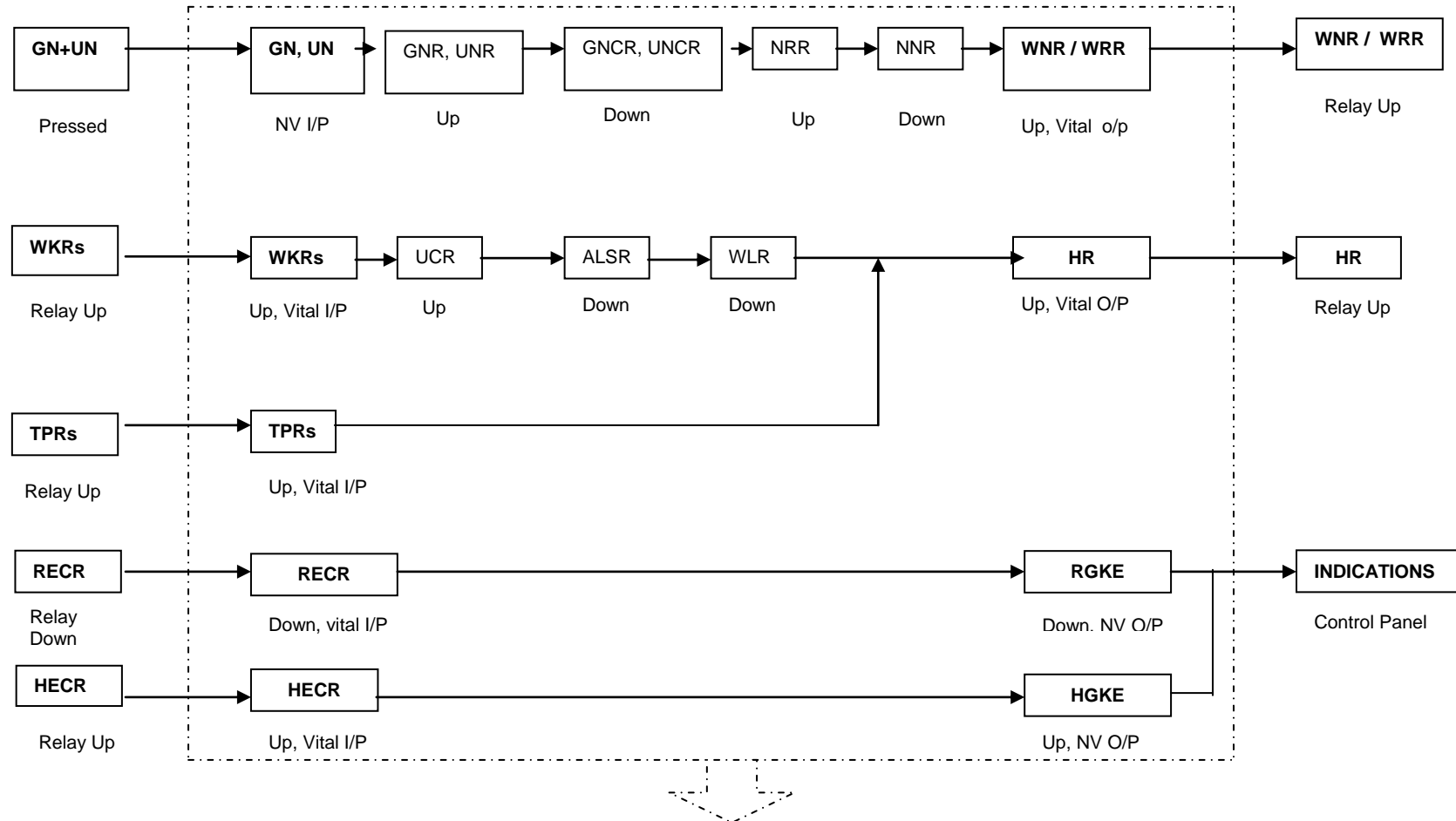Program is divided in various parts :

- Local I/O bit definition section.

- Serial bit definition section.

- Boolean bit definition section.

- Timer Section.

- Log bit definition section.

- Constant definition.

- System configuration.

- Numeric section.

- Logic section.

- Logic compilation.

Conventional PI Logic

GN,UN	→	GNR, UNR	→	GNCR, UNCR	→	NRR	→	NNR	→	WNR / WRR
Pressed		Up		Down		Up		Down		**Up**

WKRs	→	UCR	→	ALSR	→	WLR			HR
Up		Up		Down		Down			**Up**

TPRs
Up

RECR		RGKE
Down		**Down**

HECR		HGKE
Up		**Up**

Concept of MLKII Application Logic

GN+UN	**GN, UN**	GNR, UNR	GNCR, UNCR	NRR	NNR	**WNR / WRR**	**WNR / WRR**
Pressed	NV I/P	Up	Down	Up	Down	Up, Vital o/p	Relay Up

WKRs	**WKRs**	UCR	ALSR	WLR	**HR**	**HR**
Relay Up	Up, Vital I/P	Up	Down	Down	Up, Vital O/P	Relay Up

TPRs	**TPRs**
Relay Up	Up, Vital I/P

RECR	**RECR**	**RGKE**	**INDICATIONS**
Relay Down	Down, vital I/P	Down. NV O/P	Control Panel

HECR	**HECR**	**HGKE**
Relay Up	Up, Vital I/P	Up, NV O/P

Logic section:

I.   Non-vital Section :

- Consists button relay logics and indication logics.

- The relays such as GNR, UNR and indications such as RGKE, HGKE, WLKE etc. are defined in Non-vital I/O board definition section.

- Rest of the relays GNCR, UNCR are defined in NV Boolean bit definition section.

- These logics are written as "**NV ASSIGN** " statement.

II.   Vital Section :

- Consists complete interlocking logic except button relay and indication logics.

- The names of Vital relays such as HR, DR, RECR, HECR, TPR etc. are defined in Vital I/O board definition section.

- And rest of the relays such as GNR, NNR, UCR, ALSR etc. are defined in Vital Boolean bit definition section.

- These logics are written as "**ASSIGN**" statement.

Timer Section :

- "Slow to Pick "or "Slow to Release" time delay for any function are defined in this section.

- The definition works as Condenser-Resistor combination generally used in conventional installation.

- "**Slow to Pick**" is defined as **"SET=1 SEC".**

- "**Slow to Release**" is as **"CLEAR=1 SEC".**

Serial Section :

- Communicate the STATUS of any bit to other compatible system (VDU, MLKII etc).

- Output BIT from one system becomes Input BIT to other system and vice a versa.

- Output BIT and Input Bit definition sections are different.

- The order of BIT definition shall be same in both systems.
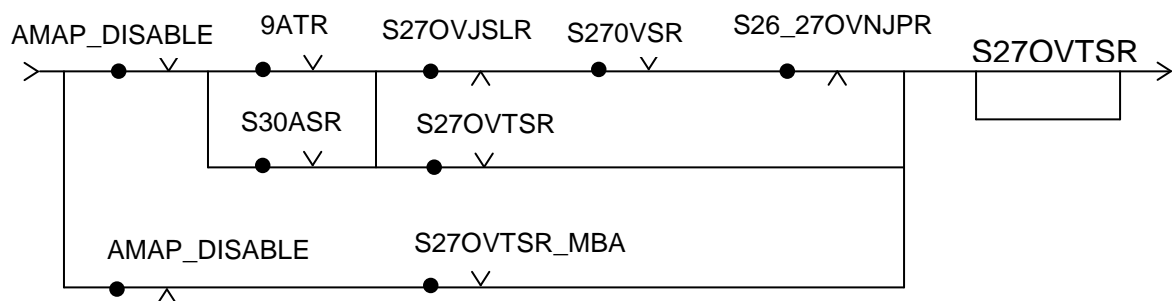
Symbols Used in Application Program

*	-	SERIES
+	-	PARALLEL
(	-	START OF PARALLEL PATH
)	-	END OF PARALLEL PATH
~	-	BACK CONTACT
,	-	BIT SEPERATION
;	-	END OF STATEMENT/ SECTION
@	-	Exclusive OR

Conversion of Circuit to Equation
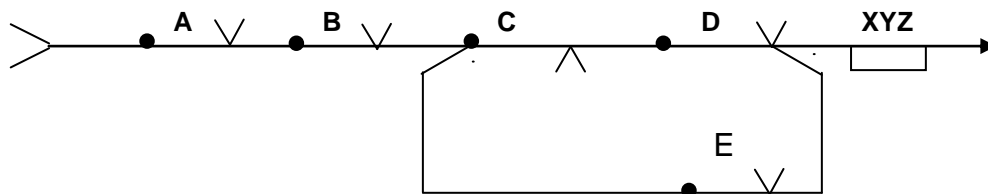
ASSIGN   A * B * (~ C * D + E)   To   XYZ ;

Example 1:

ASSIGN   AMAP_DISABLE * (19ATR + S30ASR) * (~S27OVJSLR *
    S27OVSR   *   ~S26_27OVNJPR   +   S27OVTSR   )+
    ~AMAP_DISABLE * S27OVTSR_MBA TO S27OVTSR ;

Example2:
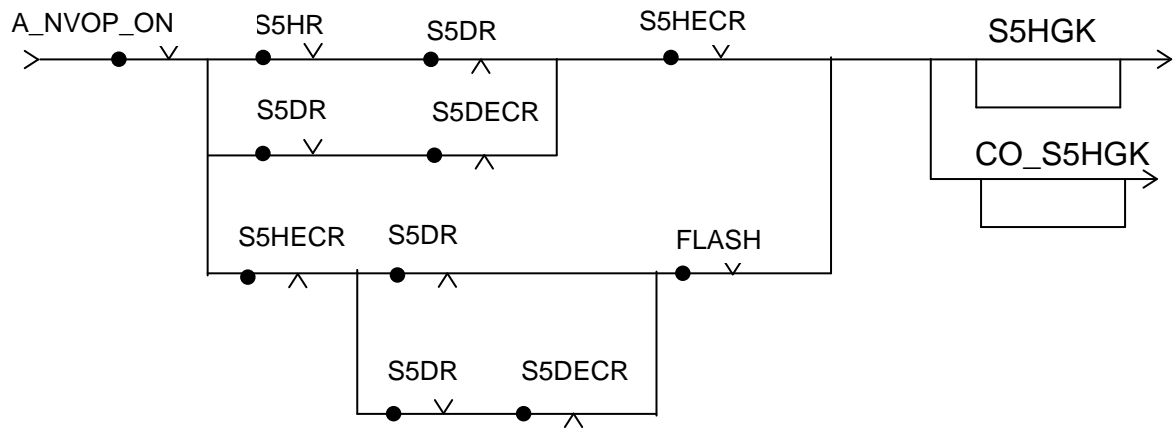
NV.ASSIGN   A_NVOP_ON * ((S5HR * ~S5DR + S5DR * ~ S5DECR) *

S5HECR + ~S5HECR * (~S5DR + S5DR * ~S5DECR) *

FLASH)   TO   S5HGK, C0_S5HGK;

Compilation of Application Program

- Program shall be stored as "PROGRAM.**ML2**" file name.

- Compilation is carried out with help of Microlok II Compiler.

- Result of compilation will be two files viz. 'PROGRAM.**MLL**" & "PROGRAM.**MLP**".

- "MLL" file is a listing file, which gives any errors, warnings, no. of BITs used, no. of time one bit used and so many other important information. This also gives unique identification numbers called as "CHECKSUM" & "CRC".

- "MLP" file is a data file, which is loaded in memory of CPU of MLK II using MLK II Maintenance tool.

# Uploading the Application Program to MICROLOK II using Maintenance tool :

New and revised application programs are uploaded to the Microlok II system CPU using the Microlok II Maintenance Tools program loaded on a Maintenance PC. One of the Maintenance PC serial ports is connected to the CPU board diagnostic port (Port-5).

Open the Maintenance tool software on Maint. PC. The system displays the Maintenance tools screen as shown below.
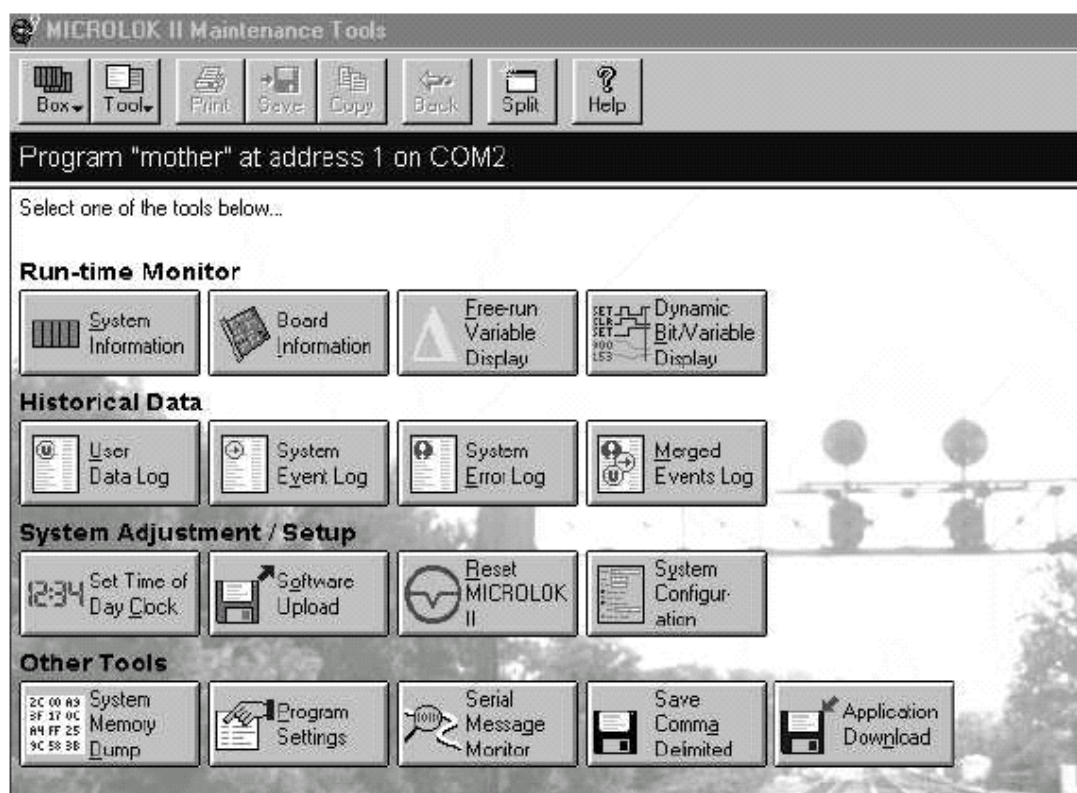

Use the following procedure to upload an application program to the Microlok II CPU:

1. Select the **Software Upload** option on the Maintenance Tools main menu. This will display a message window " Be sure the programming jumpers on the MICROLOK II board are in the program position before continuing" to remind you to adjust the programming jumpers, if required so that the application can be rewritten. The jumper 20,23 & 30 to be set for program position.

2. The system displays the software upload screen as shown below. The screen prompts you to reset the Microlok II CPU.
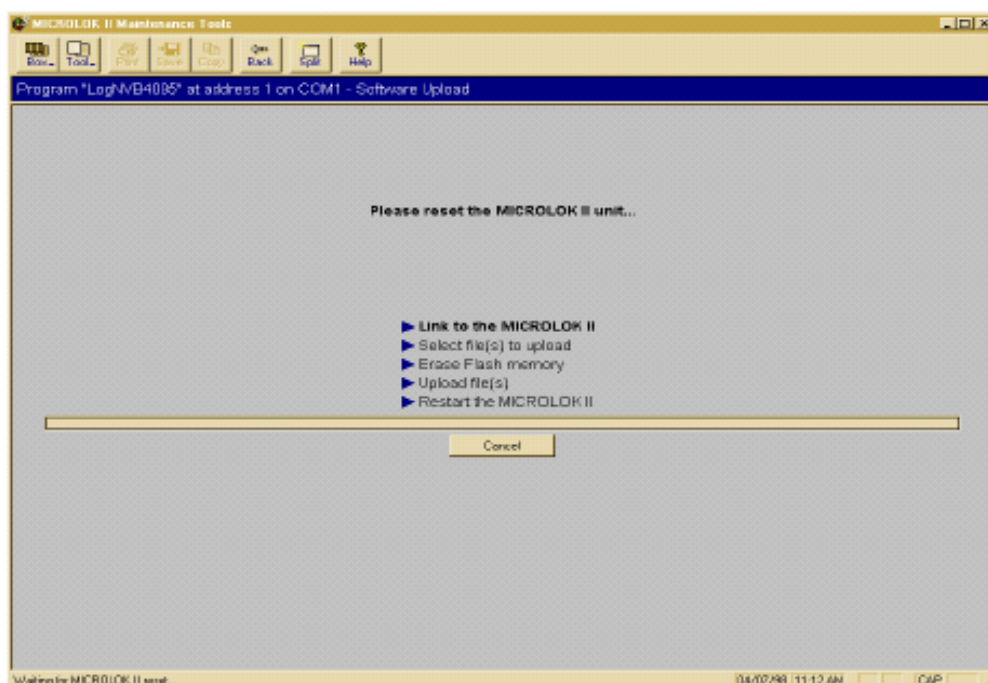
3. Press the RESET pushbutton on the CPU board front panel of MICROLOK II system.

4. When the CPU board reset has completed (the upper 4-character display on the CPU will read **Boot**), a new display appears that prompts you to select the application logic file to download as shown below.
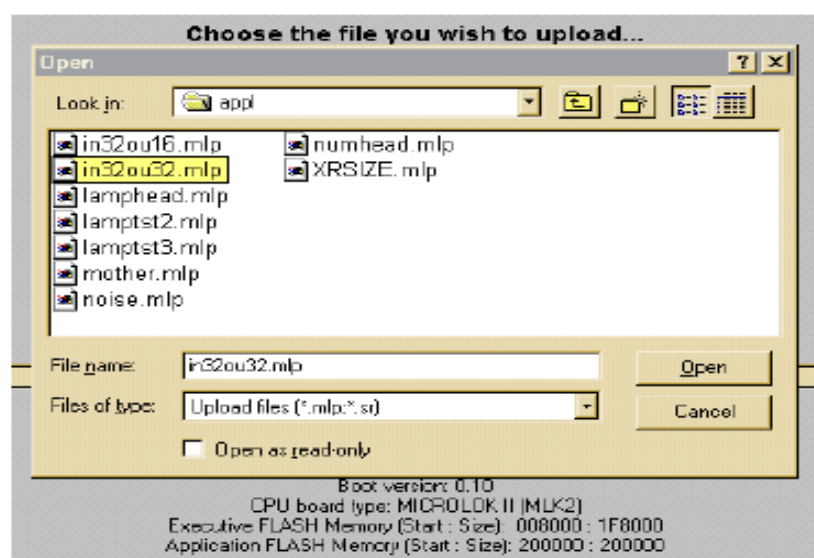

5. Select the desired application program name. Files that the Microlok II CPU can upload generally have the suffix **mlp** or Files of type (*.mlp). This suffix indicates that the application program has been successfully compiled and is in the proper format to be uploaded to the system.

6. Click on the appropriate application program file name (the file name becomes highlighted as shown above) and then click on the **Open** button. The system will begin the process of linking to the file. At this point, the system closes the file selection window so that only the software upload window appears on the screen.

7. As the system completes its link and prepares to load the application, it displays the following file upload confirmation prompt. This message reminds you that you are going to replace the current application with the one you selected. It also alerts you to the checksum value, which is unique to each application. Click on the **Yes** button to continue.
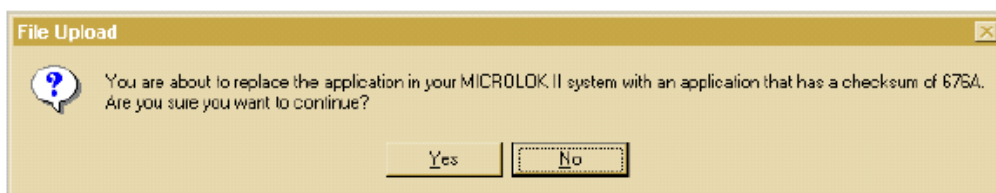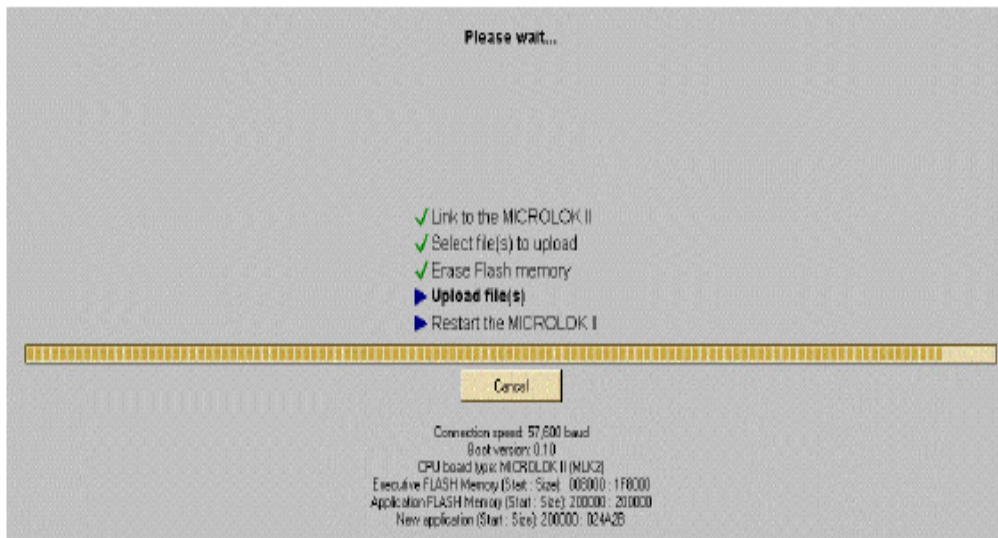

8. The system displays another confirmation prompt with a warning to ensure that the user has a functional application with which to replace the current one. Click on **Yes** to continue.
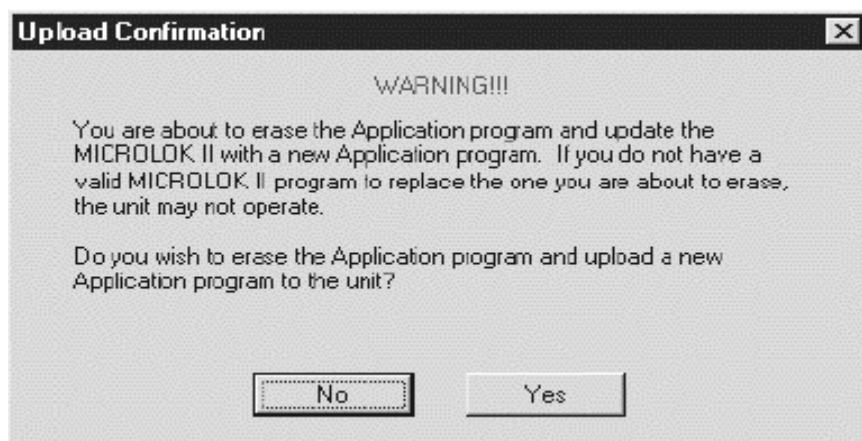
9. The system continues the process of uploading the new application. From this point, the process consists of three main operations:
   - Erase Flash memory
   - Upload file (s)
   - Restart the MICROLOK II

These operations are listed as steps on the software upload screen (see below). As the system completes each step, a checkmark appears beside the operation (as it did previously for the **Link to Microlok II** operation). You can also monitor the status bar under the list. The bar fills from left to right as the system completes its uploading activities.

Please wait...

✓ Link to the MICROLOK II
✓ Select file(s) to upload
✓ Erase Flash memory
▶ Upload file(s)
▶ Restart the MICROLOK I

Cancel

Connection speed: 57,600 baud
Boot version: 0.10
CPU board type: MICROLOK II (MLK2)
Executive FLASH Memory (Start : Size): 008000 : 1F8000
Application FLASH Memory (Start : Size): 200000 : 200000
New application (Start : Size): 200000 : 024A2B

10. When the status bar is completely filled, the system will then reset itself and the system displays the following reminder to readjust the programming jumpers in order to protect the inadvertent application changes.

File Upload

ⓘ The upload process has been completed.
Move the programming jumpers into the position to protect against inadvertent changes.

OK

11. Click on the **OK** button. Then the Maintenance Tools program main menu will be redisplayed.

12. After the CPU reset as mentioned in 10 above, allow the Microlok II CPU board to perform the startup tests. The startup test routines should complete successfully and the CPU board will assume the on-line mode of operation. We can tell when the system is in the on-line mode by observing a number of cardfile indications:

- The CPU board 'ON-LINE' LED will be on.
- The CPU board 'VPP ON' LED will be OFF.
- The 'RESET' LED will be off.
- The CPU upper 4-character display will scroll the phrase **US&S MICROLOK II**.
- The CPU lower 4-character display will scroll the pre-programmed application name. Here it is " IRISETA_VER1.5"
- The power supply board VCOR LED will be illuminated.

Date: Signature of the trainee