



MICROLOK® II Troubleshooting Flowcharts

January 2009 Revision 1.a



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1 TROUBLESHOOTING MICROLOK II

1.1 Introduction

This troubleshooting process is based upon the following assumptions:

- The system in question has been in normal operation for a period of time without failure.
- Commercial input power is available and been checked (including fuses).
- Battery power is available and adequate (including fuses).
- Verify +12VDC, -12VDC, and +5VDC on the cardfile.
- No external variables (e.g., trenching in the vicinity of the location, or track work) has altered the location's physical status.
- The maintainer performing the troubleshooting has a working familiarity with the $MICROLOK^{@}$ II System.

If work has been performed on the cardfile check the following first:

• Ensure that all PCBs are firmly seated in the cardfile.

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- Ensure the PCB top rear I/O connectors are firmly attached to the cardfile rear.
- Ensure that all addressable PCBs have address jumpers installed.

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MICROLOK II Troubleshooting



1.2 Purpose

These charts provide a common ground for maintainer-engineer collaboration in the troubleshooting process.

The engineer can refer to a given flowchart confident that the first response maintainer has performed the flowchart steps and thereby perform a better assessment of the problem.



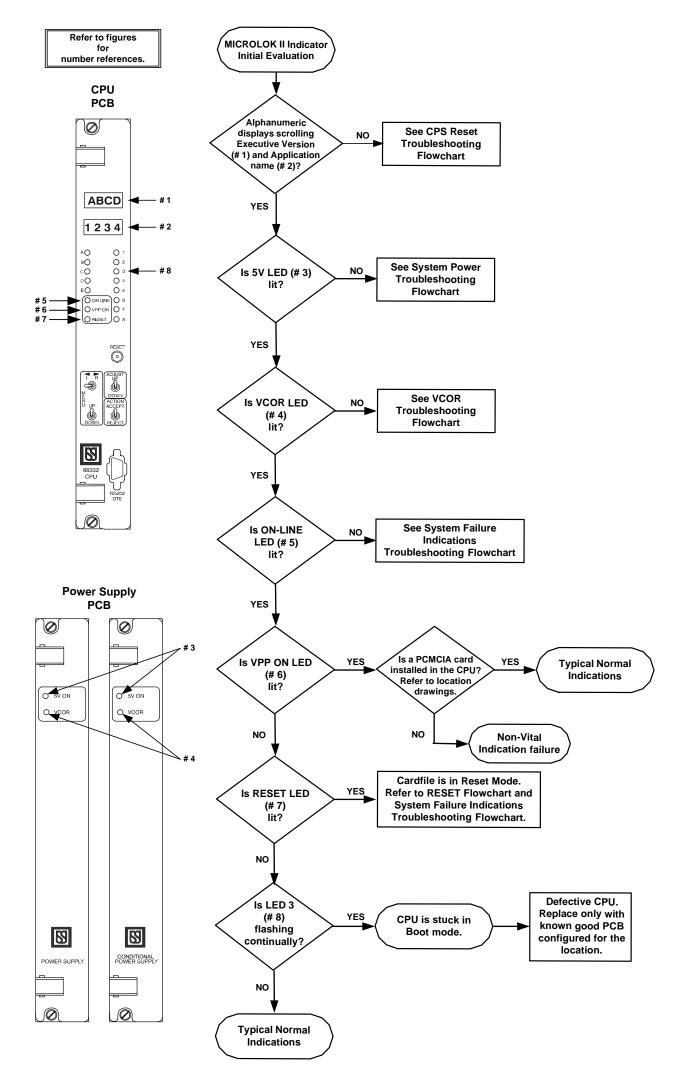


Figure 1-1. MICROLOK II Initial Indication Evaluation



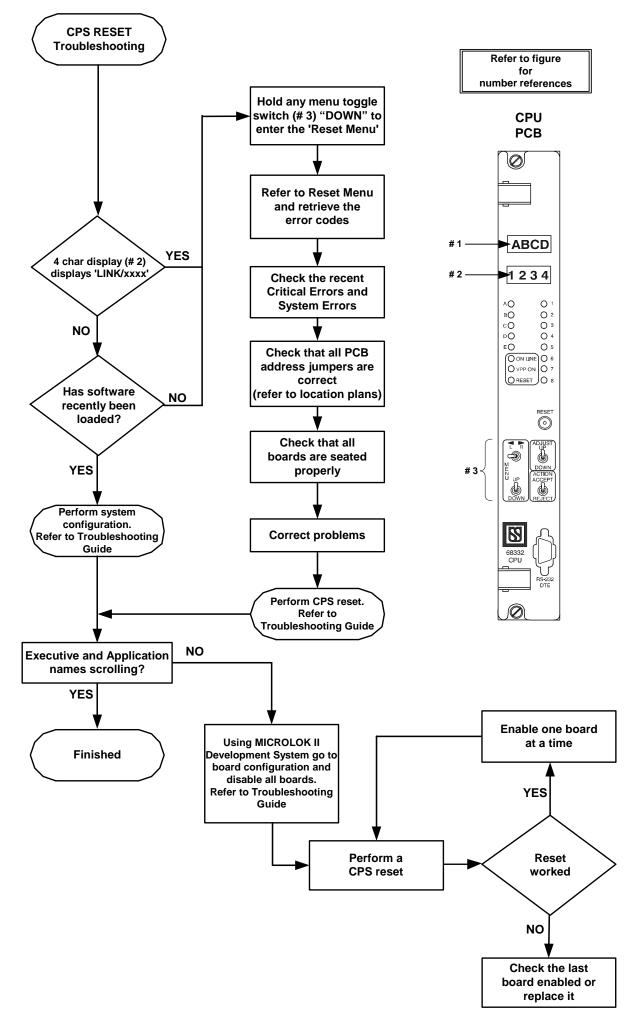


Figure 1-2. CPS Reset Troubleshooting Flowchart



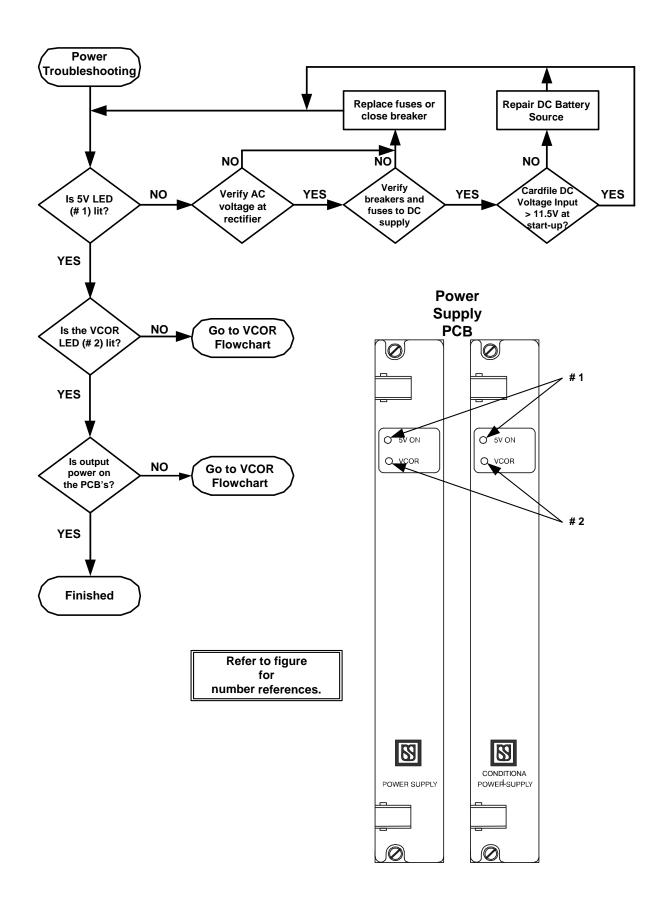


Figure 1-3. System Power Troubleshooting Flowchart



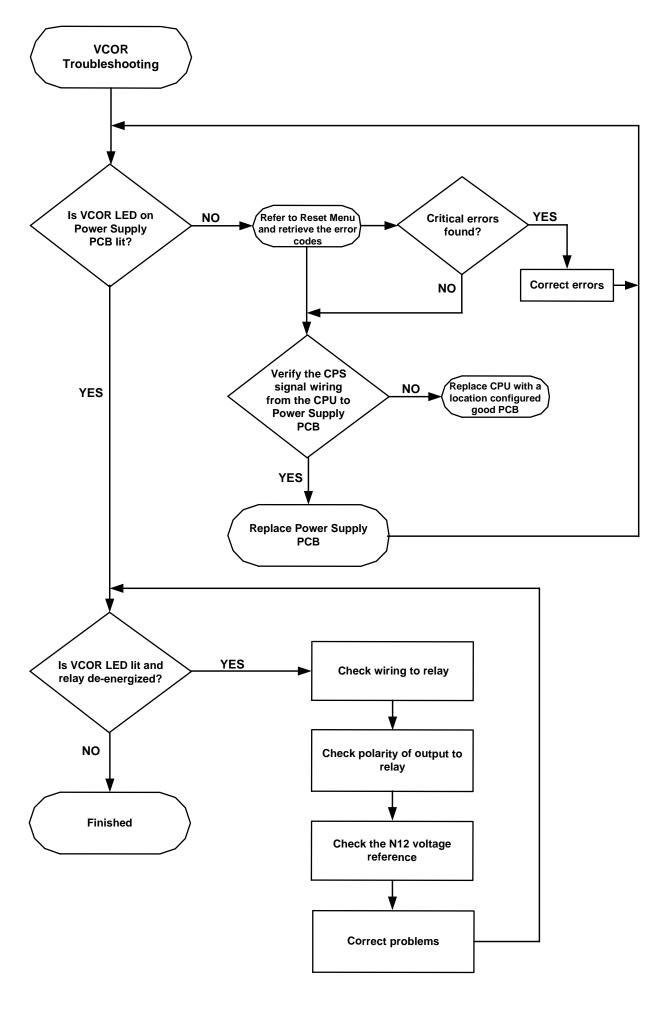


Figure 1-4. VCOR Troubleshooting Flowchart



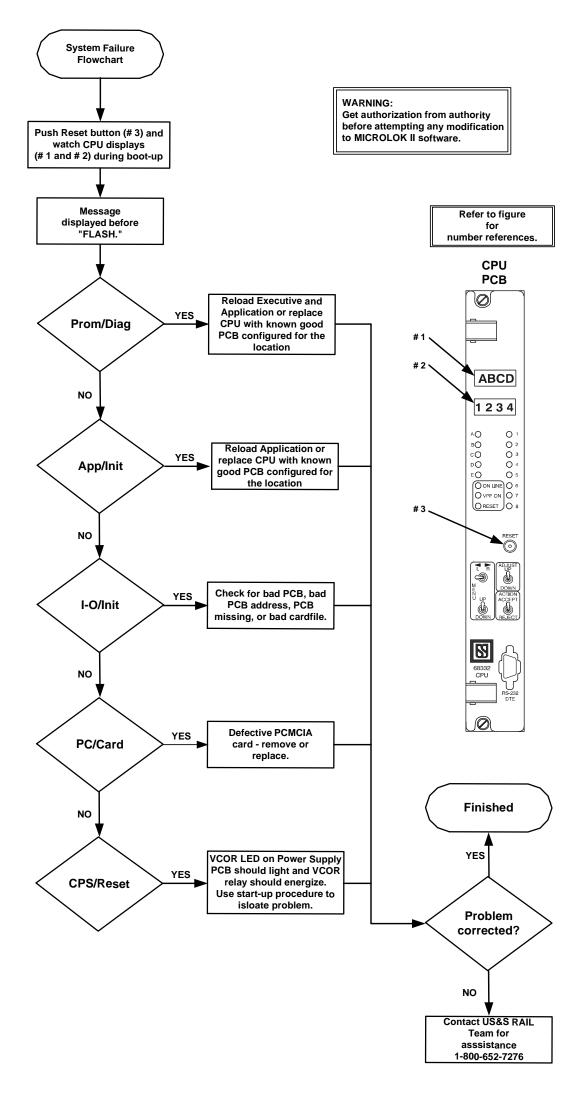


Figure 1-5. MICROLOK II System Failure Indications



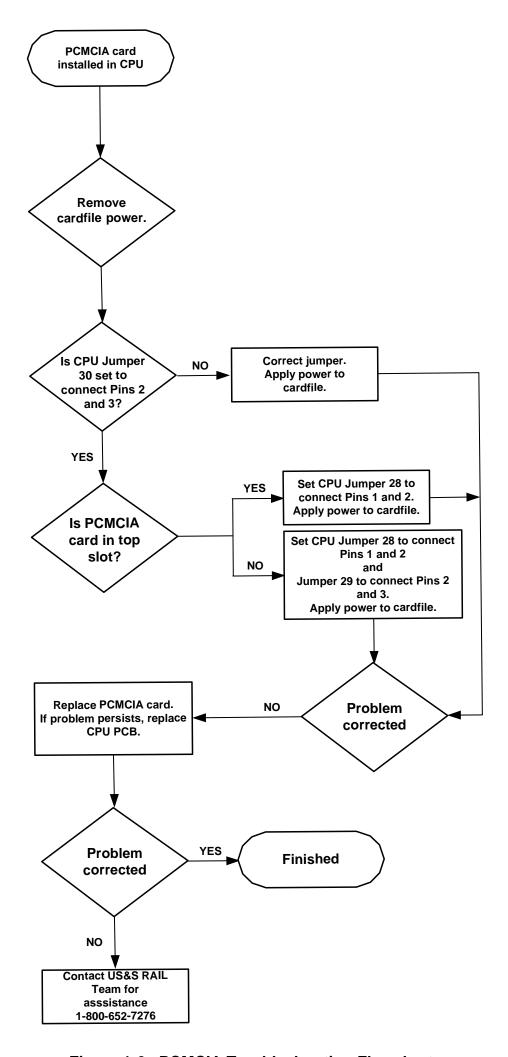


Figure 1-6. PCMCIA Troubleshooting Flowchart



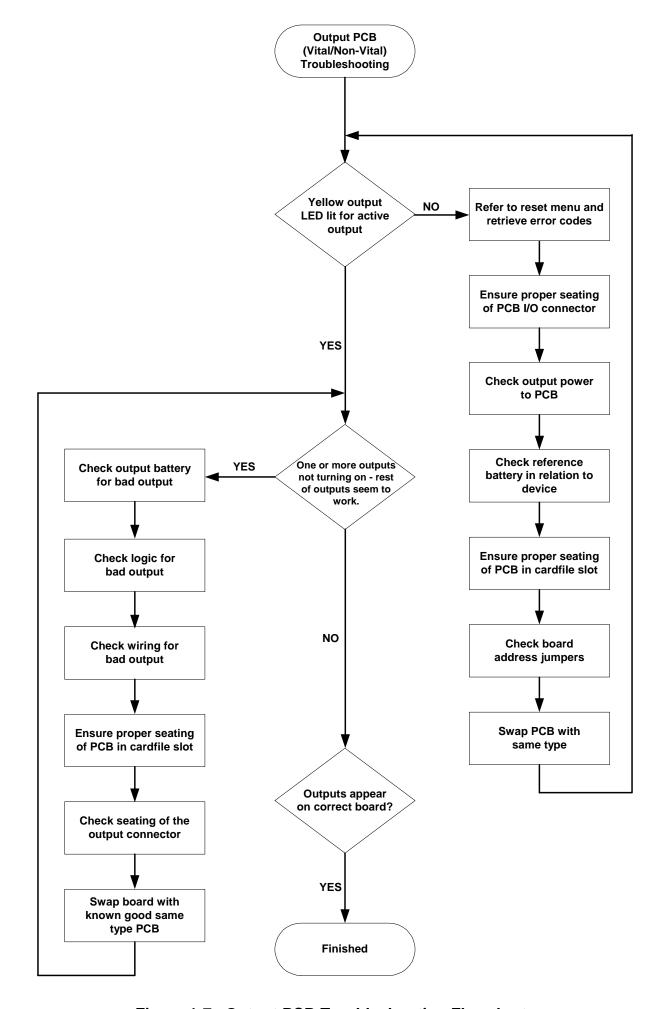


Figure 1-7. Output PCB Troubleshooting Flowchart



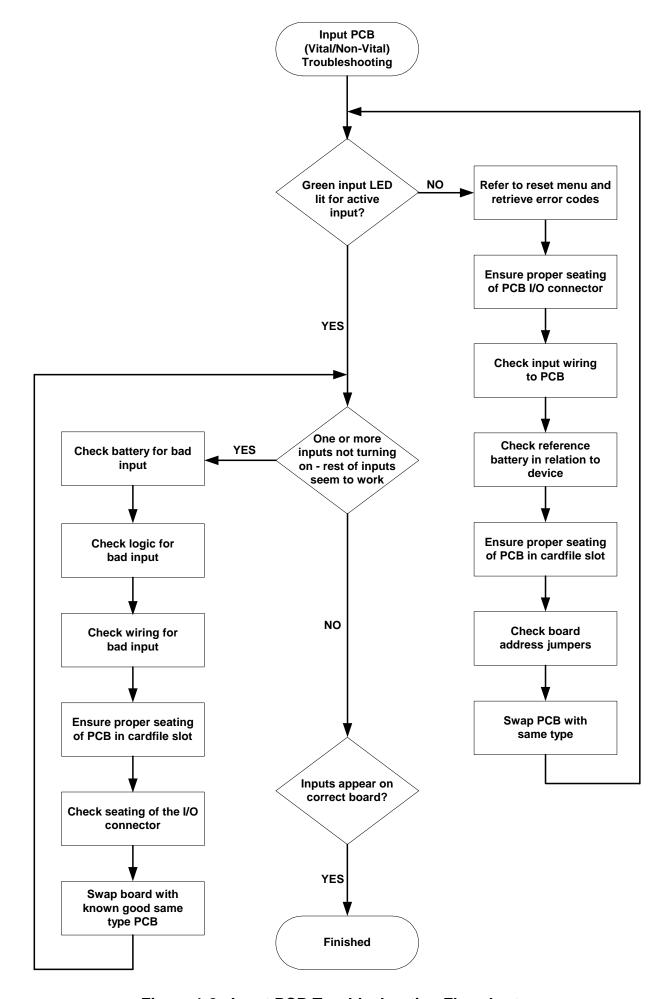


Figure 1-8. Input PCB Troubleshooting Flowchart



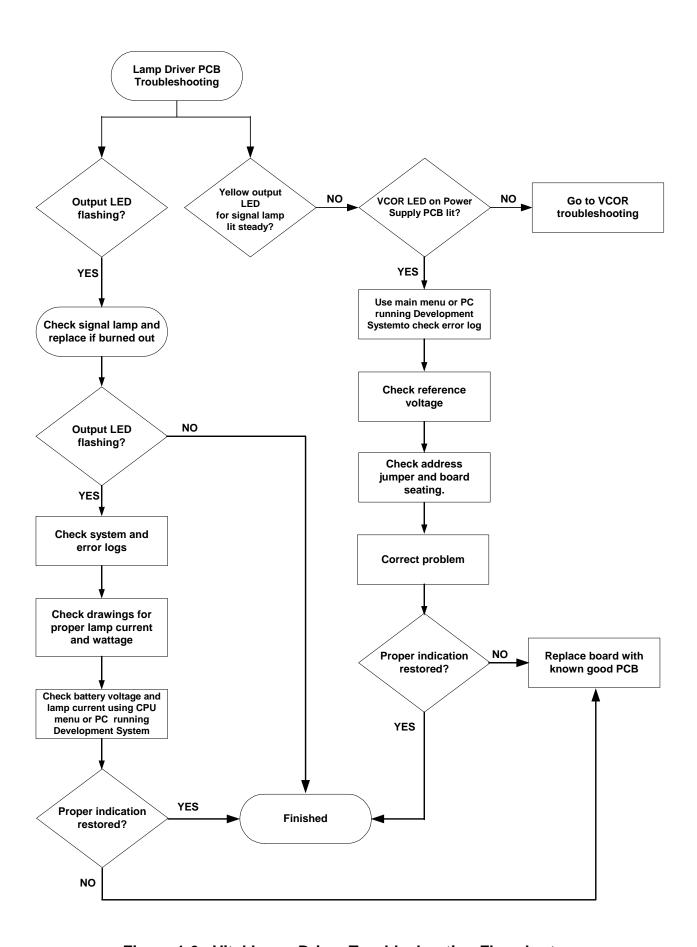


Figure 1-9. Vital Lamp Driver Troubleshooting Flowchart



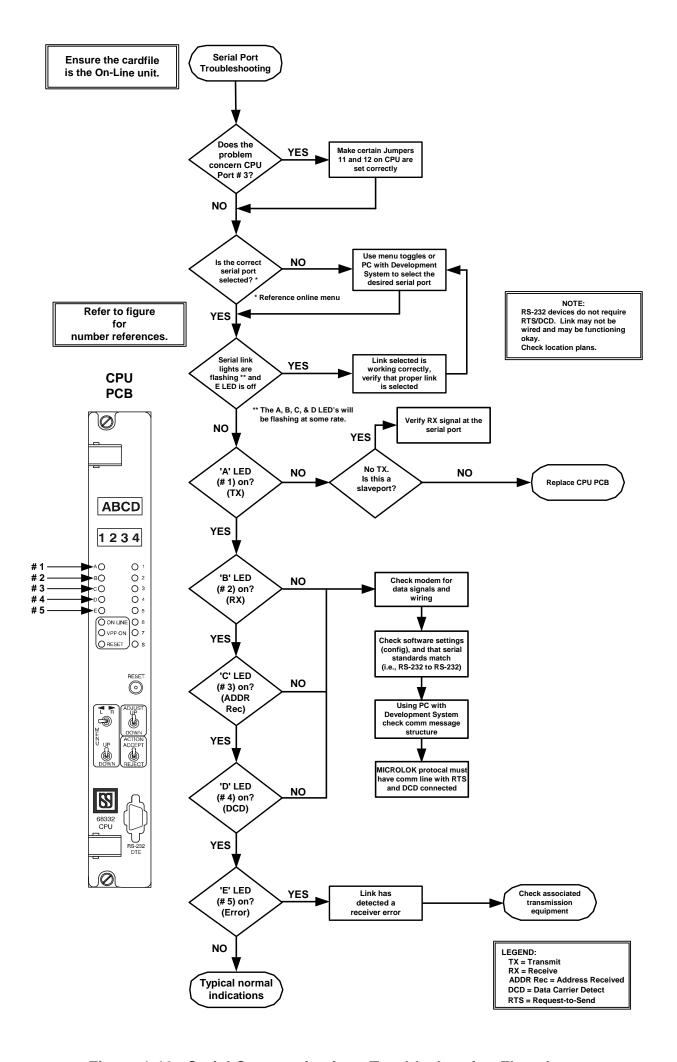


Figure 1-10. Serial Communications Troubleshooting Flowchart



2 MICROLOK II CPU MENUS

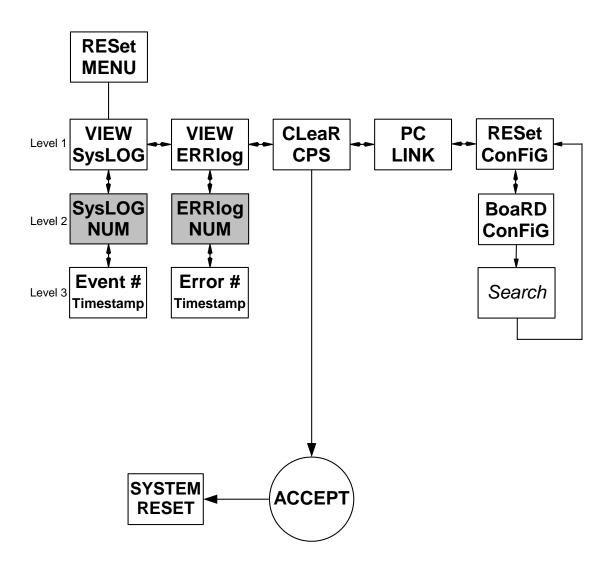


Figure 2-1. CPU Reset Menu – A

(System without Configurable PCBs)



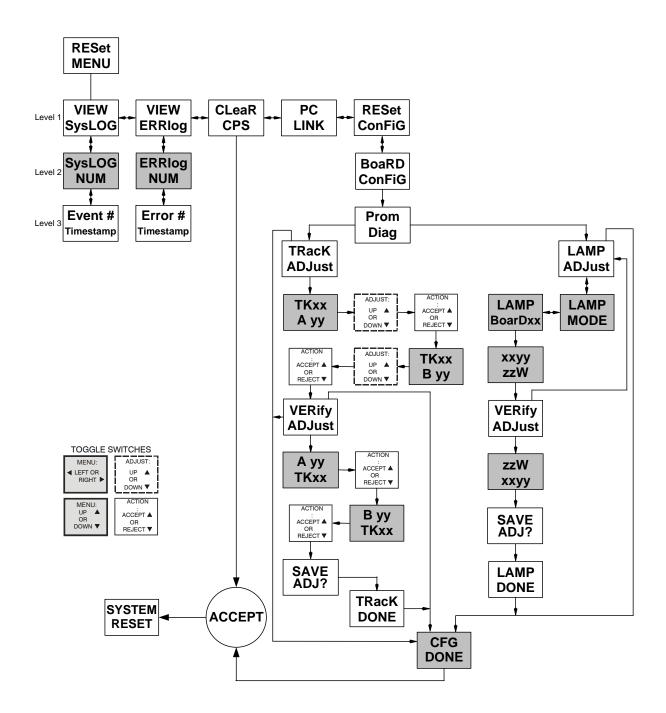


Figure 2-2. CPU Reset Menu – B

(System with Configurable PCBs)



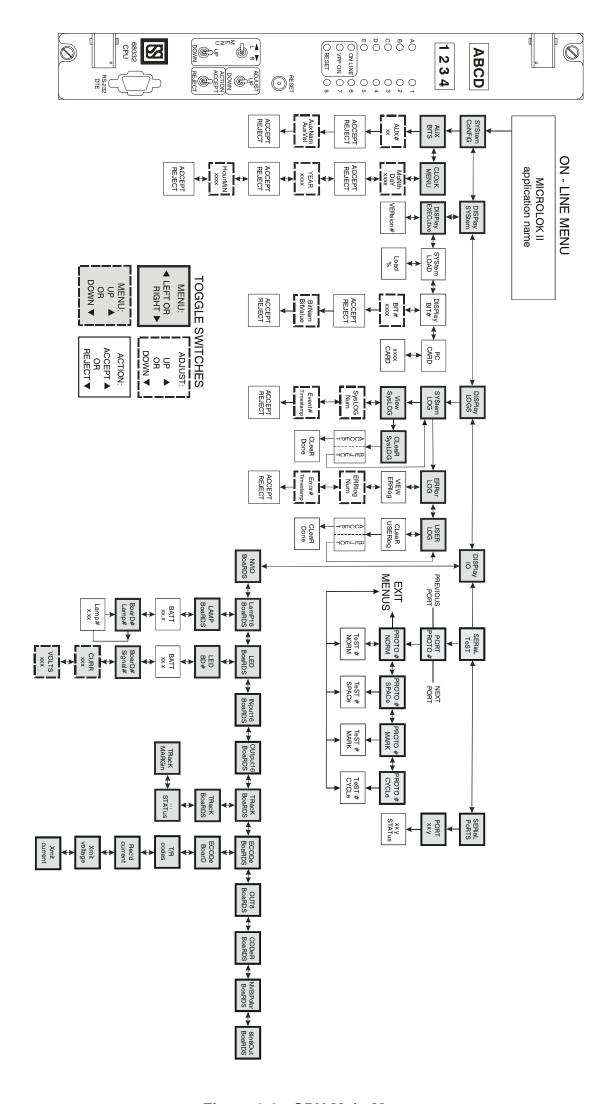


Figure 2-3. CPU Main Menu



3-1

3 NOTES



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