Synchronization PCB

Notice

This module is one of a series of modules that describe the components of the MICROLOK II system.

Proprietary Notice

Revision History

REV.	ISSUE DATE	REVISION DESCRIPTION
1	July 2009	Initial Release.
2	October 2009	Section 2.6 added. Revised Figure 2–3.
3	November 2009	Added Note in Section 2.2 referring to Figure 2–3. Added Figure 2–4. Revised LED descriptions in Section 2.3.

1. SYNCHRONIZATION DESCRIPTION

The Synchronization PCB allows two MICROLOK II units to connect to each other in order to form a synchronized pair for a seamless redundant application. Each MICROLOK II cardfile contains a Synchronization PCB. The MICROLOK II cardfiles are linked through an Ethernet interface, receive the same physical inputs, deliver the same physical outputs, and have the same hardware and software architecture and same physical I/O.

One unit of each synchronized pair is identified as the on-line unit and the other unit is identified as the off-line unit. Each MICROLOK II unit monitors the state of the other MICROLOK II unit via the synchronization Ethernet link and the physical I/O on the Synchronization PCB. Both units deliver synchronized physical outputs so that if one unit is disabled (due to a system reset, power down or other error condition), the internal and output states remain unchanged and control will transfer to and seamlessly continue with the second unit.

2. SYNCHRONIZATION PCB

The Synchronization PCB contains its own microprocessor, has four vital isolated inputs, two vital isolated outputs, and other I/O circuitry in order to interface with two independent MICROLOK II units.

Two versions of the Synchronization PCB are available: one for 12 volt operation (ASTS USA part number N17066401) and one for 24 volt operation (ASTS USA part number N17066402).

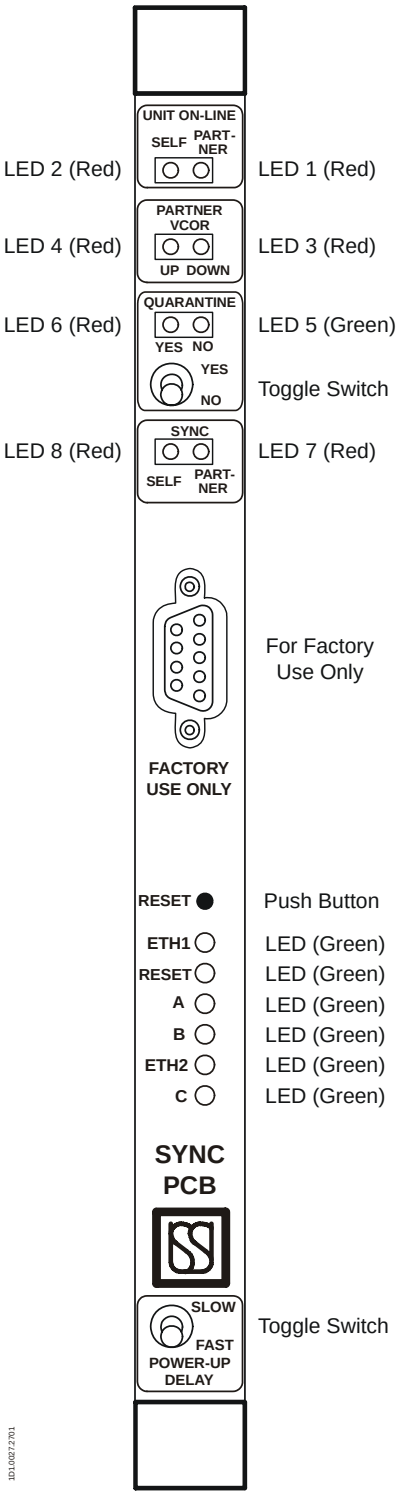

Figure 2–1. Synchronization PCB Front Panel Detail

2.1. Operation

A block diagram of the Synchronization PCB is shown in Figure 2–2.

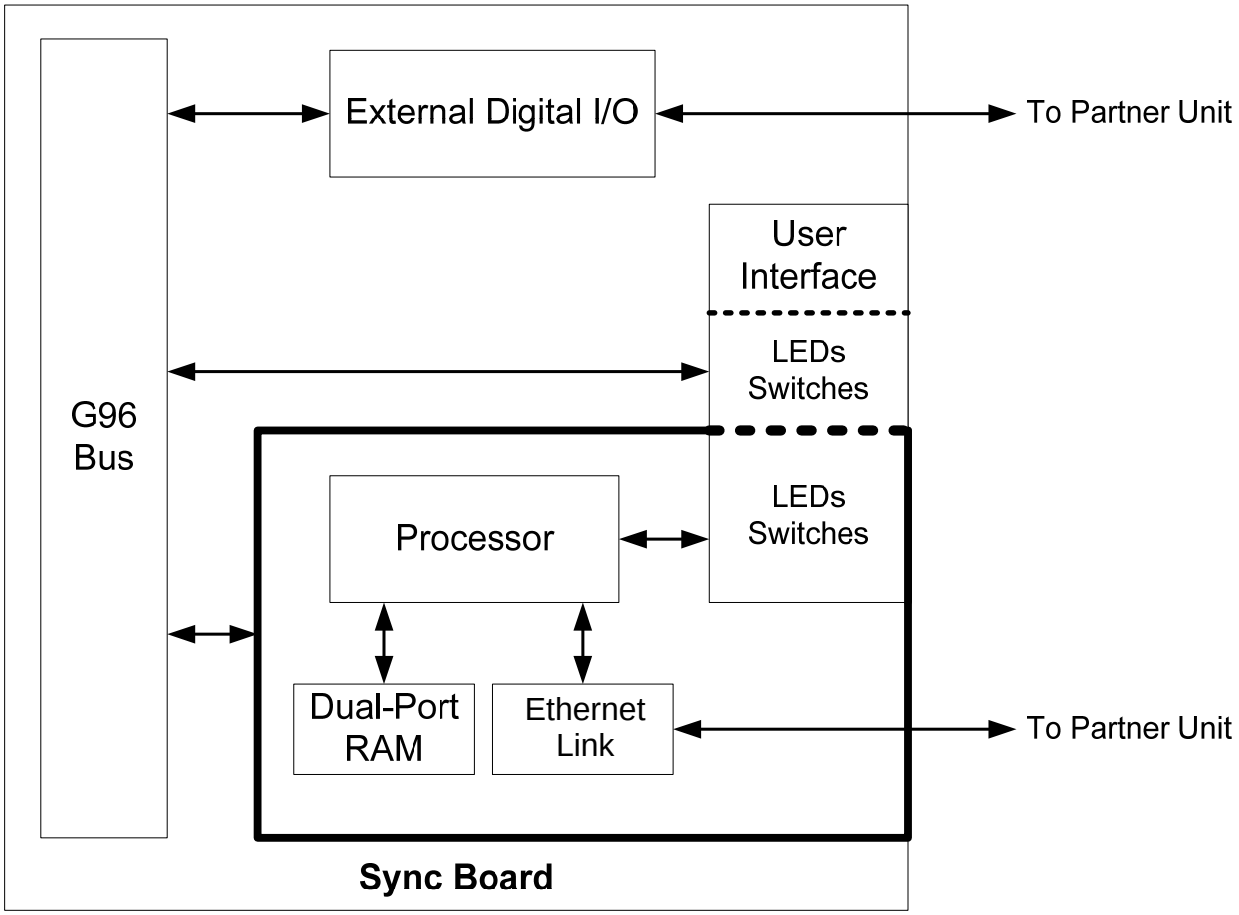

Figure 2–2. SYNCHRONIZATION PCB Block Diagram

The Synchronization PCB circuitry is divided into two functional sections:

1. External Digital I/O
2. User Interface

2.2. I/O Interface

The Synchronization PCB interfaces through an external board connector ASTS USA Part Number N39908001. See Figure 2–3. The connector contains address selection jumpers (SW2, SW3, and SW4) and two RJ45 jacks (ETH1 and ETH2) for the Ethernet ports. This allows a standard Ethernet cable to be plugged directly into the back of the MICROLOK II cardfile. I/O cables can also be wired to the screw terminals of connectors J2 and J3.

NOTE

Only Ethernet Channel 1 can be used for the synchronization application.

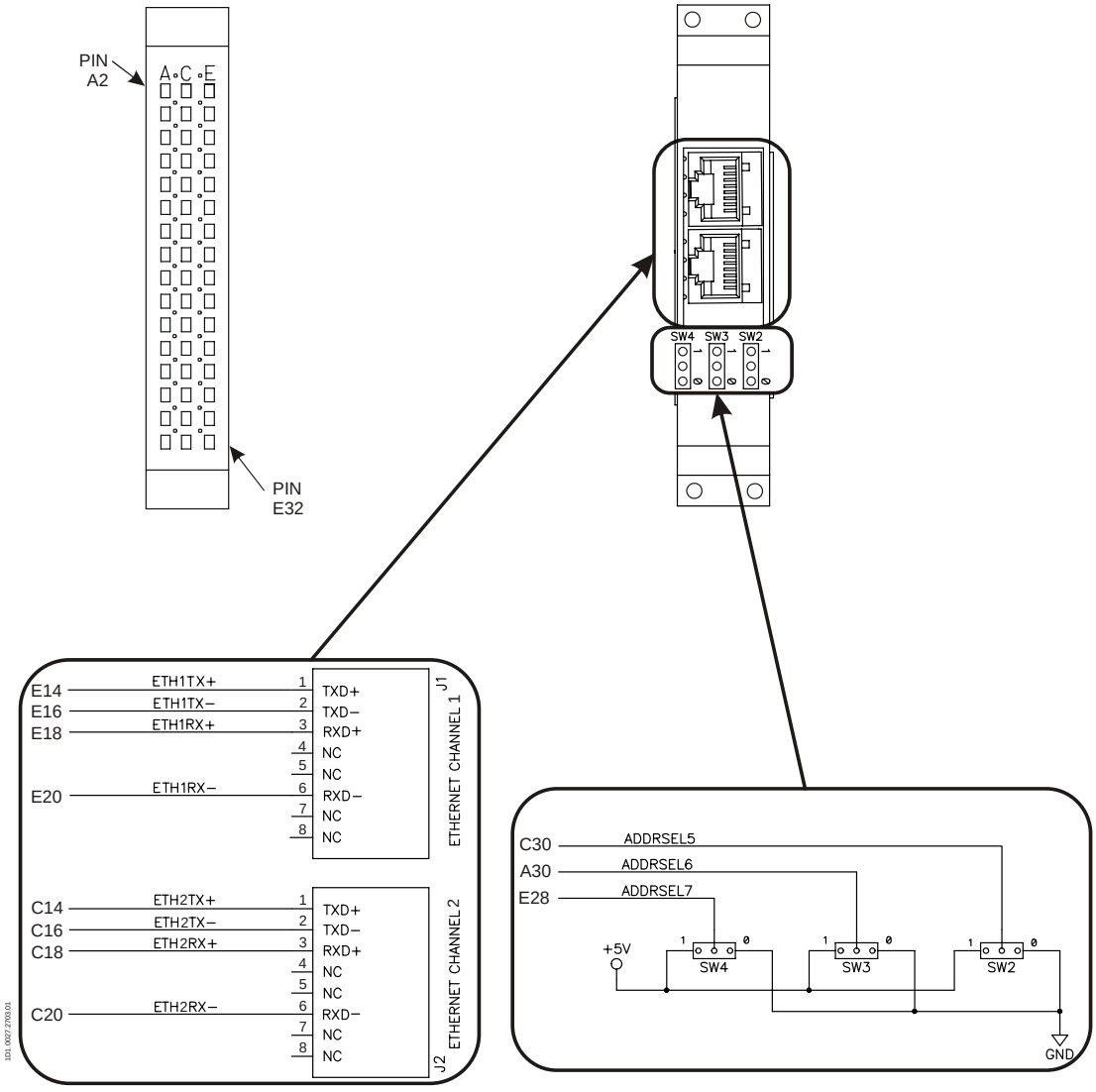

Figure 2–3. Synchronization PCB Connector (part number N39908001)

NOTE

The jumper positions of the Address Selection jumpers (SW2, SW3, and SW4 shown in Figure 2–3) are determined by the software application. The settings can be found in the MICROLOK II compiler's .mll list file.

2.3. User Interface

The front panel contains one DB9 connector, a reset button, fourteen LEDs, and two toggle switches. See Figure 2–1.

- The DB9 connector is used for factory diagnostic testing.
- The reset button resets the Synchronization PCB.

LEDs 1 through 8 are software-controlled and only provide valid information when the MICROLOK II is in Quarantine or Operational mode. The LEDs provide the following indications when lit:

- LED 1 Unit On-Line Partner – (Input) lights red when the partner MICROLOK II system is on-line.
- LED 2 Unit On-Line Self – (Output) lights red when this MICROLOK II system is on-line. Lights steady when the CPS is up. Flashes when the CPS is down (selective shutdown mode).
- LED 3 Partner VCOR Down – (Input) lights red when the partner MICROLOK II's VCOR is deenergized.
- LED 4 Partner VCOR UP – (Input) lights red when the partner MICROLOK II's VCOR is energized.
- LED 5 Quarantine No - lights green when this MICROLOK II is in normal operational mode.
- LED 6 Quarantine Yes - lights red when this MICROLOK II is quarantined. Flashes when attempting to establish synchronization with partner unit.
- LED 7 Sync Partner – (Input) lights red when the partner MICROLOK II is synchronized with this unit.
- LED 8 Sync Self – (Output) lights red when this MICROLOK II is synchronized with the partner unit. Lights steady when the CPS is up. Flashes when the CPS is down (selective shutdown mode).
- ETH1 - Ethernet Port 1 activity - flashes when there is activity on Ethernet port 1.
- RESET - Synchronization PCB reset indication.
- A – Flashes when the executive has successfully booted.

- B – Flashes when the executive has successfully booted.
- C – Flashes when the executive has successfully booted.
- ETH2 - Ethernet Port 2 activity - flashes when there is activity on Ethernet port 2.

The quarantine toggle switch – toggles this MICROLOK II unit to Quarantine mode (YES) or not in Quarantine mode (NO).

The Power-Up delay toggle switch – sets a power-up delay to either a slow power-up or a fast power-up.

Typical Synchronization PCB wiring between two MICROLOK II units is shown in Figure 2–4.

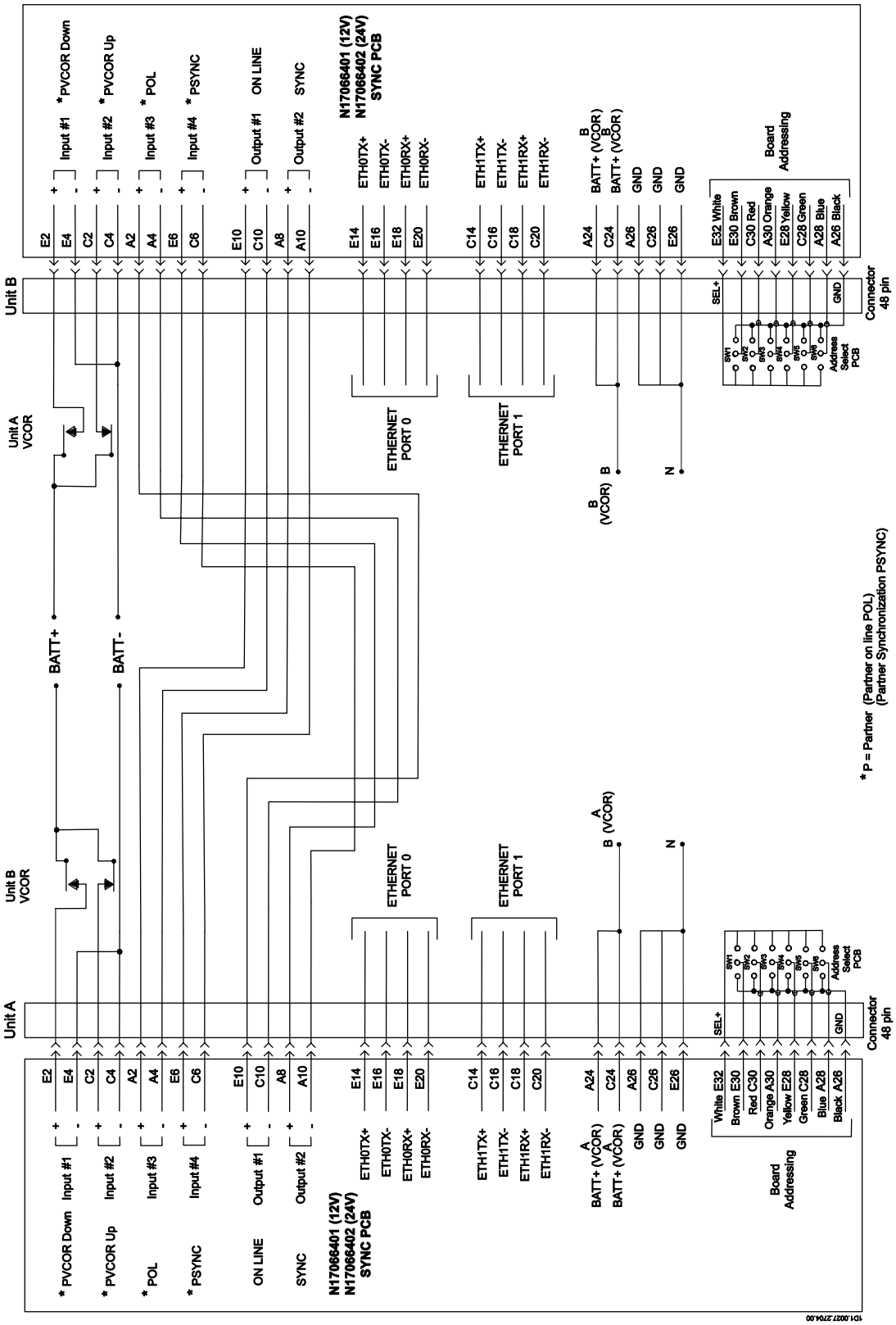

Figure 2–4. Typical Synchronization PCB Interface Wiring

2.4. PCB Keying

Each type of ASTS USA PCB has a different combination of six keying fingers.

Keying fingers are designated by ASTS USA. Their purpose is to ensure that the PCB is being inserted into its proper cardfile slot. Therefore, keying tabs must not be removed or altered by the user. Table 2–1 lists the keying for the Safe-P Synchronization PCB.

Table 2–1. PCB Keying

PRINTED CIRCUIT BOARD	PART NO.	KEYING PLUG LOCATION											
		1	2	3	4	5	6	7	8	9	10	11	12
Synchronization PCB, 12V	N17066401	✓		✓			✓	✓	✓		✓		
Synchronization PCB, 24V	N17066402	✓		✓			✓	✓	✓			✓	

The "✓" in Table 2–1 indicates a keying tab removed on the PCB connector and a keying plug installed on the motherboard connector. Correspondingly, no entry in the table indicates a keying tab not removed on the PCB connector and no keying plug installed on the motherboard connector. See Figure 2-5.

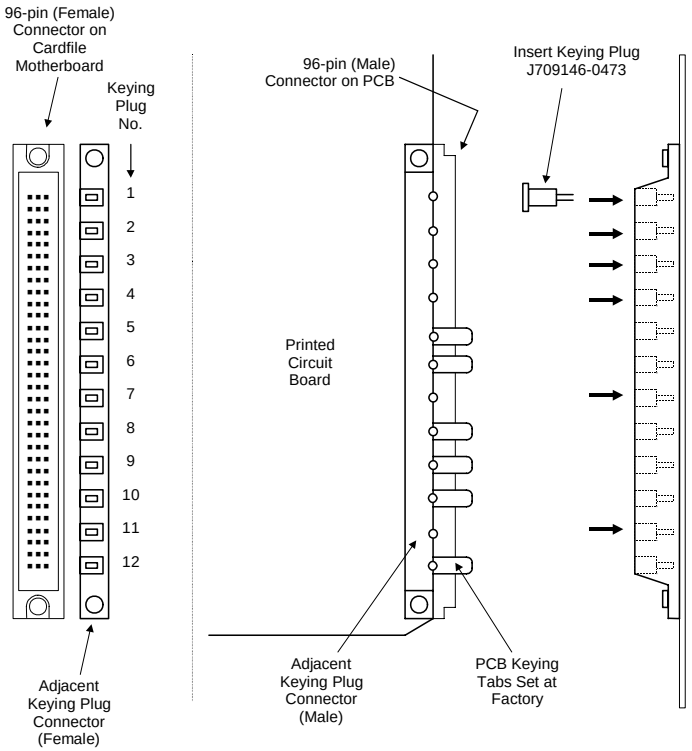

Figure 2-5. Typical Keying Tab and Pin Arrangement

2.5. System Cardfiles

The systems that support the use the Synchronization PCB listed in Table 2-2.

Table 2-2. Synchronization PCB System Applications

US&S PCB PART NO.	APPLICABLE CARDFILES					
	MICROLOK II	MICROLOK II HB	END POINT	LED12 INTERMEDIATE	I-LOK	GENISYS II
N17066401	✓					
N17066402	✓					

2.6. Noise Filtering

It is recommended that a CMF-101 Common Mode Filter (ASTS USA part number N4515522001) should be installed on the input power lines to the Microlok II cardfiles that contain a Communication PCB. The CMF-101 filters out common mode noise on the battery-supplied power input lines. The filter should be mounted as close to the Microlok cardfile as possible. The input wires (dirty) and output wires (clean) should be physically separated from each other. Figure 2-6 shows how the CMF-101 is to be wired in the power input circuit.

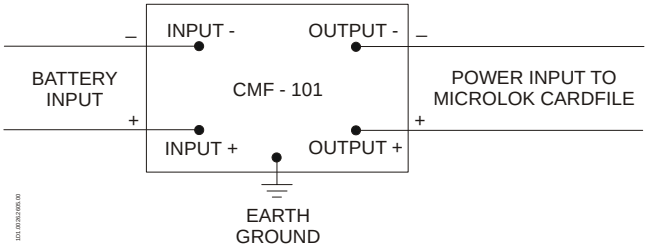

Figure 2-6. CMF-101 Wiring Diagram

2.7. Configuration Options

This board is defined under the Interface Section – LOCAL Sub-Section of the application program.

Only one Synchronization PCB is allowed to be installed in the cardfile and it must be one of the first seven boards defined in the program.

The board may be Enabled/Disabled via the MICROLOK II Development System. This is the only software interface available for this board.

2.8. Software Compatibility

Refer to the MICROLOK II Application Programming Guide to verify that this PCB is compatible with the MICROLOK II executive software.

End of Module