UNION SWITCH & SIGNAL

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MICROLOK II

Integrated Vital Interlocking, Coded Track Circuit, and Non-Vital Code Line Controller

Hardware Installation

- Installation
- Maintenance

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Important Notice

US&S constantly strives to improve our products and keep our customers apprised of changes in technology. Following the recommendations contained in the attached service manual will provide our customers with optimum operational reliability. The data contained herein purports solely to describe the product, and does not create any warranties.

Within the scope of the attached manual, it is impossible to take into account every eventuality that may arise with technical equipment in service. Please consult your local US&S sales representative in the event of any irregularities with our product.

We expressly disclaim liability resulting from any improper handling or use of our equipment, even if these instructions contain no specific indication in this respect. We strongly recommend that only approved US&S spare parts be used as replacements.

Revision History

Rev.	Date	Nature of Revision
3	December 2005	Incorporate ECO 140125-1; Corrected voltage levels for Part No. N17061002 for the Vital Input PCBs.

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1 General Information

1.1 Introduction

This manual provides the basic information necessary to install the Microlok® II system and its peripheral equipment (subject to completion of training by a US&S®-approved source). Topics covered include equipment preparation, configuration and mounting, connection of operating power, installation of plug-in boards, and typical printed circuit board external circuit interfaces.

For reference, related Microlok II system manuals include:

SM-6800A - Microlok II System Description

SM-6800C - Microlok II System Startup, Troubleshooting, and Maintenance

SM-6800D - Microlok II System Application Logic Programming

Other manuals that provide information on related US&S systems include:

SM-6700A - GENISYS®-2000 Multi-Purpose Non-vital Control/Communications System (Application Logic Programming)

SM-6470A - MicroTrax® Coded Track Circuit System Application Logic Programming

SM-6470B - MicroTrax Coded Track Circuit System Hardware Installation and Configuration

SM-6700B - GENISYS-2000 Multi-Purpose Non-vital Control/Communications System Hardware Installation and Configuration

US&S® provides no shop maintenance procedures for the Microlok II system circuit boards. These boards are not repairable in the field.

1.2 Rail Team and Technical Support

The Rapid Action Information Link (RAIL) team was created in 1996 to serve the technical needs of current and potential US&S customers. Convenient 24-hour access and a rapid resolution to customer problems are the trademarks of this organization. The RAIL team, which is staffed primarily by US&S product and application engineers, is ready to assist and resolve any technical issues concerning the Microlok II system or any other US&S product.

Any questions regarding the contents of this service manual should be directed to the RAIL team by telephone at 1-800-652-7276 or through Internet E-mail at *railteam@switch.com*.

1.3 Hardware General Description

The Microlok II system consists of modular cardfile-mounted equipment and external peripheral devices that are used to interface the cardfile circuitry to the tracks and to other associated interlocking control systems.

Sections 1.3.1 and 1.3.2 that follow provide an overview of the hardware available for use in the Microlok II system.

1.3.1 System Components

The Microlok II interlocking control system is a multi-purpose monitoring and control system designed for railroad and rail mass transit wayside interlocking functions such as switch machine and signal lamp control, track circuit occupancy monitoring, and non-vital code line communications. Table 1-1 lists the major components of the Microlok II system that are covered in this manual:

Table 1-1 - Microlok II System Major System Components

Name	US&S Part No.	Basic Function(s)
Microlok II cardfile	N16902101	Houses all plug-in printed circuit boards and an optional local control panel.
VCOR relay	N322500-701 (US&S PN-150B)	Switches power to all cardfile vital output circuits under the control of the Microlok II CPU board.
power-off relay	J726153-0283	Detects the failure of commercial power.
isolation module	N17001101 (12V) N17001102 (50V) N17001103 (24V)	Provides the equivalent of double-break output circuit isolation (for line circuits or relays in a separate house). Also enables bi-polar operation of standard vital outputs.
coded track interface panels	N451835-0101 N451835-0102 N451835-0103 N451835-0104	Interfaces the Microlok II system to mainline coded track circuits in non-cab signal territory applications.
cab signal interface panels	N451835-0801 N451835-0802	Interfaces the Microlok II system to mainline coded track circuits in cab signal territory applications.
quick shunt module	N451052-4601	Provides reduced coded track circuit shunt response time in heavy traffic areas.
Type A serial link isolator unit	N17002201	Interfaces the code system interface circuit board (cardfile) to a Glenaire modem or MCP in ARES and serial line carrier code systems.
Type B serial link isolator unit	(to be determined)	Interfaces the code system interface circuit board (cardfile) to ATCS systems.
serial communications adapter panel	N451460-3001	Converts vital EIA serial link signals to 20mA current loop signals. Protects serial communications between different houses/cases.
local control panel	N16901301	Optional built-in LCP.

1.3.2 Cardfile and Plug-In Components

The Microlok II cardfile is designed to house standard 6UX220 Eurocard plug-in printed circuit boards. Most Microlok II printed circuit boards are equipped with integral controls and indications on the board's front panel. Some Microlok II circuit boards, however, (the OS track circuit PCB and one version of the power supply

board, for example) do not have any controls or indications. These boards are mounted behind blank front panels.

In some applications, the cardfile may be equipped with a local control panel (LCP) that takes up several cardfile slots. The LCP is interfaced to the cardfile circuitry and to the external I/O through a dedicated non-vital I/O printed circuit board that occupies a cardfile slot directly behind the LCP. Unused cardfile slots are covered with blank shield panels. These panels come in single slot and multi-slot widths. Each circuit board/panel is attached to the cardfile frame with two slotted-head machine screws. Two extraction levers are provided on each board to make board removal easier. The Microlok II cardfile can be wall or shelf mounted, and can be easily installed in a standard 19" equipment rack.

External wiring is connected to each circuit board through a 48-pin or 96-pin connector. Each connector attaches directly to the board's upper edge connector at the rear of the card file. Certain connector housings incorporate jumpers that are used to set the electrical address for the associated circuit board. The CPU connector housing has an internal EEPROM that is used to store site-specific configuration data. Even if the CPU board is replaced, the configuration data remains intact within the CPU connector's EEPROM.

The Microlok II cardfile plug-in components covered in this manual are listed in Table 1-2. See service manual SM-6800A for a detailed description of each circuit board type.

Table 1-2 - Microlok II Cardfile Plug-In Components

Name	US&S Part No.	Basic Functions
CPU PCB	N17061301	Provides system vital controlling logic, vital I/O management, external serial communications, application logic execution, internal and external diagnostics, event logging, and a user programming and diagnostics interface.
power supply PCB	N16600301* N16660301**	Regulates and protects external power input, conditions and converts the battery input voltage to the various voltage levels required for cardfile circuitry operation, provides an isolated source for external contact sensing, and energizes the VCOR relay under the control of the CPU board. * Without front panel (mounted behind LCP) ** With front panel (no LCP installed in cardfile)
standard vital output PCBs	N17060501 (12V) N17060502 (24V)	Controls standard +/- vital outputs (switch machine relay coil or Microlok II isolation module, for example).
Bi-polar non-vital output PCB (12 bi-polar outputs)	N17061801	Controls bi-polar outputs (to searchlight signal positioning mechanism, for example).
vital lamp driver PCB (16 lamps)	N17060101	Controls signal lamps in color lights and searchlight signals.

Name	US&S Part No.	Basic Functions
vital Input PCBs (16 inputs)	N17061001 (12V) N17061002 (24V) N17061003 (50V)	Receives standard +/- or bi-polar vital inputs (search light mechanism position check, switch machine correspondence, or OS track circuit occupancy, for example). Low and high minimum threshold versions available.
mixed vital I/O PCBs (eight inputs and eight outputs)	N17061601 (12V) N17061602 (24V) N17061603 (Input 50V, output 24V))	Provides same I/O functions as standard vital output PCB and vital input PCB on one board. Low voltage (12V) and high voltage (50V in, 24V out) versions are available.
code system interface PCB	N17061401	Interfaces vital CPU with non-GENISYS 2000 external code system.
non-vital I/O PCB	N17000601 (LCP) N17061501 (32/32)	LCP version interfaces cardfile LCP non-vital I/O with CPU. 32/32 version used for connection to external I/O.
non-vital isolated PCB	N17002801 (9.5-35V)	LCP version. 16 separate inputs for connection to external inputs.
non-vital isolated PCB	N17062701 (9.5-35V)	32 outputs for connection to external outputs.
non-vital isolated PCB	N17063701 (9.5-35V)	32 inputs for connection to external inputs.
coded track circuit PCBs	N451910-0701 N451910-7601 N451910-7602 N451910-7603	Provides train detection in mainline coded track circuits. Versions for non-cab applications and cab applications at various frequencies.
OS track circuit PCB	N451810-6701	Provides OS track circuit train detection in end-of-siding applications.
coder output PCB	N451910-5801	Generates standard 75, 120 and 180 CPM cab signal codes
auxiliary coder output PCB	N451910-7001	Generates two 50 CPM cab signal codes
60/100 Hz cab amplifier PCB	N451910-6401	Generates 60 or 100 Hz cab signal carrier
40/50 Hz Cab amplifier PCB	N451910-6901	Generates 40 or 50 Hz cab signal carrier

1.4 Installing a Microlok II System

WARNING

Failure to obtain approved training, and to act in accordance with the procedures and warnings outlined in these manuals, may result in serious personal injury and/or property damage.

This manual is generic in nature and is intended to cover the installation of the Microlok II system cardfile and its external support equipment for all possible applications of the system. The extent and complexity of each installation depends on the application, the equipment ordered for the application, and the as-shipped configuration of the equipment when it leaves the US&S factory.

In some cases, the entire compliment of equipment may be pre-configured and assembled at the factory. In other cases, board configuration and installation may be done at the installation site. All of these factors are determined mainly by customer preference. Thus, the installation process will differ somewhat from job to job.

Regardless of the specific configuration, there are five basic steps involved in the installation of a Microlok II system. These are:

1. Install the Microlok II cardfile.
2. Install the Microlok II printed circuit boards and make the necessary wiring connections for each specific board.
3. Install the necessary Microlok II peripheral devices and make the necessary wiring connections between the cardfile and the rails/interlocking equipment.
4. Make the necessary communications connections between the Microlok II cardfile and other remote train control equipment.
5. Power up, configure, and test the Microlok II system.

Steps 1 through 4 are detailed in this manual. Note that it may not be necessary to perform all of these steps for all Microlok II applications. Step 5 actually includes a number of system checks and configuration procedures. This information is contained in service manual SM-6800C - Microlok II System Startup, Troubleshooting, and Maintenance.

2 Cardfile and Circuit Board Installation

2.1 Installing the Cardfile

2.1.1 Mounting and Environment

The Microlok II cardfile may be mounted in a standard 19-inch equipment rack, or on a wall or shelf using the fiberglass mounting brackets supplied with the unit.* Keep the cardfile away from sources of excessive heat or battery vapors. Positive ventilation is not required. Cardfile operating temperature limits are -40° to +70°C. Cardfile mounting dimensions (including rear connectors) are shown in Figure 2-1.

* The fiberglass mounting bracket should be used to isolate the cardfile from earth ground.

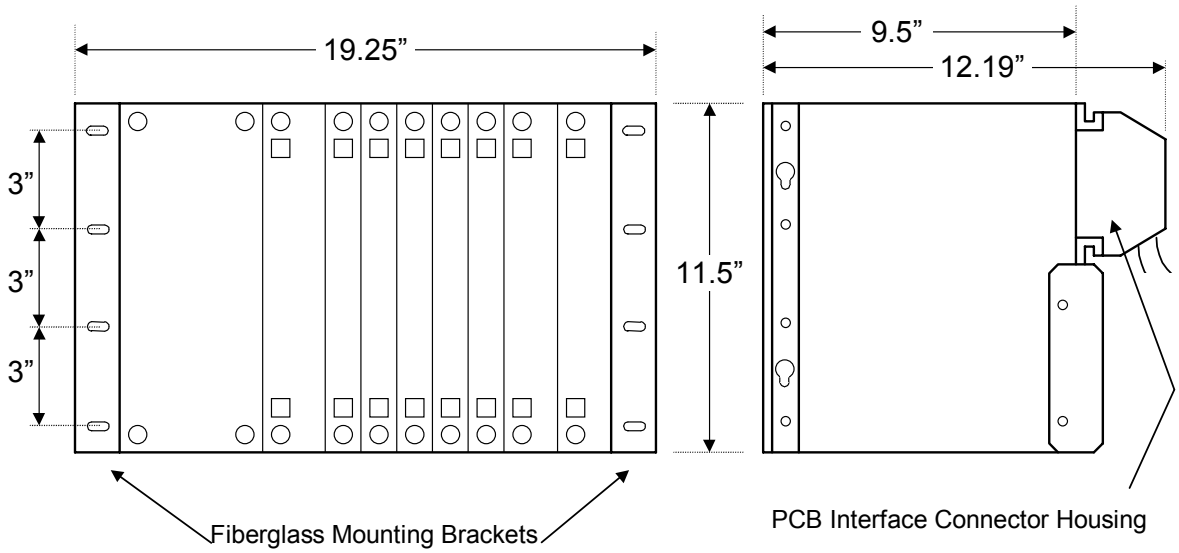


Figure 2-1 - Cardfile Installation Dimensions

2.1.2 General Wiring Practices

Microlok II installations that are wired in the field should be configured to minimize cross talk between wires. “Dirty” wiring (connections to external equipment) should be separated as much as possible from wires carrying electronic data signals. Cables and wires in general should be kept as short as possible to minimize induced line noise. (The input and output wires should be twisted in pairs.) Case/house wiring layouts should also be arranged to minimize noise. Switch heater wire runs, track leads, switch machine power wiring and any other “noisy” wiring should be separated as much as possible from Microlok II wiring, both in the case or house and in outside cable runs. Battery leads should be as short as possible and must be isolated as much as possible from noisy wiring.

2.1.3 Power Input

2.1.3.1 Source

The Microlok II cardfile requires a single, 12 Vdc (nominal) battery for operating power. The requirements for the dc input voltage are as follows:

Voltage:	
Range	9.8 to 16.2 Vdc
Nominal	12.0 Vdc
Min. Startup	11.5 Vdc
Ripple	0.5 VP-P

Current draw on the battery is determined by the application configuration, (number of signal lamps, cab signal carrier frequency, etc.). A constant voltage type charger is recommended for the battery. Note that the battery must be capable of providing a minimum voltage of 11.5 Vdc at system start-up. (This means that anytime the OFF/On switch is operated, battery voltage must be at least 11.5 V. or the unit will not start.)

2.1.3.2 Wiring and Surge Protection

Input power wiring to the Microlok II cardfile is connected through the 48-pin connector attached to the back of the power supply PCB (N16600301 or N16660301). Figure 2-2 shows the typical installation for the battery input to the Microlok II cardfile. Refer to section 2.1.6 for connector wiring data.

Internal system power (+5V, +/-12V) may also be supplied by an externally mounted power supply instead of the plug-in PCB (N16600301 or N16660301). In this case the system VCOR must be controlled by the plug-in CPS Board N451910-7501. The second drawing in Figure 2-2 shows the typical wiring for this board.

CAUTION

The surge suppression devices described below must be installed for all Microlok II applications. Failure to install these devices may result in damage to the power supply or the Microlok II system circuitry due to voltage transients.

restrictions are not followed, damage to equipment could result.

Observe the following guidelines when connecting battery power to the cardfile:

1. To minimize noise, keep the battery leads as short as possible. Whenever possible, the battery leads should be located entirely within the case or house.

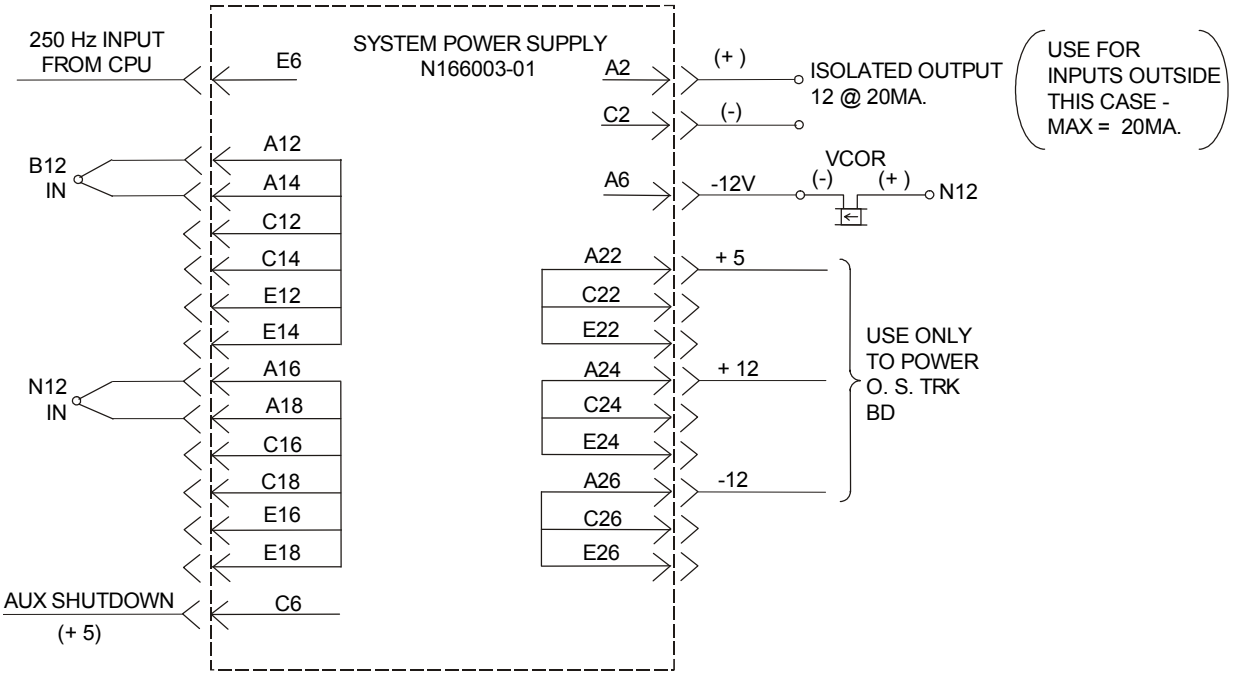
2. Lightning arrestors should not be used on the wiring between the battery and the cardfile.

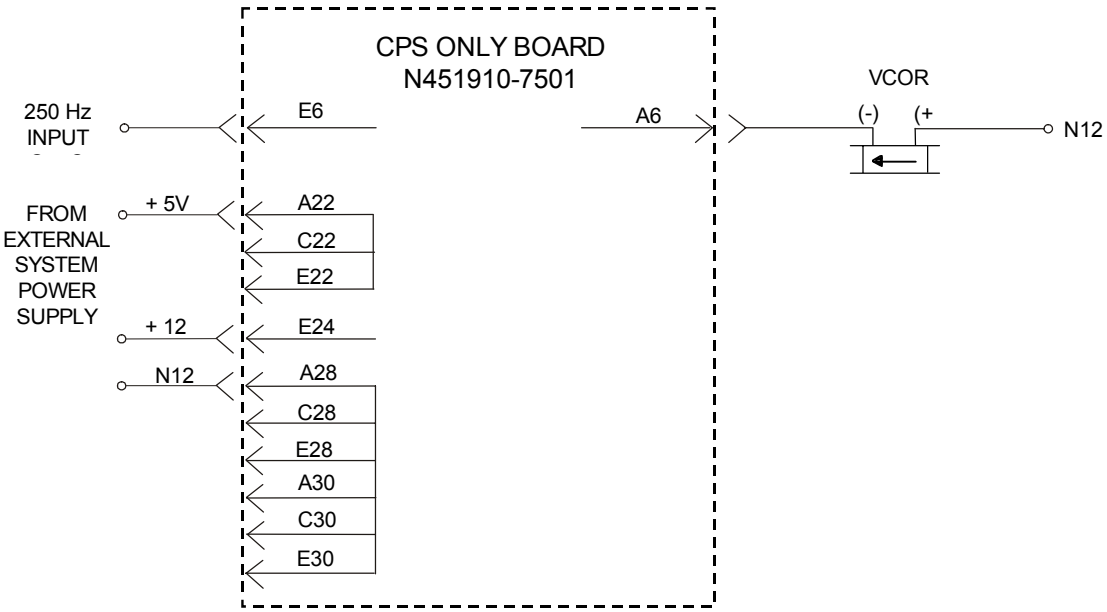
3. Install 40 mm or 60 mm line-to-line and line-to-ground MOVs as follows:

   a) If the feed is 110 Vac, use a Siemens B40K130 or B60K130, or a GE V131DA40 or V131BA60 (J582324).

b) If an isolation transformer is used, also install a block type MOV on the transformer secondary line-to-line.

4. Secondary surge suppression (US&S USSP units) and common mode filtering are not required on the battery wiring to the cardfile.





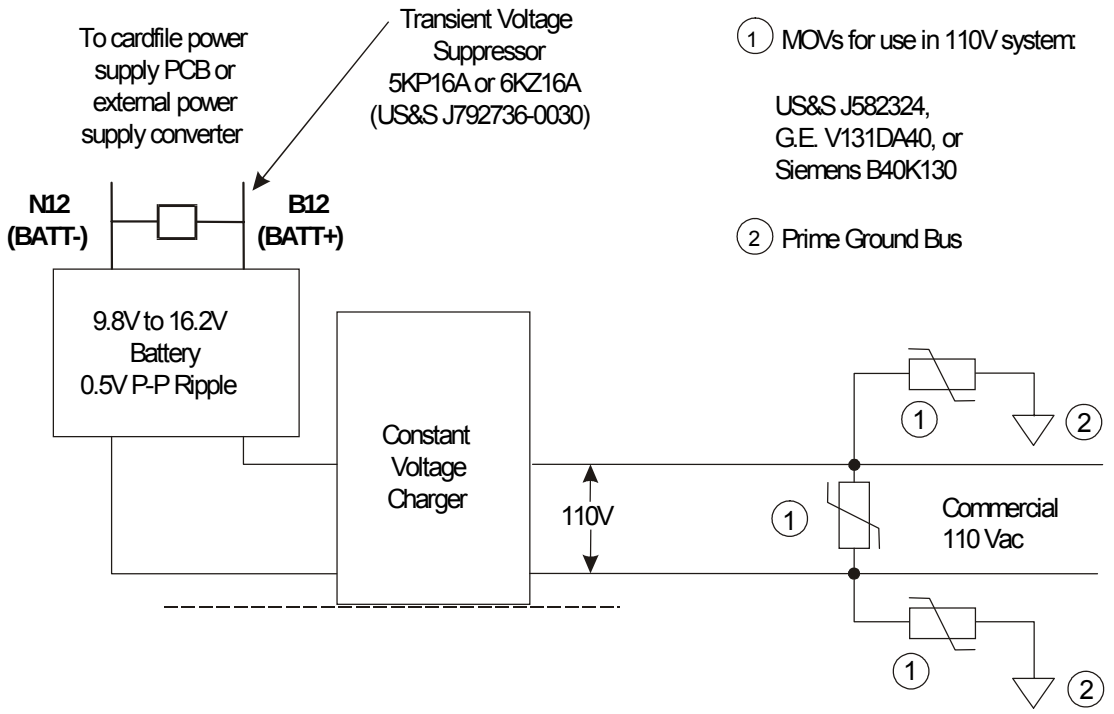


Figure 2-2 - Cardfile Power Input Wiring and Protection

2.1.4 Cardfile Grounding

All Microlok II circuitry is isolated from the Microlok II cardfile chassis. This allows the cardfile to be connected to earth ground for shielding purposes if desired.

For CE-compliant installations, cardfiles must be grounded via the metal cardfile-mounting brackets supplied with all Microlok II units beginning in late-1999. For other installations, optional fiberglass mounting brackets are available from US&S to electrically insulate the cardfile from its mounting structure if desired.

The part numbers for these fiberglass brackets are:

Right M4518114501

Left M4518114502

2.2 Installing the Microlok II Cardfile Plug-ins

Installing the Microlok II system cardfile plug-ins is a four-step process. Each of the following steps must be performed for each circuit board to be installed:

- Selecting the appropriate cardfile slot for each circuit board (section 2.2.1).
- Configuring the cardfile keying plugs for each circuit board (section 2.2.2).
- Configuring the circuit board jumpers and firmware just prior to installation (section 2.2.3).
- Install the circuit boards (section 2.2.4)

2.2.1 Circuit Board Installation Rules

Observe the following arrangement rules when installing Microlok II printed circuit boards and a local control panel (when applicable) into the card file:

A. Refer to Figure 2-3. With the following exceptions, any plug-in PCB may be installed in any cardfile slot:

- Slot 19 cannot be used because there is no corresponding buss connector.
- The code system interface PCB should be installed in slot 20 at the far right hand side of the cardfile. This slot accommodates the special width (1.1 inches) of this board.
- Power supply PCB N16660301, which has a two slot wide front panel, should be used when a local control panel is not being used for the application. Power supply PCB N16600301 (no front panel) should only be used when a local control panel is to be installed.
- If the cardfile is to be equipped with a local control panel:
  - Non-vital I/O PCB N17000601 must be positioned behind the local control panel so that the rear 48-pin connector on the panel engages the front connector of the I/O board. For example, if the LCP covers slots 1 through 7, the non-vital I/O board must be installed in slot 5.

- Power supply board N16600301 (without front panel) must be positioned behind the LCP so that its LEDs are visible in the holes provided on the panel. For example, if the LCP covers slots 1 through 7, the power supply board must be installed in slot 6.

- The OS track circuit PCB is typically mounted behind the LCP in any open slot.

- US&S recommends that the CPU board be installed in slot 18 because it is a double-width module that covers the unusable space of slot 19.

B. If needed, two useable cardfile board slots can be gained by not installing a power supply board. In this case, the cardfile must be powered from an external power supply that meets the applicable rating requirements (see section 3.1 of service manual SM-6800A). Refer to section 2.1.3 in this manual for the recommended power supply wiring scheme.

C. Any two boards can be installed adjacent to one another without concern for EMI or RF effects between the boards. Typically, the boards are grouped according to general function (I/O with I/O and coded track with coded track, for example).

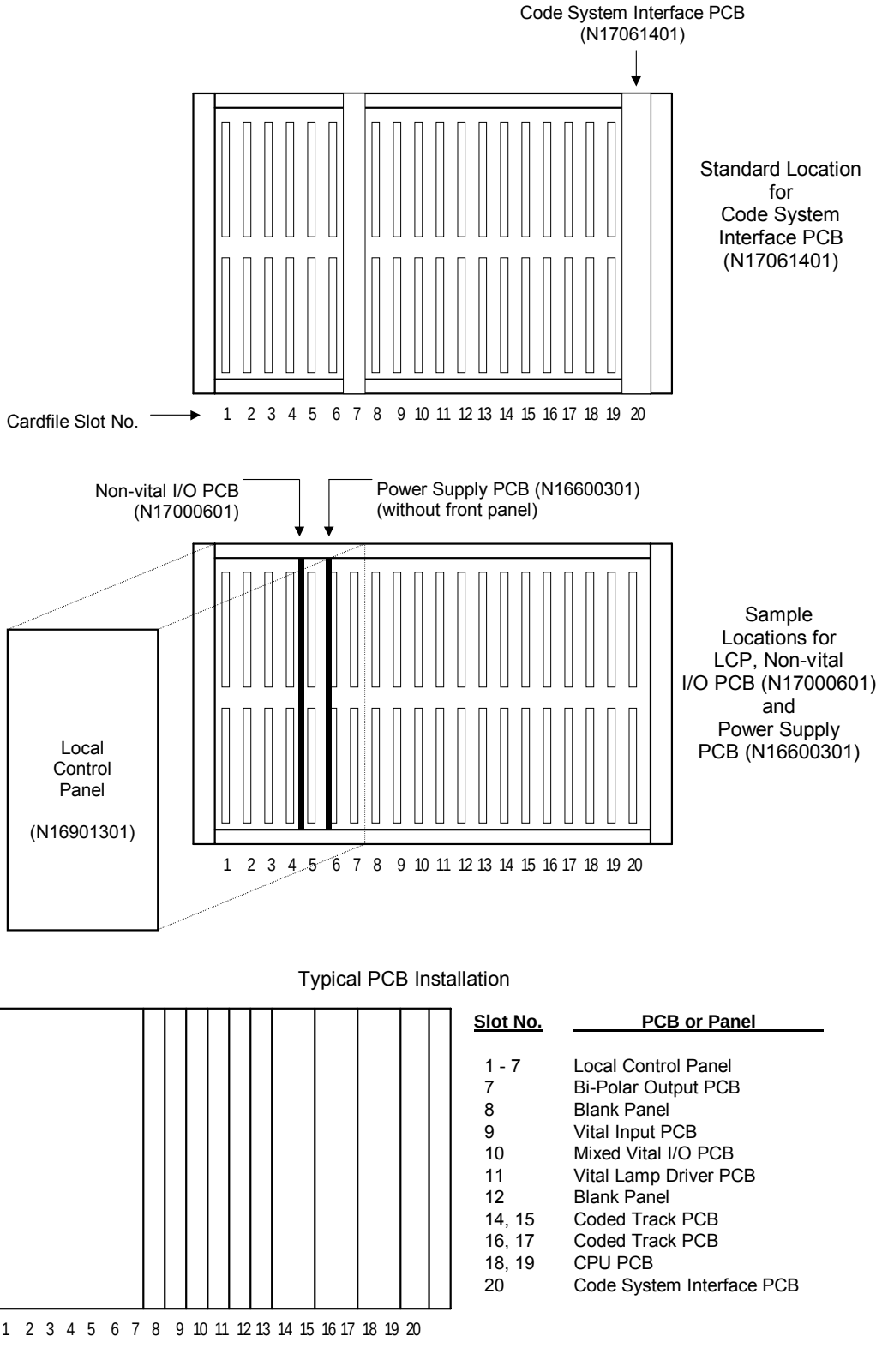
D. All unused slots and slots must be fitted with a blank shield panel so that the entire front face of the cardfile is covered. Available blank panels include:

Single slot shield panel: N451850-2902

Double slot shield panel: N451850-2901

Blank LCP replacement panel: N451850-1101

E. Once the full set of PCBs is defined for the application, keying plugs must be installed in the lower motherboard connectors. These plugs prevent insertion of the wrong replacement board for a given slot. Refer to section 2.2.2 for keying plug installation procedures.



Slot No.	PCB or Panel
1 - 7	Local Control Panel
7	Bi-Polar Output PCB
8	Blank Panel
9	Vital Input PCB
10	Mixed Vital I/O PCB
11	Vital Lamp Driver PCB
12	Blank Panel
14, 15	Coded Track PCB
16, 17	Coded Track PCB
18, 19	CPU PCB
20	Code System Interface PCB

Figure 2-3 - Cardfile PCB and Panel Installation Guidelines

2.2.2 Keying Plug Installation

Each of the Microlok II cardfile slots includes a 12-way female keying guide next to the 96-pin connector. The guide is used to ensure installation of the proper circuit board in each cardfile slot after the complete cardfile board configuration has been determined. Each board is equipped with a corresponding 12-way male keying guide; individual keying tabs are removed at the factory in a specific pattern for the board part number. Prior to installing a board, insert keying plugs (part number J709146-0473) into the corresponding cardfile motherboard keying guide as shown in Figure 2-4 and as listed in Table 2-1.

If it becomes necessary to change the type of board installed in a given slot, the previously installed keying plugs can be removed using a knife or a pair of needle nose pliers.

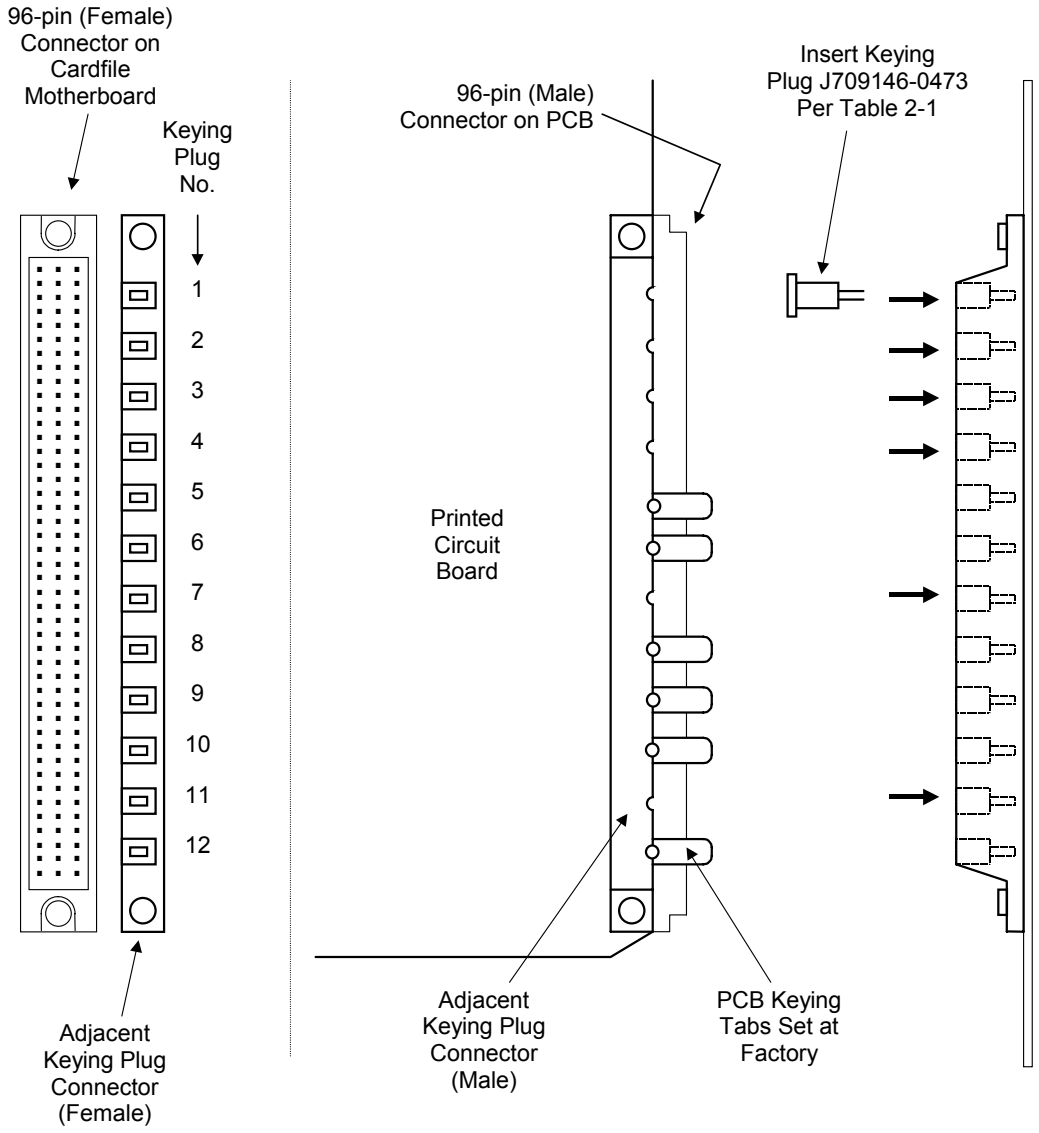


Figure 2-4 - Cardfile Slot Keying Plug Installation

Table 2-1 - Cardfile Motherboard Keying Plug Locations

Printed Circuit Board	Part No.	Keying Plug Location (Figure 2-4)											
		1	2	3	4	5	6	7	8	9	10	11	12
CPU	N17061301	✓	✓			✓	✓	✓		✓			
power supply (without panel)	N16600301	✓	✓	✓					✓	✓			✓
power supply (with panel)	N16660301	✓	✓	✓					✓	✓			✓
standard vital output (12V)	N17060501	✓	✓		✓				✓	✓			
standard vital output (24V)	N17060502	✓	✓		✓					✓		✓	✓
non-vital bi-polar output	N17061801	✓	✓		✓				✓		✓		✓
vital lamp driver	N17060101	✓	✓		✓				✓			✓	✓
vital input (12V)	n17061001	✓	✓		✓				✓	✓			✓
vital input (24V)	n17061002	✓	✓		✓						✓	✓	✓
vital input (50V)	N17061003	✓	✓					✓		✓		✓	✓
mixed vital I/O (12V)	N17061601	✓	✓		✓				✓		✓	✓	
mixed vital I/O (24V)	N17061602	✓	✓			✓	✓	✓	✓				
mixed vital I/O (50V)	N17061603	✓	✓					✓			✓	✓	✓
Serial Link Relay PCB	N17062301	✓	✓			✓		✓		✓	✓		
code system interface	n17061401	✓	✓			✓	✓	✓			✓		
non-vital I/O	N17000601	✓	✓		✓					✓	✓		✓
non-vital I/O	N17061501	✓	✓		✓					✓	✓	✓	
non-vital, isolated	N17002801	✓	✓				✓	✓			✓	✓	
non-vital, isolated	n17062701	✓	✓				✓	✓		✓			✓
non-vital, isolated	N17063701	✓	✓					✓	✓		✓	✓	
coded track circuit	n451910-0701	✓	✓	✓	✓			✓				✓	
coded track circuit	n451910-7601	✓	✓	✓	✓			✓				✓	
coded track circuit	n451910-7602	✓	✓	✓	✓			✓				✓	
coded track circuit	n451910-7603	✓	✓	✓	✓			✓				✓	
OS track circuit	N451810-6701	✓	✓	✓				✓				✓	✓
coder output	N451910-5801	✓	✓	✓			✓		✓				✓
auxiliary coder output	N451910-7001	✓	✓	✓			✓			✓	✓		

Printed Circuit Board	Part No.	Keying Plug Location (Figure 2-4)											
		1	2	3	4	5	6	7	8	9	10	11	12
60/100 Hz cab amplifier	N451910-6401	✓	✓	✓			✓			✓		✓	
40/50 Hz cab amplifier	N451910-6901	✓	✓	✓			✓			✓		✓	
CPS only power supply – no front panel	N451810-7501	No keying plugs											
CPS only power supply - with front panel	N451910-7501	No keying plugs											

2.2.3 Printed Circuit Board Jumper and Firmware Configurations

There are five types of Microlok II printed circuit boards that contain jumpers and firmware that must be configured before each board is installed. These boards are the CPU board, the code system interface PCB, the cab amplifier PCB, the coder output PCB, and the OS Track Circuit PCB.

2.2.3.1 Configuring the CPU Board

2.1.2.3.1 Jumper Settings (See Figure 2-5)

Prior to installing the CPU board in the Microlok II cardfile, the following jumpers (Table 2-2) should be checked to make certain they are in their proper positions per the system application logic software or factory requirements.

NOTE

Bold face letters indicate basic operation with the 21mHz system clock.

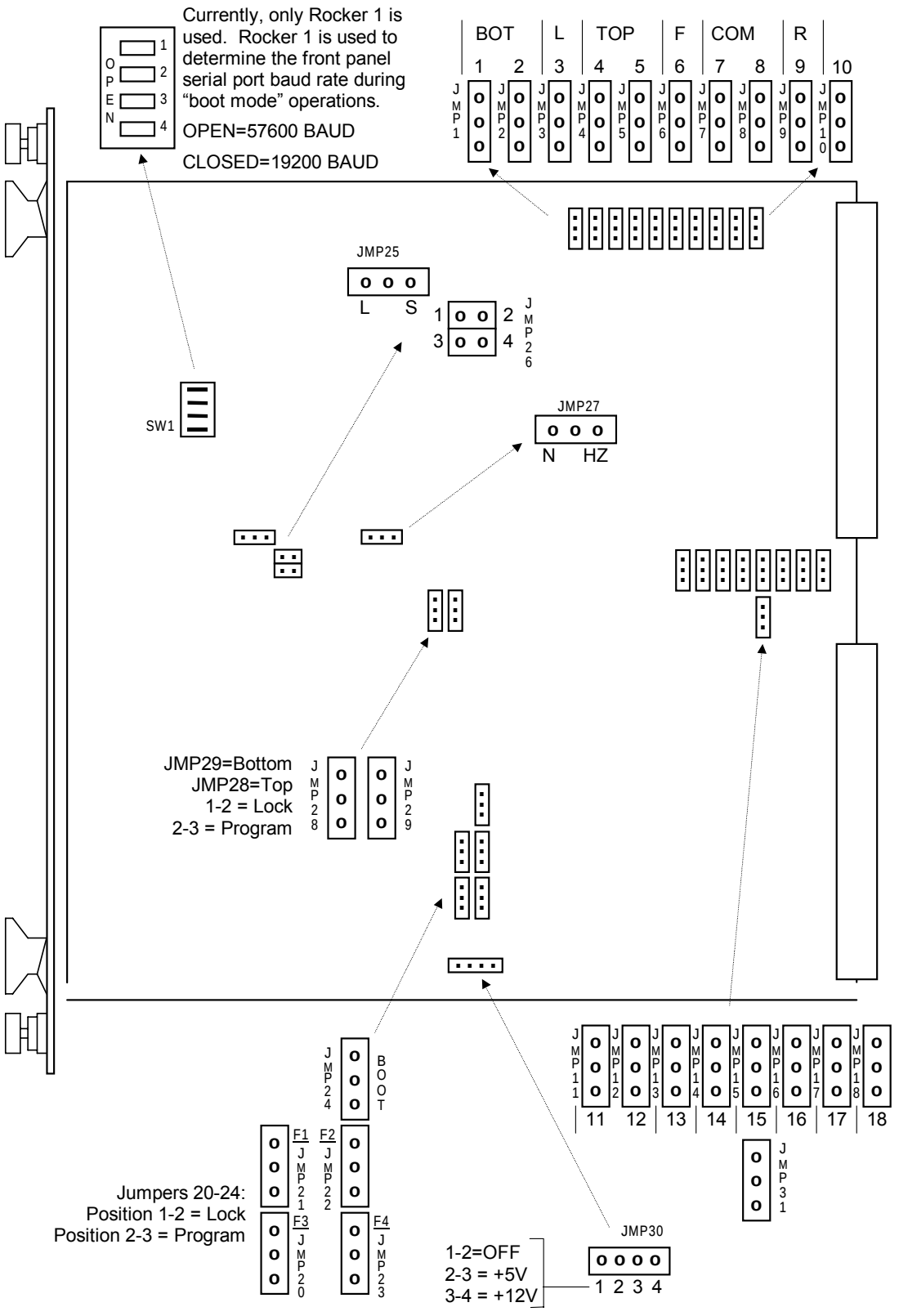


Figure 2-5 - CPU Board Jumper and Jumper Position Checks

Table 2-2 - CPU Board Jumper Positions

Jumper ID	Description		Position	Notes
JMP1	Bottom PCMCIA 2 Wait States		Position 2-3	
JMP2			Not installed	
JMP3	On-Board RAM 1 Wait State		Position 2-3	1
JMP4	Top PCMCIA 2 Wait States		Position 2-3	
JMP5			Not installed	
JMP6	FLASH 1 Wait State		Position 2-3	1
JMP7	Enable COM4 RXD		Position 1-2	
JMP8	Enable COM4 DCD		Position 1-2	
JMP9	Disable Backplane CPU Reset		Position 1-2	
JMP10	COM1 TX.CLK is an Output		Position 2-3	
JMP11	COM3 Voltage Drive Levels	RS-232 RS-423	Position 1-2 Position 2-3	
JMP12	COM3 Voltage Drive Levels	RS-232 RS-423	Position 1-2 Position 2-3	
JMP13	COM3 TX.CLK is an Output		Position 2-3	
JMP14	COM3 TX.CLK is an Output		Position 1-2	
JMP15	COM4 RX.CLK=9.83Mhz		Position 1-2	
JMP16	COM3 RX.CLK=9.83Mhz		Position 1-2	
JMP17	COM2 RX.CLK=9.83Mhz		Position 1-2	
JMP18	COM1 RX.CLK=9.83Mhz		Position 1-2	
JMP19	Not Available		N/A	
JMP20	FLASH 3 Programming Language (Application space)	Locked Program	Position 1-2 Position 2-3	2
JMP21	FLASH 1 Programming Language (Executive space)	Locked Program	Position 1-2 Position 2-3	2
JMP22	FLASH 2 Programming Language (Executive space)	Locked Program	Position 1-2 Position 2-3	2
JMP23	FLASH 4 Programming Language (Application space)	Locked Program	Position 1-2 Position 2-3	2
JMP24	FLASH 1 Boot Block (Boot space)	Locked Program	Position 1-2 Position 2-3	2
JMP25	Speaker Volume	Soft Loud Off	Position 2-3 Position 1-2 Not Installed	
JMP26	IRQ7 Off		Position 2-4	
JMP27	68332 Normal		Position 1-2	1
JMP28	Top PCMCIA Programming Voltage	Locked Program	Position 1-2 Position 2-3	2

Jumper ID	Description		Position	Notes
JMP29	Bottom PCMCIA Programming Voltage	Locked Program	Position 1-2 Position 2-3	2
JMP30	FLASH Programming Voltage	Off 5V 12V	Position 1-2 Position 2-3 Position 3-4	2
JMP31	CPS Drive Normal		Position 1-2	1

Notes:

1. If header posts are not installed in these locations, no jumper is required.
2. Settings shown in boldface are the normal jumper positions, which lock the FLASH devices and prevent their contents from being modified. Refer to the FLASH Programming Instructions for further information.

2.1.2.3.2 DIP Switch SW1

This is an unused input; the rockers may be left in any position without affecting normal system operation.

2.1.2.3.3 PCMCIA Cards

The CPU board is designed to incorporate a PCMCIA memory card module to provide additional logging capability for the User Data Log.

Installation

The PC Card can be installed in the top *or* bottom slot on the Microlok II controller board. The following jumpers must be set correctly:

ID	Description	Position
JMP28	Top PCMCIA Prog Volt Program	2 - 3
JMP29	Bottom PCMCIA Prog Volt Program	2 - 3
JMP30	FLASH Prog Volt 5V or 12 V	2 - 3 or 3 - 4

Use of the PC Card

The PC Card is used to expand the User Data Log logging capability. Currently only one type of FLASH card will be recognized by the executive software: INTEL 28F008S5. This chip has an Intelligent Identifier of 89A6h. Any SRAM card may be used in the system. Current restrictions of the hardware limit the size of the PC Card to a maximum of 6Mb. A 4Mb FLASH Card (J703105-0107) is available from US&S.

Information stored on the PC Card includes:

- Executive and Application CRCs
- First and last numeric ID numbers
- All ID Names for application variables
- User Data Log information

If no PC Card is installed, then the User Data Log is stored in internal RAM.

At reset, the card is detected and checked for correct CRCs and IDNames. IF the CRCs or IDNames do not match the ones present in the executive and application software, the PC Card will be erased and started as a new card. If these items are valid, the executive software finds the starting and ending location for any data stored on the card. If the software cannot find a starting/ending location, or finds an invalid record on the card, it will be erased.

Suggested Application Code

Display PC Card's Health on a front panel

```
NV.ASSIGN ((PCMCIA.INSTALLED & BATTERY.HEALTH) & (LOG.OK | flasher)) TO LED.X;
```

- `PCMCIA.INSTALLED` - System Bit
- `BATTERY.HEALTH` - System Bit
- `LOG.OK` - System Bit
- `flasher` - Toggling 0.5 secs ON / 0.5 secs OFF
- `X` - 1 through 8 for front panel LED

The LED will be ON steady whenever the PC Card is installed and logging information. It will be dark if no PC Card is installed. It will be flashing if a PC Card is installed but write-protected.

2.2.3.2 Configuring the Code System Interface PCB

2.2.2.3.1 EPROM Installation (see Figure 2-6)

CAUTION

When handling any Microlok II circuit board or board component, observe all electrostatic discharge (ESD) precautions. Improper handling of boards or components may result in damage to static sensitive circuitry.

The Microlok II code system interface PCB is shipped without executive or application software EPROMs. Four EPROMs are required for system operation. This includes two executive EPROMs and two application EPROMs. The sockets for these chips are marked as follows:

EXEC EVEN - socket U7

EXEC ODD - socket U6

APPL EVEN - socket U5

APPL ODD - socket U4

Install the executive and application software EPROMs according to their labels, with the "Even" EPROMs inserted in the **EVEN** sockets, and the "Odd" EPROMs inserted in the **ODD** sockets. When installing an EPROM, make certain the chip has the proper pin orientation and is fully inserted.

Executive EPROMs must be selected according to the type of code system emulation. Check the label on the chip to make certain the proper EPROM is installed for the code application. Refer to the following tabulation for application EPROM part numbers.

Application	US&S Part No.
ATC/PTS	N451800-0201
US&S GENISYS	N451800-0202
Harmon MCS-1	N451800-0204
WB&S S2	N451800-0206
Allen Bradley DF1	N451800-0207
ARES	N451800-0208
GRS Datatrain II	N451800-0210
GRS Datatrain VIII	N451800-0211
US&S GENISYS Dual Slave	N451800-0212
US&S GENISYS Dual Ind. Slave	N451800-0213

Refer to Service Manual SM-6700A for EPROM programming procedures.

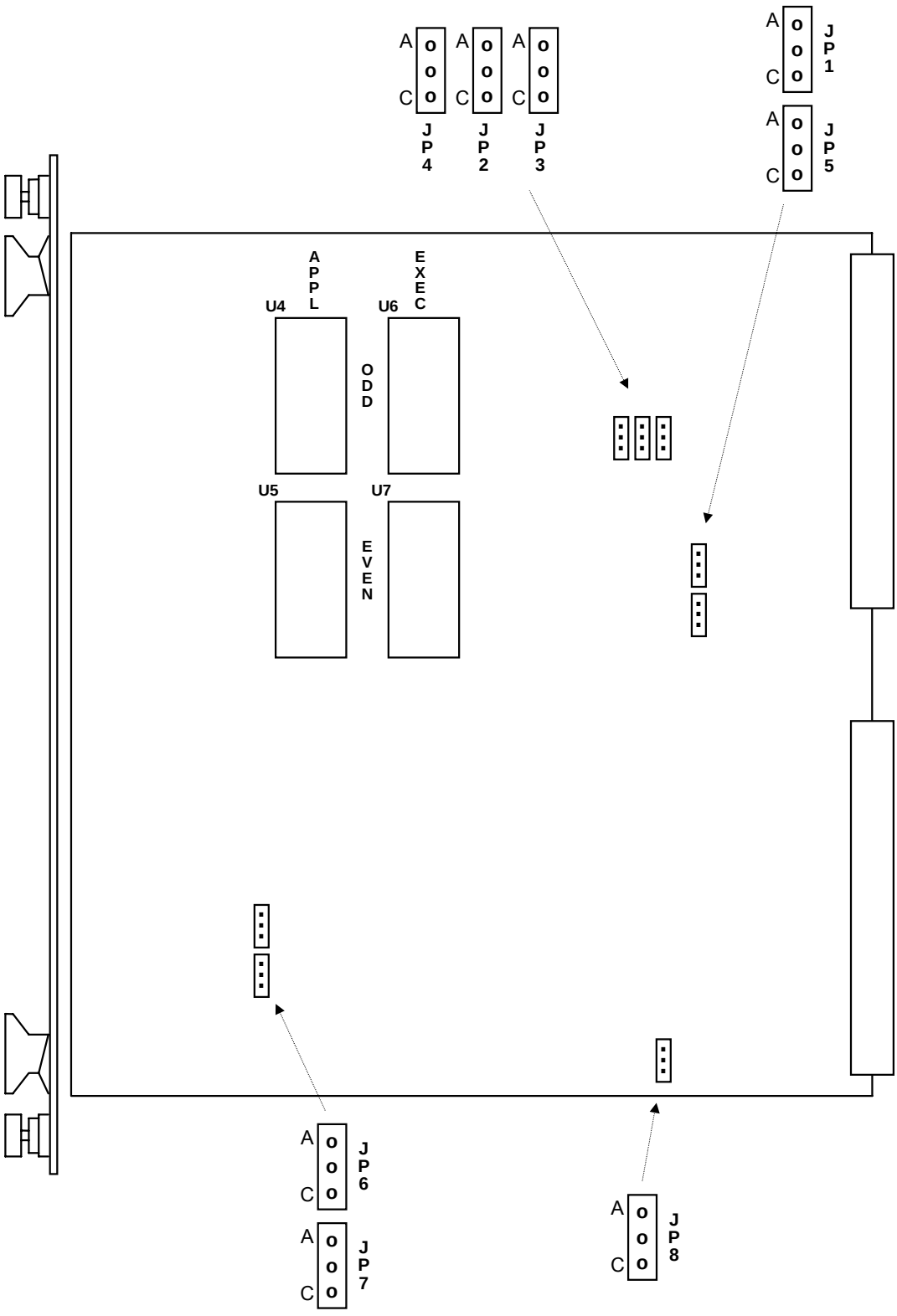


Figure 2-6 - Code System PCB EPROM Installation and Jumper Positions

2.2.2.3.2 Genisys 2000 CSIB Controller Board Jumpers

GENISYS 2000 CSIB Controller Board Jumpers

JUMPER	FUNCTION	POSITION	EFFECT
JP1	Slave port 2 - synchronous transmit clock	AB	External
		BC*	Internal
JP2	Slave port 1 - synchronous transmit clock	AB	External
		BC*	Internal
JP3	Slave port 2 - asynchronous clock; synchronous receive clock	AB	External
		BC* (1)	Internal
JP4	Slave port 1 - asynchronous clock; synchronous receive clock	AB	External
		BC* (1)	Internal
JP5	Slave port 2 - synchronous transmit clock	AB*	Internal
		BC	External
JP6	Watchdog function	AB	Disabled
		BC* (2)	Enabled
JP7	Watchdog time-out	AB* (3)	1200 ms.
		BC	150 ms.
		OPEN	600 ms.
JP8	Bus enable	AB*	Disabled
		BC	Enabled

* Indicates factory configuration.

1. For asynchronous serial port operation, asynchronous clock must be set to internal. External position is used for synchronous communication only.
2. Watchdog MUST be enabled for all normal operation. Disabled position is for factory test only.
3. Factory watchdog setting should not be changed. Lowering watchdog time-out could affect controller reliability.

2.2.2.3.3 Jumper Settings for GENISYS / 5XX, S2, and MCS-1 Slave Applications

Jumper Settings for GENISYS / 5XX, S2, and MCS-1 Slave Applications

Jumper	Position
JP1	BC
JP2	BC
JP3	BC
JP4	BC

Jumper	Position
JP5	BC
JP6	BC
JP7	AB
JP8	AB

2.2.2.3.4 Jumper Settings for ATCS Communication Application

Jumper Settings for ATCS Communication Application

Jumper	Position
JP1	BC
JP2	BC
JP3	AB
JP4	AB

Jumper	Position
JP5	AB
JP6	BC
JP7	AB
JP8	AB

2.2.2.3.5 Jumper Settings for ARES Communication Application

Jumper Settings for ARES Communication Application

Jumper	Position
JP1	AB
JP2	AB
JP3	AB
JP4	AB

Jumper	Position
JP5	BC
JP6	BC
JP7	AB
JP8	AB

2.2.3.3 Configuring the Cab Amplifier PCB

For Microlok II installations that are configured for cab signal generation, the appropriate carrier frequency must be jumper-selected on the cab amplifier PCB. Set jumper JMP-2 as shown in Figure 2-7 to select 60 Hz or 100 Hz operation on PCB –6401, or 40 Hz or 50 Hz operation on PCB -6901.

Also, position jumper JMP-1 to the HIGH position as shown in Figure 2-7. The position of this jumper may be changed during system configuration after the cab signal current levels have been set. Section 6.2.11 of service manual SM-6800C covers this procedure.

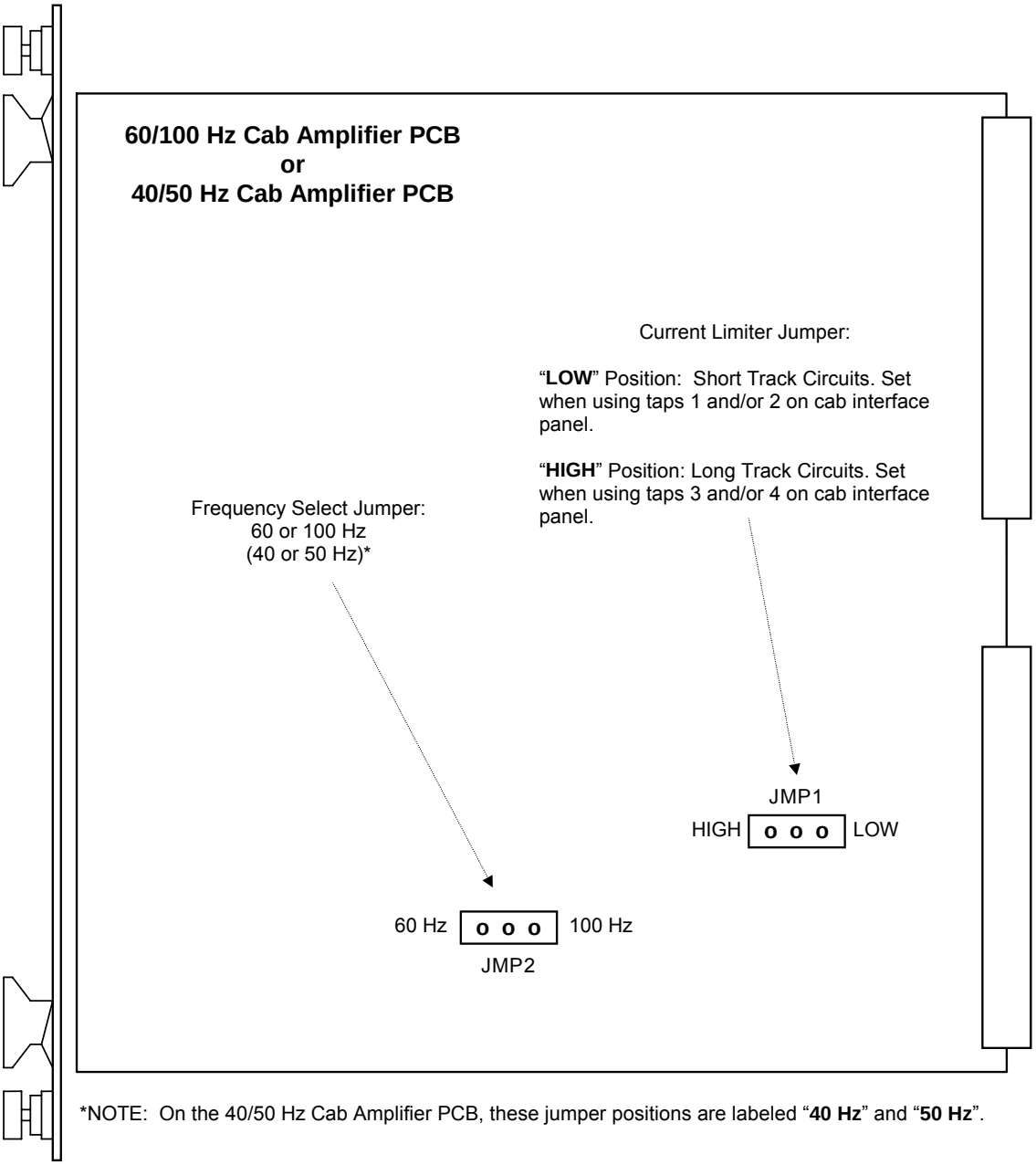


Figure 2-7 - Cab Amplifier PCB Frequency-Select and Current-Limiting Jumpers

2.2.3.4 Configuring the Coder Output PCB (Code Rate Selection)

The coder output PCB is equipped with a single jumper for setting the number of different code rates used by the Microlok II system. Set this jumper to the **3-CODE** position when the system is to be set up for the three standard code rates of 75, 120 and 180 CPM. When the system incorporates additional code rates from the auxiliary coder PCB, set this jumper to the **6-CODE** position. Figure 2-8 shows the jumper position on the board.

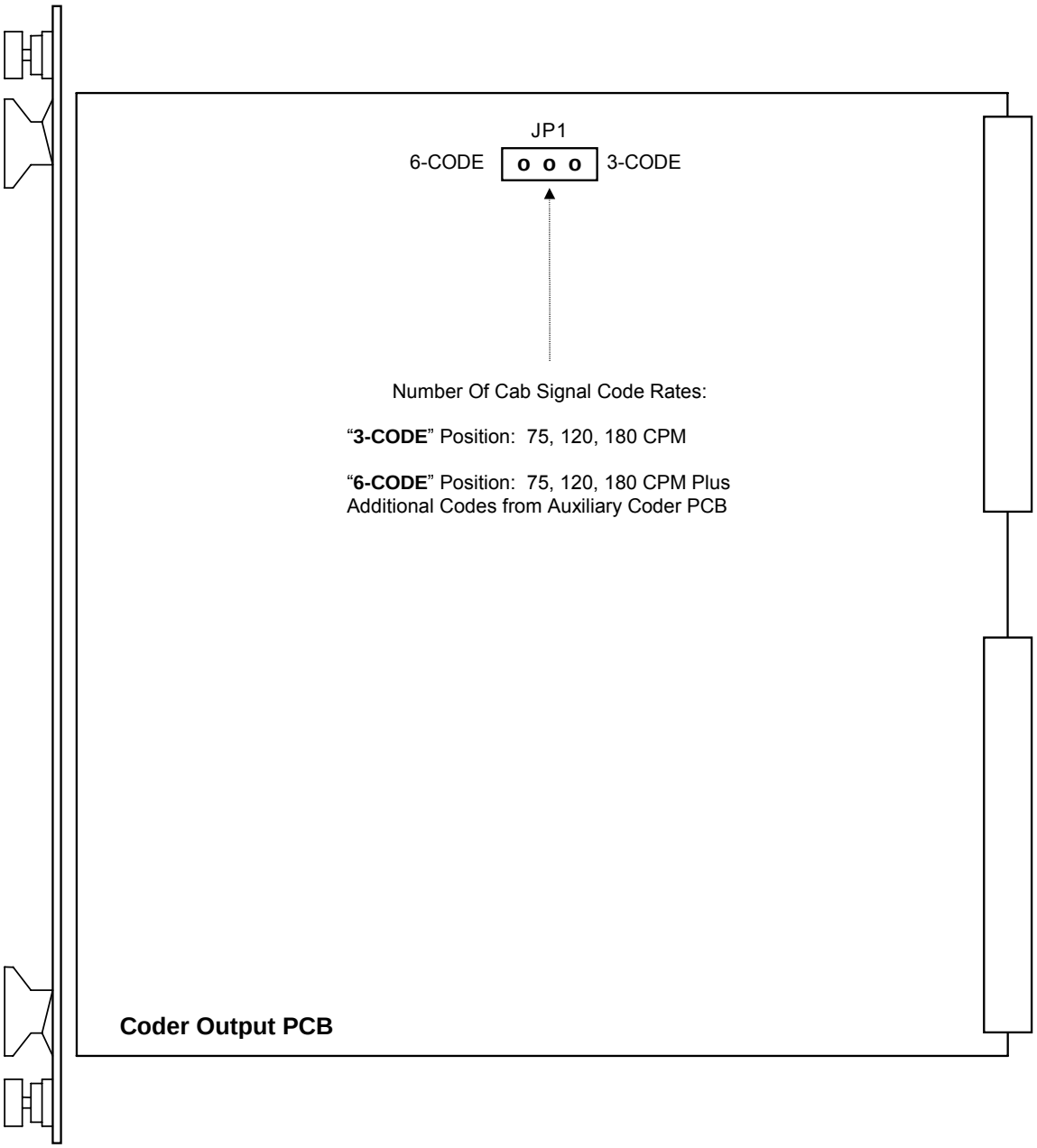
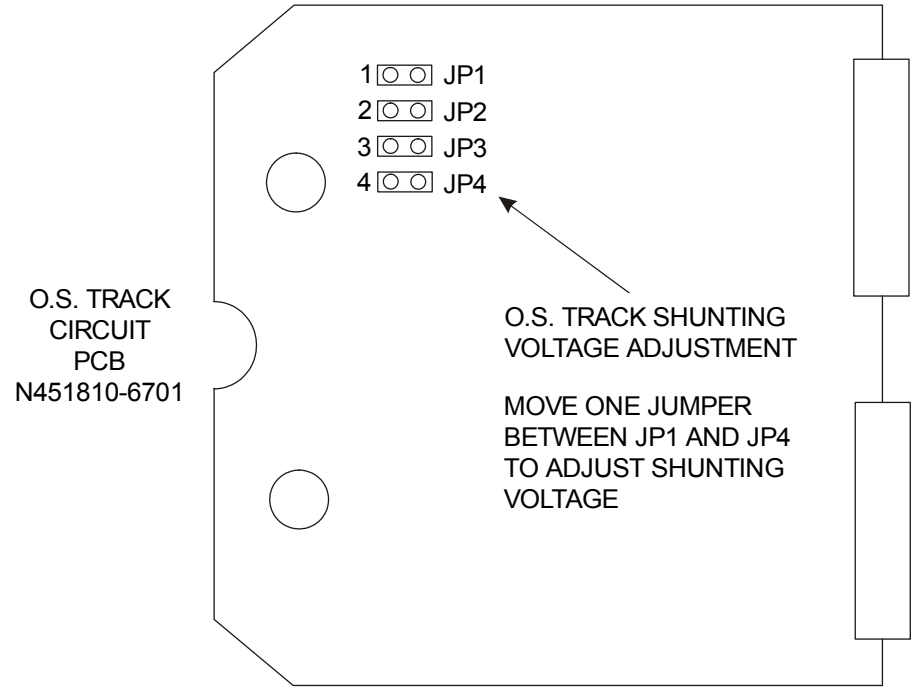


Figure 2-8 - Coder Output PCB Jumper Setting for Cab Signal

2.2.3.5 Configuring the OS Track Circuit PCB

As shown in Figure 2-9, a jumper is provided on the OS Track Circuit PCB (N451810-6701) for the purpose of selecting one of the four possible positions. JP1 represents the lowest power setting and JP4 represents the highest.

1. Connect voltmeters across the MICROTRAX inputs.
2. Select the lowest power setting that results in at least 12V dc on both inputs.
3. Verify this setting by playing a 0.06 ohm track shunt across each leg of the OS circuit, one leg at a time. Each shunt must result in at least one of the two input voltages dropping below 3V dc.



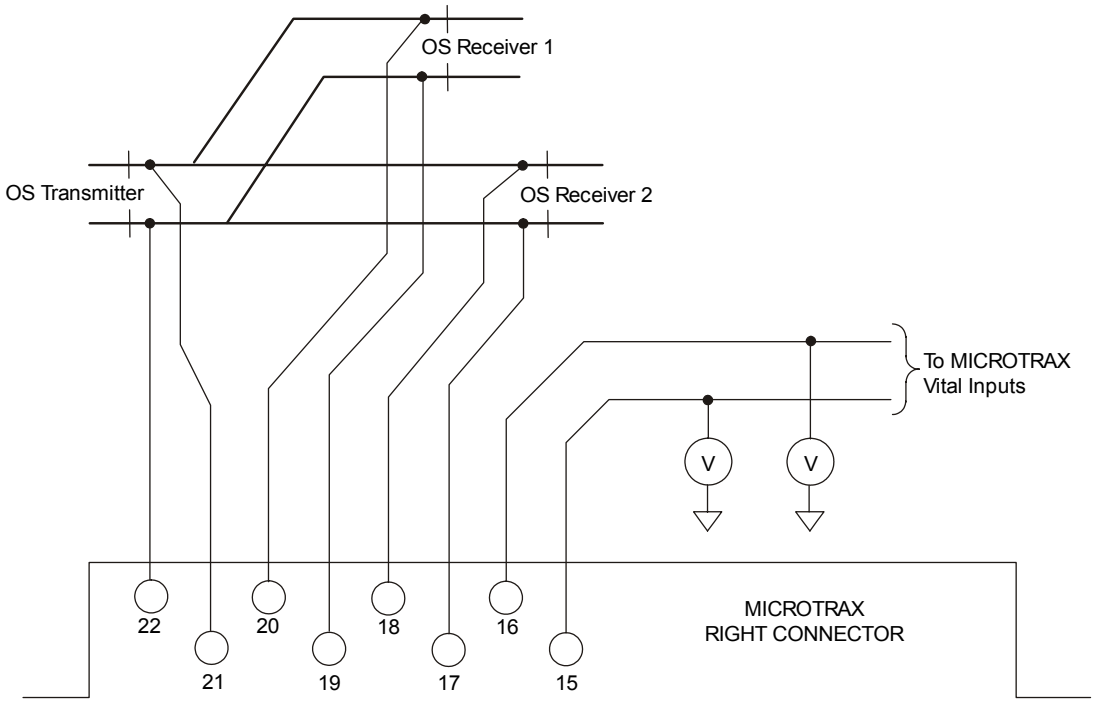


Figure 2-9 - OS Track Circuit PCB Shunting Voltage Adjustment (Jumper)

2.2.4 Installing Microlok II Circuit Boards and a Local Control Panel

US&S recommends that power is removed from the cardfile before removing or installing circuit boards.

Use the following the procedure to install the Microlok II plug-in circuit boards:

1. US&S provides stickers with each Microlok II system that are used to identify the type of circuit board installed in each cardfile slot. Obtain the proper sticker for the board to be installed. Attach the sticker to the inside bottom surface of the cardfile. Make certain that the arrow on the sticker points toward the appropriate card slot.
2. Hold the circuit board to be installed vertically in front of the cardfile.
3. Insert the board upper and lower edges into the plastic card guides inside the cardfile.

CAUTION

When installing any Microlok II circuit board into the card file, do not attempt to force the board into the slot. Damage to the circuit board and motherboard 96-pin connectors may result. If resistance is encountered when installing a board, gently rock the board to engage the male and female connectors. If the board still cannot be fully inserted into the card slot, remove the board from the cardfile and attempt to determine the source of the resistance.

4. Gently push the board into the cardfile until the board and cardfile 96-pin connectors are fully engaged. If the board has an integral front panel, make certain that the rear face of the front panel is flush against the front of the cardfile.
5. If the board has an integral front panel, secure the board into position using the two retaining screws attached to the front panel.

Use the following procedure to install a local control panel:

1. Position the LCP over the front of the cardfile.
2. Align the connector on the rear of the LCP with the connector on the front of the non-vital I/O board (N17000601) in cardfile slot 4.
3. Gently press the LCP onto the front face of the cardfile. Make certain that the rear of the LCP is flush with the front face of the cardfile. Also, ensure that the two LEDs on the power supply board (installed behind the LCP) are properly aligned with the associated holes in the LCP.
4. Secure the LCP in position using the four retaining screws that are attached to the LCP front panel.

2.3 PCB Connector Assembly and Cardfile Address Setting

2.3.1 General

NOTE

Refer to Section 3 for Microlok II printed circuit board interfaces to external circuits.

Individual Microlok II circuit boards are interfaced (as applicable) to external circuits using connector/cable assemblies with a 48-pin or 96-pin female connector housing that attaches directly to the matching connector on the applicable circuit board. All boards except the 96-pin non-vital I/O PCB (N17000601) use the 48-pin connector. Each connector housing is secured to the cardfile backplane with four small machine screws (see Figure 2-10). The complete connector/cable assemblies may be assembled to order by US&S, or assembled by the user.

The connector cable assemblies provide discrete wiring for all available I/O points on each PCB. As shown in Figure 2-9, wire bundles are routed through a protective sleeve on one of the two wiring openings of the connector housing. For most applications, the cable assemblies utilize only one cable opening on the connector housing. However, non-vital I/O PCB N17001501 may need to use both openings to accommodate the full set of 32 input and 32 output wires.

For some Microlok II circuit boards, the connector housing also includes an Address Select PCB with six two-position jumpers used to set the cardfile electrical address of the associated board. These addresses are defined in the Microlok II vital application logic (refer to section 2.4.12). The jumper settings must exactly match the values set in the application program to ensure normal system operation. The following circuit boards do not require a cardfile bus address and do not have jumpers included with the connector housing:

- CPU board
- code system interface
- power supply
- OS track circuit
- cab amplifier
- auxiliary coder output

US&S provides stickers with each Microlok II system that depict individual connector jumpers. After each jumper has been attached to the associated cardfile connector, affix a sticker to the cardfile frame directly below the connector. Use a pen or indelible marker to mark each jumper position on the sticker.

An EEPROM is included within the special connector housing used for the CPU board. This chip holds site-specific configuration data and allows the CPU to be changed while keeping the chip programming intact.

2.3.2 Connector/Cable Assembly Construction Notes

User assembly of the Microlok II connector/cable requires the parts and tools shown in Table 2-3:

Table 2-3 - Microlok II PC Board Connector Components and Tools

Figure 2-9 Item	Description	US&S Part No.	Comments/Vendor Part No.
1	connector housing assembly 48-pin 96-pin	 J709146-1105 J709146-1104	 Used with most PCBs. Used with non-vital I/O PCB N17001501.
2	connector receptacle 48-pin 96-pin	 J709146-0452 J709146-0922	 --
3	receptacle mounting screw	J525400-0001	Mounts both 48-pin or 96-pin receptacle.
4	guide 48-pin 96-pin	 J709146-1106 J709146-1107	--
5	wire crimp contact 48-pin, #16 to #20 wire 48-pin, #20 to #26 wire 96-pin, #20 to #28 wire	 j709146-0453 j709146-0853 j709146-0921	 Harting 09-06-000-8482 Harting 09-06-000-8481 Harting 09-06-000-8484
--	crimp tool, for: 48-pin, #16 to #20 wire 48-pin, #20 to #26 wire 96-pin, #20 to #28 wire	--	 Harting tool 09-99-000-0077 Harting tool 09-00-000-0076 Harting tool 09-00-000-0075
--	extraction tool, for: 48-pin, #16 to #20 wire 48-pin, #20 to #26 wire 96-pin, #20 to #28 wire	--	 Harting tool 09-99-000-0087 (Contact US&S) Harting tool 09-99-000-0101
--	insertion tool, for: 48-pin, #16 to #20 wire 48-pin, #20 to #26 wire 96-pin, #20 to #28 wire	--	 (Contact US&S) (Contact US&S) Harting tool 09-99-000-0100
--	locator tool, for: 48-pin, #16 to #20 wire 48-pin, #20 to #26 wire 96-pin, #20 to #28 wire	--	 Harting tool 09-99-000-0086 (Contact US&S) Harting tool 09-99-000-0099
6	Address Select PCB 48-pin housing 96-pin housing	 n17003101 n17003301	Used to set cardfile slot address on selected PCBs. N17003101 replaces N17002002 N17003301 replaces N17002101

Fig. 2-10 Item	Description	US&S Part No.	Comments/Vendor Part No.
1	connector housing assembly 48-pin 96-pin	 J709146-1105 J709146-1104	 Used with most PCBs. Used with non-vital I/O PCB N17061501.
2	connector receptacle 48-pin 96-pin	 J709146-0452 J709146-0922	 --

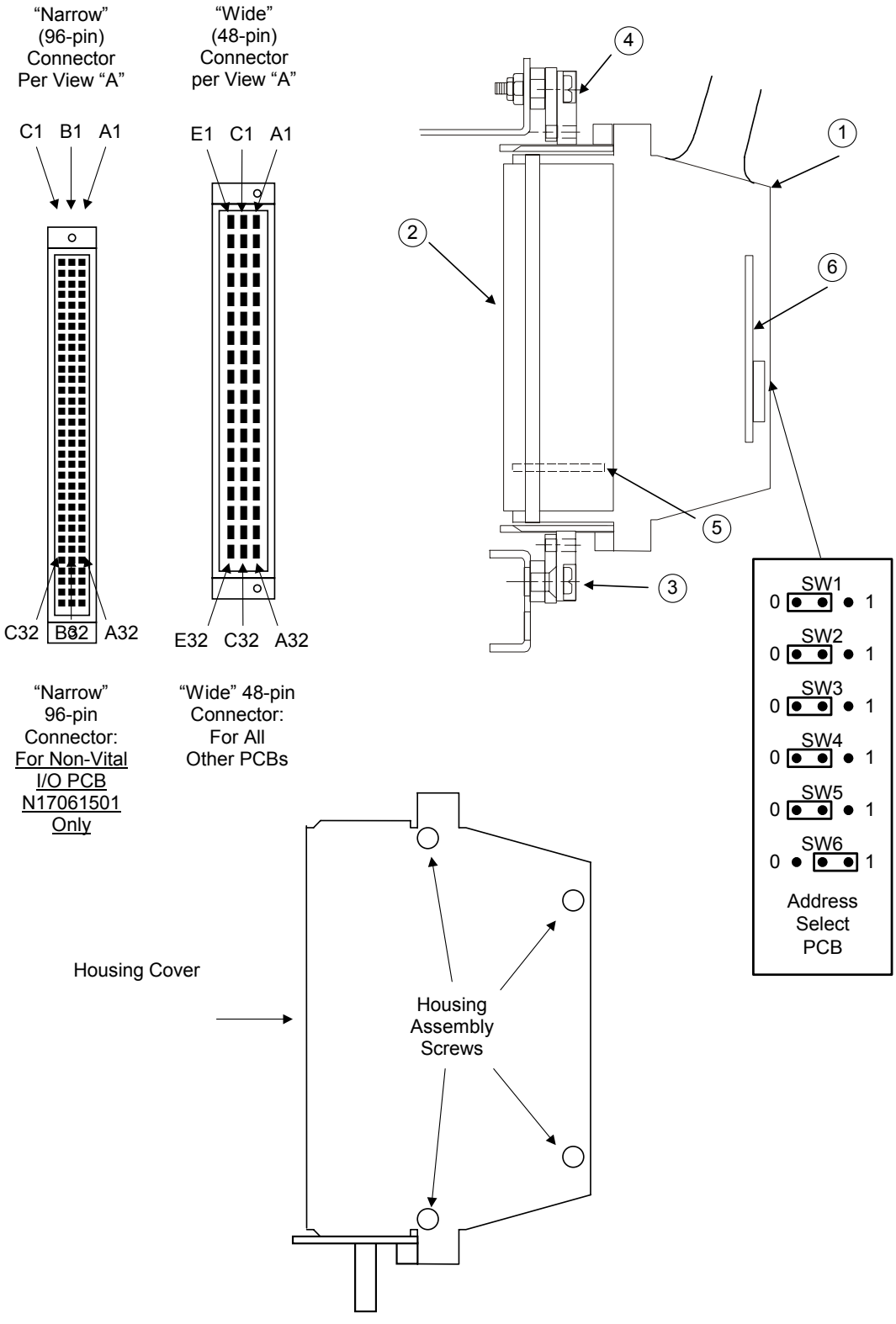


Figure 2-10 - PCB Wiring Connector Mounting and Integral Address Switch Board

2.3.3 Shelf Mounting Assembly Notes

Shelf mounting requires the use of the kit shown in Table 2-4:

Table 2-4 - Microlok II PC Shelf Mounting Kit

Figure 2-11 Item	Description	US&S Part No.	Comments/Vendor Part No.
1	Shelf mounting kit	X16903906	--

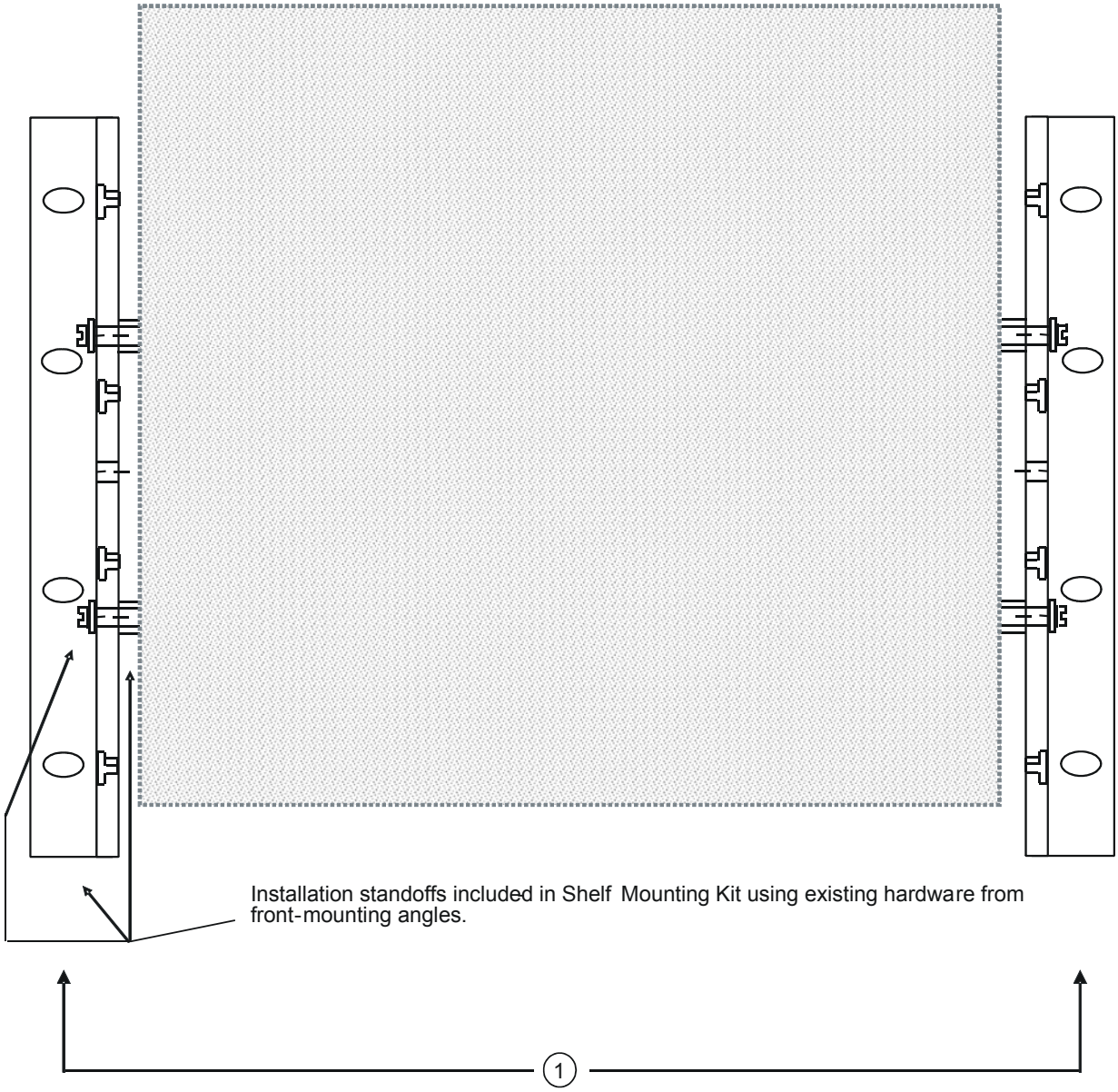


Figure 2-11 - Shelf-Mounting Kit

2.4 Circuit Board Connections to External Circuits

The configuration of the external wiring to each Microlok II printed circuit board depends entirely on the board type and the selected application. Sections 2.4.1 through 2.4.11 that follow, detail the specific connection requirements for each type of Microlok II circuit board.

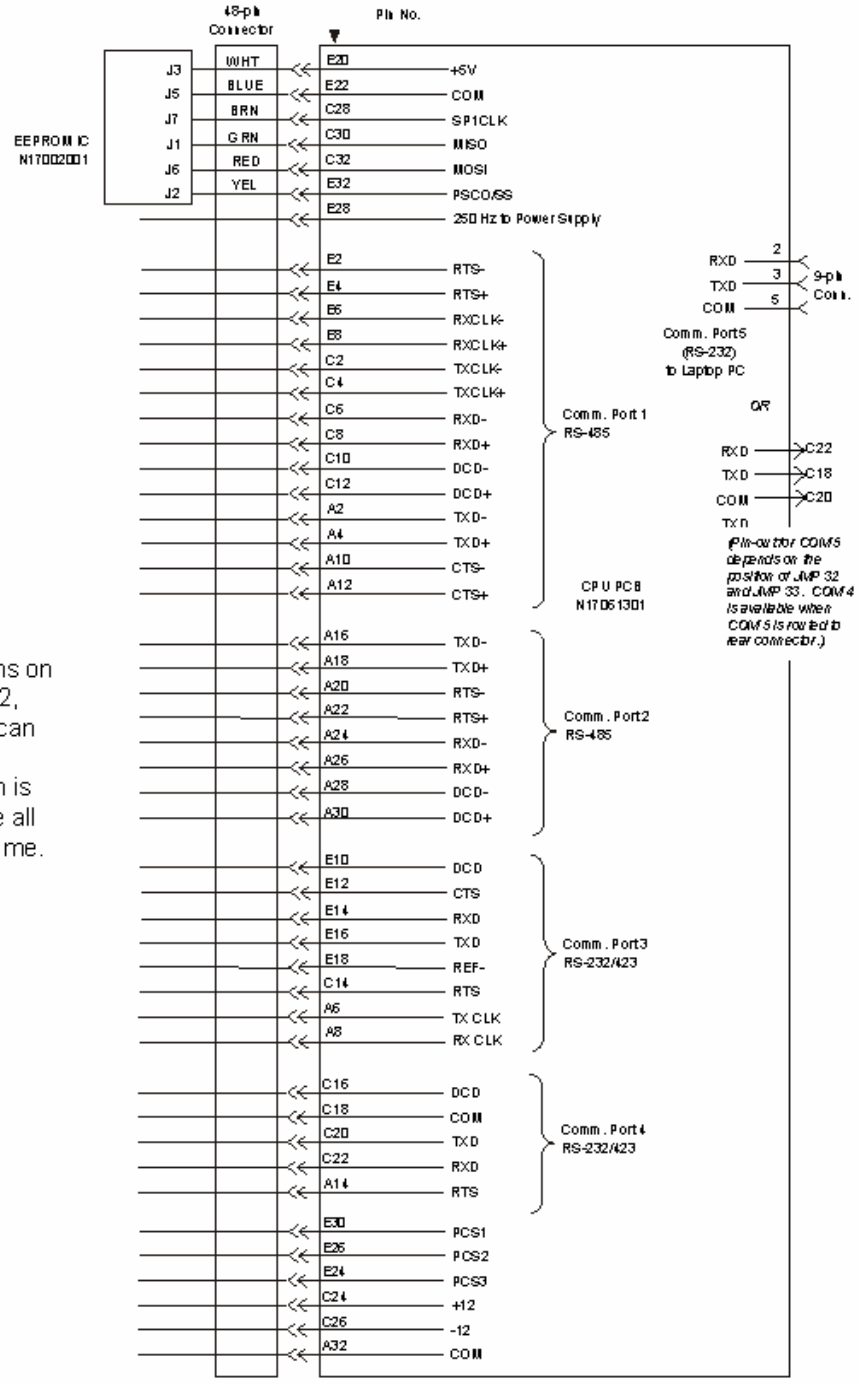
2.4.1 CPU Board

The CPU board contains the central controlling logic and diagnostic monitoring for the Microlok II system, and provides serial five data ports. Four of these ports are used for communication with external systems (see Figure 2-25). The fifth port enables the connection of a laptop PC for software maintenance, diagnostics, and data log downloading. This diagnostic port is terminated at the 9-pin connector on the CPU board front panel

The four general purpose ports can be used for vital serial communications with another Microlok II system, a Microlok system, or one of the MicroTrax systems (coded track, end-of-siding or cab signal controller). For installations where the Microlok II system is communicating with another vital system in the same house or case, the maximum serial cable length is 50 ft. A modem is required for cables longer than 50 ft.

For locations where the Microlok II system and the remote vital system are located in different cases or houses, US&S recommends the use of a serial communications adapter panel (N451460-3001). This device converts EIA-level signals to 20mA current loop signals, and is designed to protect signal lines from transient line noise. Serial communications adapter panels are required at both the Microlok II location and the remote location. Refer to section 3.6 for panel installation and wiring.

The four configurable ports can also be used as a non-vital channel to interface the Microlok II system to an external GENISYS-2000 non-vital code system. In this configuration, the non-vital application logic resides in the CPU board along with the vital application logic. Alternately, the code system interface PCB can be used to interface the Microlok II system to an external GENISYS-2000 system. In this application, the non-vital application logic resides on the code system interface PCB. Refer to section 2.4.8 for external connections to the code system interface PCB.



Note

There are three common connections on this board (C18, A32, and E22). Any pin can be used wherever a common connection is required as they are all electronically the same.

Figure 2-12 - CPU PCB - Basic Interface Wiring

2.4.2 Vital Input PCBs

Each of the vital input PCBs can accept up to 16 isolated inputs. The specifications for these boards are as follows:

US&S Part No.	Nom. Input Voltage	Min. Voltage to Ensure ON State	Voltage to Ensure OFF State	Max. Sustained Input Voltage
N17061001	12V	9.5V	7.0V or less	34V
N17061002	24V	17.0V	9.0V or less	62V
N17061003	50V	35.0V	15.0V	72V

There are no power connections required through the upper connector. When wiring a vital input PCB to a relay contact circuit contained in the same house as the Microlok II cardfile, the signal battery may be used as the energy source to activate the inputs. Terminals designated (-) may be connected to battery N12 and B12 switched over relay contacts.

When wiring a vital input PCB to a relay contact circuit outside the Microlok II house, use the isolated source that is part of the power supply. This is consistent with the practice of confining signal battery to the case in which the Microlok II unit is housed. External wiring should be protected with equalizer lightning arrestors from line-to-line (US&S part number N451552-0101) and with high voltage arrestors from line-to-ground (US&S part number N451552-0201).

As shown in Figure 2-13, inputs can also be wired in a bi-polar configuration. Note in the Figure 2-12 example that input 7 is on and input 8 is off for the polarity indicated. For the reverse polarity, input 7 is off and input 8 is on.

Noise Protection

1. US&S recommends the use of twisted pair wiring (2-3 turns per foot) for all input to minimize possible noise.

2. US&S recommends the separation of “clean” and “dirty” wiring. Ideally, all inputs are gathered in a bundle, all outputs are gathered in a bundle, and power wiring is gathered in a bundle. Each of these bundles is physically separated from other house wiring. It is particularly important to maintain this physical separation from high-current “dirty” wiring.

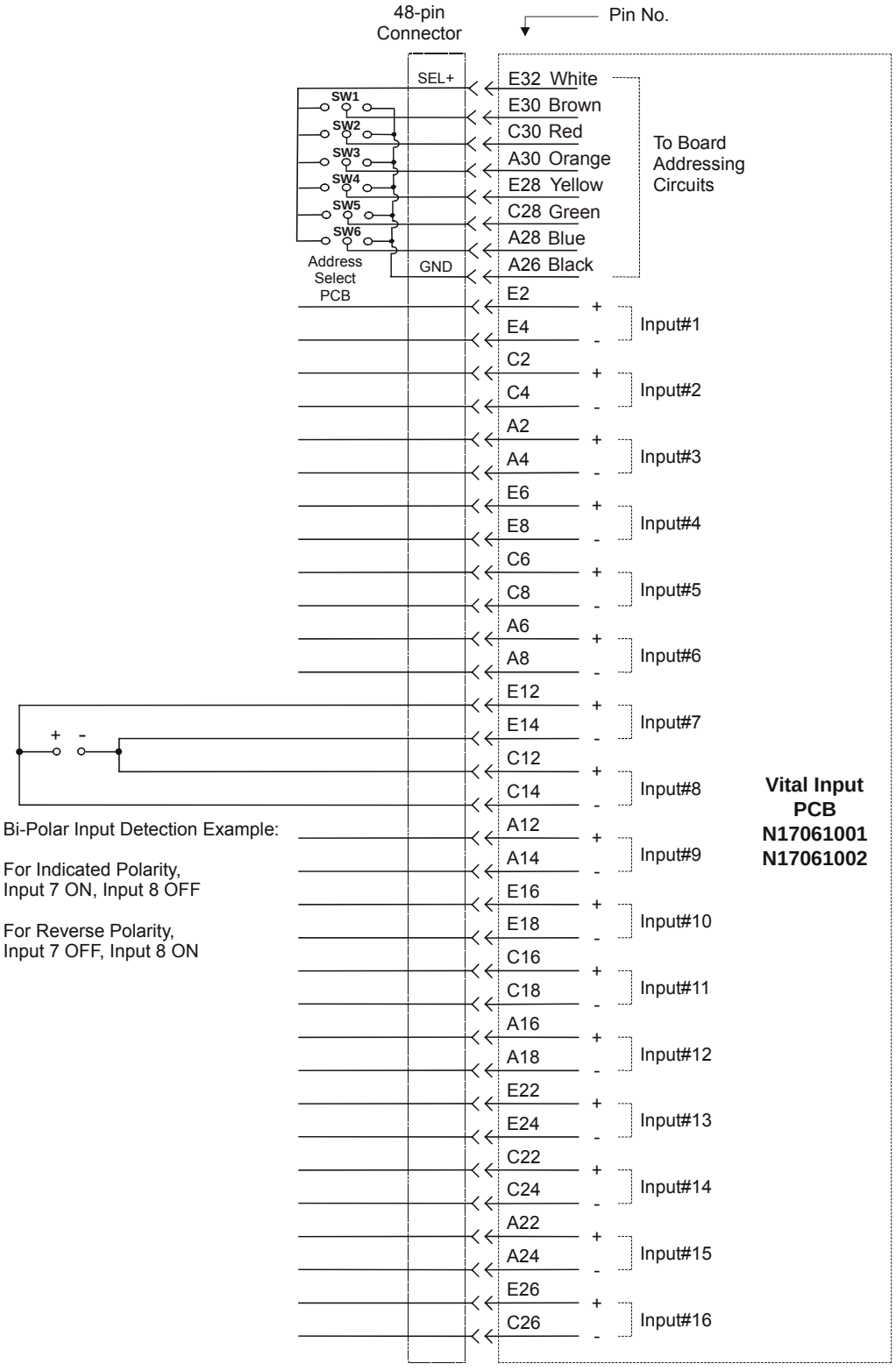


Figure 2-13 - Vital Input PCB - Basic Interface Wiring

2.4.3 Standard Vital Output PCBs

Each of the standard vital output PCBs provides up to 16 outputs. The specifications for these boards are as follows:

US&S Part No.	Voltage V_{BATT} Range	Load Resistance Range	Max. OFF Voltage	Min. ON Voltage
N17060501	12V	50 Ω - ∞	0.75V	V_{BATT} - 1V
N17060502	24V	100 Ω - ∞	1.5V	V_{BATT} - 1V

Outputs are controlled by "high side" software-controlled switches. Loads should be connected from outputs to battery negative. The high side switch is used to connect battery (+) to the output.

Each output is protected with a polyswitch, which acts like a circuit breaker. When the overcurrent trip point is reached (approximately 0.75A), the polyswitch switches to a high impedance. The switch resets to its normal low impedance when the additional load or short is removed. A short to battery (-) will trip the polyswitch and cause the VCOR relay to drop, but will not cause any damage. A short to battery (+) will not cause any damage, but since this condition is equivalent to a false output, the Microlok II CPU will cause the VCOR relay to drop. Figure 2-13 shows the suggested wiring connections for the standard vital output PCBs.

There are multiple connecting points available for both the B12 and N12 connections. A single contact can handle up to 3 amps of load current. If the anticipated load current exceeds 3 amps, use additional connecting points for the B12 and N12 feeds (one point for each additional 3 amps).

2.4.3.1 Noise Protection

Relay Coil Snub

Relay snubs are intended to dissipate large electromagnetic surges from the coil inductance and to prevent these surges from interfering with normal operation of the Microlok system. It is recommended that all relays being driven by Microlok be snubbed to prevent unwanted monitor errors. This is particularly true where the coil load to the Microlok relay driver is being broken by a series contact.

Relay snubs can also be installed on other relays that are not directly controlled by Microlok outputs, but may be contributing to possible noise due to their close proximity to the Microlok wiring.

US&S recommends the use of transorbs (J792736-0002) for relay snubbing. They will have minimal effect on relay timing.

Resistors are also suitable relay snubs. When using a resistor loading of the Microlok output an effect on timing (relay drop away) must be considered.

Diodes can also be used as snubs but:

1. They will definitely increase relay drop time.

They may cause contact burning in some circuits.

WARNING

Do not use diodes or any devices that could function as a diode in ac or dc electrified territory; otherwise, voltage induced by the device could cause a relay to remain falsely energized.

Twisted Wire

US&S recommends the use of twisted pair wiring (2 to 3 turns per foot) for all relay loads to minimize possible noise. This should be done wherever possible on all I/O wiring.

Wire Separation

US&S recommends the physical separation of clean and dirty wiring. Ideally, all outputs are gathered in a bundle, inputs are gathered in a bundle, and power wiring is gathered in a bundle. Each of these bundles is physically separated from each other (6" preferred) and all bundles are physically separated from other house wiring. It is particularly important to maintain this physical separation from high-current "dirty" wiring.

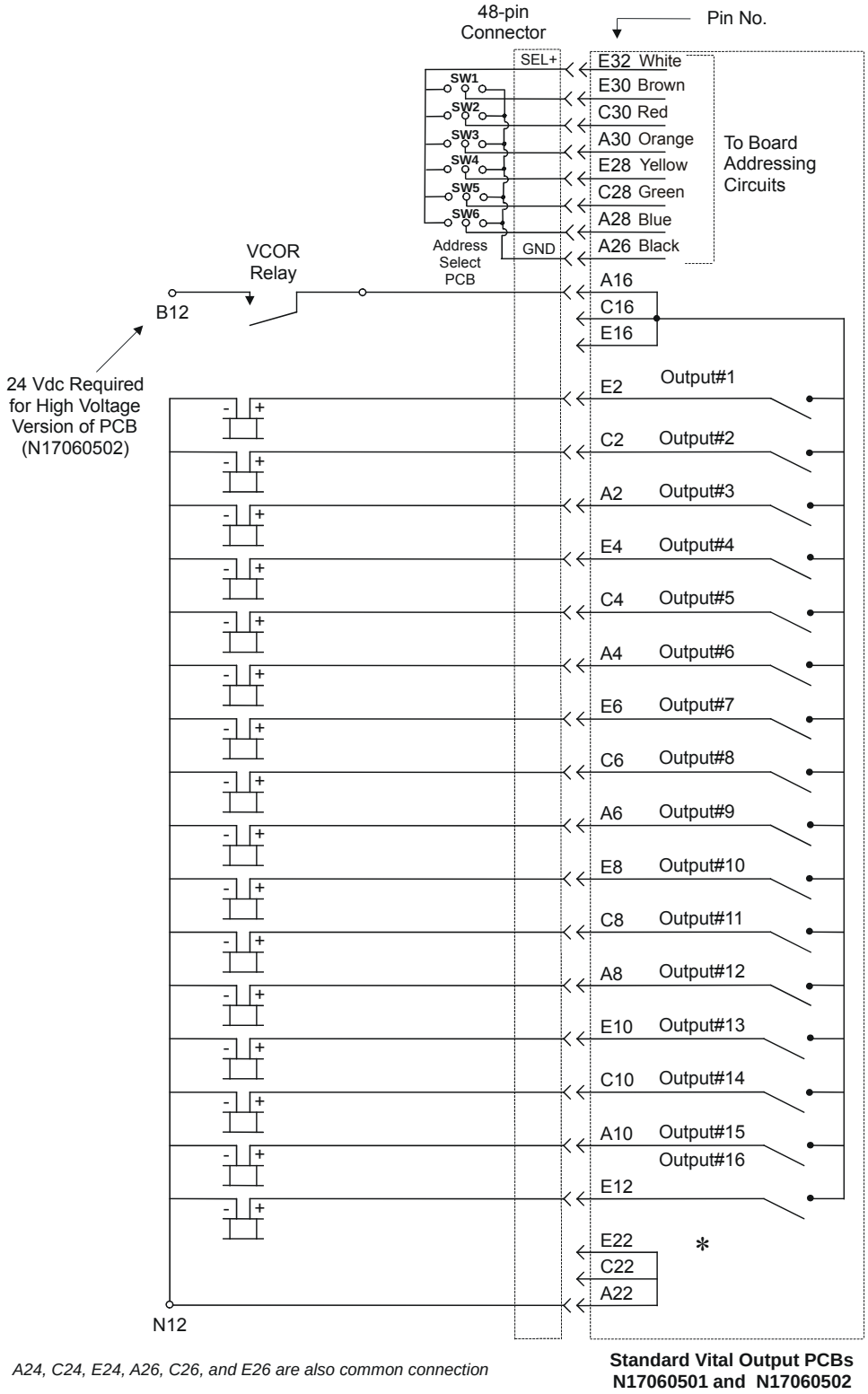


Figure 2-14 - Standard Vital Output PCB - Basic Interface Wiring

2.4.4 Bi-polar Output PCB

The bi-polar output PCB provides 12 outputs and is typically used to drive searchlight signal positioning mechanisms. The specifications for this board are as follows:

Voltage V_{BATT} Range	Load Resistance Range
12V	250 Ω - ∞

The 12 physical outputs change polarity under the control of 24 paired virtual outputs (VO). Alternate assertion of a virtual pair changes the polarity of the physical output. Each output circuit has two LEDs (one green and one yellow) on the board front panel that indicate the on/off state and the polarity of the output. If either VO associated with a bi-polar output is asserted, the associated LED, green or yellow, will be illuminated. If neither element of the pair is asserted, the output is off and the corresponding LEDs are both off.

Example:

Physical output #1 is connected to terminals E2 and E4 and is controlled by virtual outputs VO1 and VO2. If VO1 is asserted, B12 is routed to E2, N12 is routed to E4, and the yellow LED will be illuminated. If VO2 is asserted, B12 is routed to E4, N12 is routed to E23, and the green LED will be illuminated. Figure 2-14 shows the relationships of the remaining virtual outputs, physical outputs, and front panel LEDs.

Outputs on the non-vital bi-polar output PCB are protected from short circuits and inadvertent connection to either B12 or N12. If both virtual outputs of a pair are asserted, a warning will be logged on the CPU board and the output will default to an off state.

NOTE

These outputs are non-vital. When used with searchlight mechanisms, vitality is ensured by feedback of the mechanism contacts to Microlok II or a vital input. The status of the call is compared in the application software.

If a vital bi-polar output is required, the isolation module should be used. (See section 3.4 in this manual.)

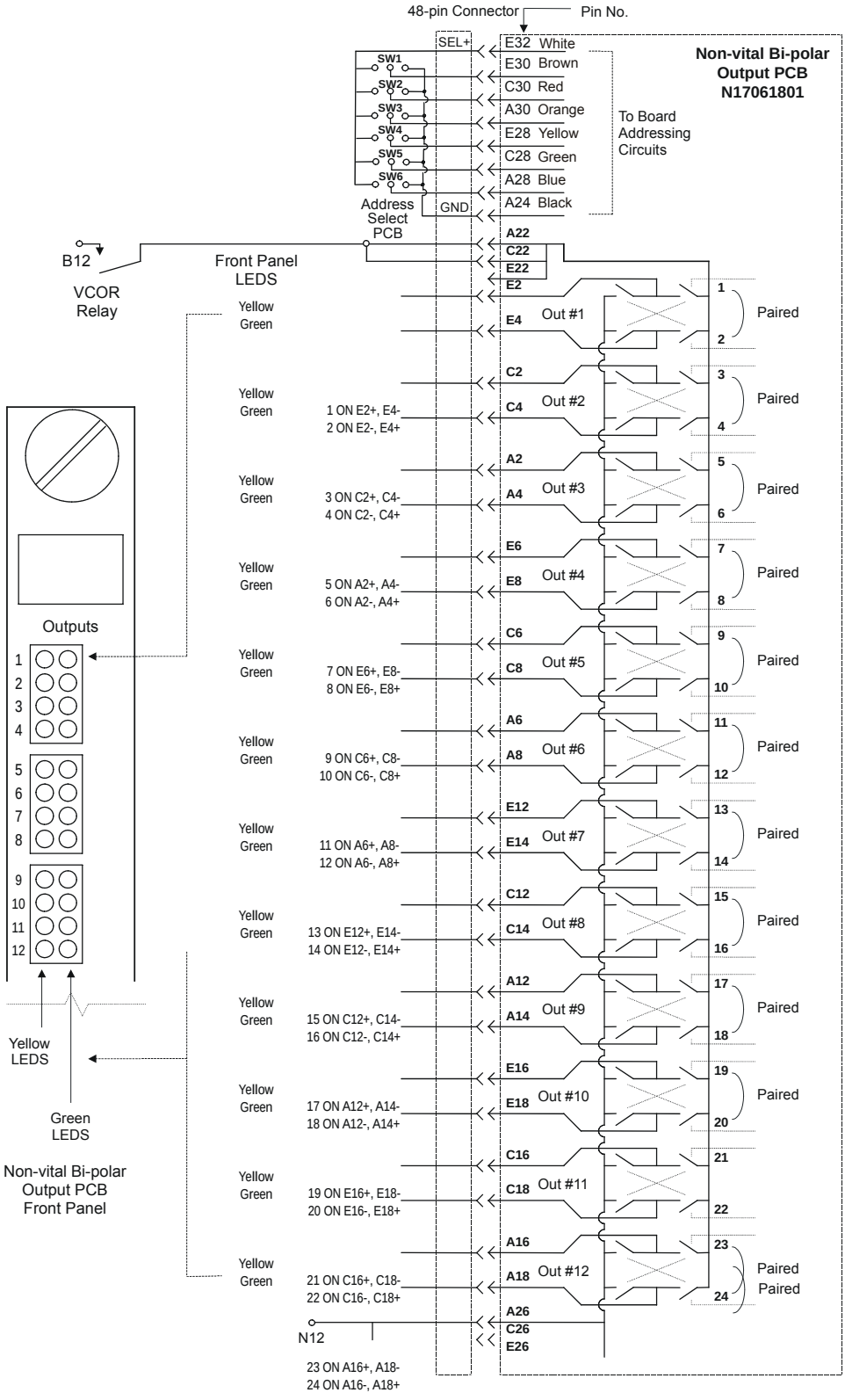


Figure 2-15 - Non-vital Bi-polar Output PCB - Basic Interface Wiring and Correspondence with Front Panel LEDs

2.4.5 Vital Lamp Driver PCB

Depending on the lamp power ratings, the vital lamp driver PCB can operate up to 8, 12, or 16 signal lamps. The specifications for this board are as follows:

Signal Lamp Volt. Range	Signal Lamp Watt. Range	Max. Activated Load	Max. No. of 25W Lamps	Max. No. of 18W Lamps	Max. No. of 36W Lamps
10V - 12V	16W - 36W	300W	12	16	8

Outputs from this board are controlled by "low side" software switches, thus lamps must be connected from the output through a front contact of the VCOR relay to battery (+). A short from an output to N12 or B12 will not cause damage, but the system will detect an error and shut down due to the false lighting of a lamp. A variable dropping resistor should be installed in the common return for each signal head to provide a means of adjusting lamp voltage. This resistor limits current in the event of a short circuit outside the house or case. This arrangement protects vital lamp driver circuitry from damage. To accommodate unusually long signal lamp leads, battery voltage on the lamp driver PCB can be increased to 18 Vdc.

Figure 2-15 shows the typical wiring of the vital lamp driver PCB. Note in the lower part of the figure that for each pair of lamps that can be lit at the same time, one return to N12 should be used. For the example shown in the figure, five lamps can be turned on at the same time, thus three N12 return connections are required.

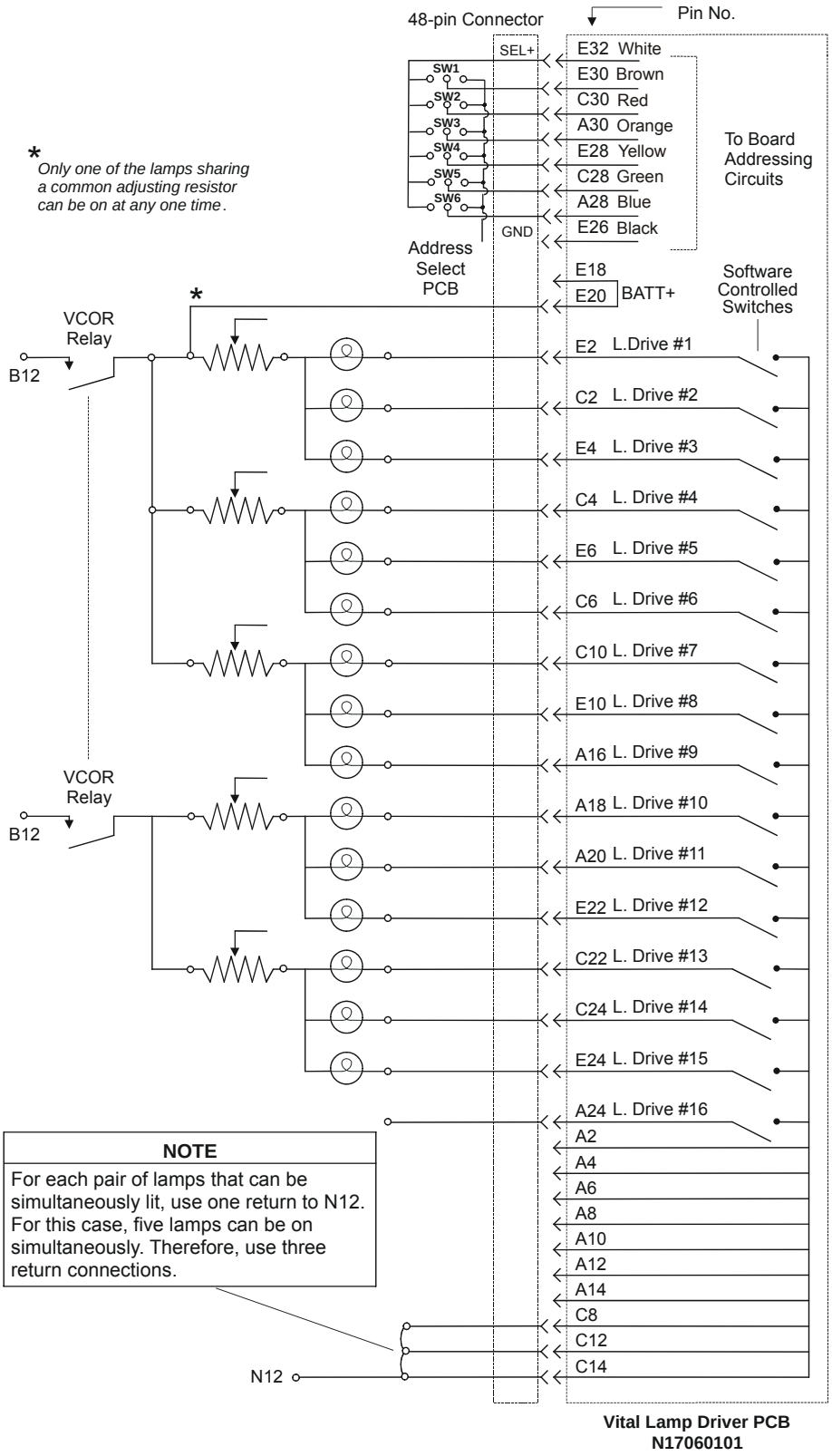


Figure 2-16 - Vital Lamp Driver PCB - Basic Interface Wiring

2.4.6 Mixed Vital I/O Boards

The mixed vital I/O boards provide up to 8 isolated inputs and 8 non-isolated outputs. This board type is used for smaller applications that do not require full vital input or standard vital output boards. The specifications for the mixed vital I/O boards are as follows:

Output Specifications				
US&S Part No.	**Voltage V_{BATT} Range**	**Load Resistance Range**	**Max. OFF Voltage**	**Min. ON Voltage**
N17061601	12V	50 Ω - ∞	0.75V	V_{BATT} - 1V
N17061602	24V	100 Ω - ∞	1.5V	V_{BATT} - 1V
N17061603	24V	100 Ω - ∞	1.5V	V_{BATT} - 1V

Input Specifications				
US&S Part No.	**Nom. Input Voltage**	**Min. Voltage to Ensure ON State**	**Voltage to Ensure OFF State**	**Max. Sustained Input Voltage**
N17061601	12V	9.5V	7.0V or less	34V
N17061602	24V	16.0V	12.0V or less	62V
N17061603	50V	35.0V	15.0V	72V

Inputs can be wired in a bi-polar configuration. Note in the Figure 2-16 example that input 7 is on and input 8 is off for the polarity indicated. For the reverse polarity, input 7 is off and input 8 is on.

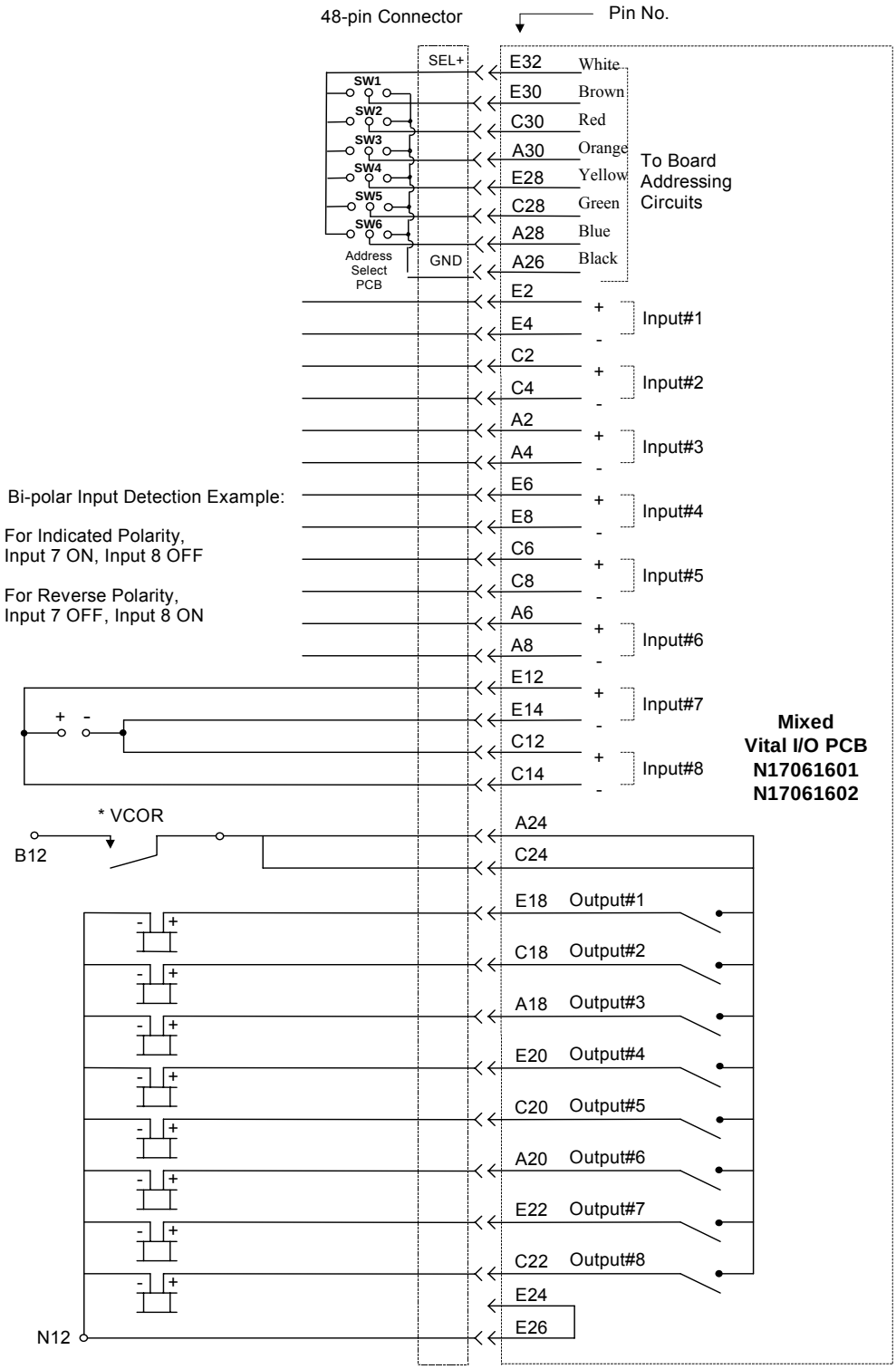


Figure 2-17 - Mixed Vital I/O PCB - Basic Interface Wiring

* Note: Even if you are using only inputs on this board, you must connect B12 to A24 and/or C24. This may or may not be through the VCOR.

2.4.7 Non-Vital I/O PCBs

Two versions of the non-vital NV.IN32.OUT32, I/O PCBs are available. The LCP version (N17000601) is designed for use with the optional Microlok II Local Control Panel (LCP) – N16901301. This version of the board is fitted with a 48-pin connector on the front and back. The front connector engages the LCP. The remaining I/O (16 inputs and 8 outputs) are available on the rear connector. The other version of the NV.IN32.OUT32 board (N17061501) connects each of it's 32 inputs and outputs to a 96-pin connector mounted on the rear of the board. Both boards are treated as the same type of board in the Microlok II application software.

Non-vital, optically isolated I/O PCBs are available as NV.OUT32 (N17062701), NV.IN32 (N17063701), and NV.IN32.OUT16 (N17002801). See Figures 2-19A, B, and C for basic interface wiring diagrams.

The NV.OUT32 PCB provides 32 isolated, outputs for control of external devices such as indicators and relays. The outputs are divided into two groups of 8 outputs and one group of 16 outputs, each group having a separate bussed common (negative DC) reference output. Isolation allows switching power from sources isolated from the Microlok II power supply battery. Outputs are designed to operate at battery voltages between 9.5 and 35VDC. Outputs switch positive battery and are capable of supplying up to .5AMPS. Nominal voltage drop per output is load dependent and usually less than 2.5volts.

The NV.IN32 PCB provides 32 isolated external inputs. The 32 inputs are divided into two groups of 8 inputs and one group of 16 inputs, each group having a separate bussed common (negative DC) reference input. External input voltages between 6 and 35VDC represent logical "1".

The NV.IN32.OUT16 PCB provides 16 isolated external inputs. These external inputs each have separate (+) and (-) connections and present a logical "1" when the applied voltage is 6 to 35VDC. This board also utilizes a Local Control Panel (LCP) N1700290X connected via a 96-pin connector to the front edge of the PCB. The LCP controls and monitors local non-vital circuits and devices through 16 inputs from the PCB and 16 outputs from the LCP to the PCB. Sixteen of the inputs are selectable by the front panel LCP pushbuttons. The 16 PCB outputs feed the LED indicators on the LCP.

Specifications for the non-vital I/O PCBs are as follows:

Non-Vital I/O Printed Circuit Boards				
US&S Part No.	**Input and Output Voltage Range**	**Externally Available Inputs**	**Externally Available Outputs**	**Current Rating On Outputs**
N170006101	6.0 to 30.0VDC	16	8	Outputs 25-30: 0.5A fuse Outputs 31, 32: 5.0A fuse*
N17061501	6.0 to 30.0VDC	32	32	Outputs 1-30: 0.25A (polyswitch-protected) Outputs 31, 32: 5.0A fuse*
N17062701	9.5 to 35VDC	0	32	Outputs 1-32: 0.5AMPS
N17002801	6.0 to 35VDC	16**	0	
N17063701	6.0 to 35VDC	32	0	
N17061801	9.8 to 16.2VDC	0	12 bi-polar outputs	250Ω min load

*Suitable for lighting lamp up to 25W.

**Other 16 inputs and outputs are used by LCP panel.

Figure 2-18 and Figure 2-7 show the generic interface wiring for both versions of the board.

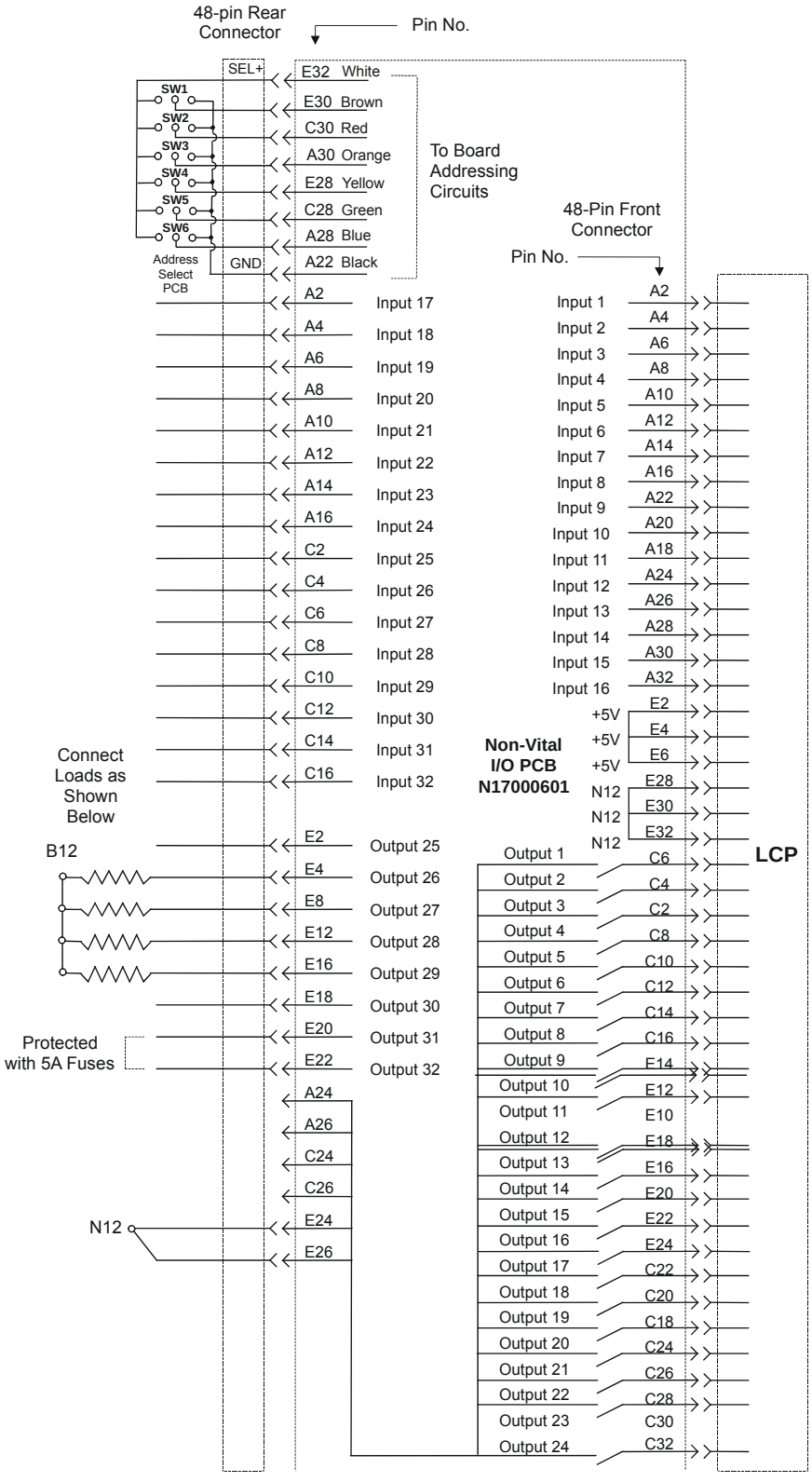


Figure 2-18 - Non-Vital I/O PCB, LCP Version - Basic Interface Wiring

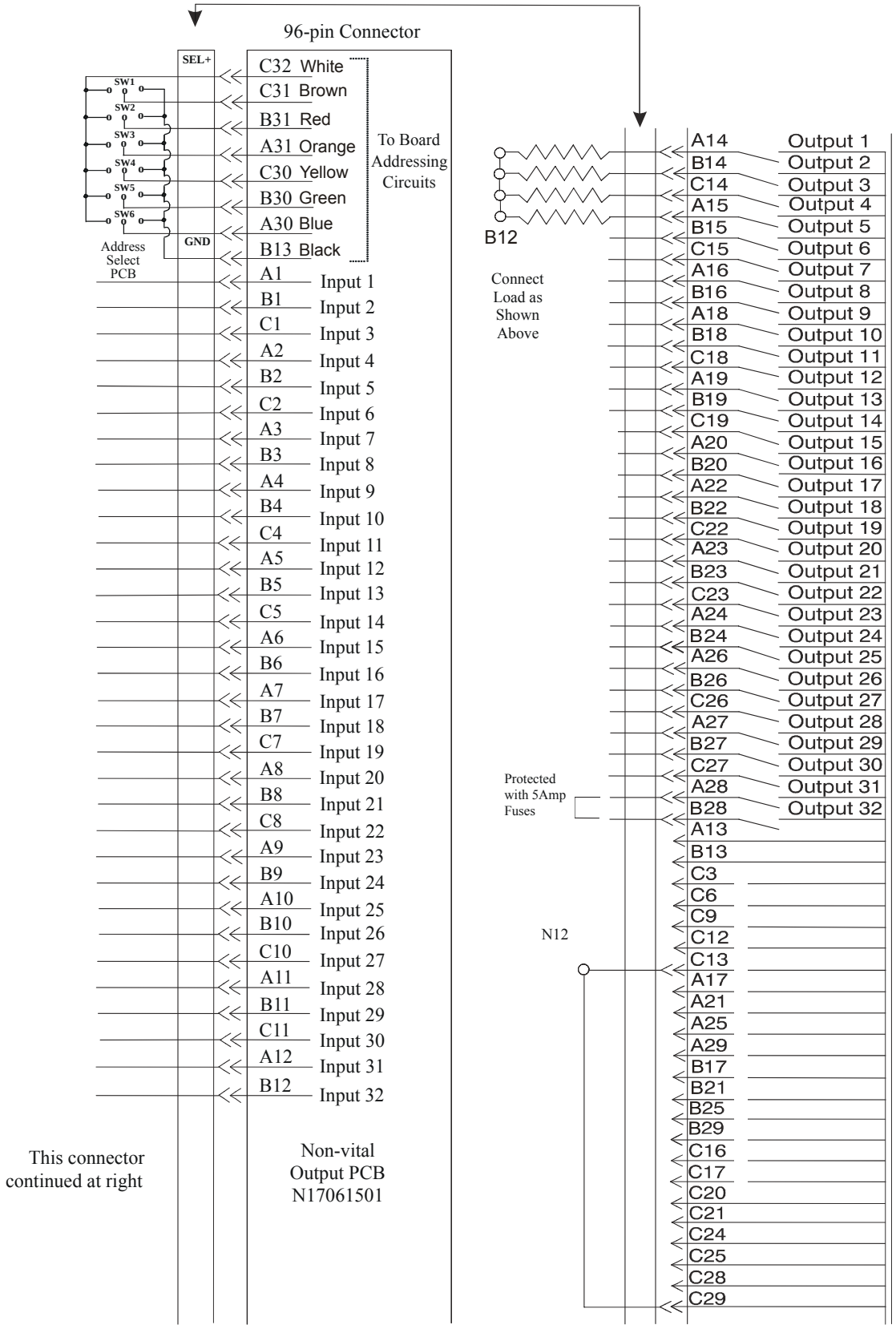


Figure 2-19 - Non-vital I/O PCB, 32/32 Version - Basic Interface Wiring

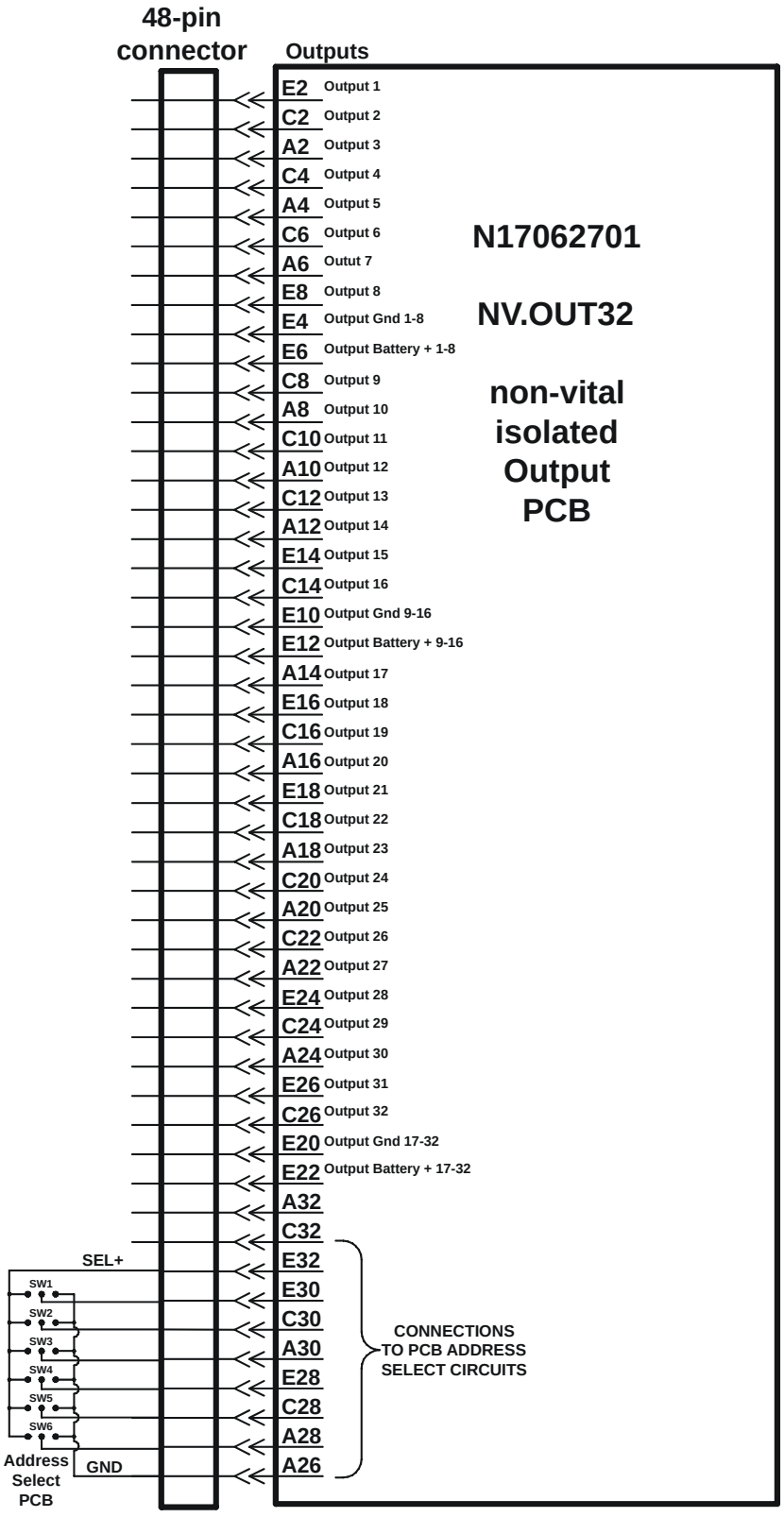


Figure 2-20 - Non-Vital, Isolated NV.OUT32 PCB – Basic Interface Wiring

NOTE

In Figure 2-18, , pins A13 – C29 are common connector pins. The number of required common returns depends on the number of outputs activated.

The general guidelines are: .

a. Outputs 31 and 32 are intended for high current; add a return for each used.

b. For each of the other outputs, add one return for every 8 outputs used.

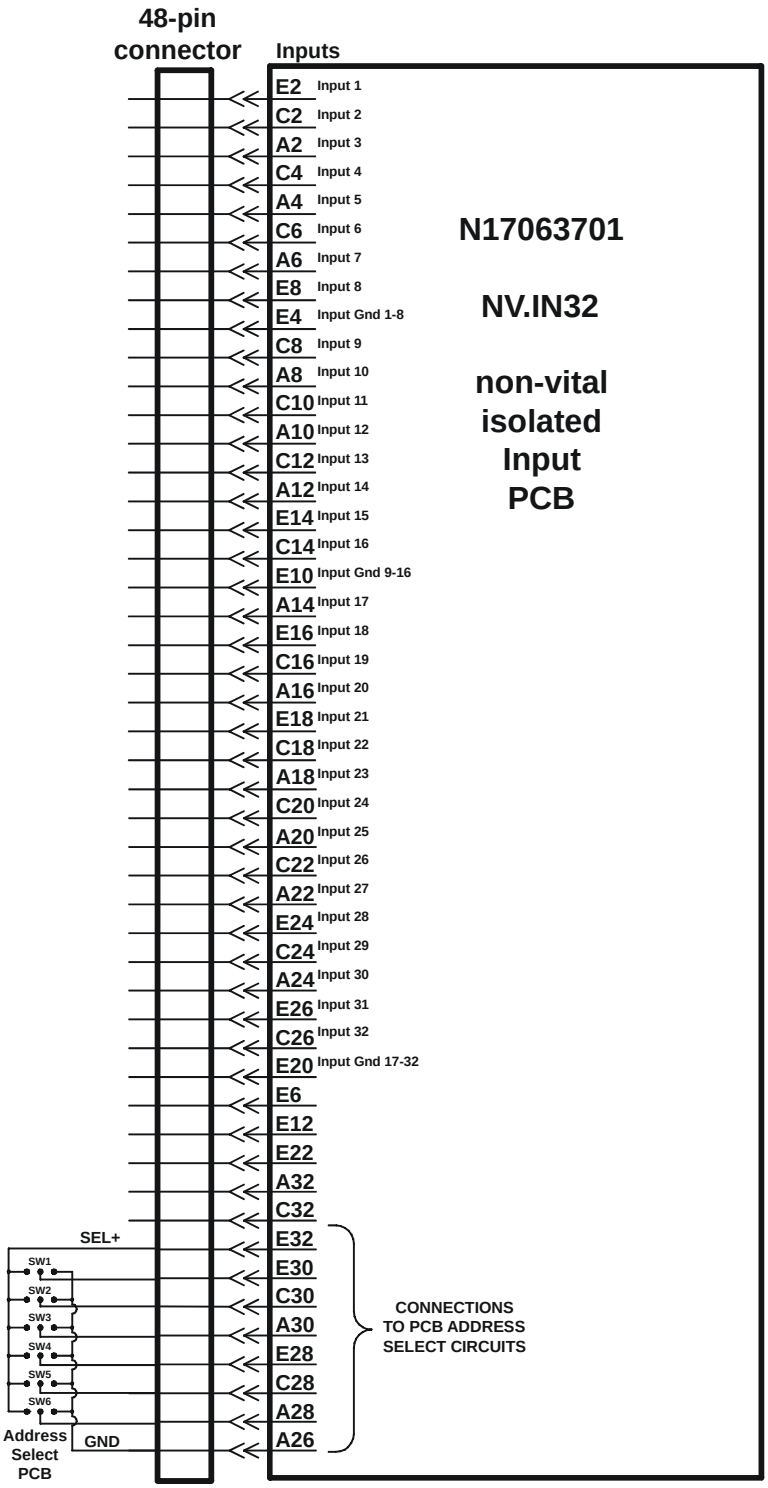


Figure 2-21 - Non-Vital, Isolated NV.IN32 PCB – Basic Interface Wiring

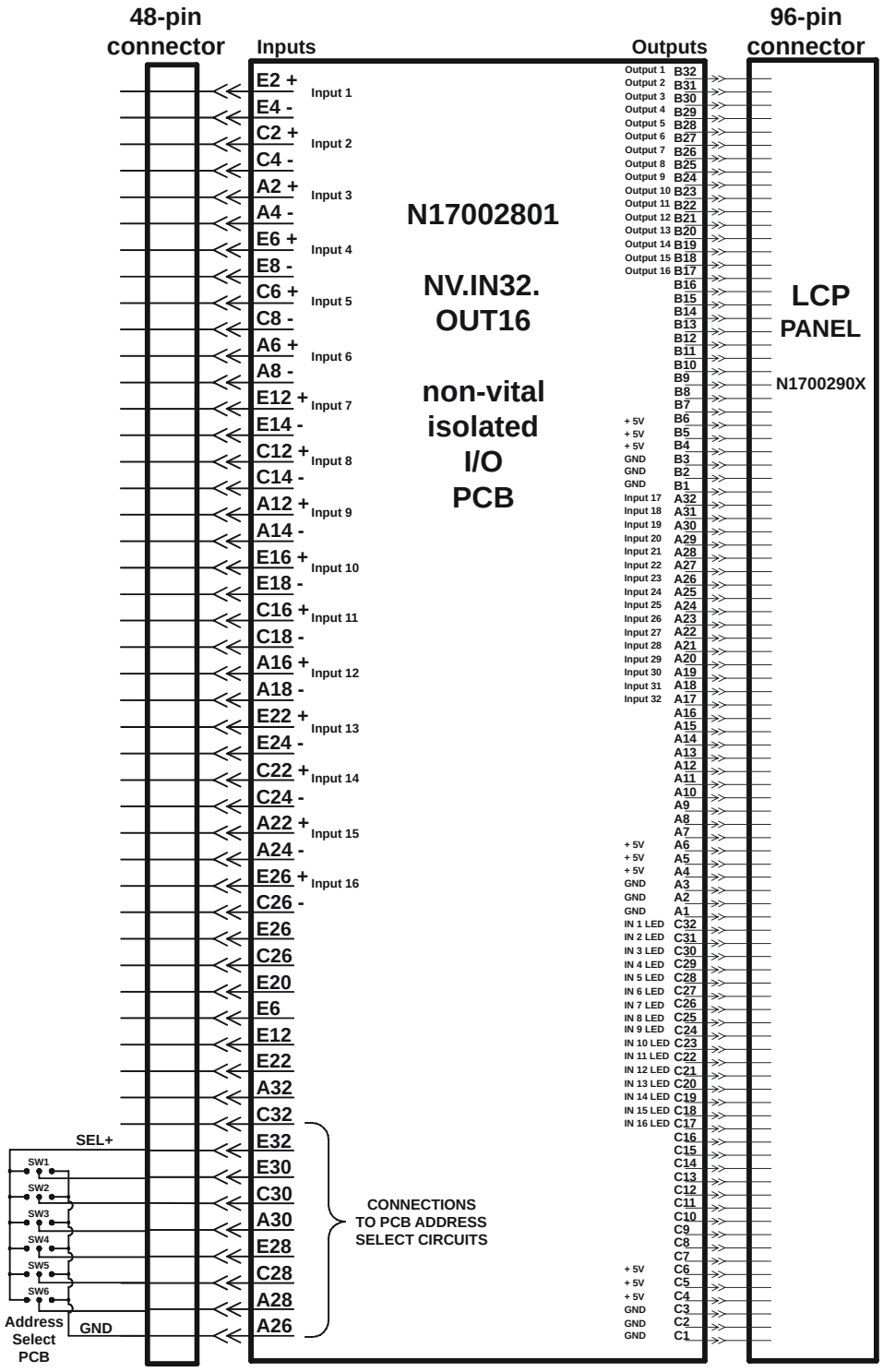


Figure 2-22 - Coded Track Circuit PCBs – Basic Interface Wiring

2.4.8 Code System Interface PCB

The code system interface PCB interfaces the Microlok II system to various types of non-vital code lines. Basic functions include conversion of the particular code line protocol to a format compatible with the Microlok II system (and vice-versa) and operation as a non-vital logic controller. This board is electrically identical to the

enhanced controller PCB used in the US&S GENISYS-2000 systems, and uses executive and application software that is identical to that used on the enhanced controller board. The GENISYS-2000 hardware is modified to make the board mechanically compatible with the Microlok II cardfile.

The basic interfacing rules for the code system interface PCB are as follows:

A. This board must be used when interfacing the Microlok II system to all types of non-vital code systems except GENISYS. Either the code system interface PCB or the Microlok II CPU board (refer to section 2.4.1) can be used for the GENISYS interface.

B. When interfacing the Microlok II system to a DC code line, an external GENISYS unit must be included to provide the electrical interface to the code line. The Microlok II system does not include an equivalent to the GENISYS code line interface PCB.

C. Microlok II serial link isolator units should be included in the interface to the code line to protect circuits on both ends of the interface from potentially damaging voltage transients. These units are different from the GENISYS surge suppression/serial interface panels. The latter cannot be used as a substitute. Serial link isolator unit specifications are as follows:

Unit Type	US&S Part No.	Unit Specifications
Type A serial link isolator unit	N17002201	Interfaces the code system PCB (cardfile) to a Glenaire modem or MCP in ARES and serial line carrier code systems. Input Power: 9.5 to 16.2 Vdc Modem Power Outputs: +12 Vdc and –12 Vdc
Type B serial link isolator unit	(Contact US&S)	Interfaces the code system interface board to ATCS systems. Signal compatibility: Balanced RS-485 and unbalanced RS-423 ports

Figure 2-20 shows the standard interface wiring pin-outs for the code system interface PCB.

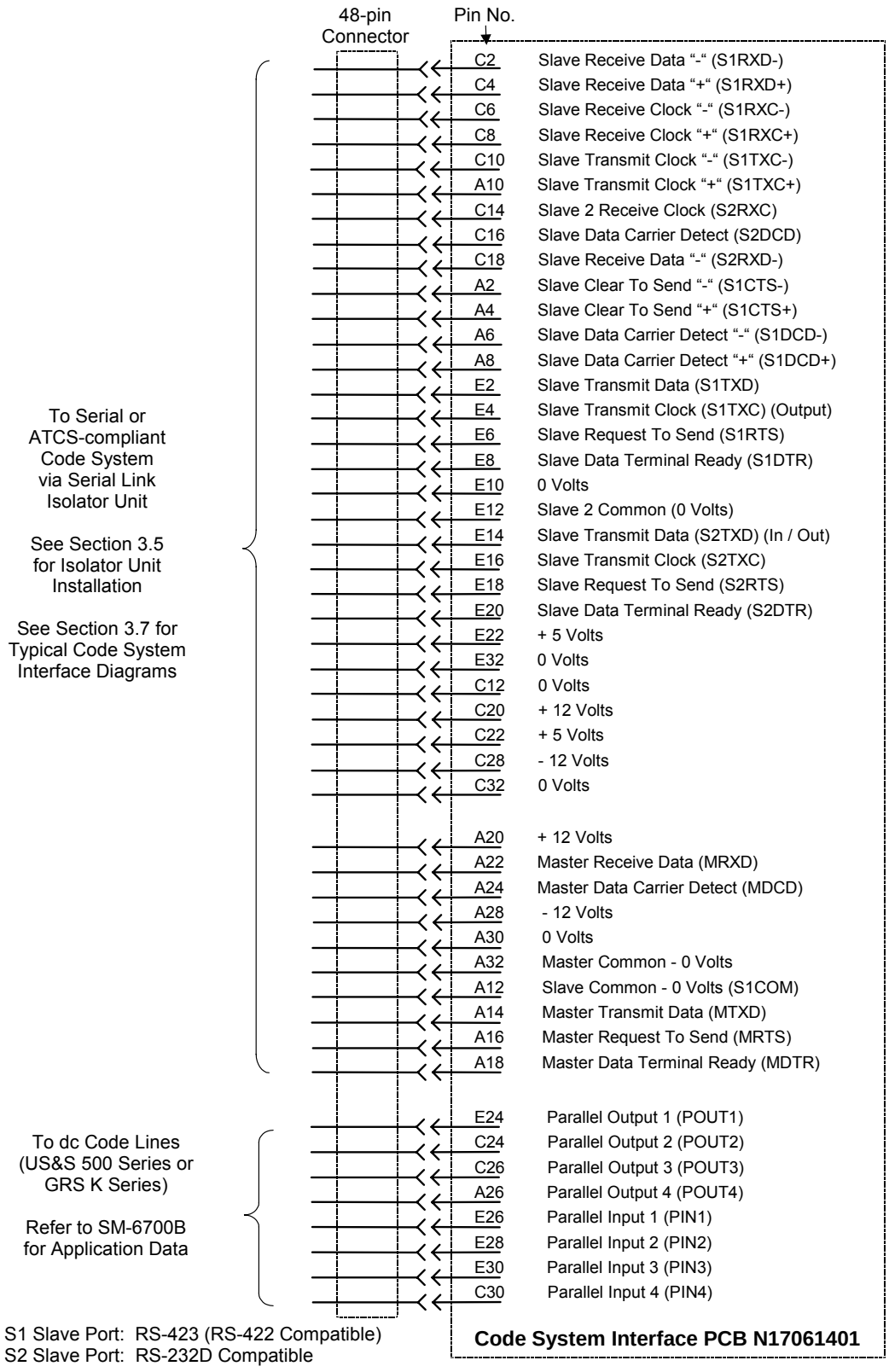


Figure 2-23 - Code System Interface PCB - Basic Interface Wiring

2.4.9 Coded Track Circuit PCBs

The coded track circuit PCBs interface the Microlok II system to the mainline coded track circuits (with and without cab signals). The specifications for these boards are as follows:

US&S Part No.	Track Circuit Application	Track Circuit Operating Power
N451910-0701	General non-cab and 100 Hz cab signal	9.8 to 16.2 Vdc
N451910-7601	Required for 40 Hz cab signal	9.8 to 16.2 Vdc
N451910-7602	Required for 50 Hz cab signal	9.8 to 16.2 Vdc
N451910-7603	Required for 60 Hz cab signal	9.8 to 16.2 Vdc

The Microlok II system can accommodate up to four coded track circuit printed circuit boards in the same cardfile. Refer to Section 3.1.3 for coded track interface panel wiring to the rails.

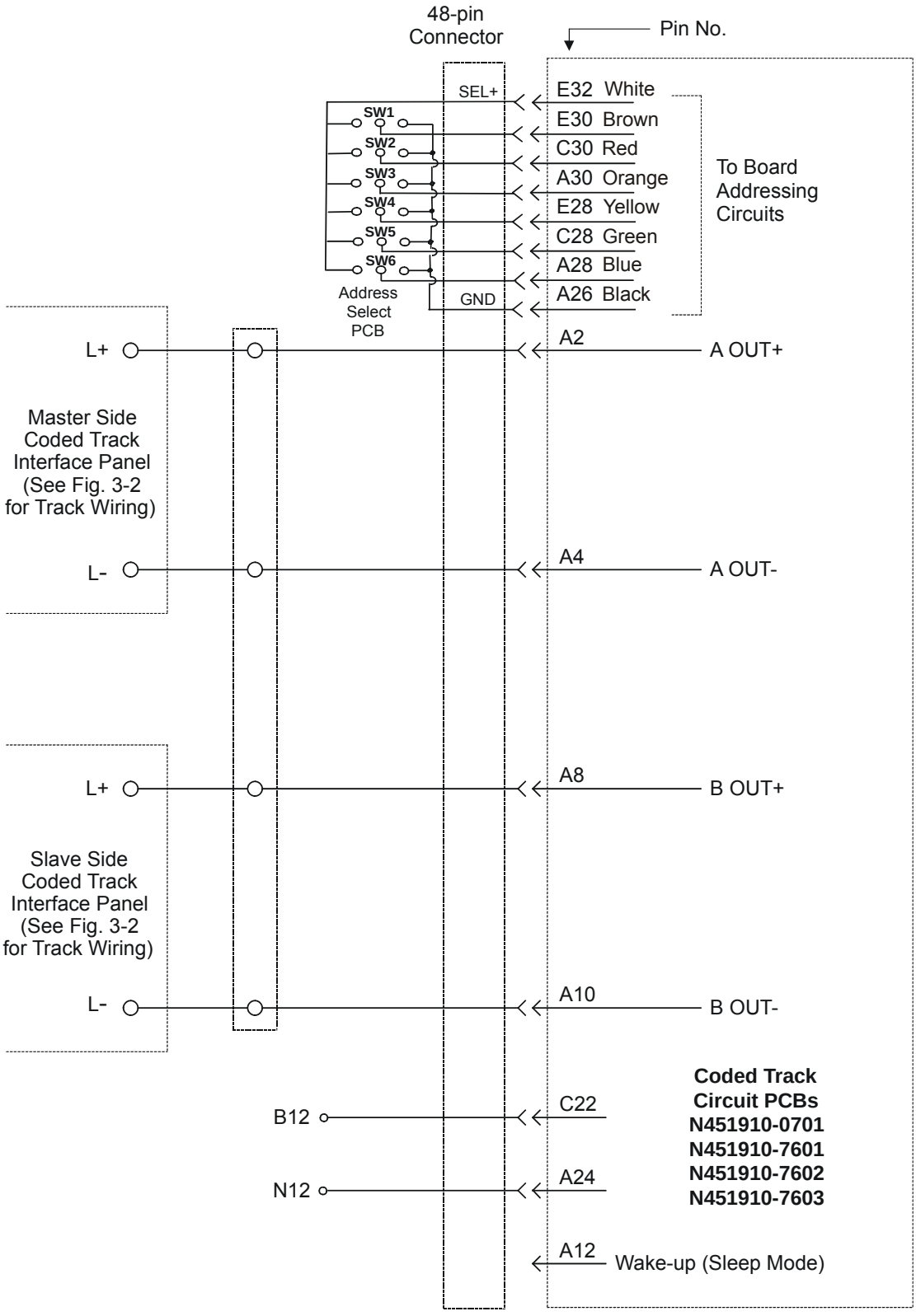


Figure 2-24 - Coded Track Circuit PCBs - Basic Interface Wiring

2.4.10 OS Track Circuit PCB

The OS track circuit PCB interfaces the Microlok II system to the OS track circuit in interlocking applications requiring one OS transmitter and two OS receivers (end-of-siding). Specifications for this board are as follows:

Transmitter/Receiver Frequency	Receiver Output Voltage	Track Circuit Length	Track Lead Resistance
400 Hz	12 Vdc to 20 Vdc 15 Vdc (nominal)	1000 ft. @ 5Ω/1000 ft. Ballast	0.5Ω (max.)

It is not necessary to connect both receivers if it is not required by the application. In many cases the transmitter is connected at the heel block and the two receivers provide independent train detection on the interlocking through and turnout tracks. Transmitter output power is insufficient to drive a relay.

Figure 2-22 shows the basic wiring of the OS track circuit PCB. Outputs OUT1 and OUT2 must be wired to one of the inputs on the vital input PCB to provide the train detection input to the CPU board. OUT1 and OUT2 should each be wired to a "+" input on the vital input PCB, with N12 connected to each negative input. See Figure 2-11 for vital input PCB wiring pin-outs.

Separate B12/N12 and +5V connections are also required to power the OS track circuit PCB transmitters and board circuitry. Also note the installation of primary surge protection on the wiring.

CAUTION

Lightning arrestors (shown in Figure 2-20) must be used in all Microlok II OS track installations, otherwise the system could be damaged from lightning surges or operate improperly as the result of transient signals.

Refer to service manual SM-6800C for procedures to adjust the OS track circuit PCB power output for various track circuit lengths.

CAUTION

The OS track circuit provides a transmitter and 2 receivers. at an "end of siding" type location this puts either a transmitter or receiver at each end of the OS circuit. All OS track circuits operate at the same frequency. If multiple OS circuits are used at a double-crossover type location, a defective joint potentially could cause a falsely energized track output.

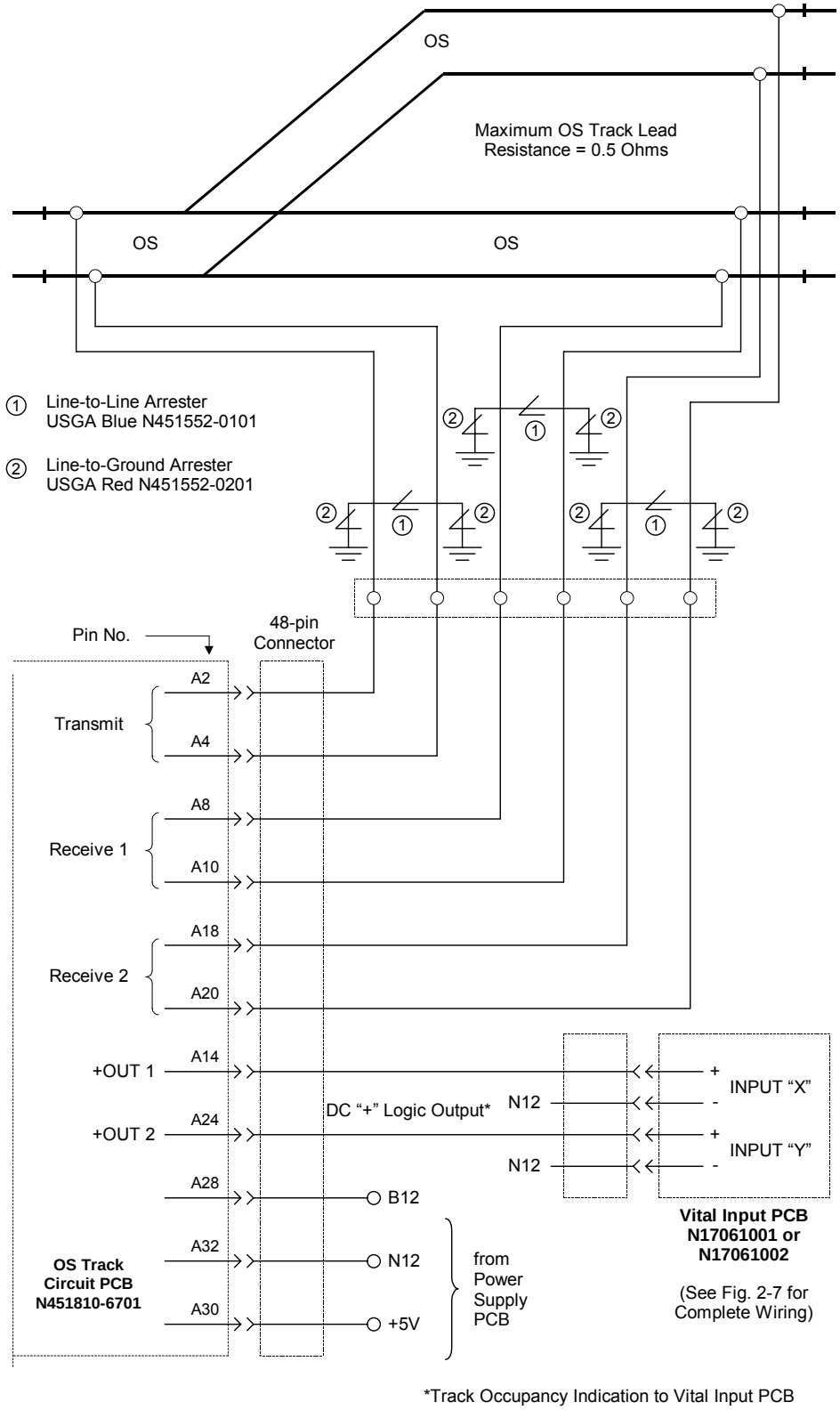


Figure 2-25 - OS Track Circuit PCB - Basic Interface Wiring

2.4.11 Cab Signal Coder PCBs and Cab Amplifier PCBs

The coder output and cab amplifier printed circuit boards are used to generate cab signal carrier frequencies and code rates, and output these signals to the rails through cab signal interface panels. Each Microlok II cab signal application requires one coder output board and one or two cab amplifier boards installed in the following combinations:

Amplifier PCB	Coder PCB(s)	Application
N451910-6401	N451910-5801	For 60 or 100 Hz carrier, 75/120/180 code rates
N451910-6901	N451910-5801, N451910-7001	For 40 or 50 Hz carrier, 50/75/120/180 code rates

The -5801 coder output PCB (75/120/180 CPM) is controlled by the Microlok II CPU board and requires an Address Select PCB with six two-position jumpers in the connector housing to set its cardfile bus address. When the additional 50 CPM code rate is required, it is produced by the -7001 board, which feeds the rate to the cab amplifier board through the -5801 coder output board. (A jumper must be set on the -5801 board for this configuration; refer to service manual SM-6800C). The -7001 coder output PCB does not communicate over the Microlok II cardfile bus and is only connected to the -5801 coder output board through the upper wiring connector.

Code rates produced by the single -5801 board or combination -5801/-7001 boards are delivered to the cab amplifier PCB through the upper wiring connectors, not the cardfile bus. The cab amplifier PCB also operates separately from the CPU board (no cardfile bus communications). The cab amplifier PCB output is wired to the cab signal interface panel for final connection to the rails.

Figure 2-23 shows the standard wiring options for the four Microlok II cab signal boards. Cab amplifier output connections to cab panel transformer primary are doubled to carry the extra current load. The East and West direction relays on the panel are energized through three additional wire connections. A jumper is required between pin-outs E14 and E16 on coder output PCB. This jumper provides the east/west direction input from output #4 on the coder output PCB.

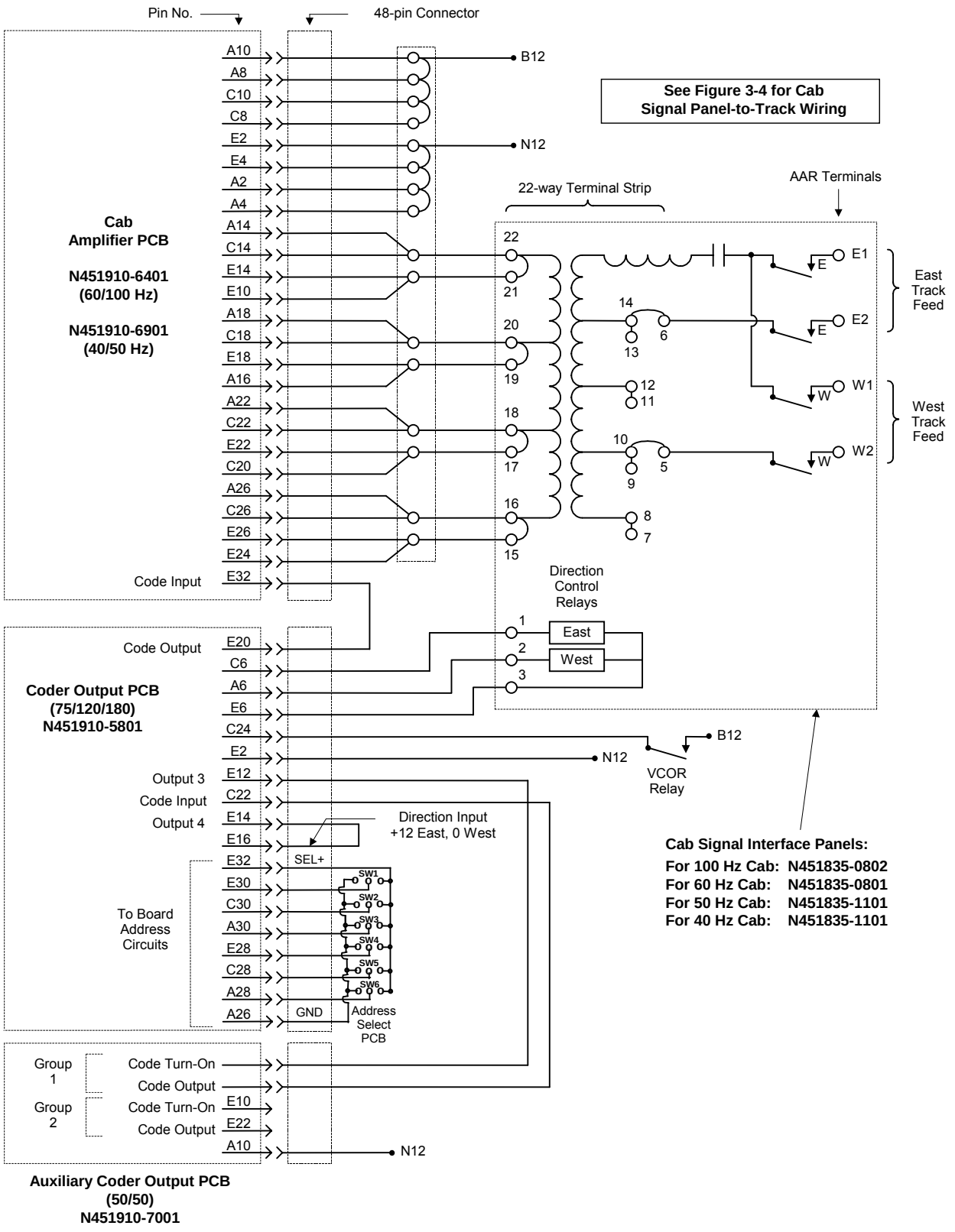


Figure 2-26 - Coder Output and Cab Amplifier PCBs - Basic Interface Wiring

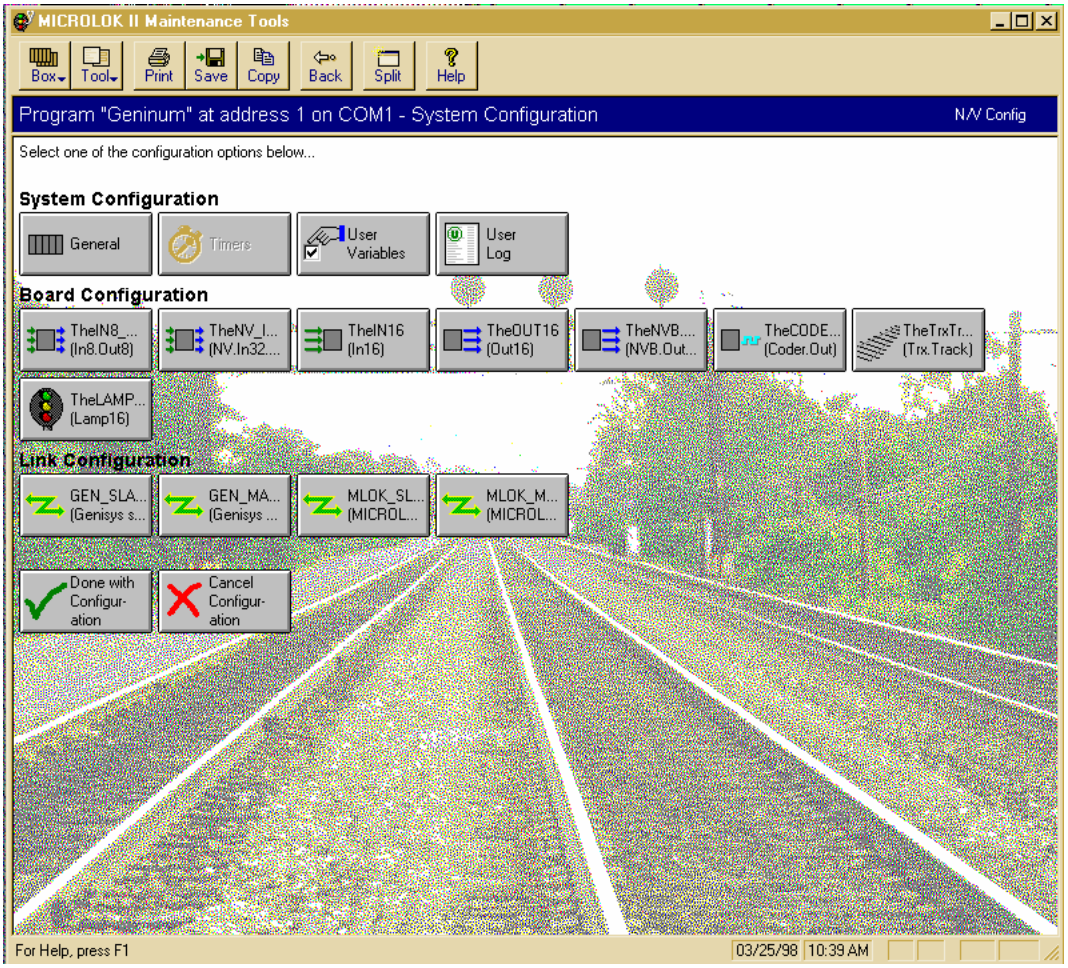
2.4.12 Address Select Jumper Settings

On the PCBs that use them, the address select jumpers are used for board addressing. The jumper settings are automatically determined by the compiler when the application program is written. This information is clearly defined and available to the user in the list file (.mll), which is one product of compiling an application text file (.ml2). If this file is unavailable, the user can determine the jumper settings by following the instructions below. By far the best way to determine the jumper settings, however, is to use the list file.

The jumper settings for each board are determined by the order in which the boards are defined in the application. The jumper settings *do not* depend on the order the boards happen to appear in the cardfile. If the application program and list file are both unavailable, then the order can also be found by looking at the configuration menu in the Microlok II Maintenance Tool. (See Section 6.2 in the 6800C manual.) The buttons for the board listing in the configuration window are in the same order, from left to right, as they are in the application.

There are two types of boards: 8-bit and 16-bit. Lamp boards are 16-bit boards, and all other boards are 8-bit boards. So, for this purpose, there are lamp boards and non-lamp boards. The following table shows how to set the jumpers for each type of board (lamp and non-lamp). Each type must be counted separately to determine the order and, therefore, the proper jumper setting.

Note: Each jumper may be set to either a "0" or "1" position.



Board Order	Non-Lamp Board Jumpers						Lamp Board Jumpers					
	1	*2*	*3*	*4*	*5*	*6*	*1*	*2*	*3*	*4*	*5*	*6*
1	0	0	0	0	0	1	0	0	0	0	0	0
2	0	1	0	0	0	1	0	1	0	0	0	0
3	0	0	1	0	0	1	0	0	1	0	0	0
4	0	1	1	0	0	1	0	1	1	0	0	0
5	0	0	0	1	0	1	0	0	0	1	0	0
6	0	1	0	1	0	1	0	1	0	1	0	0
7	0	0	1	1	0	1	0	0	1	1	0	0
8	0	1	1	1	0	1	0	1	1	1	0	0
9	0	0	0	0	1	1	0	0	0	0	1	0
10	0	1	0	0	1	1	0	1	0	0	1	0
11	0	0	1	0	1	1	0	0	1	0	1	0
12	0	1	1	0	1	1	0	1	1	0	1	0
13	0	0	0	1	1	1	0	0	0	1	1	0
14	0	1	0	1	1	1	0	1	0	1	1	0
15	0	0	1	1	1	1	0	0	1	1	1	0
16	0	1	1	1	1	1	0	1	1	1	1	0

For example, for the first non-lamp board, jumpers 1 through 5 are set to "0", while jumper 6 is set to "1". The second non-lamp board will have jumpers 2 and 6 set to "1" with the rest at "0", and so on. The first lamp board listed will have all jumpers set to "0". The fifth lamp board listed will have jumper 4 set to "1", and the rest set to "0".

As an example, the following list was formed using the table above:

Non-Lamp Boards	Settings:					
	1	*2*	*3*	*4*	*5*	*6*
1. TheIN8_OUT8	0	0	0	0	0	1
2. TheNV_IN32_OUT32	0	1	0	0	0	1
3. TheIN16	0	0	1	0	0	1
4. TheOUT16	0	1	1	0	0	1
5. TheNVB.OUT12	0	0	0	1	0	1
6. TheCODEROUT	0	1	0	1	0	1
7. TheTrxTrack	0	0	1	1	0	1

Lamp Boards	Settings:					
	1	*2*	*3*	*4*	*5*	*6*
TheLAMP16	0	0	0	0	0	0

It is assumed that the application software defines the boards as they are shown above, i.e., Board #1 is an NV.IN32.OUT16 board, etc. It is the order in which they are defined in the application program that determines the board number, *not* the relative position in the cardfile.

2.4.13 AC Lamp Drive

With some additional hardware, Microlok II can provide AC lighting of nominal 12V signal lamps. The required hardware includes:

12V Vital Input Board

12V Vital Output Board

AC Lamp Driver Module

AC Lamp Hot Filament Checker

Part numbers and wiring details are contained in US&S service manual SM-8525.

3 Installing Microlok II System Peripheral Devices

3.1 INSTALLING CODED TRACK AND CAB SIGNAL INTERFACE PANELS

3.1.1 Coded Track and Cab Signal Panel Selection

Four coded track interface panels and three cab signal interface panels are available for use in Microlok II systems. Make certain to use the unit appropriate to the application:

Table 3-1 - Coded Track and Cab Signal Interface Panel Applications

Description	Application	US&S Part No.
Coded track interface panel with 10 mH inductor	General applications without cab signal	N451835-0101
Coded track interface panel with 15 mH inductors	Non-cab territories with 86 Hz crossing predictors.	N451835-0102
Coded track interface panel with 20 mH inductors	Cab signal territories with 100 Hz carriers. Use with cab signal interface panel N451835-0802.	N451835-0103
Coded track interface panel with 40 mH inductors	Cab signal territories with 60 Hz carriers. Use with cab signal interface panels N451835-0801 and N451835-1101.	N451835-0104
Cab signal interface panel	Cab signal territories with 60 Hz carriers. Use with coded track interface panel N451835-0104.	N451835-0801
Cab signal interface panel	Cab signal territories with 100 Hz carriers. Use with coded track interface panel N451835-0103.	N451835-0802
Cab signal interface panel	Cab signal territories with 40 Hz carriers. Use with coded track interface panel N451835-0104.	N451835-1101

3.1.2 Mounting the Panels

Refer to Figure-3-1. When two coded track interface panels are being mounted in the same location, they must be separated by at least 12 inches to minimize magnetic interference between them. The optional quick shunt module should be mounted close to the coded track interface panel.

In Microlok II applications where the system is also used to generate cab signals, the cab signal interface panel should be mounted close to the cardfile. This panel can be mounted on a wall or shelf, and can be installed in a standard 19-inch rack. For this application, the associated track interface panels should be mounted nearby because the track leads are shared with the cab signal interface panel.

The temperature limits on these panels are the same as those for the cardfile. See section 3.11 of service manual SM-6800A for environmental limitations on the Microlok II system.

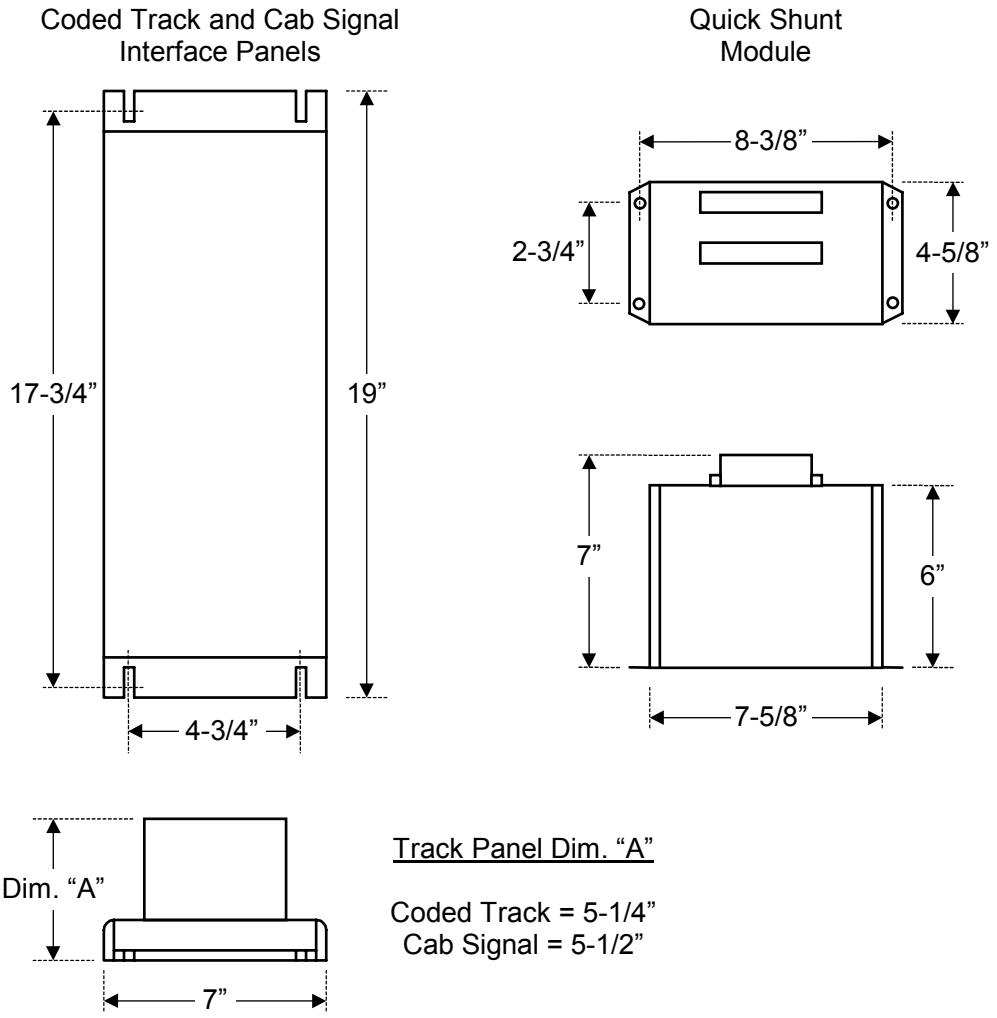


Figure-3-1 - Mounting Dimensions for Coded Track/Cab Signal Interface Panels and Quick Shunt Module

3.1.3 Coded Track Interface Panel Wiring, Grounding, and Surge Protection

3.1.3.1 Track Leads and Surge Protection

Refer to Figure 3-2. Per standard railroad practice, leads from the coded track interface panel should be equipped with line-to-line and line-to-ground lightning arresters. Special track surge protection or common mode filtering is not required on these leads.

CAUTION

The track leads to the Microlok II coded track interface panel must be equipped with US&S-specified lightning arresters. Damage to the Microlok II equipment may result from lightning surges if the arresters are not properly installed.

3.1.3.2 Grounding

Chassis grounds are not required for the coded track interface panels.

3.1.3.3 Track Polarity

Figure 3-2 shows how to connect the coded track interface panels to the rails so that proper polarity is established between adjacent track circuit blocks. Note in the figure that the polarity of the panel terminals (**L+, L-, T+, T-**) is reversed from one end of the panel to the other. To confirm the proper track circuit polarity, use the procedure in section 7 of service manual SM-6800C. Section 7 also provides procedures for all coded track circuit adjustments that must be made during system startup.

CAUTION

Track polarity between adjacent tracks must be reversed to prevent a Microlok II system from communicating through a faulty insulated joint connection.

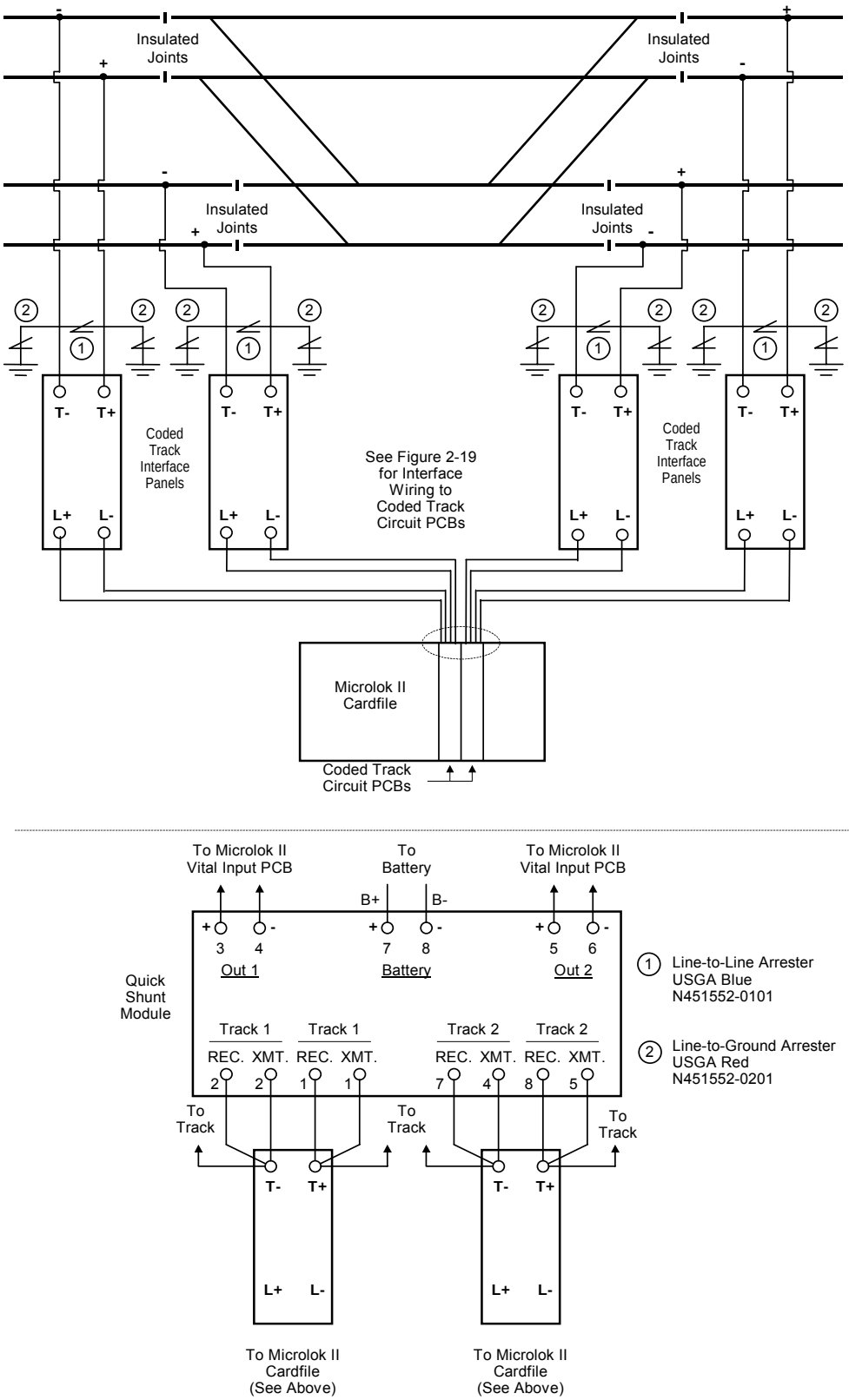


Figure 3-2 - Coded Track Interface Panels - Basic Track Wiring

3.1.3.4 Installing a Termination Capacitor PCB

When using coded track interface panels N451835-0103 or -0104, a special termination capacitor PCB (part number N451923-2501) should be mounted on the two panel terminals wired to the Microlok II cardfile. This PCB contains two back-to-back electrolytic capacitors and is designed to prevent the high power output of the Microlok II cab transmitter from interfering with the coded track messages. This board also filters 60 Hz induction interference from power lines. For the 100 Hz cab signal frequency, no other filtering is required. For lower cab signal frequencies, special track printed circuit boards are required (contact US&S). Figure 3-3 shows the termination capacitor PCB installation.

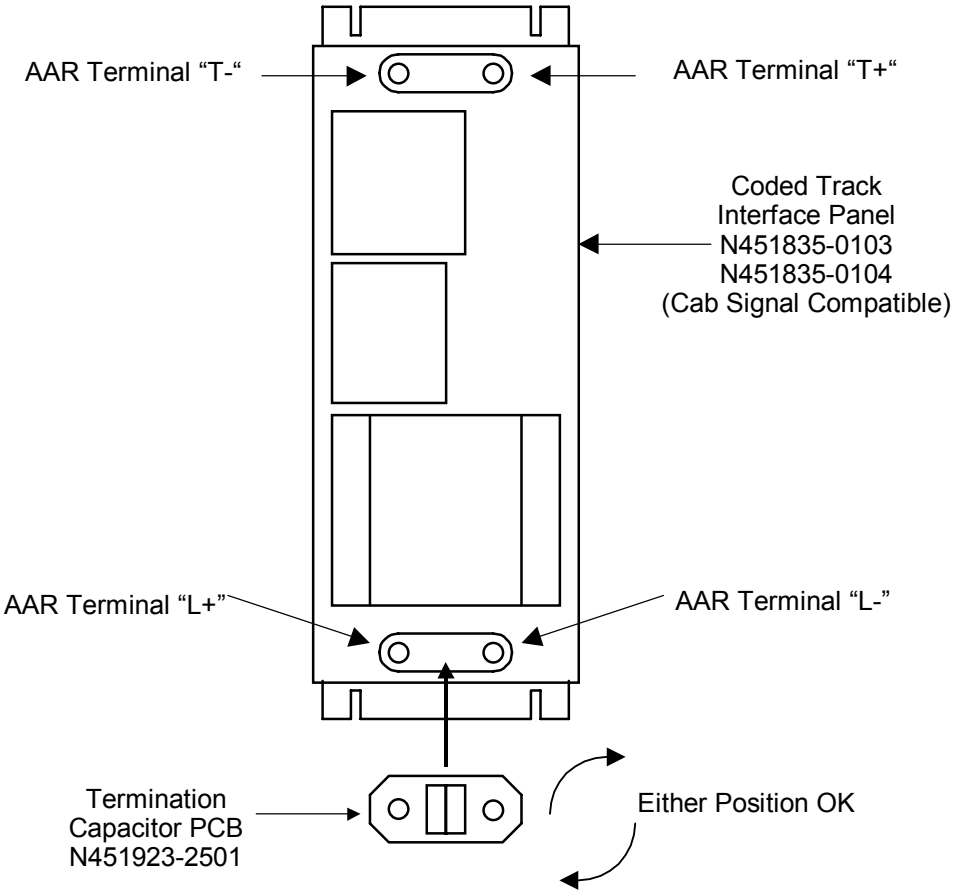


Figure 3-3 - Termination Capacitor PCB Installation on Coded Track Interface Panels

3.1.4 Quick Shunt Module Application and Installation

The optional quick shunt module (N451052-4601) is used in applications where an improved shunt detection time is required. The quick shunt module reduces the detection time to approximately 100 milliseconds and contains circuitry for independent train detection on both sides of the insulated joint. Two 8-way screw-lock connectors are provided for external wiring.

The two independent receivers on this device should be connected to the coded track interface panels as shown in Figure 3-2. With this configuration, true shunt mode operation is attained without the need for separate track termination leads. The detection zone is limited to approximately 75 feet. For greater lengths, the transmitted and receiver track terminations must be separated.

3.1.5 Cab Signal Interface Panel Wiring, Grounding and Surge Protection

3.1.5.1 Single-Cab Signal Configuration Wiring

3.1.1.5.1 Track Leads

For Microlok II installations that control one cab signal interface, track leads from the cab signal interface panel are connected to the track terminals of the coded track interface panels, as shown in Figure 3-4. No special line filtering or surge suppression is required on these terminals.

3.1.1.5.2 Cab Interface Panel-to-Cardfile Wiring

Refer to section 2.4.11 and Figure 2-21 for wiring of the cab interface panel to the Microlok II cardfile.

3.1.5.2 Dual-Cab Signal Configuration Wiring

Consult US&S for Microlok II cab signal applications where the system is generating separate cab signal codes to different interlocking tracks (main and siding tracks).

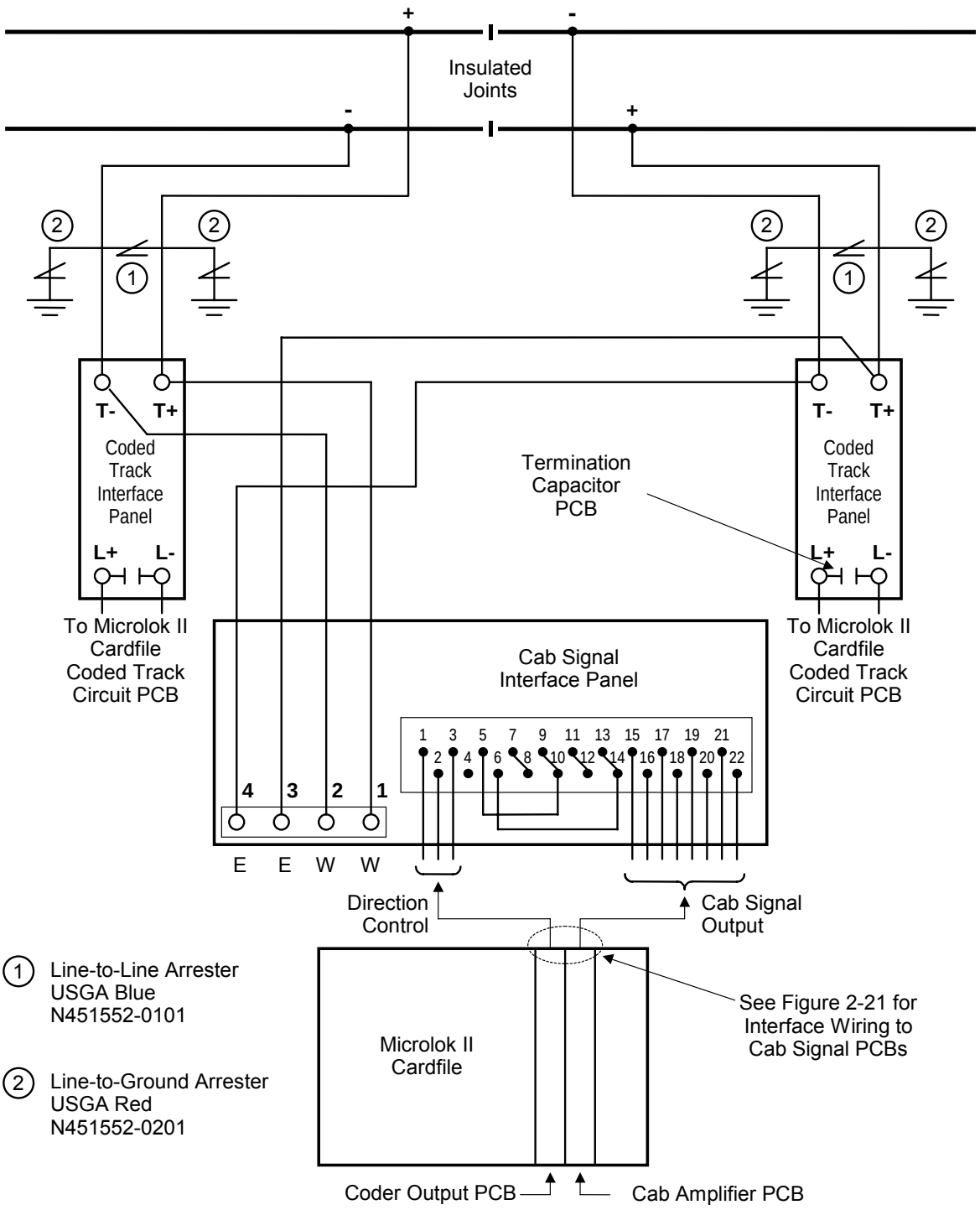


Figure 3-4 - Cab Signal Interface Panel Basic Wiring - Single Cab Configuration

3.2 VITAL CUT-OFF RELAY (VCOR) INSTALLATION AND WIRING

The VCOR controls power to all Microlok II vital outputs under the control of the Microlok II CPU board. Power for the relay coil is supplied by the cardfile power supply PCB. A US&S PN-150B relay (part number N322500-701) is used for all VCOR installations. The components required to rack-mount the relay are listed below.

Item	US&S Part No.
PN-150B relay	N322500-701
relay mounting base	N451376-0302
contact springs for #14 - #16 wire	M451142-2702
rack mounting bars (2 required)	M381333
mounting bar clamps (4 required)	M381298

Double battery and return paths are wired to the relay to eliminate voltage drops. Use #14 wire for connections between the cardfile and the relay. Also, use parallel contacts of the VCOR where possible. Figure 3-5 shows the wiring between the Microlok II cardfile and the VCOR for the various types of vital output boards.

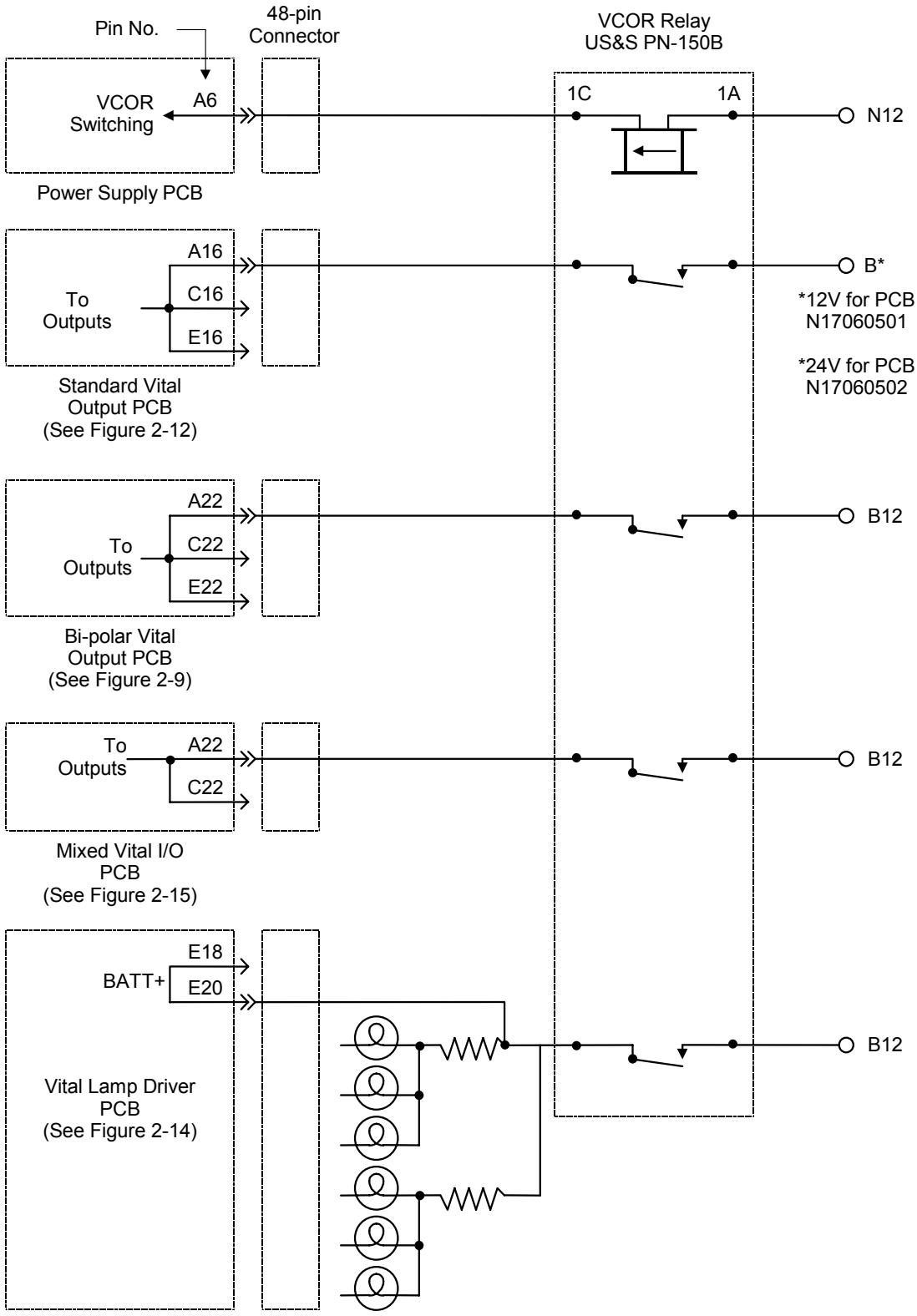


Figure 3-5 - VCOR Relay Wiring

3.3 POWER-OFF RELAY INSTALLATION AND WIRING

The power-off relay is provided for Microlok II installations that require the detection of commercial power failure. A loss of commercial power drops the relay and closes a normally open relay contact. The contact closure makes an input circuit to the non-vital I/O PCB in the Microlok II cardfile. (See Figure 3-6.)

The power-off relay is mounted on a plug-in base and secured with a spring clip. This base is designed for attachment to a standard equipment rack DIN rail, or can be secured to a flat surface using a screw hole in the base under the relay. The part numbers are as follows:

Item	US&S Part No.
relay	J726153-0283
base	J581782-0026
spring clip	J680167-0009

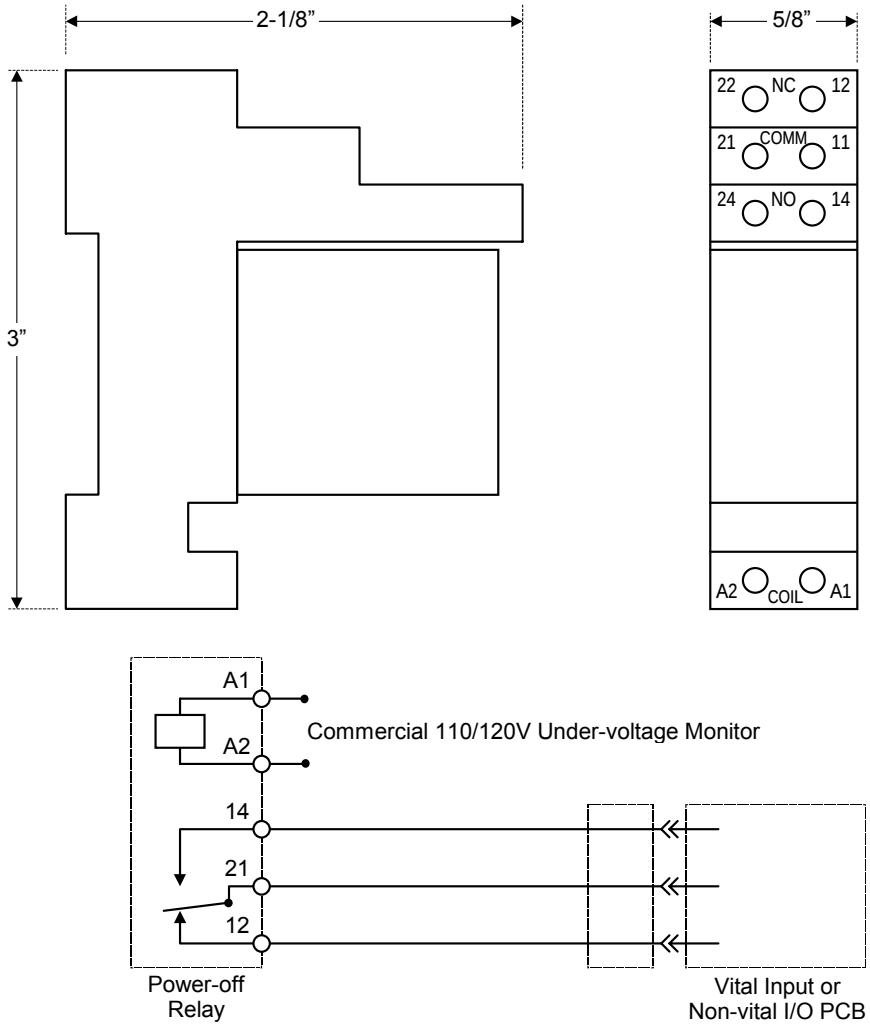


Figure 3-6 - Power-off Relay Design and Interface Wiring

3.4 ISOLATION MODULE INSTALLATION AND WIRING

The isolation module is used for Microlok II applications that require the equivalent of a double-break output circuit. When connected to an output of the standard vital output PCB or mixed vital I/O PCB, the isolation module creates an isolated output suitable for connection to line or relay circuits in a different house or case. The module contains two independent circuits that can be interconnected to create a single, isolated bi-polar output when required by the application. Figure 3-7 shows the module mechanical design. The module is typically rack mounted on a DIN rail, but can also be wall mounted.

Three versions of the isolation module are available. All three models are controlled by a nominal 12V vital output. Module N17001101 (12V output) provides an output slightly greater than the battery source voltage. Current is limited to 0.4A with voltage fold-back occurring at that point. Module N17001102 (50V output) also provides an output proportional to the battery source voltage, with fold-back occurring at approximately 0.13A. Module N17001103 (24V output) also provides an output proportional to the battery source voltage, with fold-back occurring at approximately 0.4A.

Outputs are short circuit protected and will withstand a single cross to B12 or N12 without damage. Outputs will also withstand 2000V RMS to battery or to earth ground.

Refer to Figure 3-8. Isolation module terminals **B12** and **N12** designate battery positive and battery negative, respectively. For two independent outputs, with terminal **IN1** activated by a nominal +12 voltage relative to N12, output 1 is activated with the indicated polarity (**OUT1+** or **OUT1-**). Output 2 is similarly activated.

For bi-polar operation, make the following connections:

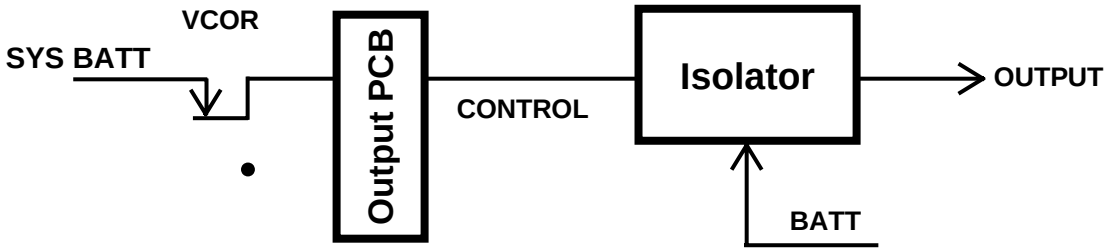
Jumper between **J1A** and **J2B**

Jumper between **J2A** and **J1B**

Load between **BP1** and **BP2**

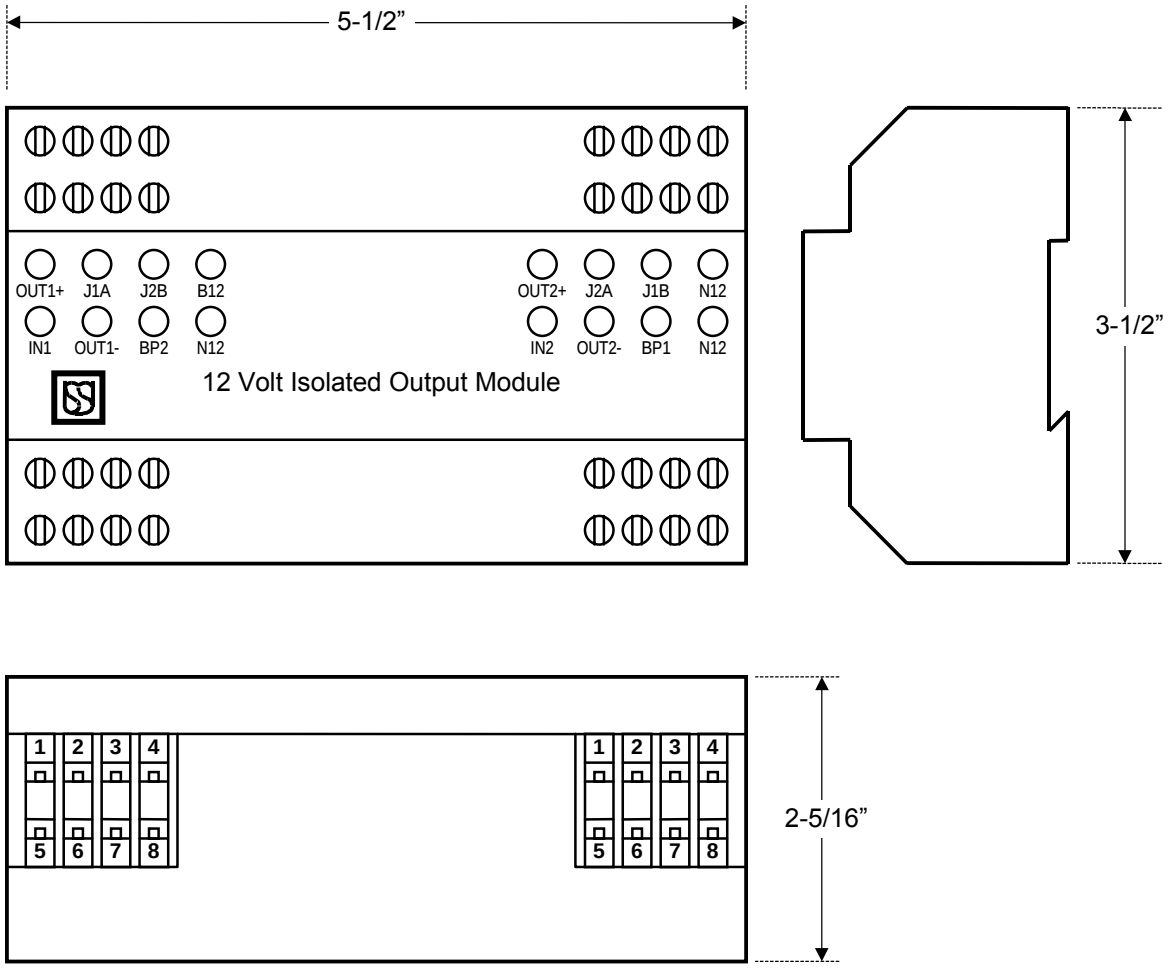
Polarity will establish **BP1** positive relative to **BP2** with **IN1** activated. Polarity is reversed when **IN2** is activated. For bi-polar operation, both inputs should never be activated simultaneously.

The drawing and table below summarize the operations:



PART NUMBER	SYS BATT	BATT	OUTPUT VOLTAGE
1101	12 Vdc	9.6 Vdc	10 Vdc
1101	12 Vdc	16.2 Vdc	18 Vdc
1102	12 Vdc	14 Vdc	40 Vdc
1102	12 Vdc	18 Vdc	55 Vdc
1103	12 Vdc	18 Vdc	18.2 Vdc
1103	12 Vdc	35 Vdc	36.8 Vdc

NOTE: 1102 assumes a 500 Ω or greater load.
1103 assumes a 1000 Ω or greater load.



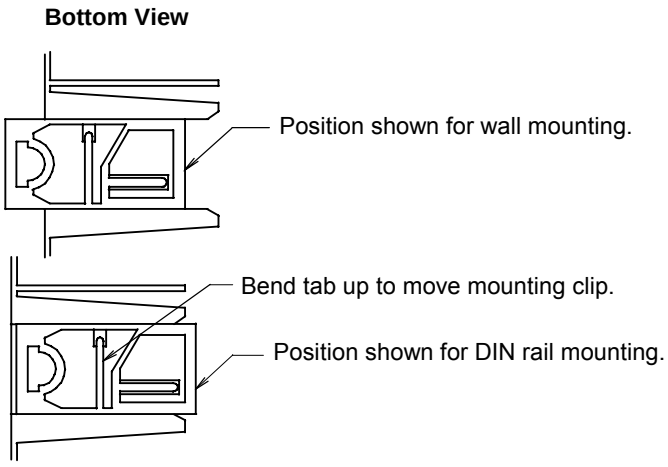
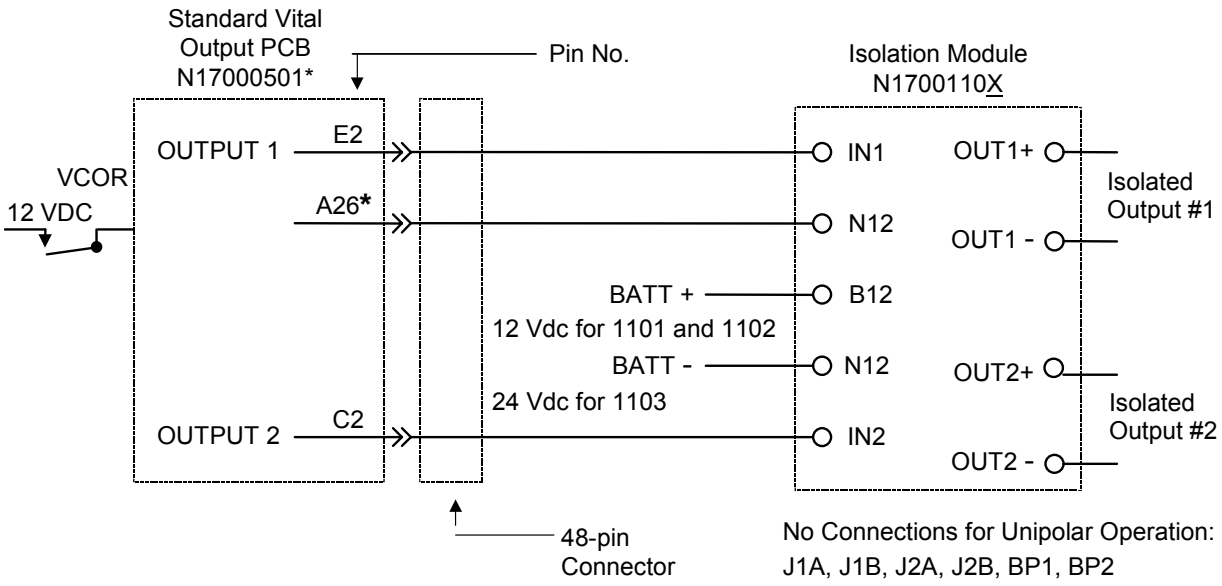
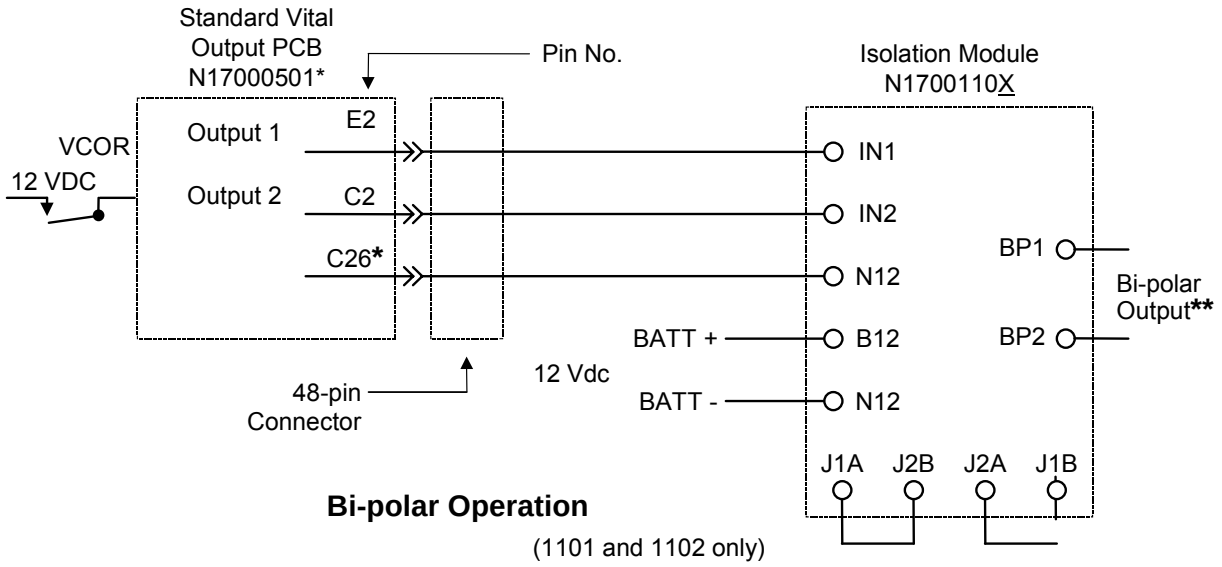


Figure 3-7 - Isolation Module Mechanical Design



Unipolar Operation



Bi-polar Operation

(1101 and 1102 only)

***Other Available Common (N12) Connections:**
E26, A24, C24, E24, A22, C22, E22

****Note:**

- Do not energize output 1 and output 2 at the same time.
- BP1 will be positive with respect to BP2 when output 1 is energized. The reverse is true when output 2 is energized.

Figure 3-8 - Isolation Module Typical Wiring

3.5 CONNECTING MICROLOK II TO EXTERNAL SERIAL DEVICES

The MICROLOK II controller board has four independent serial ports. The MICROLOK II application program determines the function of each of these ports. Each port may be designated as a MICROLOK protocol master, a MICROLOK protocol slave, a GENISYS protocol master, or a GENISYS protocol slave. The function of serial ports may be designated in any combination.

The four serial ports support three different hardware interface standards. Ports 1 and 2 support an RS-485 hardware interface while port 3 supports an RS-423 interface and port 4 supports an RS-232 interface. These standards (RS-485, RS-423, and RS-232) define only the characteristics of the hardware interface. They define characteristics such as interface voltage levels, whether signals are balanced or unbalanced with respect to signal common, and whether or not outputs can be set to a high impedance state for compatibility with multi-drop communication circuits. They have no bearing on the protocols or data that may be passed through these ports. Any of the four serial ports may be used to pass any of the protocols currently supported by MICROLOK II. The only restriction is that ports must connect to external ports which support a like hardware standard. RS-485 ports can be connected to RS-485 or RS-422 compliant ports, RS-423 ports can be connected to RS-423 compliant ports, and RS-232 ports can be connected to RS-232 compliant ports. RS-232 and RS-423 ports can usually be interconnected.

Typically, the RS-485 serial ports are reserved for direct, local connections between two or more RS-485 capable units located in the same equipment facility and powered by the same vital battery power supply. The RS-485 ports utilize balanced signal drivers and receivers that offer a high degree of immunity to ambient electrical noise. In addition, RS-485 serial ports may be connected directly to a multi-drop, hard-wired, serial communication circuit without the use of external signal processing hardware (signal splitters, etc.). The allowable length of the communication circuit is essentially unlimited as long as no part of the circuit leaves the equipment room or signal house where it originates. (MICROLOK II RS-485 circuits cannot be run between signal houses without serial communication circuit isolation hardware.) RS-423 and RS-232 serial ports are most easily connected to common serial devices and commercially available modems. The RS-423 port may be used in simple, short distance, multi-drop applications while the RS-232 port may be used only in short distance point-to-point applications. Short distance, in this case, means less than 50 feet. The RS-423 port should normally be reserved for direct connections to other RS-423 devices such as MICROTRAX EOS when required. The RS-232 port should normally be reserved for use as a GENISYS protocol slave port to be employed as a serial interface to a central control office when such an interface is required. In this case the RS-232 port would normally connect to the master port of the GENISYS 2000 code system interface CPU or directly to an RS-232 modem depending on the specific application.

Serial devices are generally identified as DTE (Data line Terminating Equipment) or DCE (Data Carrying Equipment). In DCE equipment, transmit data (TXD) and request to send (RTS) are inputs and receive data (RXD) and data carrier detect (DCD) are outputs. Modems are generally DCE devices. All MICROLOK II serial ports are labeled as DTE or terminal devices. This means that transmit data (TXD) and request to send (RTS) signals are outputs and receive data (RXD), data carrier detect (DCD), and clear to send (CTS) are inputs. When connecting DTE devices to DCE devices (when connecting a MICROLOK II serial port to a modem, for example) it is necessary to connect TXD to TXD, RTS to RTS, RXD to RXD, and DCD to DCD.

To establish a useable direct bi-directional connection between two MICROLOK II serial ports (both DTE devices), TXD and RXD signals and signal common (COM) must always be connected. The serial port assigned to this connection on one of the two units must be designated as the master port and the serial port assigned on the other unit must be designated as a slave. (A MICROLOK or GENISYS protocol communication link may have multiple slaves but it may have only one master unit.) The ports assigned to this connection must be set to the same protocol (MICROLOK or GENISYS). The data transmitter (TXD) on the

master unit must be connected to the data receiver (RXD) on the slave unit(s). Likewise, RXD on the master unit is connected to TXD on the slave unit(s). The signal common (COM) for master and slave units is connected together. This connection is the simplest connection that allows data to be passed in both directions between master and slave units.

Protocols such as the MICROLOK protocol require message "framing" signals that tell the port at the receiving end of the communication circuit where a message starts and ends. This information is passed by cross-connecting RTS and DCD. In other words RTS on the master unit is connected to DCD on the slave unit(s) and DCD on the master unit is connected to RTS on the slave unit(s). This control signal connection coupled with the data signal connection described in the paragraph above is often referred to as a NULL MODEM connection or a connection between serial ports implemented without the use of modems. The RTS signal on the sending unit signals the beginning of the message when it is asserted. This occurs shortly before data transmission begins. The RTS signal is deasserted shortly after the end of data transmission.

The NULL MODEM connection may always be used to connect two units located in the same equipment facility, which are to communicate using MICROLOK or GENISYS protocols. Of these two protocols, however, only the MICROLOK protocol actually REQUIRES the connection of RTS and DCD. The GENISYS protocol requires only that TXD, RXD, and COM be connected. The DCD signals may be strapped in the asserted state for any unit supporting the GENISYS protocol or simply left disconnected for MICROLOK II or GENISYS 2000 units. (These units are designed to ignore the DCD signal UNLESS half-duplex or keyed carrier communication is selected.)

3.5.1 Connecting MICROLOK and GENISYS Protocol Serial Ports Using Modems

Whenever it is necessary to connect MICROLOK or GENISYS protocol ports which are not located in the same equipment facility, some type of modem or communication device which provides serial common isolation and secondary transient protection MUST be used. While the operating characteristics of modems vary widely, there are a few requirements that apply to all serial interface applications which employ modems.

MICROLOK and GENISYS protocols can only be passed through modems that are capable of passing asynchronous data. Most low speed modems (19,200 bps. or less) and carrier sets have this capability. Neither MICROLOK nor GENISYS protocol implementations support the use of transmit and receive data clocks that are separate from the data signals. Therefore, modems which support only a synchronous serial interface to connected serial equipment, as a general rule, cannot be used.

GENISYS protocol requires modems that can process all messages without the use of either hardware or in-band flow control. This means that either the modems must not buffer outbound data or the modem's outbound data buffer must be large enough to hold the longest message that is expected to be transmitted on the communication link. This constraint applies to modems only. Simple carrier sets generally are not capable of buffering data. MICROLOK protocol MUST NOT be transported by modems that buffer data in any way. Such modems pose a safety risk when they are used to transport the MICROLOK protocol as it is possible that they may buffer complete MICROLOK protocol messages. Care must be exercised in configuring more sophisticated modems to insure that all of the above requirements are met.

3.5.2 Connecting GENISYS Protocol Serial Ports Using Modems

GENISYS protocol may be transported using either half-duplex or full-duplex modems. Half-duplex modems do not support simultaneous transport of data in both directions while full duplex modems do. Half-duplex modems require that both the master and slave end modem interfaces be wired to key the outbound carrier on and off using the RTS signal. Full duplex modems allow the master-end carrier to be strapped permanently in the ON state. Full duplex modems have an advantage in that the master end of the circuit does not have to wait for carrier to stabilize before the transmission of each message as the outbound office carrier is always on.

Typically, the slave end of the communication circuit always keys its outbound carrier on and off whether a half-duplex or full duplex circuit is used. This is because a GENISYS protocol master usually communicates with more than one slave and the slaves would interfere with each other if they did not turn on their outbound carrier only when responding to the master. However, on a point-to-point full duplex communication circuit (a circuit having only one GENISYS protocol master and slave), both master and slave ends may operate with their carrier strapped continuously in the ON state. In this case, the GENISYS protocol port RTS output signal is not connected to the modem RTS (or KEY ON) input. The modem RTS input is permanently strapped in the active state by applying the appropriate voltage to the modem RTS input or by configuring the modem to transmit continuously.

The GENISYS protocol requires only that the DCD input signal be connected to the DCD output of the modem for half duplex modems. For full duplex modems, the DCD input of the GENISYS protocol serial port is either left disconnected or strapped in the active state.

In a typical full duplex modem installation, only TXD, RXD, and COM are connected on the master end and RTS, TXD, RXD, and COM are connected on the slave end. In a half duplex modem installation, RTS, TXD, RXD, DCD, and COM are connected on both master and slave ends of the communication circuit.

The CTS signal, when it is available, can be used to shorten the required delay between the assertion of RTS and the transmission of the first byte of outbound data. This delay is often called the key-on delay. Typically, when data is to be transmitted via a modem and keying of carrier is required, RTS is asserted and a delay timer is started by the serial port handler to delay the transmission of the first byte of data. This is to allow outbound carrier time to stabilize prior to the beginning of data transmission. This timer is normally set to the worst-case carrier stabilization time for the modem. The CTS output from a modem is asserted when the outbound carrier is ACTUALLY stable and ready to transport data. While the use of CTS is optional, it can improve the efficiency of the communication link by allowing data transmission to begin as soon as outbound carrier is stable and before the worst-case carrier stabilization time has elapsed.

3.5.3 Connecting MICROLOK Protocol Serial Ports Using Modems

MICROLOK protocol may only be transported using full duplex modems. RTS, TXD, RXD, DCD, and COM must always be connected on both master and slave ends of the circuit. The outbound carrier signal must stabilize quickly (within 50 bit times at all supported bit rates) when RTS becomes active and must shutdown quickly (within 50 bit times) when the RTS signal is set inactive. When it is available, the CTS signal may optionally be connected as described above to shorten the average outbound carrier key-on delay. The presence of the carrier signal at the receiver must be accurately reflected in the DCD signal, as the MICROLOK protocol requires that received messages be framed by the DCD signal. (Note that many modern, full duplex modems do not manipulate DCD in a way that is useful in framing MICROLOK protocol messages. These modems cannot be used to transport the MICROLOK protocol.)

3.5.3.1 Connecting to RS-485 Serial Ports (Refer to Figure 3-10 -)

Serial ports 1 and 2 are the RS-485 serial ports. Port 1 supports TXD and RTS output signals and RXD, DCD, and CTS input signals. Data clock signals including transmit clock (TXC) which may be either an input or an output and receive clock (RXC) which is an input are present on port 1 but are not currently not supported by the MICROLOK II executive. These signals should not be connected. These signals may be supported in a future release of the MICROLOK II executive. Port 2 supports TXD and RTS output signals and RXD and DCD input signals.

Each RS-485 port signal is transported by a twisted pair of wires labeled as XXX- and XXX+ (TXD- and TXD+, for example). Outputs labeled with a (-) always connect to inputs labeled (-) or (A). Outputs labeled with a (+) always connect to inputs labeled (+) or (B). Differential voltage between (-) and (+) conductors of a pair is typically 1.5 to 5 volts with the (-) conductor negative with respect to the (+) conductor when the signal is

not asserted. (For data lines TXD and RXD, the quiescent or unasserted state is identified as the MARK state.) In addition, the signal commons (COM) for all ports on an RS-485 communication link must be connected together to equalize potential between signal commons for the connected units. When two MICROLOK II units powered by the same battery are serially connected, the connection of serial commons is made through negative battery and does not have to be made through the serial cable. Note that COM cannot be connected to frame or earth ground as it is directly connected through the MICROLOK II power supply to negative vital battery. RS-485 ports should be interconnected using ONLY twisted pair cable with an over-all shield. For best performance, the interconnecting cables should not contain extra, unused pairs. Any unused pairs should be connected together at both ends of the cable and connected to signal common (COM) for best noise immunity. If connected, the shield should be connected to frame ground at one end of the cable only. On the units at each end of the communication circuit, 120 ohm, ½ watt external load resistors should be placed across the TXD and RTS transmitters and across the RXD and DCD receivers. Any units in-between should simply "bridge" the circuit using a bridging "stub" which is as short as possible. On a multi-drop communication circuit (a circuit to which more than two units are connected), the DCD input on the master unit should be biased in its unasserted state. This may be done by connecting 470 ohm, ½ watt resistors between the DCD- input and 0V and between the DCD+ input and +5V. The load resistor for the master DCD input should be 240 ohms, ½ watt (rather than 120 ohms) to maintain the required circuit impedance for the biased circuit. If the CTS input on any serial port is available but not used, it should be forced to its unasserted state. To permanently force an unused RS-485 input to its unasserted state, the (+) input should be connected to +5V and the (-) input should be connected to COMMON (0V). To force an RS-485 input to its asserted state the (+) input should be connected to COMMON (0V) and the (-) input should be connected to +5V or +12V.

3.5.3.2 Connecting to RS-423 Serial Ports (Refer to Figure 3-11)

Serial port 3 is the RS-423 serial port. Serial port 3 supports TXD and RTS output signals and RXD, DCD, and CTS input signals. Data clock signals including transmit clock (TXC) which may be either an input or an output and receive clock (RXC) which is an input are present but are not currently supported by the MICROLOK II executive. These signals should not be connected. These signals may be supported in a future release of the MICROLOK II executive.

In an RS-423 interface, outputs are referenced to signal common (COM) while inputs have their own independent common, receive common (RXCOM). Signal outputs are connected to signal inputs by a single wire as the are in the RS-232 interface but COM on each end is connected to RXCOM on the other end. As this connection of commons does not equalize potential between the signal commons (COM) of the two connected units, an additional connection must be made between COM terminals on the connected units. The quiescent or inactive state for all signals is between –3.6 and –6 volts. (For data lines TXD and RXD, the quiescent state is the MARK state.). The active state for all signals is between +3.6 and +6 volts. RS-423 ports should be interconnected using only multi-conductor cable with an over-all shield. The cable should not contain any twisted pairs. The serial port commons (COM) should be connected using one of the conductors in the cable (NOT the shield). For best performance, interconnecting cables should not contain extra wires. Extra wires should be connected together and connected to COM at both ends for best noise immunity. Note that COM cannot be connected to frame or earth ground as it is directly connected through the MICROLOK II power supply to negative vital battery. The cable shield should be connected to frame ground at one end of the cable only. If CTS is not used, it must be forced to its unasserted state. To permanently force an input to its unasserted state, the input should be connected to -12V. To force an input to its asserted state, the input should be connected to +12V.

RS-423 ports may be connected to RS-232 ports by strapping COM and RXCOM terminals together on the RS-423 end and connecting signals as described under the RS-232 connection scheme below.

3.5.3.3 Connecting to RS-232 Serial Ports

Serial port 4 is the RS-232 serial port. Serial port 4 supports TXD and RTS output signals and RXD and DCD input signals. Each RS-232 signal is transported by a single wire and is referenced to signal common (COM). When any RS-232 signal is not asserted the voltage level for that signal is between –3 and –15 volts. (For data lines TXD and RXD, the quiescent or unasserted state is the MARK state.). The asserted state for all signals is between +3 and +15 volts. RS-232 ports should be interconnected using only multi-conductor cable with an over-all shield. The cable should not contain any twisted pairs. The serial port signal commons (COM) should be interconnected using one of the conductors in the cable (NOT the shield). For best performance, interconnecting cables should not contain extra wires. Extra wires should be connected together and connected to COM at both ends for best noise immunity. If connected, the cable shield should be connected to frame ground at one end of the cable only. The length of interconnecting cables should be limited to 50 feet or less. If it is necessary to permanently force an input to its unasserted state, the input should be connected to -12V. To force an input to its asserted state, the input should be connected to +12V.

3.5.4 Isolation of Serial Port Signal Common

Application engineers should note that the serial commons for all MICROLOK II serial ports are connected directly to negative vital battery AND to each other. This means that anything connected to any serial port signal common IS ALSO CONNECTED TO NEGATIVE VITAL BATTERY. Furthermore, anything connected to the serial common of any equipment that is directly connected to any MICROLOK II serial port is connected to negative vital battery through MICROLOK II. This imposes serious restrictions on the characteristics of the devices that can be DIRECTLY CONNECTED MICROLOK II serial ports. It should be noted, for example, that most commercial data modems connect their serial common to earth ground in some way, either directly or through a low resistance. It should also be noted that most data radios connect their serial common directly to their antenna ground. Both of these conditions create a problem since they introduce a connection between negative vital battery and earth ground. (Vital battery is required to float with respect to ground.) This effectively means that devices like these MUST be connected to MICROLOK II through a serial line isolator which provides a high level of isolation between the signal commons of MICROLOK II and serial devices such as modems and data radios.

Isolation between serial signal commons is also necessary when serially connecting MICROLOK II units that are powered by different batteries. As these battery power supplies are considered vital and are required to float with respect to ground, significant potential differences can develop between the battery negatives. These potential differences can wind up being equalized by the connection between serial commons. This situation poses a threat both to communication circuit reliability and the electrical integrity of the connected MICROLOK II units. In addition, interconnection of battery commons by any means is not a recommended practice. This situation, too, can be remedied by introducing a serial line isolator in the serial line between the MICROLOK II units. It is strongly recommended that all MICROLOK II units NOT connected to the same battery power supply be interconnected serially using communication devices that provide serial common isolation. Furthermore, care must be exercised to insure that devices that ARE serially connected directly to a MICROLOK II unit DO NOT have serial connections to devices that might ground serial common.

3.5.5 Physical Connections to Serial Ports

SIGNAL	PORT 1 RS-485	PORT 2 RS-485	PORT 3 RS-423	PORT 4 RS-232
TXD-	A2	A16	E16	C20
TXD+	A4	A18		
RXD-	C6	A24	E14	C22
RXD+	C8	A26		

SIGNAL	PORT 1 RS-485	PORT 2 RS-485	PORT 3 RS-423	PORT 4 RS-232
RTS-	E2	A20	C14	A14
RTS+	E4	A22		
CTS-	A10		E12	
CTS+	A12			
DCD-	C10	A28	E10	C16
DCD+	C12	A30		
TXC-	C2		A6	
TXC+	C4			
RXC-	E6		A8	
RXC+	E8			
RXREF			E18	
COM (0V)	A32	A32	C18	E22
+12V	C24	C24	C24	C24
-12V	C26	C26	C26	C26

3.5.6 Configuring MICROLOK II Serial Ports

All four MICROLOK II serial ports have many configuration options. These are made available to accommodate most requirements that might be encountered in modern communication equipment. Most of the available options are not intended to be used in the "typical" MICROLOK II installation. In most typical installations, only one port configuration should be used for GENISYS protocol and one for MICROLOK protocol.

3.5.6.1 Serial Port Configuration for Operation on a Direct Wire, Point-to-Point, Communication Circuit

MICROLOK II serial ports 1, 2, and 3 are designed to operate on a direct wire, multi-drop communication circuit. When any of these three ports is designated as either a MICROLOK or GENISYS protocol slave port, the default port configuration is set by the MICROLOK II compiler to accommodate a multi-drop communication circuit. This causes transmit data (TXD) and request to send (RTS) drivers to assume a high impedance state whenever these ports are not actively placing data on the communication circuit. This configuration may not be acceptable for most point-to-point communication circuits as external biasing resistors may be required on inputs to which RTS and TXD are connected to positively hold those inputs in an unasserted state when RTS and TXD drivers go to their high impedance state. This problem can be overcome without the use of external biasing resistors by setting the point-to-point serial port configuration parameter to 1 (POINT.POINT: 1;). This causes RTS and TXD outputs to actively drive the inputs to which they are connected at all times.

Note that for ports designated as master ports, this need not be done. The default configuration of all master ports is point-to-point. Note also that serial port 4 is capable only of point-to-point operation regardless of its designated function and the value of the POINT.POINT parameter for port 4.

3.5.6.2 GENISYS Protocol Serial Port Configuration

The standard GENISYS protocol configuration is:

STOPBITS:	1;	
PARITY:	NONE;	
CARRIER.MODE:	CONSTANT;	
SECURE.MODE:	ON;	(GENISYS MASTER PORT ONLY)
MASTER.CHECKBACK:	OFF;	(GENISYS MASTER PORT ONLY)
CRC.SIZE:	16;	

Some configuration items are intended to vary with the requirements of the installation. The data rate (BAUD:), should be set to accommodate the requirements of the communication system and system responsiveness. When interconnection of units is accomplished by direct wire, a data rate of 19200 BPS should be used to insure good communication response. When modems are used, a data rate appropriate for the selected modems should be used. This can be determined by referring to the application information that accompanies the modem being used.

Key-on (KEY.ON.DELAY:) and key-off delays (KEY.OFF.DELAY:) should be set to 0 for direct wire connections. For modem connections, key-on and key-off delays should be set to a value appropriate for the modems being used. This can be determined by referring to the application information that accompanies the modem. When simple, frequency shift modems are used (such as those manufactured by RFL Industries), 8 to 12 bit times is a good value for key-on and key-off delays. More sophisticated modems and more sophisticated communication links (those with regenerative repeaters, for example) may require longer key-on and key-off delays. The approximate required key-on and key-off delays may often be determined empirically by setting the delays to a high value (about 64 bit times) and attempting to establish communication. Once communication is established, the delays can be progressively reduced until communication becomes erratic. About 4 to 8 bit times should be added to the values which produce erratic operation.

Master port polling timeout (MASTER.TIMEOUT:) must be set to accommodate the worst-case delay time required for a slave to respond. The default value of 500 milliseconds is usually adequate. However, when a GENISYS protocol master is communicating with many slaves on a communication circuit where all slave units may not always be answering, a shorter timeout may be appropriate to insure minimum communication delays when slaves occasionally fail to respond. In any case, the timeout must always be long enough to allow a slave which is capable of responding sufficient time to respond. This time is approximately equal to twice the worst case end-to-end delay for the communication channel plus the worst case communication channel turnaround delay (relevant only for half-duplex channels) plus the worst case turnaround delay for a MICROLOK II slave port (the time between receiving the last byte of a message and transmitting the first byte of the response). The worst case delays for the communication channel may be determined by referring to application information for the communication equipment being used. The worst case turnaround delay for a MICROLOK II slave port is typically less than 50 milliseconds. The average turnaround delay is less than 20 milliseconds.

The master port polling interval parameter (POLLING.INTERVAL:) is provided to adjust communication loading on a MICROLOK II unit which is heavily loaded (many complex logic equations in the application program which execute very frequently). The polling interval is the time inserted between the completion of one message exchange initiated by the master port and the start of the next. Typically, the default value for this parameter should be used. Increasing the value of this parameter decreases the load on the MICROLOK II processor due to communications and increases communication delays because additional time is inserted between messages transmitted by the master. Decreasing the value of this parameter increases the load on the MICROLOK II processor due to communications and decreases communication delays. This parameter should be adjusted only if processor loading problems have been confirmed.

3.5.6.3 MICROLOK Protocol Serial Port Configuration

The standard MICROLOK protocol configuration is:

STOPBITS: 1;

PARITY: NONE;

Some configuration items vary with the requirements of the installation. The data rate (BAUD:), should be set to accommodate the requirements of the communication system and system responsiveness. When interconnection of units is accomplished by direct wire, a data rate of 19200 BPS should be used to insure good communication response. When modems are used, a data rate appropriate for the selected modems should be used. This can be determined by referring to the application information that accompanies the modem.

Key-on (KEY.ON.DELAY:) and key-off delays (KEY.OFF.DELAY:) should be set to 12 for direct wire connections except that at a data rate of 19200 BPS., a key-on delay of at least 30 bit times should be used to allow for worst case receiver enable delays. For modem connections, key-on and key-off delays should be set to a value appropriate for the modems being used. This can be determined by referring to the application information that accompanies the modem. When simple, frequency shift modems are used (such as those manufactured by RFL Industries), 12 bit times is a good value for key-on and key-off delays. More sophisticated modems and more sophisticated communication links (those with repeaters, for example) may require longer key-on and key-off delays. For the MICROLOK protocol, key-on delays of less than 12 bit times should never be used. The approximate required key-on and key-off delays may often be determined empirically by setting the delays to a high value (about 64 bit times) and attempting to establish communication. Once communication is established, the delays can be progressively reduced until communication becomes erratic. About 4 to 8 bit times should be added to the values which produce erratic operation.

Master port polling timeout (MASTER.TIMEOUT:) must be set to accommodate the worst-case delay time required for a slave to respond. The default value of 500 milliseconds is usually adequate. However, when a MICROLOK protocol master is communicating with many slaves on a communication circuit where all slave units may not always be answering, a shorter timeout may be appropriate to insure minimum communication delays when slaves occasionally fail to respond. In any case, the timeout must always be long enough to allow a slave which is capable of responding sufficient time to respond. This time is approximately equal to twice the worst case end-to-end delay for the communication channel plus the worst case communication channel turnaround delay (relevant only for half-duplex channels) plus the worst case turnaround delay for a MICROLOK II slave port (the time between receiving the last byte of a message and transmitting the first byte of the response). The worst case delays for the communication channel may be determined by referring to application information for the communication equipment being used. The worst case turnaround delay for a MICROLOK II slave port is typically less than 50 milliseconds. The average turnaround delay is less than 20 milliseconds.

The master port polling interval parameter (POLLING.INTERVAL:) is provided to adjust communication loading on a MICROLOK II unit which is heavily loaded (many complex logic equations in the application program which execute very frequently). The polling interval is the time inserted between the completion of one message exchange initiated by the master port and the start of the next. Typically, the default value for this parameter should be used. Increasing the value of this parameter decreases the load on the MICROLOK II processor due to communications and increases communication delays because additional time is inserted between messages transmitted by the master. Decreasing the value of this parameter increases the load on the MICROLOK II processor due to communications and decreases communication delays. This parameter should only be adjusted if processor loading problems or communication timing problems have been confirmed.

3.5.7 Configuring MICROLOK II CPU Serial Communication Jumpers

The MICROLOK II hardware and executive software current at the time of release of this document REQUIRE that jumpers JMP7, JMP8, JMP10, JMP13, JMP14, JMP15, JMP16, JMP17, and JMP18 be placed in the factory default position. Future releases of the MICROLOK II hardware and executive software may support other jumper settings. Both jumpers JMP11 and JMP12 must be set in the same position but may be set as required by the specific installation. However, the default setting for JMP11 and JMP12 is recommended for ALL installations.

The following table shows the function of all serial communication jumpers and their default position:

JUMPER	FUNCTION	POSITION	EFFECT
JMP7	Port 4 receive data input	1-2* 2-3	ENABLED DISABLED
JMP8	Port 4 data carrier detect input	1-2* 2-3	ENABLED DISABLED
JMP10	Port 1 synchronous transmitter clock	1-2 2-3*	INPUT OUTPUT
JMP11	Port 3 output driver low level	1-2* 2-3	RS-232 RS-423
JMP12	Port 3 output driver high level	1-2* 2-3	RS-232 RS-423
JMP13	Port 3 synchronous transmitter clock	1-2 2-3*	INPUT OUTPUT
JMP14	Port 3 synchronous transmitter clock	1-2* 2-3	OUTPUT INPUT
JMP15	Port 4 asynchronous clock input	1-2* 2-3	INTERNAL OFF
JMP16	Port 3 asynchronous clock or synchronous receiver clock input	1-2* 2-3	INTERNAL EXTERNAL
JMP17	Port 2 asynchronous clock input	1-2* 2-3	INTERNAL OFF
JMP18	Port 1 asynchronous clock or synchronous receiver clock input	1-2* 2-3	INTERNAL EXTERNAL

Jumper positions marked with (*) are the factory default.

3.5.8 Panel Installation and Power Input

The serial communications adapter panel (N451460-3001) is provided for Microlok II vital serial communications links that run between separate houses or cases. This device consists of a 5-1/4 inch by 19-inch panel with a circuit board mounted on standoffs. The panel is typically mounted in a standard 19-inch equipment rack. The following hardware is required to mount the panel:

Item	US&S Part No.
Nut	J480203
screw, #12-24 x 1/2 pan head	J507261
washer, #12 shakeproof lock	J047750

The panel requires two power sources: a +5 Vdc source that powers the electronics and a 12 Vdc source that powers the interface signals. Fasten terminals are provided on the panel for power connections.

3.5.9 Interface Wiring

- Figure 3-9 - shows a typical 20 mA current loop interface between master and slave Microlok II systems using the serial communications adapter panel. Transmit Data, Request-to-Send, Data Carrier Detect, and Receive Data are each placed in a twisted pair with a separate ground wire. This is done to improve noise immunity from external sources and eliminate possible cross talk between lines.
- The current loop cable assembly is cut to length per the application and fitted with connectors. The cable specifications are as follows:

Maximum Cable Length	Maximum Total Cable Path Length	Nominal Cable Wire Gauge/Type	Minimum Cable Wire Gauge/Type	Wire Capacitance	Wire Resistance
5,000 ft.	10,000 ft.	#19 AWG twisted pair	#24 AWG twisted pair	0.09 mF/1000 ft.	30 ohms/mile

The 20 mA current loop cable should be run below ground where it runs outside of the equipment house or case to minimize possible lightning damage. The shield wire at the end of the cable should be grounded using one of the 25-pin "D" connector attachment screws on the interface panel. Also, a rack ground wire should be run from the panel's **EARTH GROUND** dual Fasten terminal to the equipment rack prime ground bus. Keep this wire as short as possible and minimize the number of bends. Make certain that both ends of the serial link have both shield and rack ground connections as shown in Figure 3-10. The current loop cable should also be provided strain relief by securing it to the rack frame with wire tie straps.

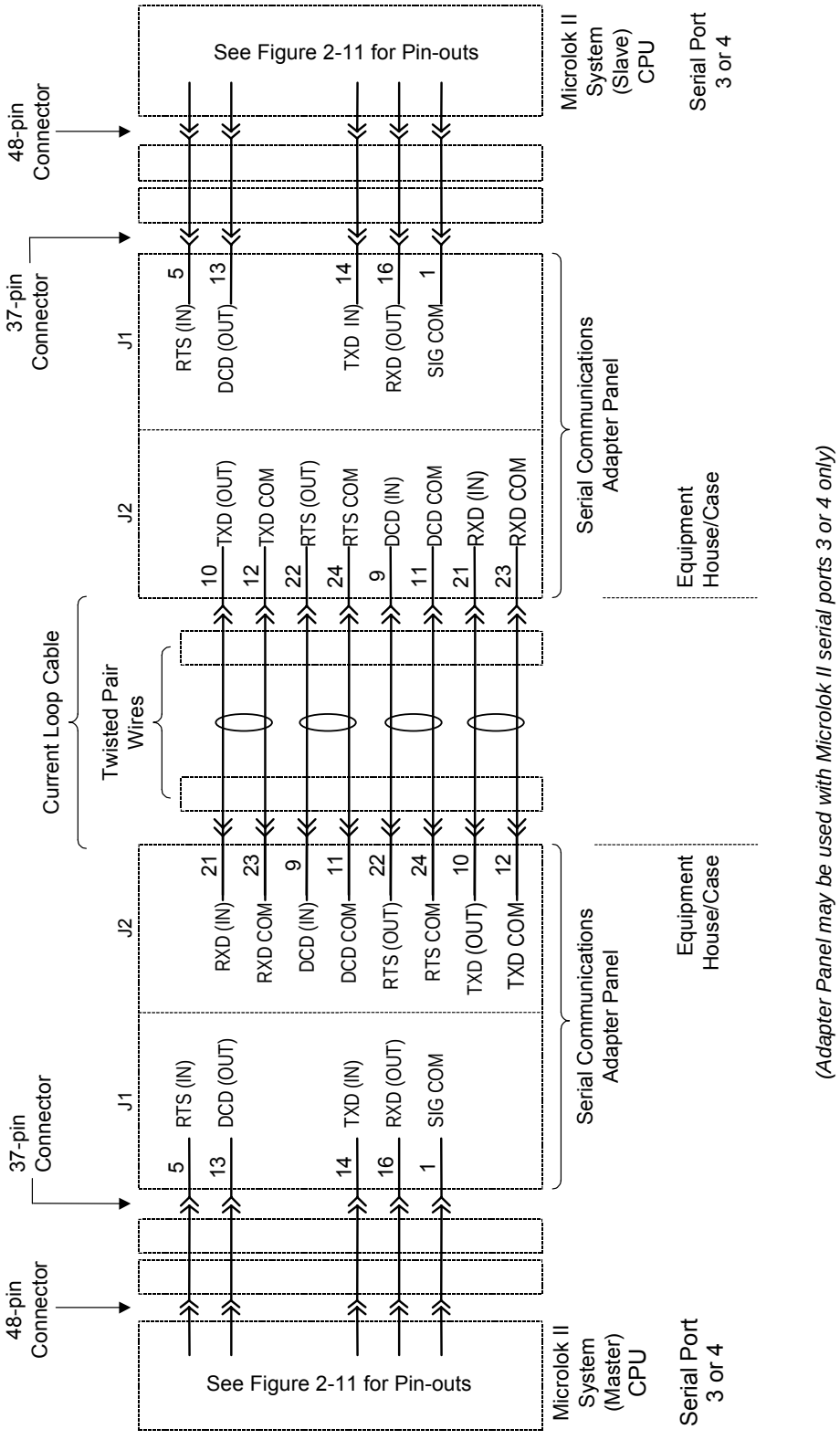


Figure 3-9 - Typical Adapter Panel Application - Master and Slave Microlok II Systems

3.6 SERIAL INTERFACE SCHEMATIC DIAGRAMS

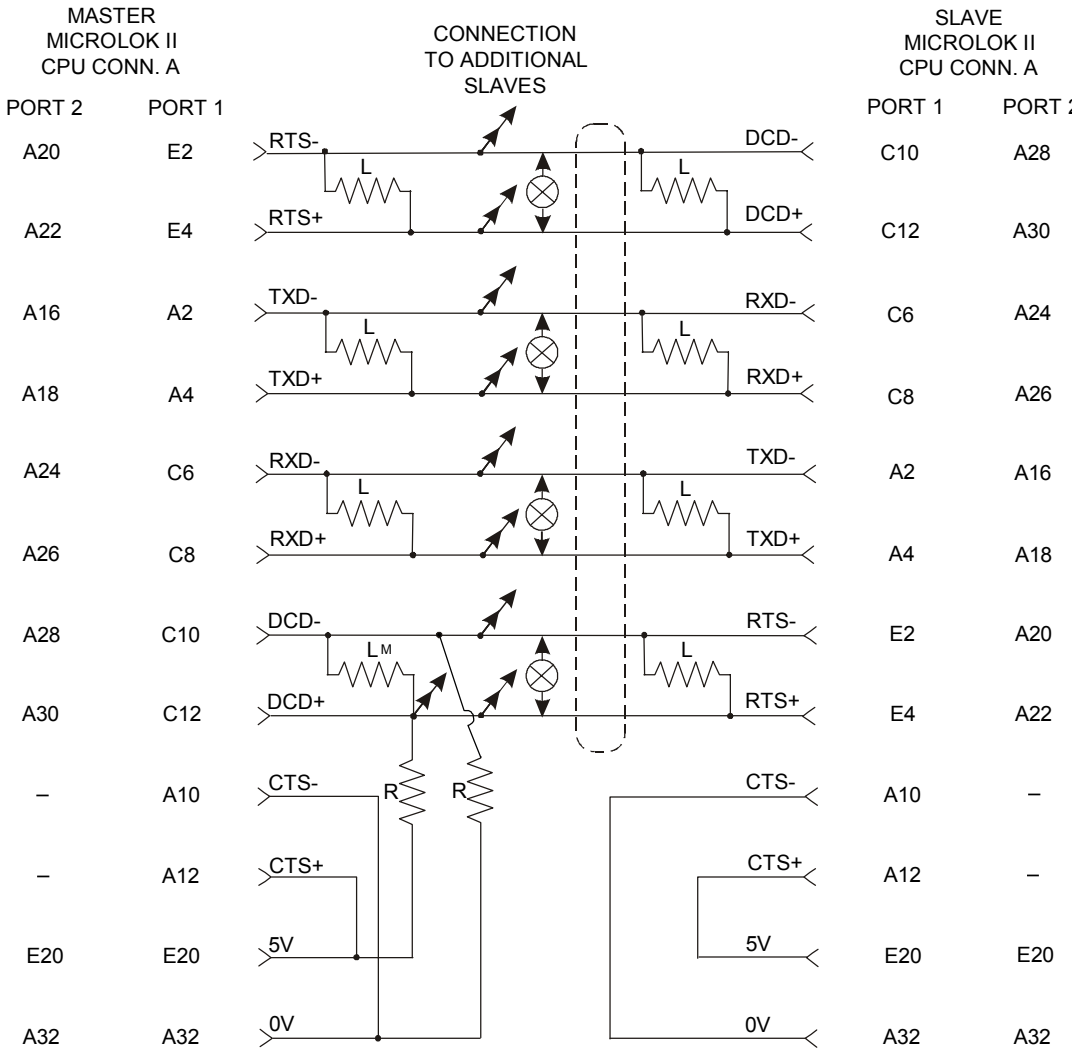


Figure 3-10 - Typical Microlok II Master To Microlok II Slave RS-485 Direct Wire Serial Interface Units Powered By Same Battery (Microlok Protocol Or Half-Duplex Genisys Protocol)

1. Resistors (R) are 470 Ohm, ½ watt.

2. For full duplex Genisys Protocol RTS and DCD need not be connected.

3. Serial commons are interconnected through a battery that powers Microlok II units.

4. Load resistors (L) are 120 Ohm, 1/2 watt and are to be installed externally on the master and on the most distant slave on the circuit only. Load resistor (Lm) is 240 Ohm, ½ watt and is installed on master DCD only, as shown.

5. Do not connect COMMUNICATION COMMON to ground.

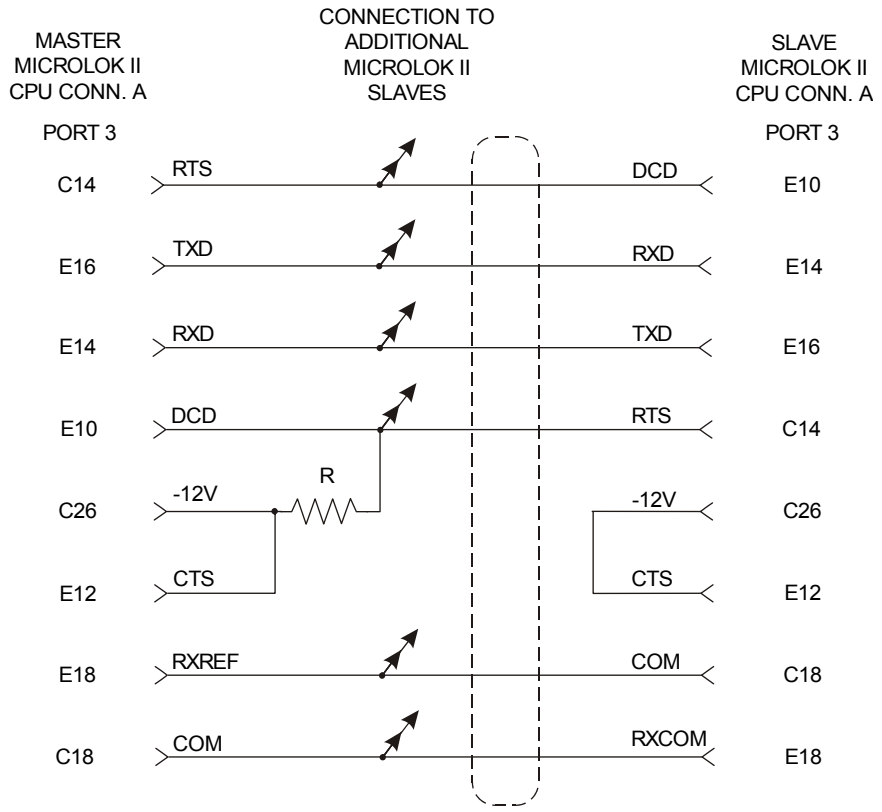


Figure 3-11 - Typical Microlok II Master To Microlok II Slave RS-423 Direct Wire Serial Interface Units Powered By Same Battery (Microlok Protocol Or Half-Duplex Genisys Protocol)

1. Resistor (R) is 10KΩ, ½ watt.
2. For full duplex Genisys protocol connection, RTS and DCD need not be connected.
3. Serial commons are interconnected through battery which powers units.

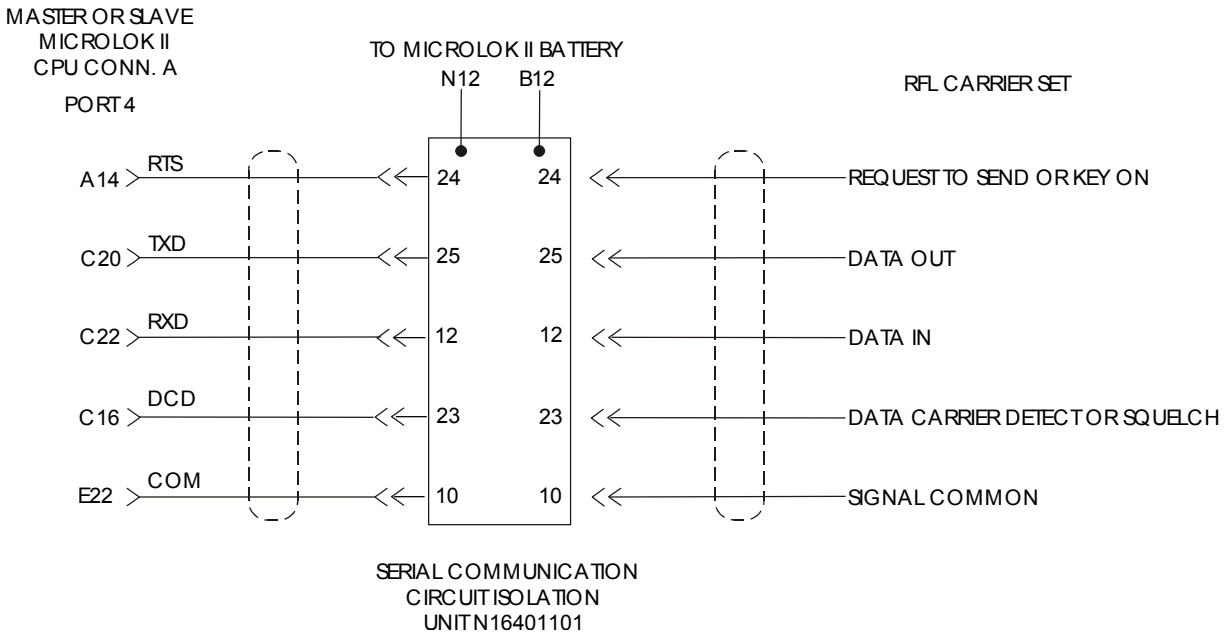


Figure 3-12 - Typical Microlok II Master or Slave to RFL Modem Serial Interface RS-232 Port 4 with Serial Isolator (Microlok or Genisys Protocol)

DCD need not be connected for Genisys protocol on a full-duplex communication link.

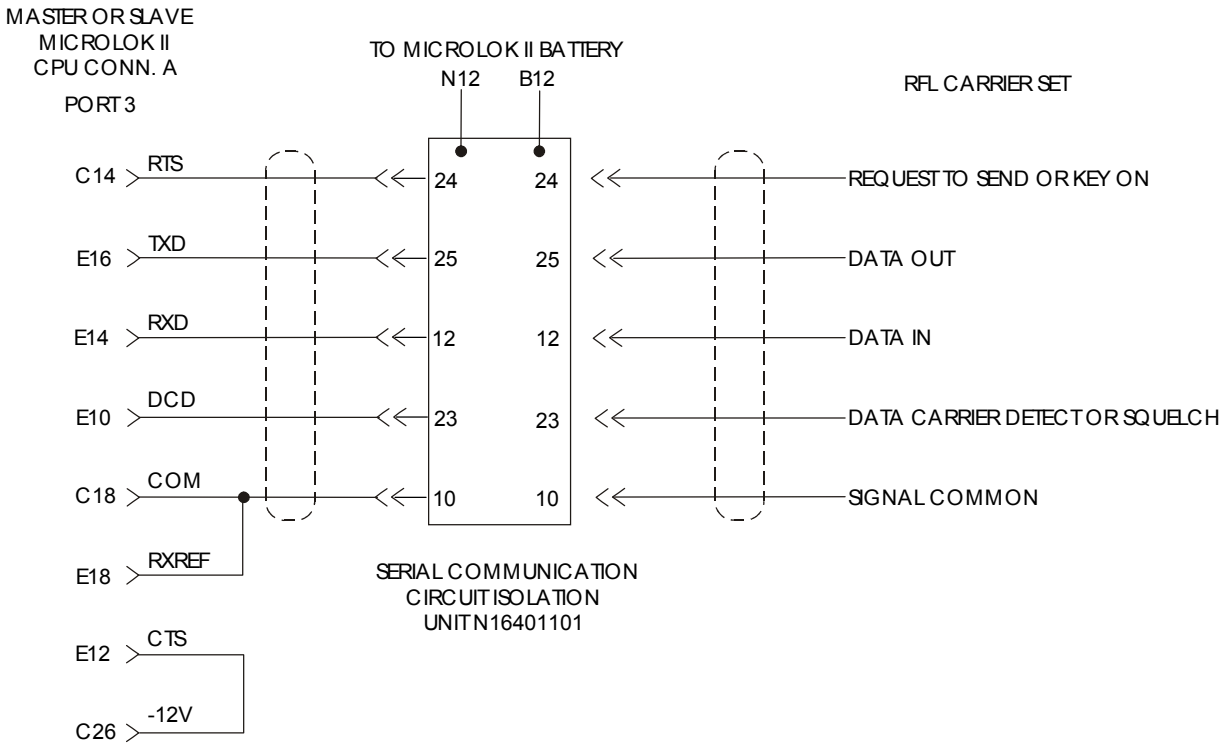


Figure 3-13 - Typical Microlok II Master or Slave to RFL Modem Serial Interface RS-423 Port 3 with Serial Isolator (Microlok or Genisys Protocol)

DCD need not be connected for Genisys protocol on a full-duplex communication link.

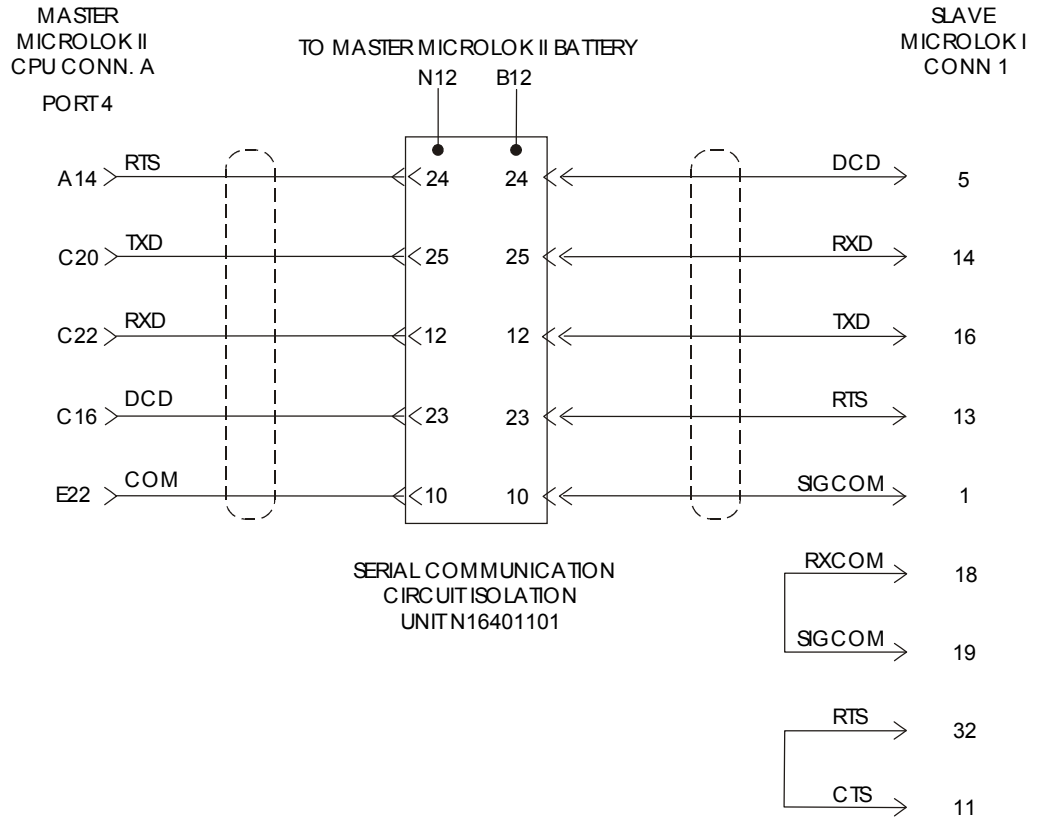


Figure 3-14 - Typical Microlok II Master to Microlok Slave Serial Interface RS-232 Port 4 with Serial Isolator (Microlok or Genisys Protocol)

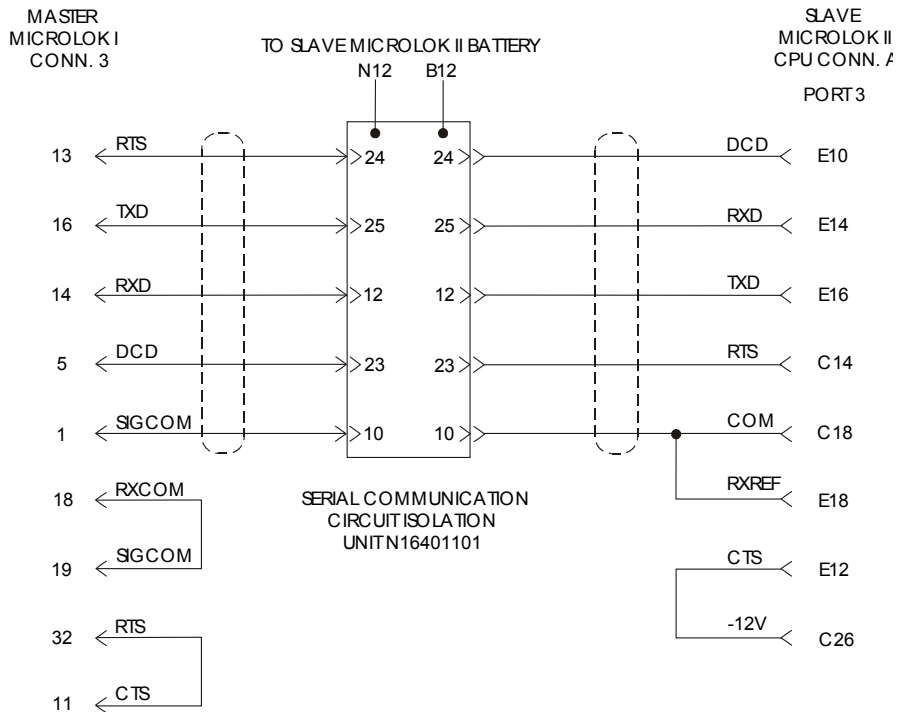


Figure 3-15 - Typical Microlok Master to Microlok II Slave Serial Interface RS-423 Port 3 with Serial Isolator (Microlok Protocol)

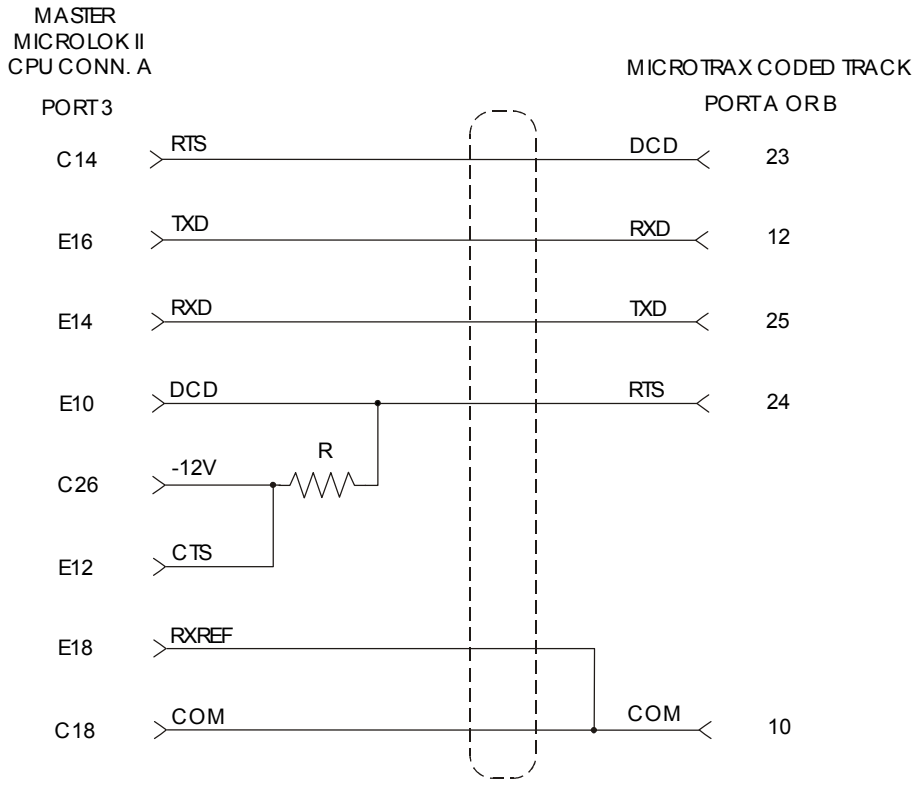


Figure 3-16 - Typical Microlok II Master to Microlok Combo Track Slave Serial Interface RS-423 Direct Wire Interface (Microlok Protocol) Units Powered By Same Battery

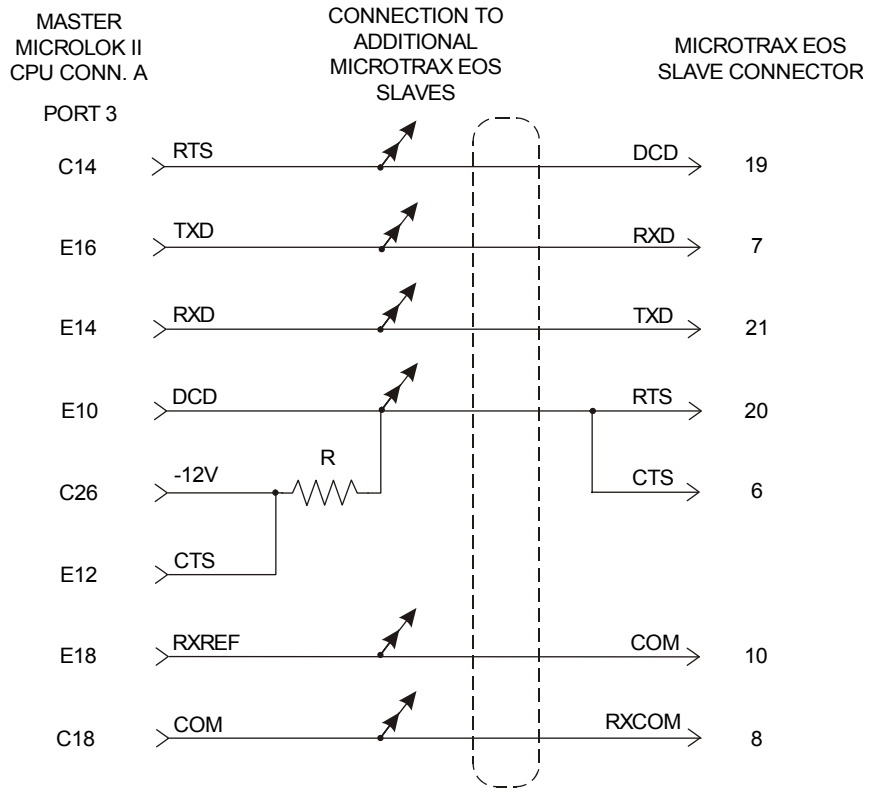


Figure 3-17 - Typical Microlok II Master to Microtrax EOS Slave RS-423 Direct Wire Serial Interface (Microlok Protocol) Units Powered By Same Battery

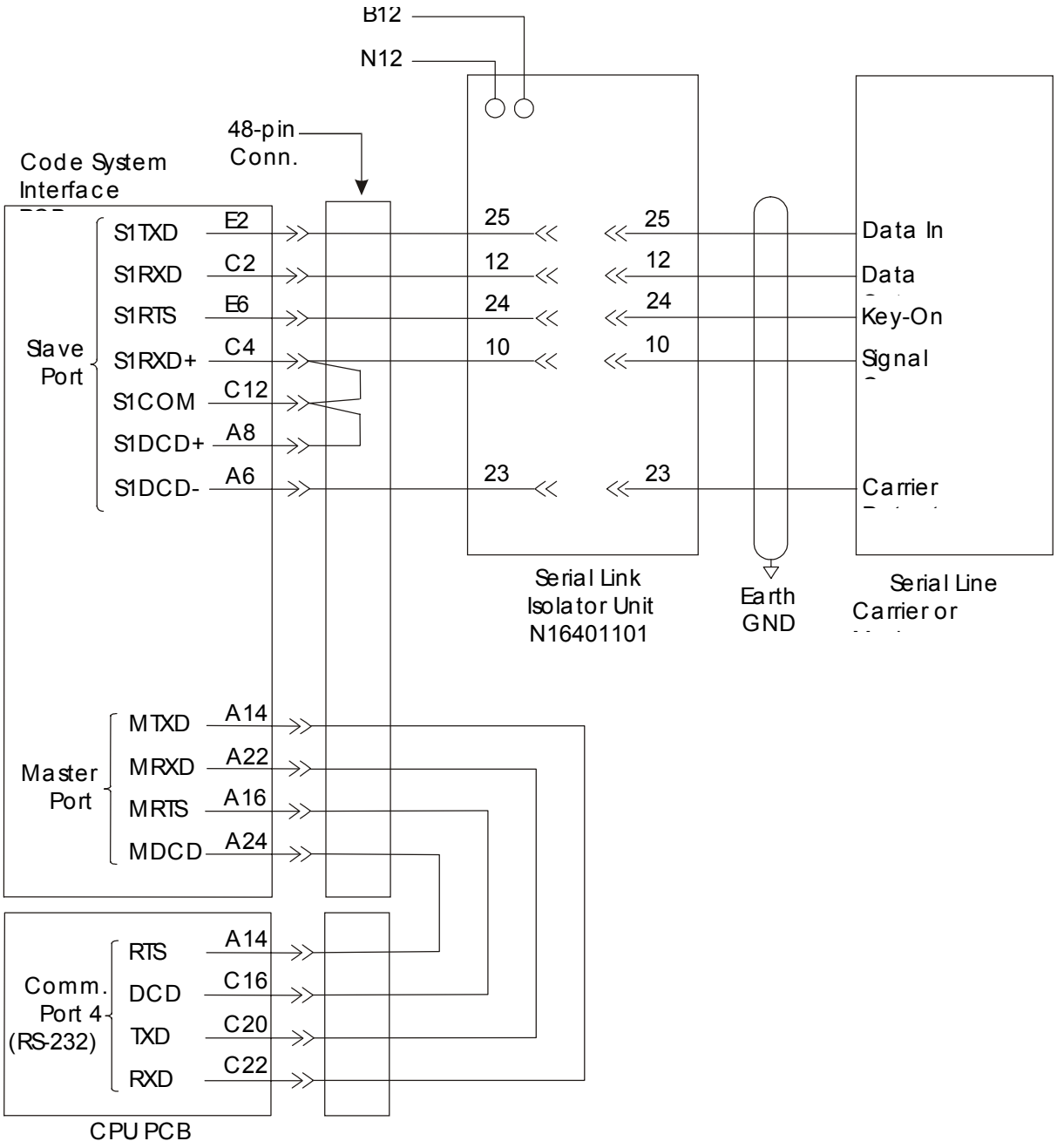


Figure 3-18 - Typical Code System PCB Interface to Serial Line Carrier

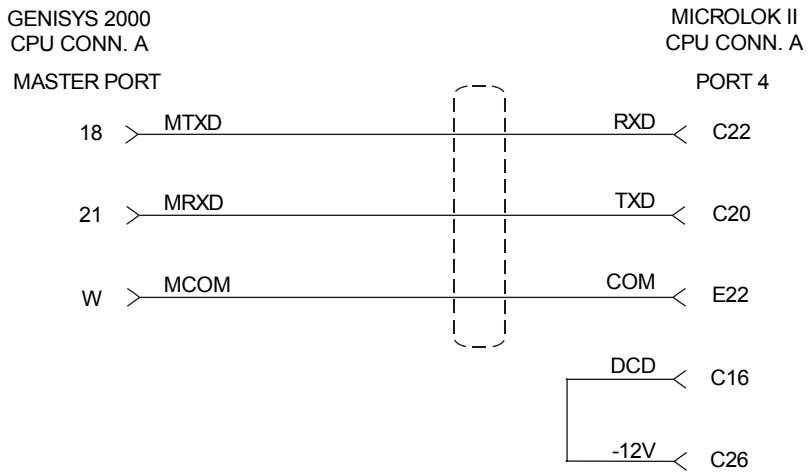


Figure 3-19 - Typical GENISYS 2000 Master To Microlok II Slave RS-232 Direct Wire Serial Interface Units Powered By Same Battery (Genisys Protocol)

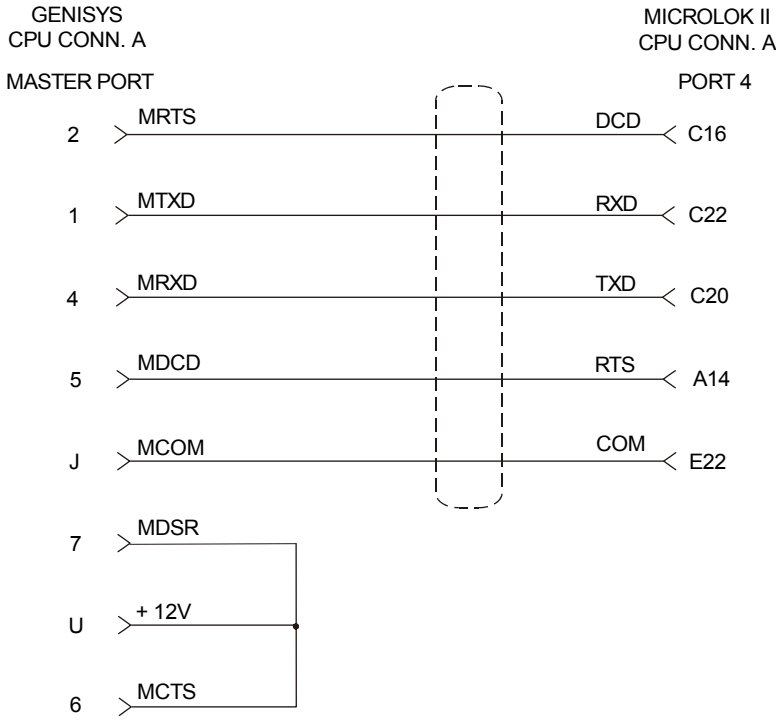


Figure 3-20 - Typical GENISYS Master To Microlok II Slave RS-232 Direct Wire Serial Interface Units Powered By Same Battery (GENISYS Protocol)

4 Installation Parts List

4.1 MAJOR SYSTEM ASSEMBLIES

Item/Description	US&S Part No.	Comments
system cardfile	N16902101	Empty enclosure without field-replaceable components (PCBs and panels). Reference section 4.2 for components.
VCOR relay	N322500-701	US&S PN-150B. Reference section 4.4 for installation parts.
isolation module	N17001101 N17001102 N17001103	12V model 50V model 24V model Reference section 3.4 for applications.
coded track interface panels	N451835-0101 N451835-0102 N451835-0103 N451835-0104	General non-cab applications Non-cab with 86 Hz crossing predictors. Compatible with 100 Hz cab signal. Compatible with 60 Hz cab signal. Reference section 3.1 for applications.
quick shunt module	N451052-4601	Reference section 3.1.4 for applications.
cab signal interface panels	N451835-0801 N451835-0802 N451835-1101	Compatible with 60 Hz cab signal. Compatible with 100 Hz cab signal. Compatible with 40 Hz cab signal. Reference section 3.1 for applications.
serial link isolator units	N16401101	Genisys and Microlok protocols.
serial communications adapter panel	N451460-3001	Reference section 4.4 for installation hardware. Reference section 3.6 for applications.

4.2 MAJOR CARDFILE COMPONENTS

4.2.1 Plug-in Printed Circuit Boards and Front Panels

Item/Description	US&S Part No.	Comments
CPU PCB	N17061301	--
power supply PCBs	N16600301	Without cardfile front panel
	N16660301	With cardfile front panel
standard vital output PCBs	N17060501	16 outputs at 12V
	N17060502	16 outputs at 24V
vital lamp driver PCB	N17060101	16 lamp outputs
non-vital bi-polar output	N17061801	12 bi-polar outputs

Item/Description	US&S Part No.	Comments
vital input PCBs	N17061001	16 inputs at 12V
	N17061002	16 inputs at 24V
	N17061003	16 inputs at 50V
mixed vital I/O PCBs	N17061601	8 inputs at 12V, 8 outputs at 12V
	N17061602	8 inputs at 24V, 8 outputs at 24V
	N17061603	8 inputs at 50V, 8 outputs at 24V
code system interface PCB	N17061401	Without executive EPROMs. Reference section 4.2.2 for EPROMs.
non-vital I/O PCBs	N17000601	IN32.OUT32 w/LCP version
	N17061501	IN32.OUT32 w/o LCP version
non-vital, isolated Output PCB	N17062701	32 isolated outputs
non-vital, isolated Input PCB	N17063701	32 isolated inputs
non-vital isolated I/O PCB w/LCP	N17002801	16 isolated inputs, 16 in and 16 out LCP lines
coded track circuit PCBs	N451910-0701	General non-cab and 100 Hz cab-compatible
	N451910-7601	40 Hz cab-compatible
	N451910-7602	50 Hz cab-compatible
	N451910-7603	60 Hz cab-compatible
OS track circuit PCB	N451810-6701	--
coder output PCB	N451910-5801	75, 120, 180 CPM
auxiliary coder output PCB	N451910-7001	Two 50 CPM cab codes
60/100 Hz cab amplifier PCB	N451910-6401	60 or 100 Hz cab signal
40/50 Hz cab amplifier PCB	N451910-6901	40 or 50 Hz cab signal
local control panel	N16901301	Use with N17000601
local control panel (w/key)	N17002901	Use with N17002801
local control panel (w/o key)	N17002902	Use with N17002801
1-wide blank front panel	N451850-2902	--
2-wide blank front panel	N451859-2901	--
CPS	N451910-7501	With front plate
CPS	N451810-7501	Without front plate

4.2.2 Code System Interface PCB Executive EPROMs

US&S Part No.	Comments
N451800-0201	ATC/PTS
N451800-0202	US&S GENISYS
N451800-0204	Harmon MCS-1
N451800-0206	WB&S S2
N451800-0207	Allen Bradley DF1
N451800-0208	ARES
N451800-0210	GRS Datatrain II
N451800-0211	GRS Datatrain VIII
N451800-0212	US&S GENISYS Dual Slave
N451800-0213	US&S GENISYS Dual Ind. Slave

4.2.3 PCB Interface Cable Assembly Components and Tools*

Item/Description	US&S Part No.	Comments*
48-pin connector assembly	J709146-1105	Used with all PCBs except N17061501.
96-pin connector assembly	J709146-1104	Used with non-vital I/O PCB N17061501.
48-pin connector receptacle	J709146-0452	--
96-pin connector receptacle	J709146-0922	--
receptacle mounting screw	J525400-0001	48-pin or 96-pin receptacle
48-pin guide	J709146-1106	--
96-pin guide	J709146-1107	--
wire crimp contacts	j709146-0453	48-pin, #16-#20, (Harting # 09-06-000-8482)
	j709146-0853	48-pin, #20-#26 (Harting # 09-06-000-8481)
	j709146-0921	96-pin, #20-#28 (Harting # 09-06-000-8484)
Address Select PCB	n17003101	48-pin housing (replaces N17002002)
	n17003301	96-pin housing (replaces N17002101)
EEPROM PCB	n17002001	CPU PCB connector assembly only.
crimp tools	--	48-pin, #16-#20 (Harting # 09-99-000-0077)
	--	48-pin, #20-#26 (Harting # 09-00-000-0076)
	--	96-pin, #20-#28 (Harting # 09-00-000-0075)
extraction tools	--	48-pin, #16-#20 (Harting # 09-99-000-0087)
	Contact US&S	48-pin, #20-#26 Wire

Item/Description	US&S Part No.	Comments*
	--	96-pin, #20-#28 (Harting # 09-99-000-0101)
insertion tools	Contact US&S	48-pin, #16-#20
	Contact US&S	48-pin, #20-#26
	--	96-pin, #20-#28 (Harting # 09-99-000-0100)
locator tools	--	48-pin, #16-#20 (Harting tool 09-99-000-0086)
	Contact US&S	48-pin, #20-#26
	Contact US&S	96-pin, #20-#28 (Harting tool 09-99-000-0099)
*** Reference section 2.1.6.2 and Figure 2.5 for parts locations.**		

4.2.4 Misc. Cardfile Installation Parts

Item/Description	US&S Part No.	Comments
PCB keying plug	J709146-0473	Reference section 2.1.5.2 for installation.
L.H. cardfile mounting bracket	M451811-4501	Included with cardfile.
R.H. cardfile mounting bracket	M451811-4502	Included with cardfile.

4.3 POWER/SIGNAL CONDITIONING AND PROTECTION EQUIPMENT

Item/Description	US&S Part No.	Comments
termination capacitor PCB	N451923-2501	Reference section 3.1.3.4 for application.
USGA blue lightning arrester	N451552-0101	Applications: Coded track circuit Reference section 3.1.3 and Figure 2-19 OS track circuit Reference section 2.2.10 and Figure 2-16
USGA red lightning arrester	n451552-0201	Applications: Same as above.
metal oxide varistor	J582324	Application: Cardfile system power input Reference section 2.1.3.2 and Figure 2-2. Equivalent: GE V131DA40 or Siemens B40K130.
transient voltage suppressor	J792736-	Application: Cardfile system power input Reference section 2.1.3.2 and Figure 2-2. Equivalent: 5KP16A or 16KZ16A.

4.4 MISCELLANEOUS UNIT INSTALLATION HARDWARE

Item/Description	US&S Part No.	Comments
VCOR relay mounting parts		Reference section 3.2.
PN-150B relay	N322500-701	--
relay mounting base	N451376-0302	--
contact springs	M451142-2702	#14 - #16 wire
rack mounting bars	M381333	2 required
mounting bar clamps	M381298	4 required
power-off relay		Reference section 3.3.
relay	J726153-0283	--
base	J581782-0026	--
spring clip	J680167-0009	--
serial communication adapter panel		Reference section 3.6.
nut	J480203	--
screw, #12-24 x 1/2 P-head	J507261	--
washer, #12 lock	J047750	--
4MB FLASH PCMCIA Card	J703105-0107	Reference section 2.2.3.1.3