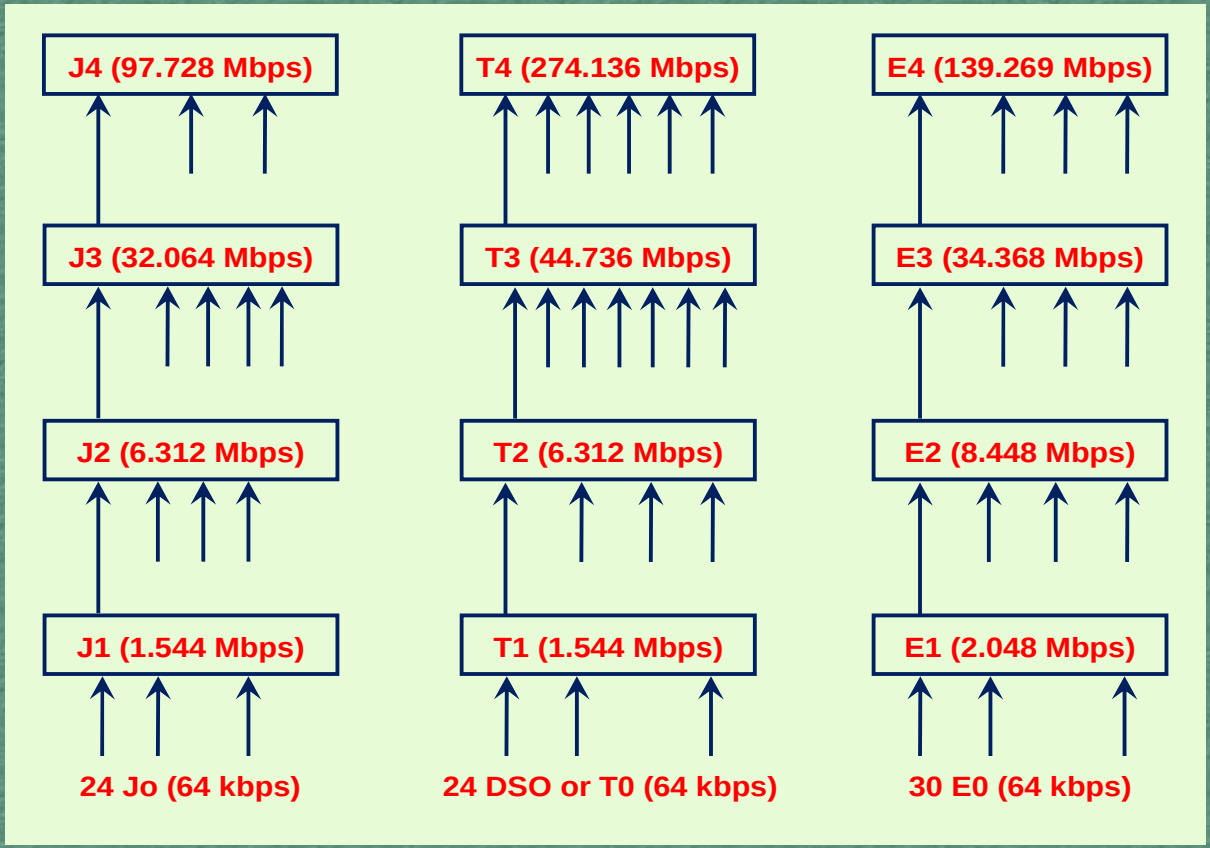
इरिसेट IRISET

TCT2

PDH PRINCIPLES



Indian Railways Institute of
Signal Engineering and Telecommunications
SECUNDERABAD - 500 017

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INDIAN RAILWAYS INSTITUTE OF SIGNAL ENGINEERING & TELECOMMUNICATIONS, SECUNDERABAD - 500 017

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CHAPTER 1

PCM PRINCIPLES

1.1 Introduction

In mid 19th century, a long distance or local conversation between two persons was provided using a pair of either open wire overhead alignment or underground cable. However, due to fast industrial development and increased telephone awareness, demand for trunk and local traffic went on increasing at a rapid rate. To cater to the increased demand of traffic between two stations or between the subscribers at the same station, the use of increased number of pairs either on the open wire alignment or in underground cable was resorted to. This solved the problem for sometime only, as there is a limit to the number of open wire pairs, which can be installed on overhead alignment due to headway considerations and maintenance problems. Similarly, increasing the number of pairs in the underground cable is uneconomical and leads to maintenance problems.

It, therefore, became imperative to think of new technical innovations which could exploit the available bandwidth of transmission media, namely, open wire lines or underground cables, to provide more number of circuits on same pair. The technique of providing a number of circuits using a single transmission pair is called multiplexing.

Initially frequency division multiplexing was used, but to overcome its shortcomings, time division multiplexing was evolved and Pulse Code Modulation (PCM) technique was used in transmission, as well as, in switching of channels. This chapter briefly describes the PCM techniques, and various processing steps the signal has to undergo, in PCM systems.

1.2 Multiplexing Techniques

There are basically two types of multiplexing techniques

- Frequency Division Multiplexing
- Time Division Multiplexing.

Frequency Division Multiplexing (FDM):

The FDM technique is the process of translating individual speech channels, having the bandwidth 300-3400 Hz., into pre-assigned frequency slots within the bandwidth of the transmission medium. The frequency translation is done by Amplitude Modulation of an appropriate carrier frequency by the audio frequency. At the output of the modulator, a filter network is connected to select either the lower or the upper side band. Since, the signal intelligence is carried in either of the side bands, Single Side Band suppressed Carrier mode of AM is used. This results in substantial saving of bandwidth and also permits the use of low power amplifiers. In this way, a number of channels can be combined by using different carrier frequencies for different channels, and transmitting all of them on a single medium is as shown in Fig. 1.1.

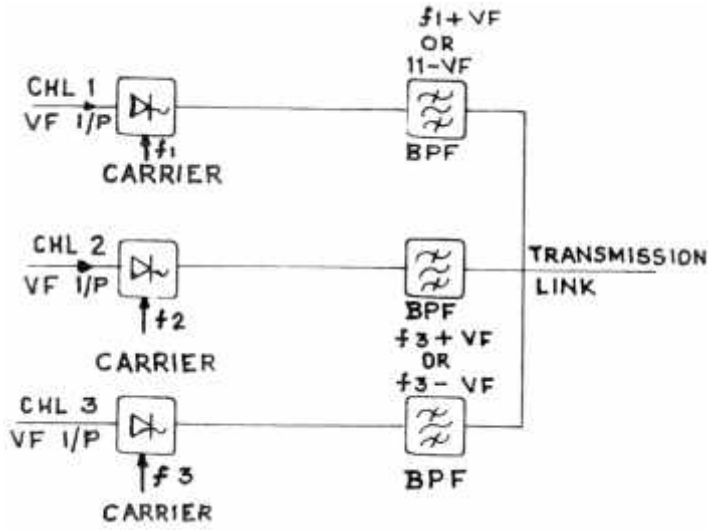


Fig.1.1. FDM Principle

FDM technique usually finds its applications in analogue transmission systems, i.e., in a system used for transmitting continuously varying signals.

Time Division Multiplexing (TDM):

Basically, TDM involves time sharing of a transmission. This can be achieved by establishing a sequence of time slot durations during which individual channel (Circuit) is transmitted. Thus the entire bandwidth is periodically available to each channel. This is illustrated in Fig. 1.2.

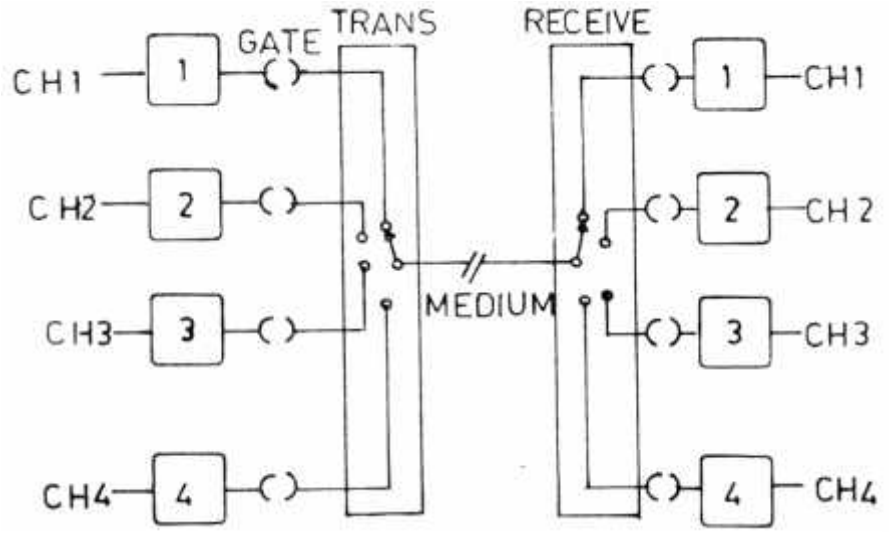


Fig. 1.2. Time Division Multiplexing

Each channel is sampled at a specific rate and transmitted for a fixed duration. All channels are sampled, one by one and transmitted. Normally, all the time durations are equal. Each channel is assigned a time duration with a specific common repetition period. The channels are connected to individual gates, which are opened one by one, in a fixed sequence. At the receiving end also, similar gates are opened in unison with the gates at the transmitting end.

The signal received at the receiving end will be in the form of discrete samples, which are combined to reproduce the original signal. Thus, at a given instant of time, only one channel is transmitted through the medium, and by sequential sampling, a number of channels can be staggered in time as in FDM systems.

TDM technique is used in Digital Transmission systems and Digital Switching systems, where the discrete values of the codified signals are employed.

1.3 Pulse Code Modulation:

In 1938, Mr.A.H.Reaves of U.S.A., developed a Pulse Code Modulation (PCM) system to transmit the spoken word in digital form. Since then, digital speech transmission has become a better alternative to the analogue systems.

PCM systems use TDM technique to provide a number of circuits on the same transmission medium, viz., open wire pair, underground cable pair, a channel provided by carrier, coaxial or microwave system.

1.3.1 Basic Requirements of PCM System: The steps in obtaining PCM signal from analog signal are :

- Filtering
- Sampling
- Quantizing
- Encoding
- Line Coding

Filtering: Filters are used to limit the speech signal to the frequency band 300 - 3400 Hz.

Sampling: Sampling is the most basic requirement for TDM. Suppose an analogue signal, is applied across a resistor, ‘R’, through a Switch, “S”, as shown in Fig. 1.3. Whenever S is closed, an output appears across ‘R’. The rate, at which S is closed, is called the sampling frequency, because during the make periods of ‘S’, the samples of the analogue signal appear across ‘R’, as shown in Fig.1.3

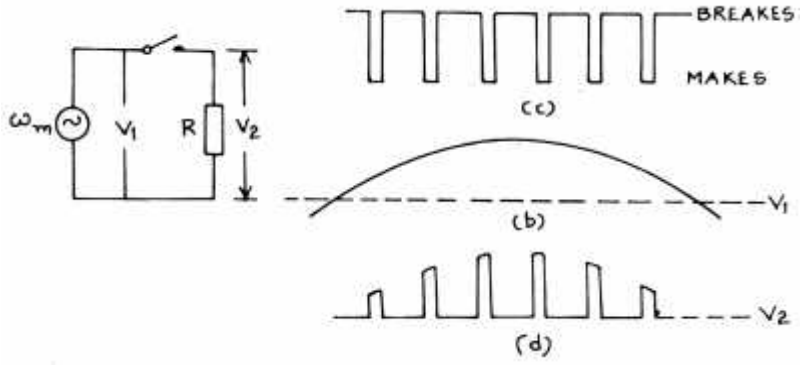


Fig. 1.3. Sampling Process

In other words, the voltage appearing across 'R' is a stream of samples of the input signal. The amplitude of the sample depends upon the amplitude of the input signal, at the instant of sampling. The duration, of each sampled pulse, is equal to the duration for which the switch, 'S' is closed.

It is necessary to determine a minimum limit for the number of samples to be taken, for proper reconstruction of the analogue signal, with acceptable limits of distortion. This sampling rate is defined by sampling theorem.

1.3.2 Sampling Theorem:

A complex signal, such as human speech, has a wide range of frequency components. The frequency components may have different amplitudes. In other words, only the component frequencies have certain amplitudes, and all other frequencies, either higher or lower, have no amplitude. Let us presume that these component frequencies occupy a bandwidth B. As the signal does not have any frequency component beyond this bandwidth, it is said to be band limited. Thus, the magnitude of B depends on the highest and lowest frequency components present in the signal.

Definition of Sampling Theorem: 'If a band-limited signal is sampled at regular intervals of time and at a rate equal to or more than twice the highest signal frequency in the band, then the sample contains all the information of the original signal'. Mathematically.

$$\mathbf{fs \ \tilde{n} \ 2f_H}$$

fs = Sampling Frequency; f_H is the highest frequency in the band.

Let us assume that the voice signals are band-limited to 0 to 4 kHz, then the sampling frequency may be 8 kHz. Hence, the time period of sampling

T_s = 1/8000 sec. = 125 microseconds.

If we have just one channel, then the signal can be sampled every 125 microseconds. But, if N channels are sampled, one by one, at the rate specified by the sampling theorem, then the time available for sampling each channel would be equal to T_s / N.

A method of sampling and combining a number of channels is shown in Fig.1.4.

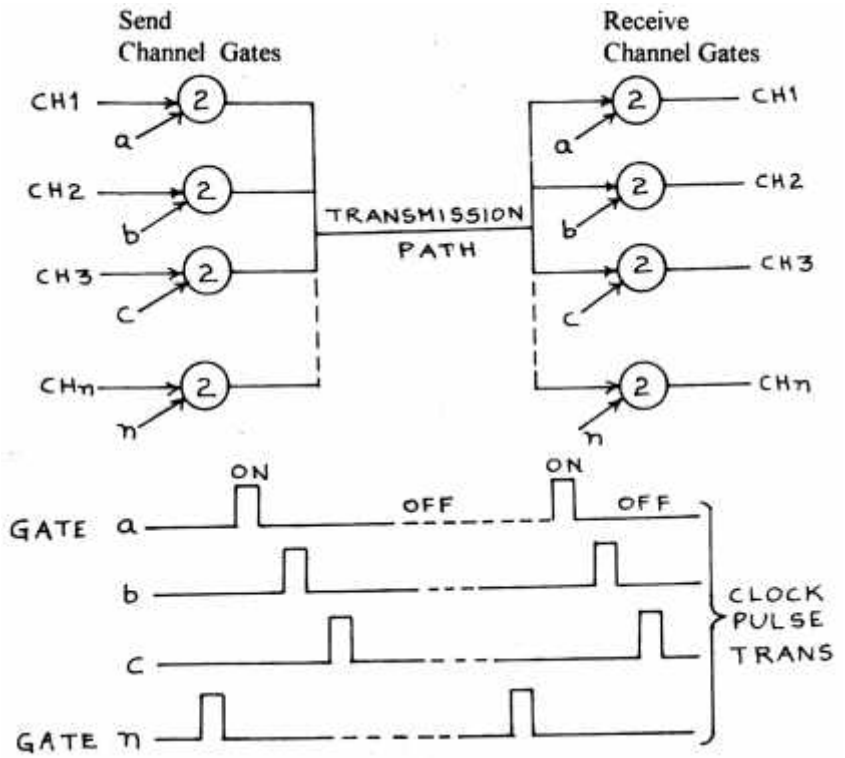


Fig. 1.4 Sampling & Combining Channels

The channel gates a,b – correspond to the switch, 'S' of sec. 2.5. They are called gates because they actually connect the channels to the transmission medium when closed, and isolate them when open. These gates are controlled by a series of pulses, called 'clock pulses'. During the ON period of clock pulses, the gates are closed and during OFF period, the gates are opened.

The clock pulses, for each gate are staggered so that only one pair of gates in trans and receive sides, is open at any given instant and, therefore, only one channel is through, via the transmission medium. The time interval for which the common transmission medium is allocated to a particular channel, is called the Time slot for that channel. The duration of this time slot will depend upon the number of channels to be combined, and the clock pulse frequency, i.e., sampling frequency.

In a 30 channel PCM system, the sampling time period ts of 125 microseconds is divided into 32 time slots, 30 time slots for transmission of speech, one time slot for signalling of all the 30 channels, one timeslot for synchronizing the transmitter and the receiver. Hence, the time available per channel.

$$ts = Ts/N = 125 / 32 = 3.9 \text{ microseconds}$$

Thus, in a 30 channel PCM system, a time slot duration is 3.9 microseconds and time period of sampling i.e., the interval between 2 consecutive samples of a particular channel, is 125 microseconds. In other words, all the 32 time slots, constituting one frame, are repeated every 125 microseconds.

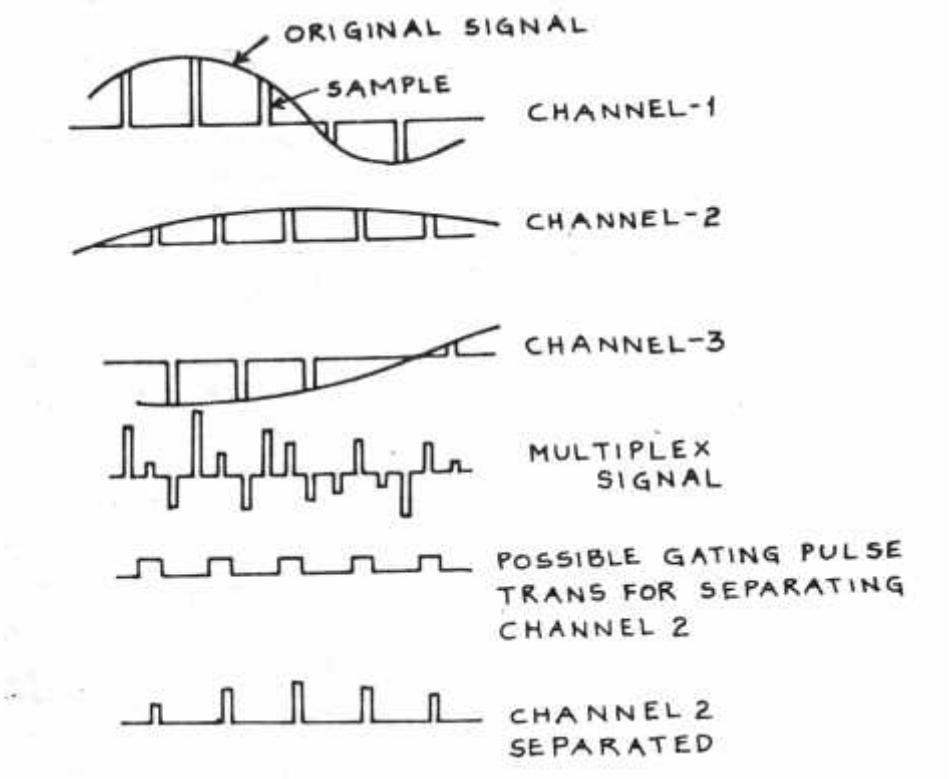


Fig. 1.5. PAM Output Signals

The signals on the common medium (highway) of a TDM system, will consist of a series of pulses whose amplitudes are proportional to the amplitudes of the individual channels at the respective sampling instants. It is, therefore, called Pulse Amplitude Modulation (PAM). This is illustrated in Fig.1.5.

1.3.5 Quantizing:

In PCM system, PAM signals are converted into digital form by Quantization. The discrete level of each sampled signal is quantified with reference to a certain specified level of an amplitude scale. The scale and the number of points should be so chosen that the signal is effectively reconstructed, after demodulation.

Quantizing, is also defined as a process of breaking down a continuous amplitude range into a finite number of amplitude values or steps.

A sampled signal exists only at discrete times but its amplitude is drawn from a continuous range of amplitudes of an analogue signal. Hence, an infinite number of amplitude values are possible. However, a suitable finite number of discrete values can be used to get an approximation of the infinite set.

The discrete value of a sample is measured by comparing it with a scale, having a finite number of intervals called the 'quantizing intervals' and identifying the interval in which the sample lies. For example, a 0.1 volt signal can be divided into 10 mv ranges, like 0- 10 mv, 10-20mv, 20-30 mv, 30-40 mv, and so on. The interval 0-10 mv may be designated as level 0, 10-20 mv as level 1, 20-30 mv as level 2, etc

For transmission, these levels are given a binary code. This process is called encoding. In practical systems, quantizing and encoding are a combined process, but for the sake of explanation, these are treated separately.

Quantization levels

Let a signal be sampled at instants a,b,c,d and e., as shown in Fig.1.6. For the sake of explanation, let us assume that the signal has maximum amplitude of 80 mV.

In order to quantize these five samples of the signal, the total amplitude may be divided into eight ranges or intervals. Samples 'a' lies in the range 5. Accordingly, the quantizing process will assign a binary code corresponding to 5, i.e., 101. Similarly, codes are assigned for other samples also. Here the quantizing intervals are of the same size, hence, it is called Linear Quantizing.

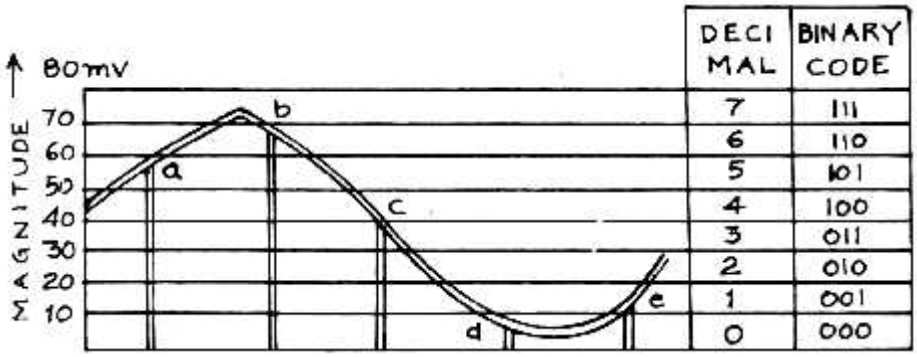


Fig. 1.6 Quantizing Positive Signal

Assigning a value 5 for sample 'a', 7 for sample 'b' etc., is the Quantizing process. Assigning binary codes 101 to sample 'a' 111 to sample 'b' etc., is the encoding process.

Quantizing has to be done for both positive and negative swings. As shown in Fig.1.7 eight quantizing levels are used for each direction of the swing.

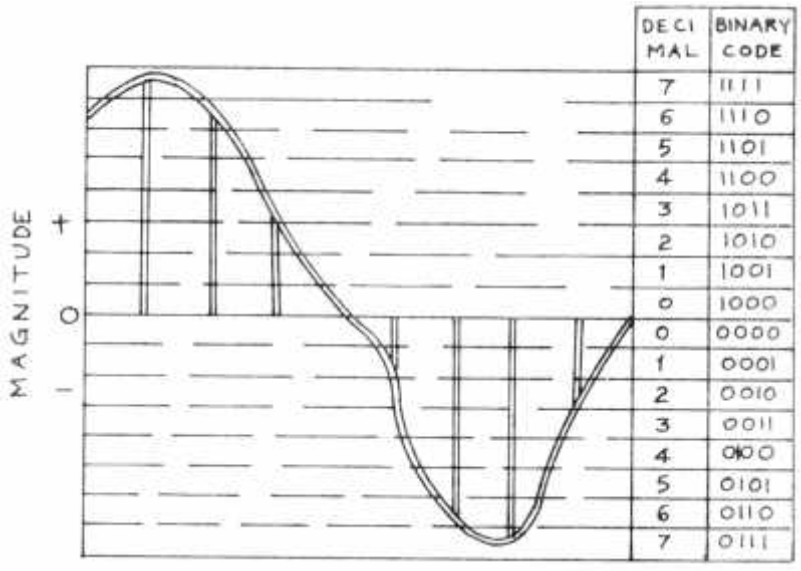


Fig. 1.7. Quantizing Signal With Positive & Negative Values

To indicate whether a sample is negative or positive, an extra bit is added to the binary code. This extra bit is called the sign bit. In Fig. 1.7 the sign bit is '1' for positive values, and '0' for negative values.

Relation between Binary Codes and Number of levels:

Because the quantized samples are coded in binary form, the quantization intervals are in powers of 2. For a 4 bit code, we can have 2^4 - 16 levels. Practical PCM systems use an eight bit code with the first bit as sign bit. It means that there are 2^8 = 256 levels for quantizing, 128 in the positive direction and 128 in the negative direction.

Quantization Distortion:

Analogue Signal amplitude Range	Quantizing Level	Binary Code	Decoded O/P	Maximum Error
0 – 10 mV	0	1000	5mV	± 5mV
10 – 20 mV	1	1001	15 mV	± 5mV
20 – 30 mV	2	1010	25 mV	± 5mV
30 – 40 mV	3	1011	35 mV	± 5mV
40 – 50 mV	4	1100	45 mV	± 5mV

Table. 1.1 Illustration of Quantization Distortion.

In quantization, the lower value of each interval is assigned to a sample falling in that particular interval.

At the receiving end, the mid value of the interval is assigned, while decoding. Let us consider an example as given in tabular form in Table 1.1

If a sample has an amplitude, say 23 mV or 28 mV, it will be assigned the level 2, in either case. This is represented in binary code as 1010. When these are decoded at the receiving end, the decoder will convert them into analogue signals of amplitude 25mV each. Thus, the process of quantization leads to an approximation of the input signal with some deviations in amplitude. These deviations, between the amplitudes of samples at the transmitting and the receiving ends, i.e., the difference between the actual value and the reconstructed value, gives rise to quantization error or distortion.

Non Linear Quantization:

In linear quantization, equal step size results in equal error for all amplitudes. Thus, the signal to noise ratio for weaker signals will be poorer in comparison with signal to noise ratio for stronger signals.

To reduce this error, it is, therefore, necessary to reduce step size. In other words, the number of steps in the given amplitude range should be increased. This would however, increase the transmission bandwidth because bandwidth is $B = f_H \log N$,

Where N is the number of quantum steps and f_H is the highest signal frequency. But as per the speech statistics, the probability of occurrence of small amplitude is much greater than that a large one. It, therefore, seems appropriate to provide more quantum levels (V_L = low value) in the small amplitude region and only a fewer quantum levels (V_H = high value) in the region of higher amplitudes. In this case, no increase in transmission bandwidth will be required, provided that the total number of specified levels remains unchanged. This will also bring about uniformity in signal to noise ratio at all levels of input signal. This type of quantization is called Non linear Quantization, as shown in Fig 1.8.

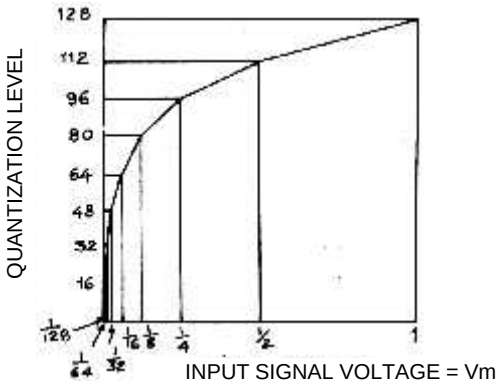


Fig. 1.8. Segmented Companding Curve

In practice, non linear quantization is achieved using segmented quantization. There are equal number of segments for both positive and negative excursions. In order to specify the location of a sample value it is necessary to know.

- Sign of the sample (positive or negative)
- Segment number
- Quantum level within the segment

As seen from Fig.1.8, the first two segments in either polarity are collinear, i.e., the slope is the same and hence, they may be considered as one segment. Thus, the total number of segments appears to be 13. However, for purpose of analysis, all the 16 segments are to be considered separately.

Companding:

The non linearity introduced by the non-uniform quantizing can be neutralized by a reverse procedure.

As the non linearity, before the transmission, is achieved by 'compressing' the signal, it can be neutralized by 'expanding' the received signal. Hence, the procedure is called 'companding', in short.

1.3.6 Encoding:

Conversion of quantized analogue samples to binary signal is called encoding. To represent 256 steps, an 8-bit code is required. This 8 bit code is also called as word. The 8-bit word appears in the form

P	ABC	WXYZ
Polarity bit '1' for +ve '0' for –ve	Segment code	Step number in the segment

The MSB indicates the sign of the sample. Next 3 bits indicate one out of eight segment numbers. Last 4 bits indicate one out of 16 positions in the segment. A voltage 'Vc' will be encoded as 11110101, as shown in Fig.1.9.

The quantizing and encoding are done by a circuit called coder. The coder converts PAM signals, into an 8 bit binary code, in accordance with the compression curve, shown in Fig. 1.9. The curve has the following characteristics :

- It is symmetrical about the origin. Zero code corresponds to zero voltage.
- It is a logarithmic function approximated by 13 straight segments, numbered 0 to 7 in positive direction and 0 to 7 in the negative direction. However, four segments 0, 1, 0^1 and 1^1, lying between levels +Vm/128 & -Vm/128 are taken as one segment, being collinear.
- The maximum voltage of each successive segments are in the ratio of 2, viz.,, Vm/128, Vm/64, Vm/32, Vm/16, Vm/8, Vm/4, Vm/2, and Vm, where Vm is the maximum voltage.
- There are 128 quantification levels in the positive part of the curve and another 128 in the negative part.

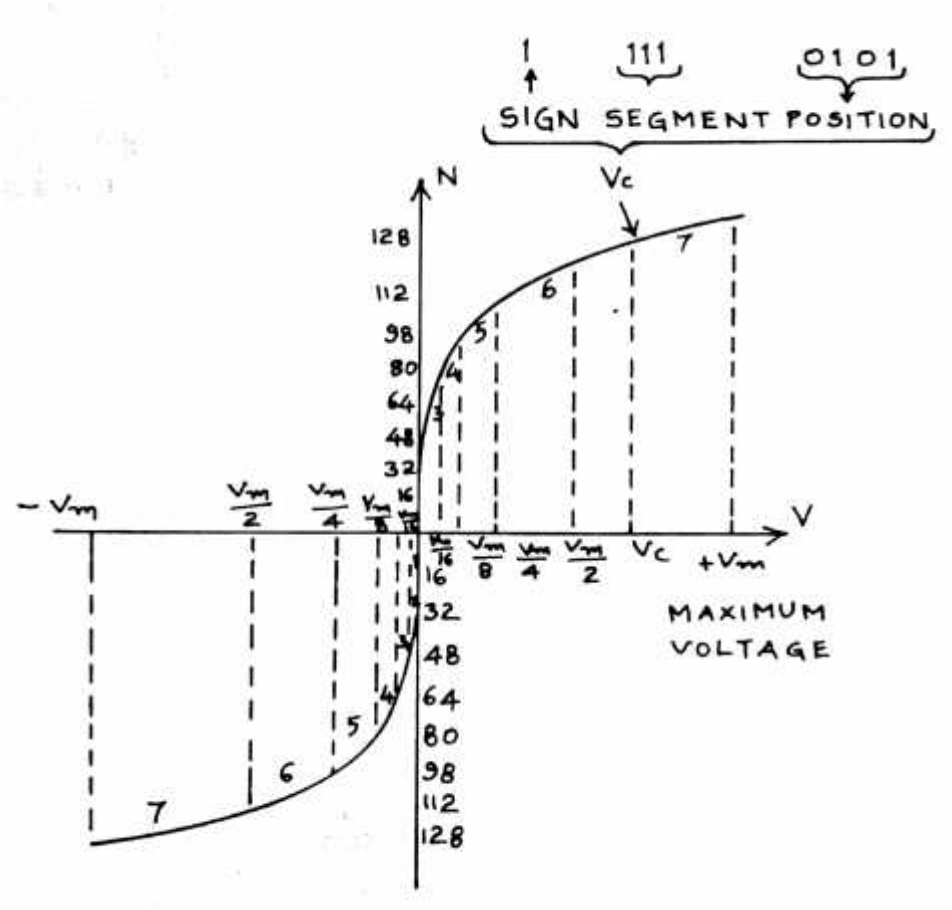


Fig. 1.9. Encoding Curve with Compression 8 bit code.

In a PCM system, the channels are sampled, one by one, by applying the sampling pulses to the Sampling Gates, as shown in Fig.1.10.

The analogue signals pass through them for the duration of the pulse. Since, only one gate is activated at a given instant, a common encoding circuit for quantizing and encoding the samples can be used for all channels. The encoded samples of all the channels and signals are combined in the Digital combiner and transmitted over the medium.

The reverse process is carried out at the receiving end, to retrieve the original analogue signals. The Digital separator separates the incoming digital streams into individual timeslots by operating the Receive sampling gates in the same sequence, in synchronism with the Transmit Sampling Gates. The sample in each timeslot is decoded to give PAM (Pulse Amplitude Modulated) sample.

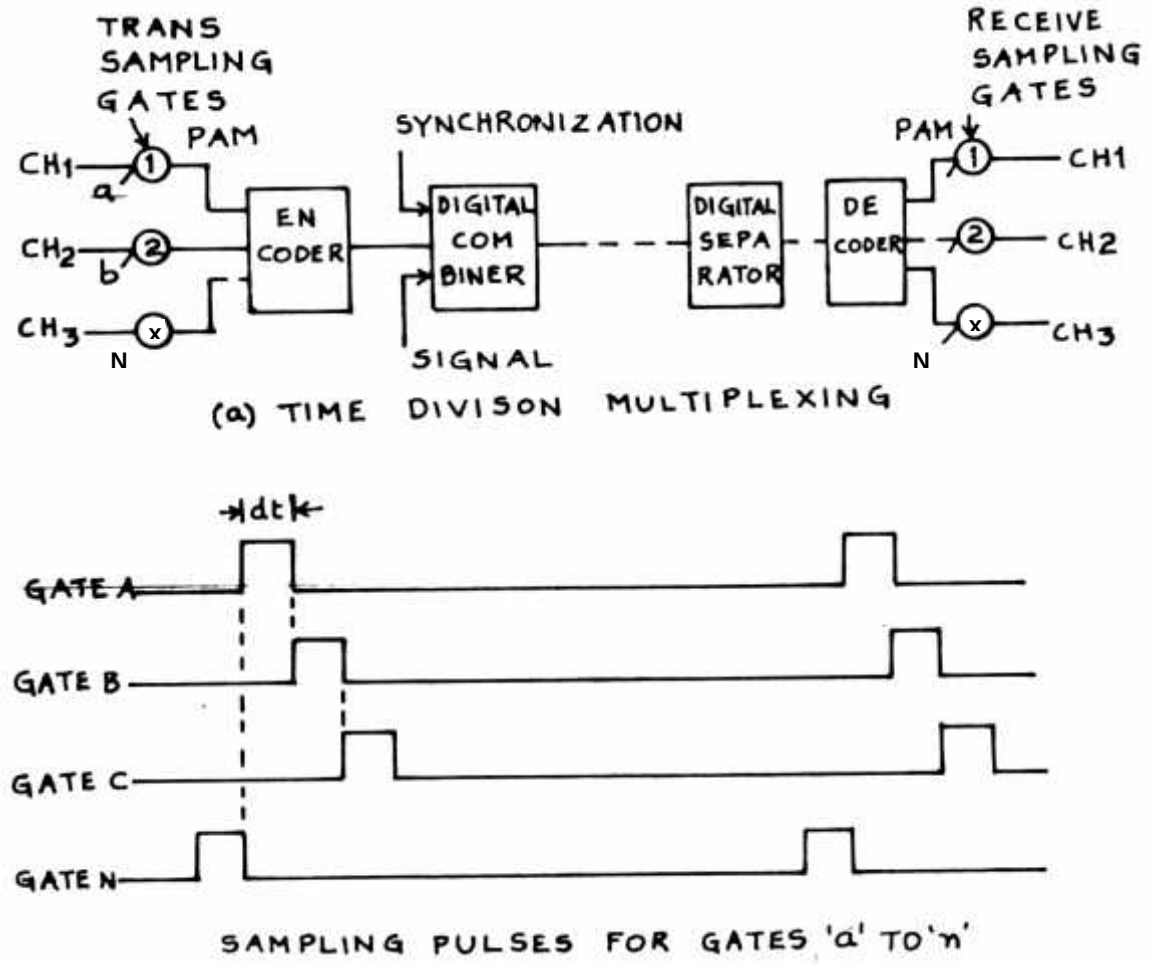


Fig.1.10. PCM Systems

1.4 PCM Frame:

The sampling pulse has a repetition rate of Ts secs. and a pulse width of ts. When a sampling pulse arrives, the sampling gate remains open during the time ts and remains closed till the next pulse arrives. It means that a channel is activated for the duration ts.

Since Ts is much larger than ts, a number of channels may be sampled, each for a duration of ts within the time Ts . With reference to Fig. 1.10, the first sample of the first channel is taken by pulse ’a’ encoded and is passed on to the combiner. Then the first sample of the second channel is taken by pulse ‘b’ encoded and passed on to the combiner. Likewise, the remaining channels are also sampled sequentially and are encoded before being fed to the combiner. After the first sample of the nth channel is taken and processed, the second sample of the first channel is taken, followed by second sample of second channel, and so on. The collection of all the samples taken within the duration Ts, is called a "frame". Thus the set of first samples of all channels is one frame, the set of second samples is second frame, and so on.

1.4.1Structure of Frame of 30 Channel PCM System:

A frame of 125 microsecond duration has 32 time-slots. These time-slots are numbered TS0 to TS31.

The TS0 carries the synchronization signal. Hence, the word in this timeslot is called frame Alignment word FAW.

The signalling information is transmitted in timeslot TS 16. TS 1 to TS 15 carry speech signals of channels 1 to 15, respectively. TS 17 to TS31 carry speech signals of channels 16 to 30, respectively.

1.4.2 Bit Rate:

Sometimes, the system may also be designated by its bit rate. It is denoted by the total number of bits transmitted every second. For a 30 channel system, there are 32 timeslots in each frame. Each timeslot carries an eight bit word. Hence,

Total number of bits per frame = 32 x 8 = 256

As the sampling frequency is 8 kHz, the frequency of frames is also 8000/sec. Therefore, total number of bits in one second :

256 x 8000 = 2, 048,000 = 2048 k bits

Hence, a 30 channel PCM system is also designated as 2048 k bps system or 2.048 Mbps system.

1.4.3 Frame Synchronization:

The Output of a PCM terminal is a continuous stream of bits. At the receiving end, the receiver has to discriminate between frames and channels. For this purpose, it has to recognize the start of each frame, correctly. This operation is called frame alignment or synchronization and is achieved with the help of a fixed digital pattern, called Frame Alignment Word (FAW). The FAW is inserted into the transmitted bit stream at regular intervals. The receiver looks for FAW and once detected, it knows that the next time slot contains the information for channel 1, followed by channel 2, and so on.

The digits or bits of FAW occupy seven out of eight bits of TSO in the following pattern Bit position of TS0 B I B2 B3 B4 B5 B6 B7 B8
FAW digit value X 0 011011

The bit B1 can be either ’1’ or 0. It is fixed at ’1’, when the PCM system is linked with international network.

FAW is transmitted in the Ts0 of every alternate frame.

Frames that do not contain FAW, are used for transmitting supervisory and alarm signals.

To distinguish between the Ts0 of frames carrying supervisory alarm signals, from those carrying FAW, the B_2 bit of the former is fixed at ’1’. The bit pattern is, therefore, X 1 y y y 11 for alarms.

1.4.4 How signalling is carried

In a telephone network, the signalling is used for proper connection of calls to subscribers by providing status information like dial tone, busy tone, ring-back tone, NU tone, metering pulses, trunk offering signals etc. All these functions are grouped under the general term "signalling". The signalling information is transmitted in the form of DC pulses in step by step exchange and multi-frequency pulses in Crossbar exchange.

The signalling levels retain their constant amplitudes for much longer periods than the speech, i.e., the former are slow varying signals compared to the speech signal. Therefore, a signalling can be digitized with lesser number of bits.

1.4.5 Multi frame:

In a 30 channel PCM system, timeslot TS16, in each frame, carries signalling information of two speech channels. Therefore, to cater for 30 channels, 15 frames, each having 125 microseconds duration, are required. An additional frame is required to carry synchronization data, known as Multi Frame Alignment Word (MFAW). Thus a group of 16 frames is formed to make a 'multiframe'. The duration of a multiframe is 2 milliseconds. The relationship between the bit duration, frame and multiframe is illustrated in Fig. 1.11(a)

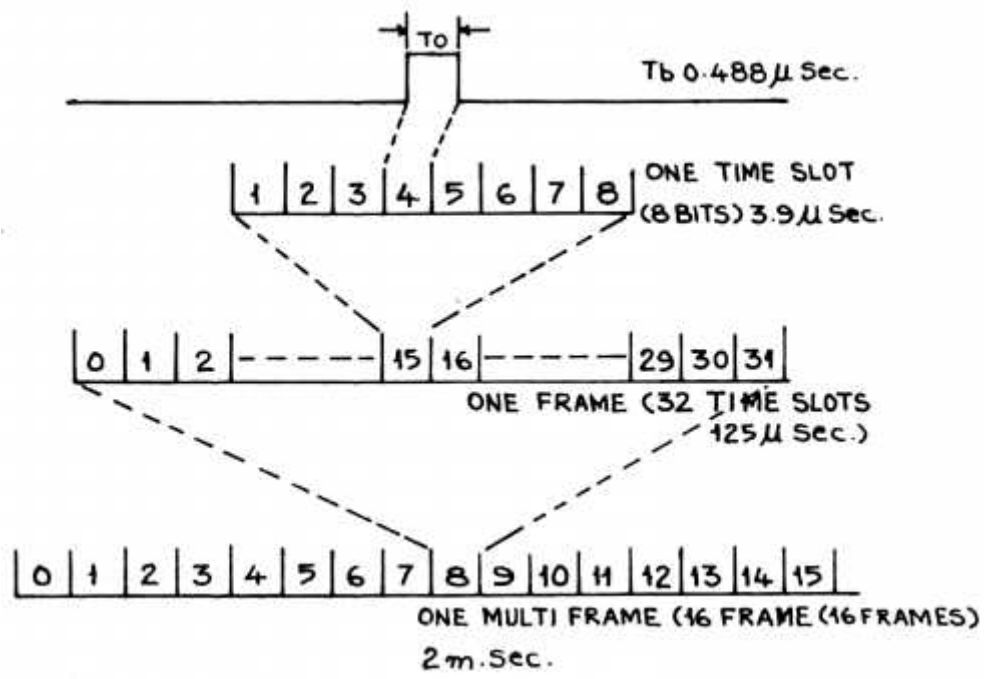


Fig.1.11(a) Multi frame Formation

Multi frame Structure:

In TS16 of frame F0, the first four bits contain the multiframe alignment word, which enables the receiver to identify the beginning of a multi frame.

The remaining four bits may be used for carrying alarm signals

TS16 of frames F1 to F15 are used for carrying the signalling information. Each frame carries signalling data for two speech channels. Four signalling bits are provided for each speech channel. For example, the first four bits of TS16 of F1, carry the signalling data of speech channel 1, and the remaining four bits carry signalling data of speech channel 16. Similarly, TS16, of F2 carries signalling data of channels 2 and 17, and so on.

As each multiframe contains 16 frames with repetition rate of 8000 frames per second, the sampling of each Sig. channel is at a rate of 500 samples / sec. Multi-frame composition is shown in fig.1.11(b)

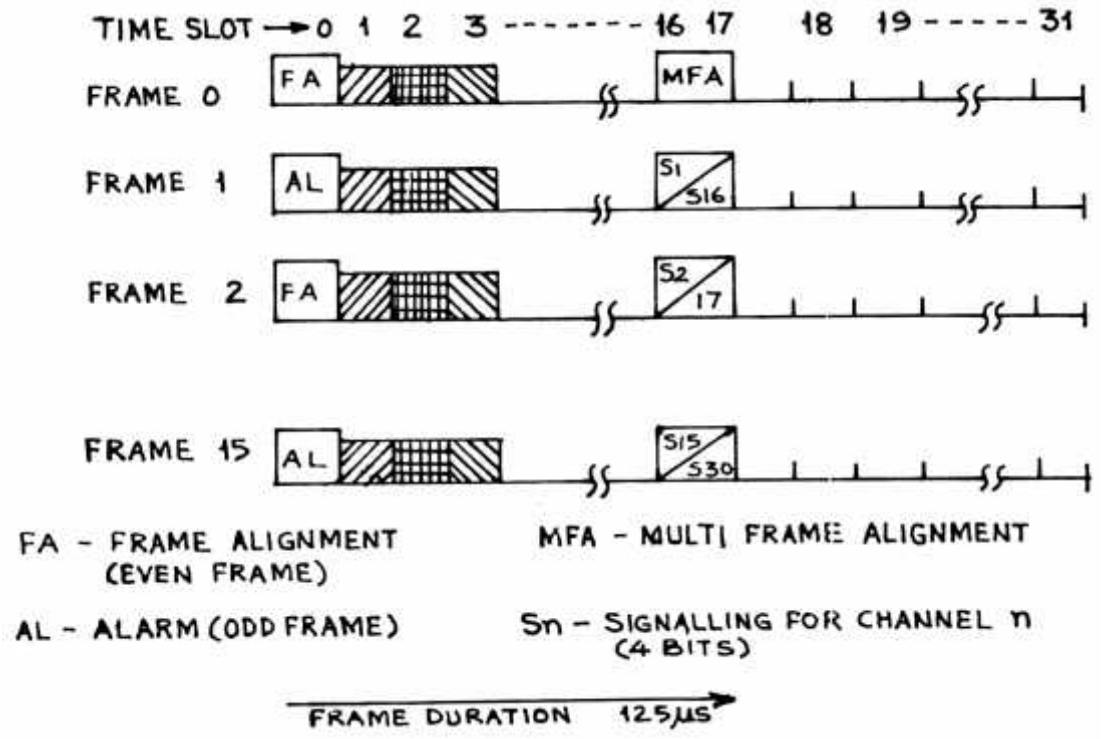


Fig. 1.11(b). Composition of Multiframe

1.5 Line Coding in PCM

The binary signal is composed of zeros and positive voltages. Its low frequency spectral energy is high, and the presence of DC component prevents the use of transformer and AC coupled circuits required for power feeding.

Moreover, in PCM working, the regenerators are required at regular intervals to regenerate the signals cleansing it from noise. Clock, needed to regenerate the signal, is generally extracted from the incoming signal. Hence, the signal should have sufficient timing information. If the unipolar signal has long sequences of 1's and 0's, the timing information will be insignificant, making clock recovery difficult.
Therefore, the output of PCM encoder, is not suitable for transmission of signal on the line and should be modified to match the characteristics of transmission line, as well as, to make the clock recovery easy. This process is known as Line Coding.

1.5.1 Characteristics of line code used in PCM

The Line Code used in PCM should have following characteristics :

- The total bandwidth of the signal should be as small as possible.
- The energy in the upper part of the frequency spectrum should low, so that the attenuation distortion is low.
- The energy in the lower part of the spectrum should also be low to reduce interference from and to VF circuits in the same cable.
- There should not be any DC component.
- It must have an inbuilt error monitoring capability.

A number of codes, having these characteristics, have been developed. However, the two codes that are currently used for PCM systems are

- AMI Code
- HDB-3 Code

1.5.2 AMI (Alternate Mark Inversion) Code:

AMI code was first devised by Barker, and became popular when it was adapted by Bell Telephone Lab for PCM working. In U.S.A., it is often termed as Bipolar signal.

In this code, successive marks (bit 1) are alternatively of positive and negative polarity and equal in amplitude. Space (bit 0) is of 0 amplitude. AMI coded signal corresponding to a binary signal is illustrated in Fig.1.12

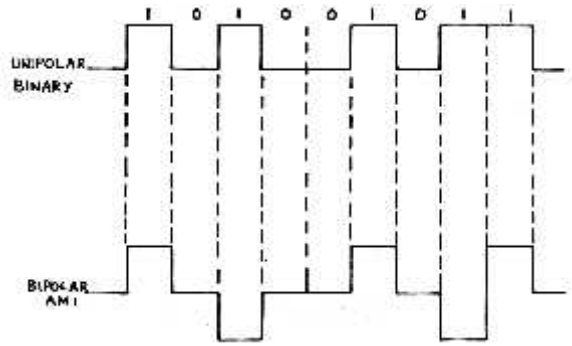


Fig. 1.12. Binary & AMI Codes

The disadvantage of the AMI code is the absence of significant timing information for long sequence of zeros. Otherwise, it meets the remaining requirements for the line code. The realization of code is also simple. Bipolar violation technique is used to detect errors in the line signal. It is used in 24 channel PCM system.

1.5.3 HDB-3 (High Density Bipolar of Order 3) Code:

To overcome the shortcomings of AMI code, HDB-3 code has been devised. It makes a substitution on binary formations containing more than 3 zeros. This substitution must obey the following rules.

- The fourth zero is converted to 1 (mark) with the same polarity as immediately preceding mark, thus violation is introduced. This bit is known as Violation (V) bit.
- The V bit, i.e., the 1 placed in place of 4th zero, must be of opposite polarity to the previous V bit.

HDB-3 signal corresponding to a binary signal is shown in Fig. 1.13.

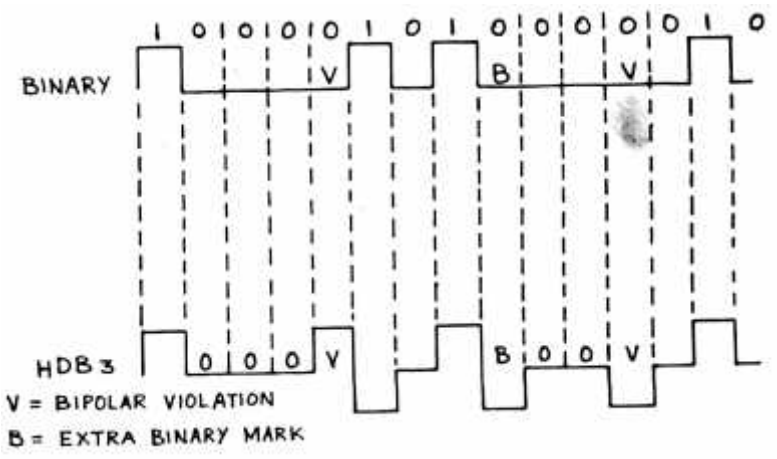


Fig. 1.13. HDB 3 Coding

The steps for conversion of a unipolar binary signal into an HDB - 3 code are as under.

- Every 4th zero is replaced by V bit.
- If the number of 1's between two V bits is even, the first zero of 4 consecutive zeros will also be made 1, called 'P' bit, if the number of I's between two V bits is even. In other words, a combination of 0000 is converted to P00V or 000V depending upon whether the number of 1's between two V bits is even or odd, respectively.
- Data bits and B bits follow one bipolar rule and V bit follow separate bipolar rule.

As the long sequence of zero is avoided, more timing information is available in the signal. Code violation technique is employed to detect errors.

The binary signals shown in Figs.1.12 and 1.13 are Non return to zero (NRZ) signals. They are converted into return to zero (RZ) signal to have clock frequency component that is not available in NRZ. Simple conversion of NRZ signals to RZ, corresponding to a NRZ Binary signal is shown in Fig. 1.14

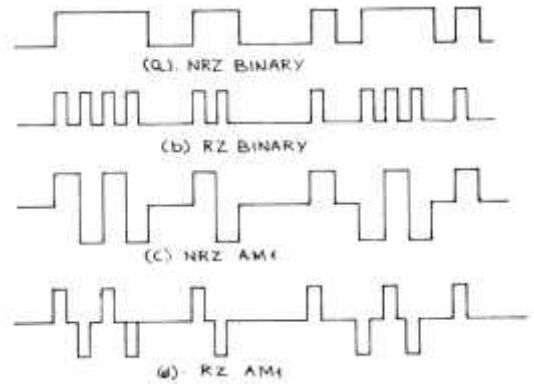


Fig. 1.14. NRZ AND RZ Signals

The signals are normally converted to RZ, in practical PCM system, to have better timing information.

1.6 Higher order PCM Systems:

Higher order PCM systems are designed for the trunk network, by assembling primary blocks of 30 channels of 2.048 M b/s in a hierarchical fashion similar to analogue groups, subgroups and super groups of FDM. Digital hierarchy, recommended by ITU-T, is shown in Fig.1.15.

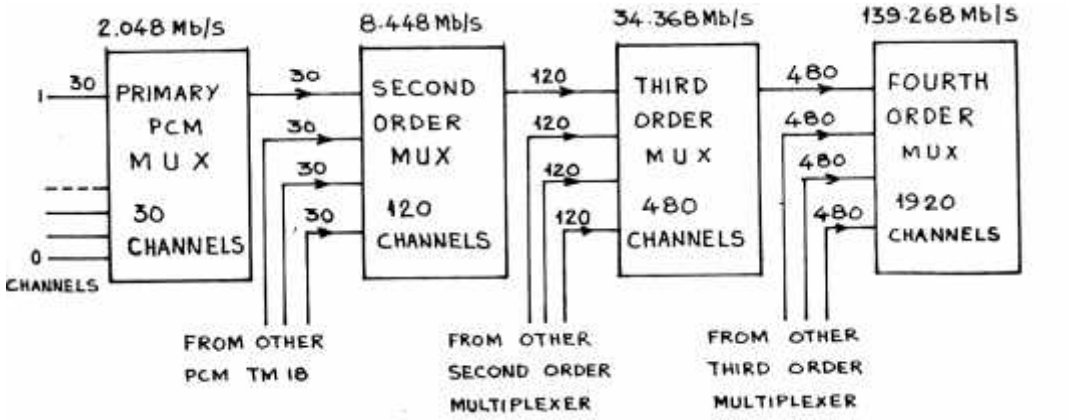


Fig.1.15 Digital Hierarchy based on 2048 Kb/s PCM Primary MUX System

In the case of Analogue FDM systems, the CCITT(replaced by ITU in the year 1993) has recommended a worldwide use of primary group of 12 channels and secondary group of 60 channels. Hence, there is only one hierarchy for Analogue FDM systems all over the world. Unfortunately, in the case of digital TDM, it has not been possible to draw up the specifications for a single type of primary multiplex equipment to be used for building up the TDM systems. Even today, there are two different types of primary multiplexers, as per ITU-T recommendations, based on 30 channel PCM (followed in India, Europe) and based on 24 channel PCM (followed in UK, North America) . They differ not only in their bit rates, but also in frame structure, FAW, signalling etc. As a result, the higher order multiplexers, derived from these two basic units differ.

Summary

Pulse Code Modulation is a time division multiplexing method to carry a number of channels on a single medium.

Each channel is allotted a timeslot during which its codified sample is transmitted. A number of time slots constitute a Frame which is repeated with a periodicity equivalent to the sampling rate. The signalling information of each channel is carried in one of the frames of a multiframe, consisting of a number of frames, required to cover the signalling information of all the channels.

The PCM signal, so obtained, is further codified in Line code to meet the requirements of the transmission medium.

For higher order PCM systems, there are two hierarchies : one based on 30 channel PCM or E-hierarchy and the other based on 24 channel PCM or T-hierarchy

Objective:

1. TDM uses _____ sharing of the transmission media.
2. Mr. A.H Reaves of USA developed _____ system.
3. Filtering is used to limit the _____ signal to the frequency band 300 to 3.4 KHz
4. Sampling is the process of _____ the analog signals at regular interval
5. Sampling Theorem states that sampling rate should be greater than _____ the highest signal frequency.
6. For a band limited signal of 4 KHz the sampling frequency is _____ KHz as per Nyquist Theorem.
7. The Time Period of Sampling in PCM is _____ seconds
8. Time available per channel basis is _____ seconds
9. The interval between two consecutive samples is _____ sec
10. PAM signals are converted into digital form by the process called _____
11. Quantization is the process of breaking down a continuous signal into _____
12. Quantization levels are given Binary values in a process called _____
13. To reduce the quantization error _____ is adopted
14. Encoding is the conversion of quantized analog samples to _____ signal
15. The signaling information is transmitted in timeslot _____
16. Alarms and supervisory are Transmitted in every _____ frame
17. The duration of multiframe is _____ second
18. The sampling rate of signaling channel is _____
19. PCM system uses _____ as line code
20. Time slot TS0 carries the _____
21. A 30 channel PCM has a bit rate _____

Subjective:

1) What are the various multiplexing Techniques adopted in communication systems?

2) Write short notes
   a. Frequency Division Multiplexing.
   b. Time Division Multiplexing.

3) Write down the Basic Requirements of PCM system?

4) What is Sampling and write down its importance in PCM system?

5) Define Quantization?

6) Define Quantization distortion?

7) What is the technique adopted to minimize Quantization distortion?

8) Define Non linear quantization?

9) Write short notes on
   a. Companding.
   b. Encoding.

10) Explain the formation of the PCM frame, how a multiframe is form in Primary multiplexing technique?

11) How you will derive the primary bit rate of 2.048 Mb/s from the first order (E1) frame?

12) Discuss how signaling is carried in PCM frame?

13) How Alarms and Frame Alignment Bits are transmitted in PCM frame?

14) What is Line Coding in PCM? What are the different types of Line Coding Adopted in PCM technology?

CHAPTER 2

TYPES OF MUX EQUIPMENT

2.1 Primary MUX Equipment

The 30 channel PCM multiplexing equipment provides multiplexing of speech, signalling and teleprinter (optional) information for multi channel junction communications in the Intra City Exchange Networks. This equipment is capable of working with associated line equipment using the existing junction cables with loading coils removed. This equipment increases the capacity of the existing junction cables and also improves the transmission quality.

The 30 channel PCM multiplexing equipment has been designed to convert speech and signalling information at the transmit end of 30 channels (channel can be voice or data at 64 kbps or aggregate of low-speed data channels < 64 kbps) into a single digital output bit stream 0f 2048 K bits/sec. At the receiving end all the original information will be extracted by proper demultiplexing operations from the incoming digital bit stream. This system provides the local / trunk exchanges with various signalling capabilities for different types of exchange equipment.

The performance of 30 channel PCM multiplexing equipment confirms to the **ITU (T)** Recommendations **G 703, G 711, G 712 and G 732.**

In primary MUX, there are two varieties:

1. Non-programmable terminal type
2. Programmable drop-insert type

2.1.1Non-programmable terminal type MUX

Non-programmable terminal type MUX has processor card, framer or PCM interface card and voice/data interface cards, power supply card. 2 Mbps aggregate interface is available with balanced (120 Ohm) and unbalanced (75 Ohm co-axial) interface for connecting to higher order MUX or transmission equipment respectively.

In this MUX, mapping of time-slots is fixed. Dropping and inserting of channels cannot be done at time-slot level. This can be done by VF patching only.

Nowadays, all Primary MUXes being used are Programmable Drop-Insert MUXes only.

2.1.2 Drop Insert Mux:

Please refer fig.2.1. Drop-Insert MUX has two aggregate 2048 kbps links. Each link has transmit and receive paths. The 30 channels on the channel side can be mapped to either of the two aggregate links. Also mapping of channels from one aggregate link to the other aggregate link is possible.

These mapping functions are otherwise known as “Cross Connections”.

Functions:

- Channel Side : It should handle
  a) Analog channels (normally voice)
  b) Digital channels (normally data)
- Aggregate Side: It should interface with two digital 2048 kbps links.
- Cross Connect: It should be capable of connecting any channel on the channel side to any channel on any of the two aggregate links.

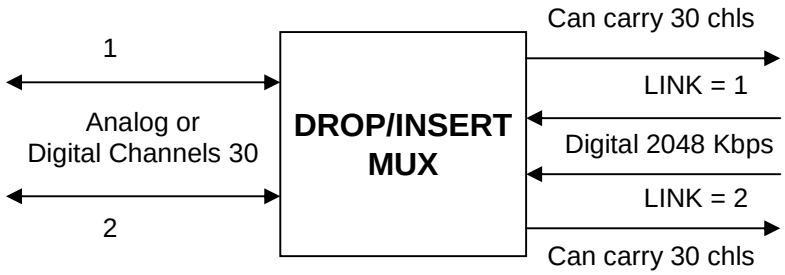


Fig. 2.1 Drop & Insert Mux

Drop-insert MUXes of three different makes viz., PCL's V-MUX, Webfil's Flexi-MUX and Nokia MUX are explained in detail in the notes T-13C

2.2 Skip MUX

Skip MUX or 2/34 MUX multiplexes 4 E1s to E2 and 4 E2s to E3 (34.368 Mbps). Since outside access is not provided at E2 or 8.448 Mbps level, it is called Skip-MUX.
Please refer fig.2.2

Fig.2.2 Skip Mux

2.3 Trans Mux:

Trans MUX is used for converting analog voice channels of 312 – 552 (one super group) into PCM 2048 Kbps and vice versa.

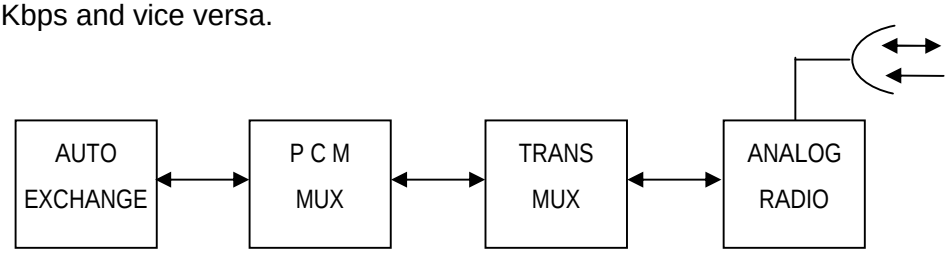


Fig.2.3 Trans Mux

In other words "Trans MUX" is an interface between analog and digital systems.

2.4 Working of PCM MUX in conjunction with Digital Radio and OFC Systems

On Indian Railways, we have E3 (34.368 Mbps) Digital MW Radio links. These radio equipment also have WS(Way-side) port for interfacing E1 directly so that long haul E3 traffic is not disturbed for dropping/inserting channels on short-haul, which is done through E1. Connection of PCM Mux to WS port of Digital Radio is shown in fig. 2.4

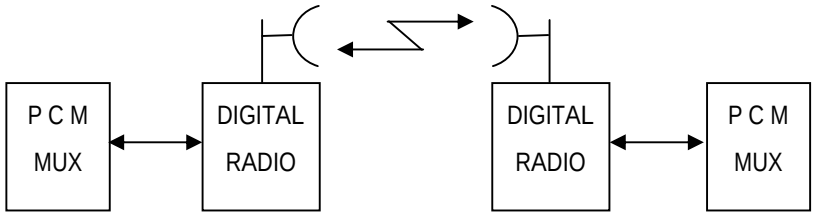


Fig.2.4 Connection of PCM Mux to WS port of Digital Radio

In case of E3 (34.368 Mbps) traffic, 16 PCMs provide the 16 E1s to 2/34 equipment, which interfaces with Digital Radio. The arrangement at terminal station is shown in fig.2.5(a).

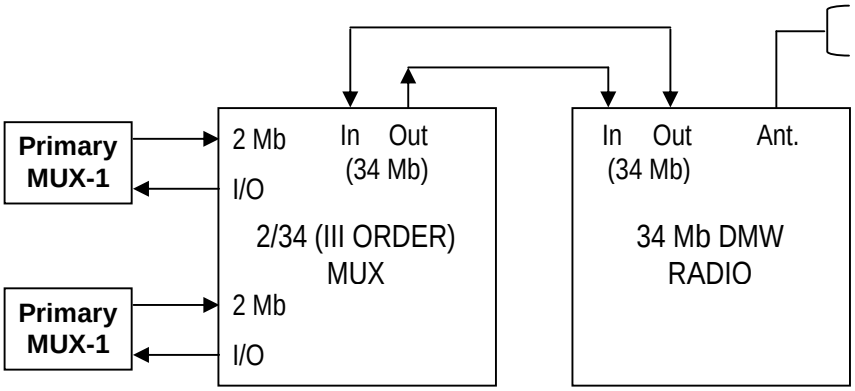


Fig. 2.5 (a) Interconnections of equipment at terminal station.

The arrangement at stations (repeaters) without channels/tributaries dropping from E3 traffic is shown in fig. 2.5(b).

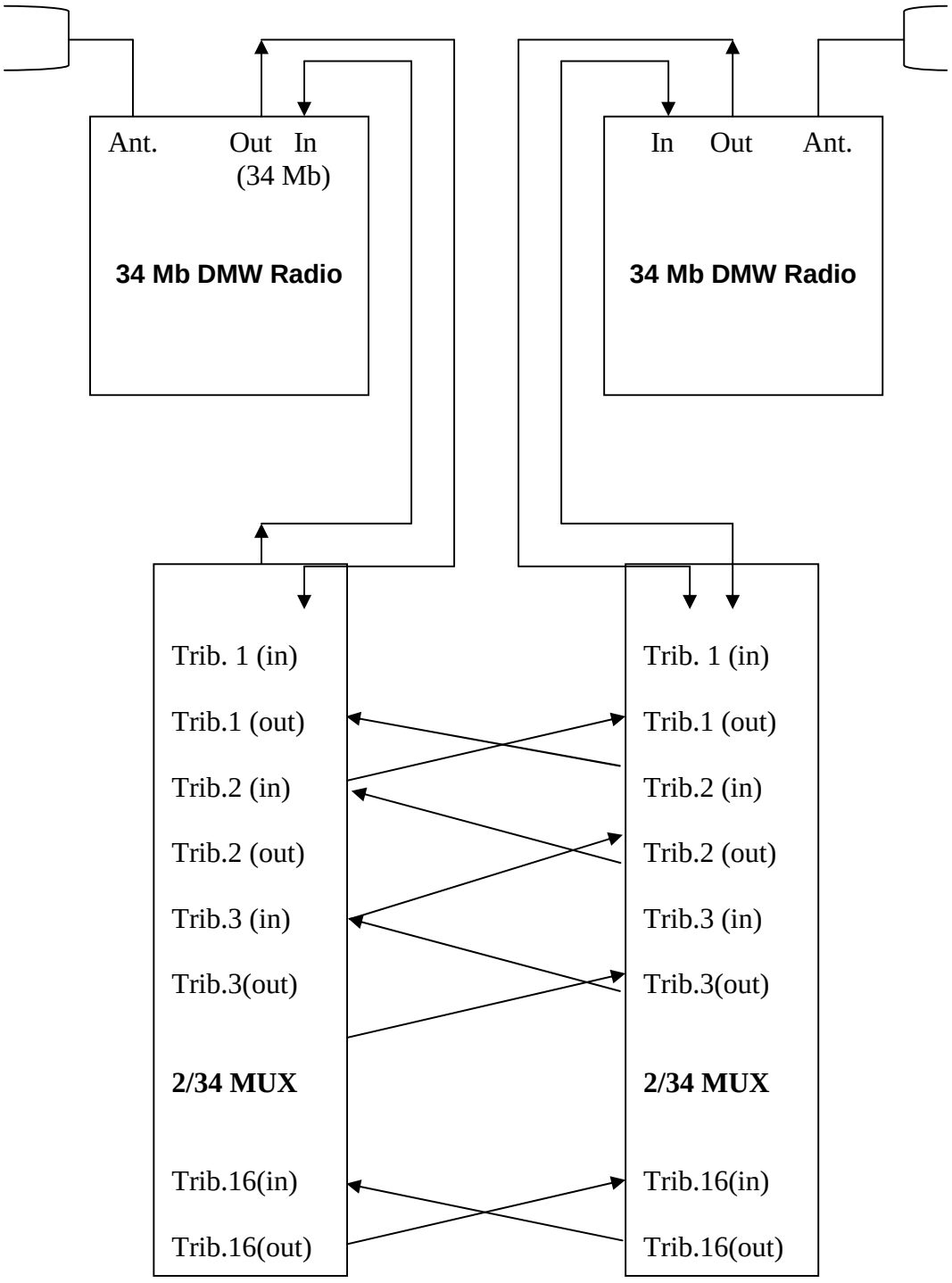


Fig. 2.5 (b) Interconnection of equipment at repeater station without channel dropping (tributary in/out connections cross-patched for all tributaries.)

The arrangement at stations (repeaters) where channels / tributaries are not dropped from E3 traffic is shown in fig. 2.5(c)

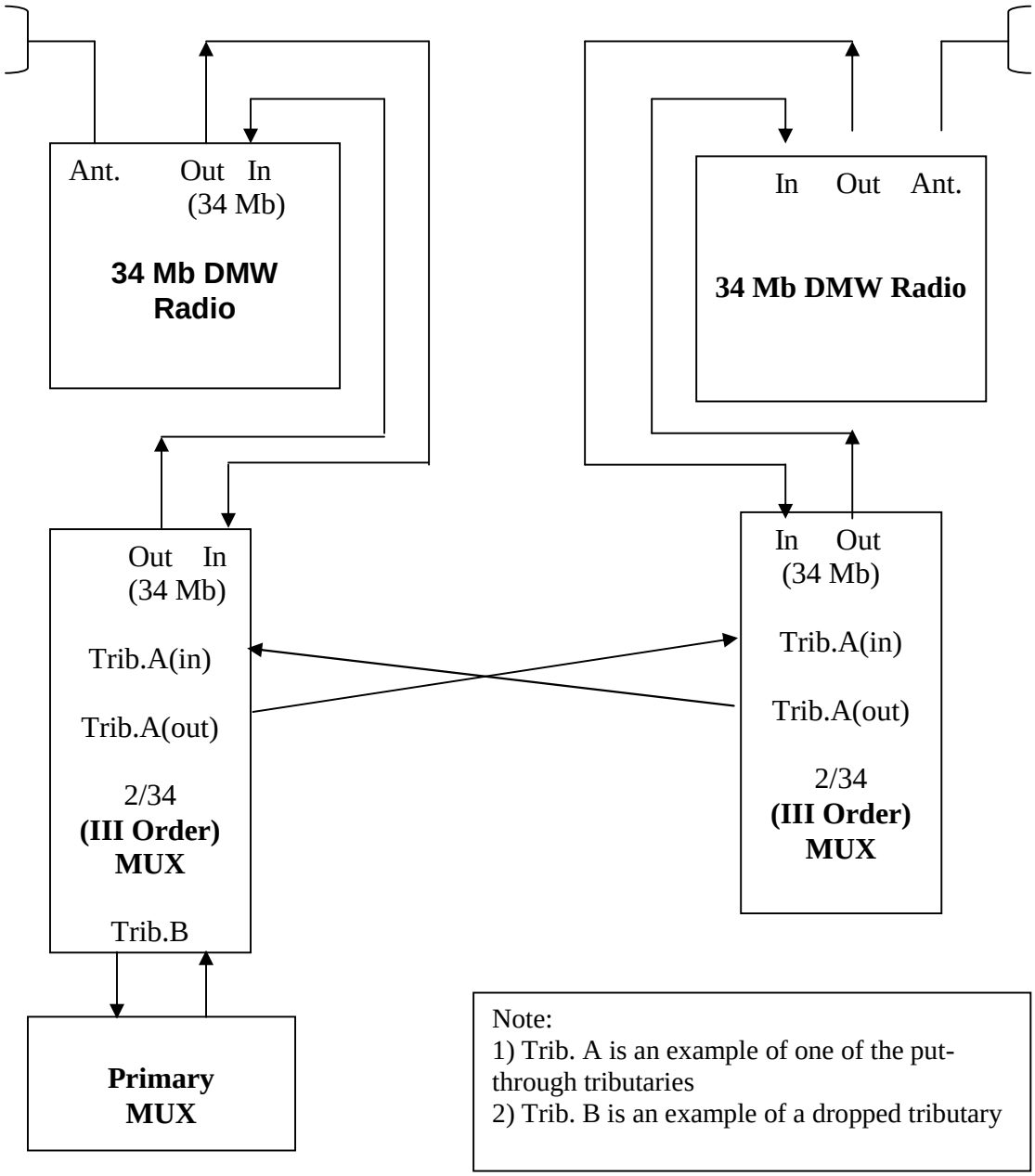


Fig.5.1(c) Interconnection of equipment at repeater station with channel dropping from E3 traffic

In case of PDH links on OFC, OLTE (Optical Line Terminating Equipment) is the transmission equipment. OLTEs of various transmission rates (2Mbps/8Mbps/34 Mbps/140 Mbps) are available. On Indian Railways, PDH links on OFC up to 34 Mbps were operational, but replaced with SDH links.

In case of SDH links, one STM-1 equipment supports 63 E1s. Each E1 interfaces with one Primary Drop Insert MUX to provide 30 VF/data channels' interface.

Objective:

Multiple Choices:

1. PCM mux equipments confirms to ITU(T) recommendation
   a) G703,
   b) G711,
   c) G712
   d) all the above

2. Primary mux comes in configuration
   a) Programmable
   b) Non programmable
   c) Drop Insert
   d) All the above

3. In Non programmable mux the time slots are
   a) Fixed
   b) Can be changed
   c) Dynamic
   d) All the above

4. Skip mux incorporate ---------- E1 channels in Input side
   a) 16
   b) 18
   c) 12
   d) All the above

5. Trans Mux convert one super group into ----------and vice versa
   a) 2048 Kbps
   b) 64 Kbps
   c) 16 Kbps
   d) None of the above

Fill in the Blanks:

1) OLTE Stands for _____

2) Railways had earlier used PDH links on OFC up to a speed of _____Mbps.

3) Digital Microwave of Indian Railways supports a speed up to_____ Mbps.

Subjective:

1. Write the different types of Multiplexing Equipment used in Indian Railways?
2. Draw the Block diagram showing the interconnection of PCM mux with OFC equipments on 2 Mb/s level?
3. Draw the Block diagram showing the interconnection of PCM mux with 34 Mb/s Digital Radio equipments?
4. Write short notes on Trans Mux and show the interconnection with 34 Mb/s Digital Radio equipments?
5. Write short notes on Skip Mux. Why do we require Skip Mux ?
6. Write short notes
   a. Drop Insert Mux.
   b. Non programmable Mux
   c. Programmable Mux.
7. What are difference between Non programmable Mux and Programmable Mux? Which one has more advantages?

CHAPTER 3

PLESIOCHRONOUS DIGITAL MULTIPLEXING (PDH)

3.1 Digital Multiplexing Hierarchies:

The ITU-T recommendation G.701, definition 4003, defines a digital multiplex hierarchy as a series of digital multiplexers (MULDEXes) graded according to the capability so that multiplexing at one level combines a defined number of digital signals, each having the digit rate prescribed for a lower order, into a digital signal having prescribed digit rate which is then available for further combination with other digital signals of the same rate in a digital multiplexer of the next higher order.

In digital multiplexing hierarchies, there are 3 generations:

1. Plesiochronous Digital Hierarchy (PDH)
2. Synchronous Digital Hierarchy (SDH)
3. Optical Transport Hierarchy (OTH)

In Plesiochronous digital hierarchy, at each hierarchical level, digital streams nominally at the same clock-rate but with the range of variation within a certain specified limits are multiplexed to form digital stream of next hierarchical level. This will be studied in this chapter. PDH transmission is used on Digital MW Radio networks as well as OFC networks. However, PDH links on OFC are being replaced with SDH links.

In synchronous digital hierarchy, at each hierarchical level, synchronous transport module is formed with information pay-load and overhead bits and a synchronizing mechanism is in-built to ensure all network elements work to a master clock reference. In this hierarchy, the data rate of next stage is exact multiple of previous stage data rate. SDH transmission is used on OFC links and in a very limited way on Digital Radios (Such radio equipment work over short ranges of up to 10 km and not used on long-haul networks with several nodes).

In optical transport hierarchy, optical data units and then optical transport units are formed as data frames. Such units are transported on every wavelength of the Wave Division Multiplexing (WDM) plan on optical fiber.

In PDH, two systems are recommended in ITU-T recommendation G.702, based on different first level bit rates 2048 Kbps & 1544 Kbps. The internationally agreed maximum level is level 4 for international interconnections. Levels higher than this are not mentioned in the recommendation. Annexure B to recommendation G.954, however, gives the digital multiplexing strategy for a 4 X 139264 Kb/s = 564992 Kb/s system.

3.1.1 Japanese System

Please refer fig. 4.1(a). This hierarchy is based on first level bit rate of 1544 kbps (T system). As per ITU-T recommendation G.702, the second level bit stream is 6312 kbps with 96 speech channels, third level may be split in to two bit streams **either** 44736 kbps the highest level for that stream with 672 speech channels **or** 32460 kbps with 360 speech channels. The 32460 kbps stream can be further multiplexed to level 4 with a resultant bit stream of 97728 kbps and 1440 speech channels. Japanese hierarchy extends this by another level with a bit stream of 400352 kbps and 5760 speech channels as level 5.

3.1.2 European system

Please refer fig.3.1 (b). This is based on first level bit rate of 2048 kbps (E system). As per ITU-T recommendation G.702, the second level bit stream is 8448 kbps with 120 speech channels, third level is 34368 kbps stream with 480 speech channels, fourth level is 139264 kbps stream with 1920 speech channels and fifth level is kbps stream with 7680 speech channels.

3.1.3 North American System

Please refer fig. 3.2. This is based on first level bit rate of 1544 kbps (T system). As per ITU-T recommendation G.702, the second level bit stream is 6312 kbps with 96 speech channels, third level is 44736 kbps stream with 672 speech channels. The North American hierarchy also adopted by Canada uses Bell (AT & T) developed system, which goes two levels higher, level 4 with 274176 kbps & 4032 speech channels, level 5 with 560160 kbps & 8064 speech channels. This system is able to accept a master group FDM assembly directly into level 3 as an additional feature.

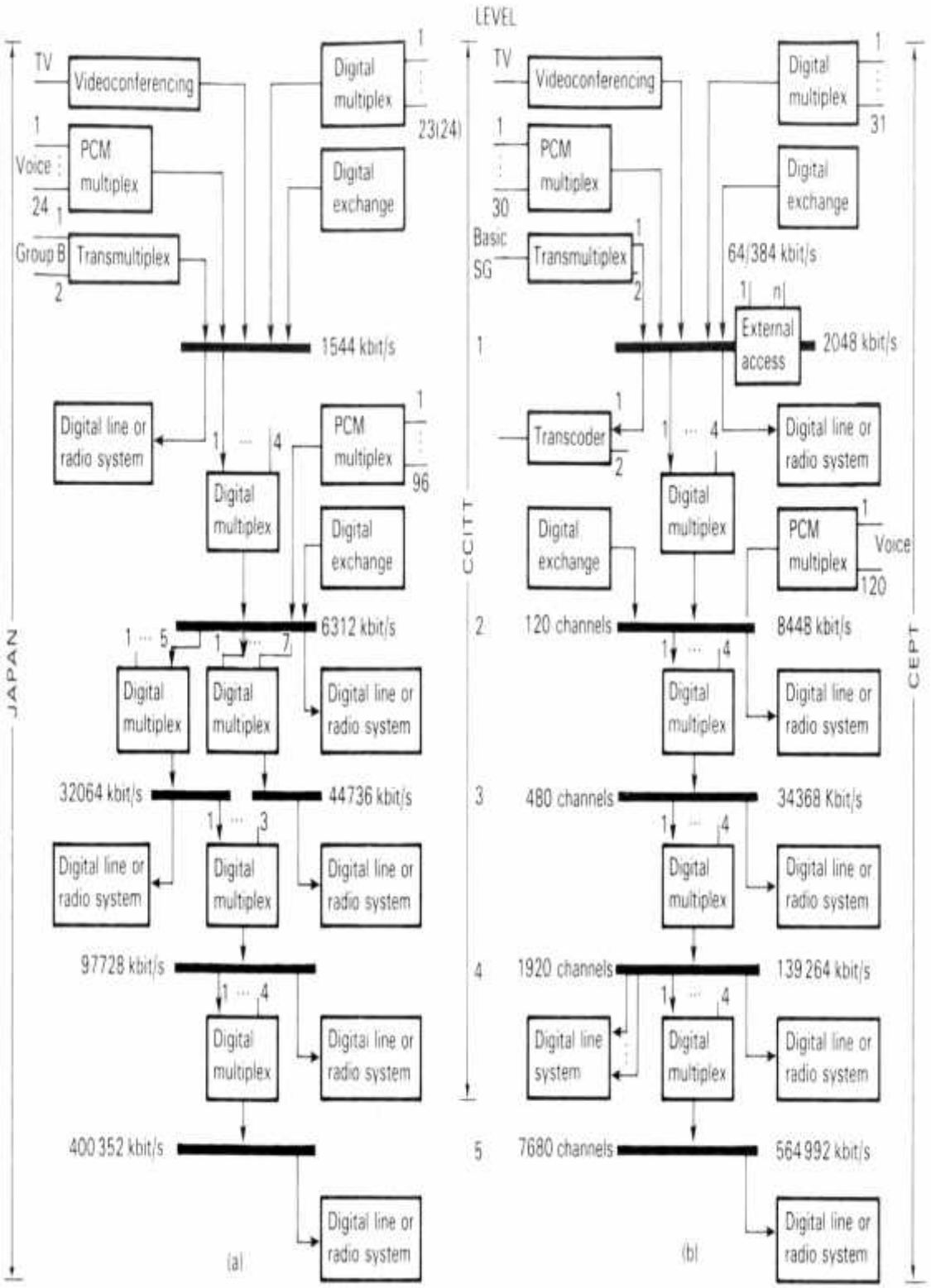


Fig.3.1 a & b ITU-T hierarchical bit rates for networks with the digital hierarchy based on primary level bit rate.

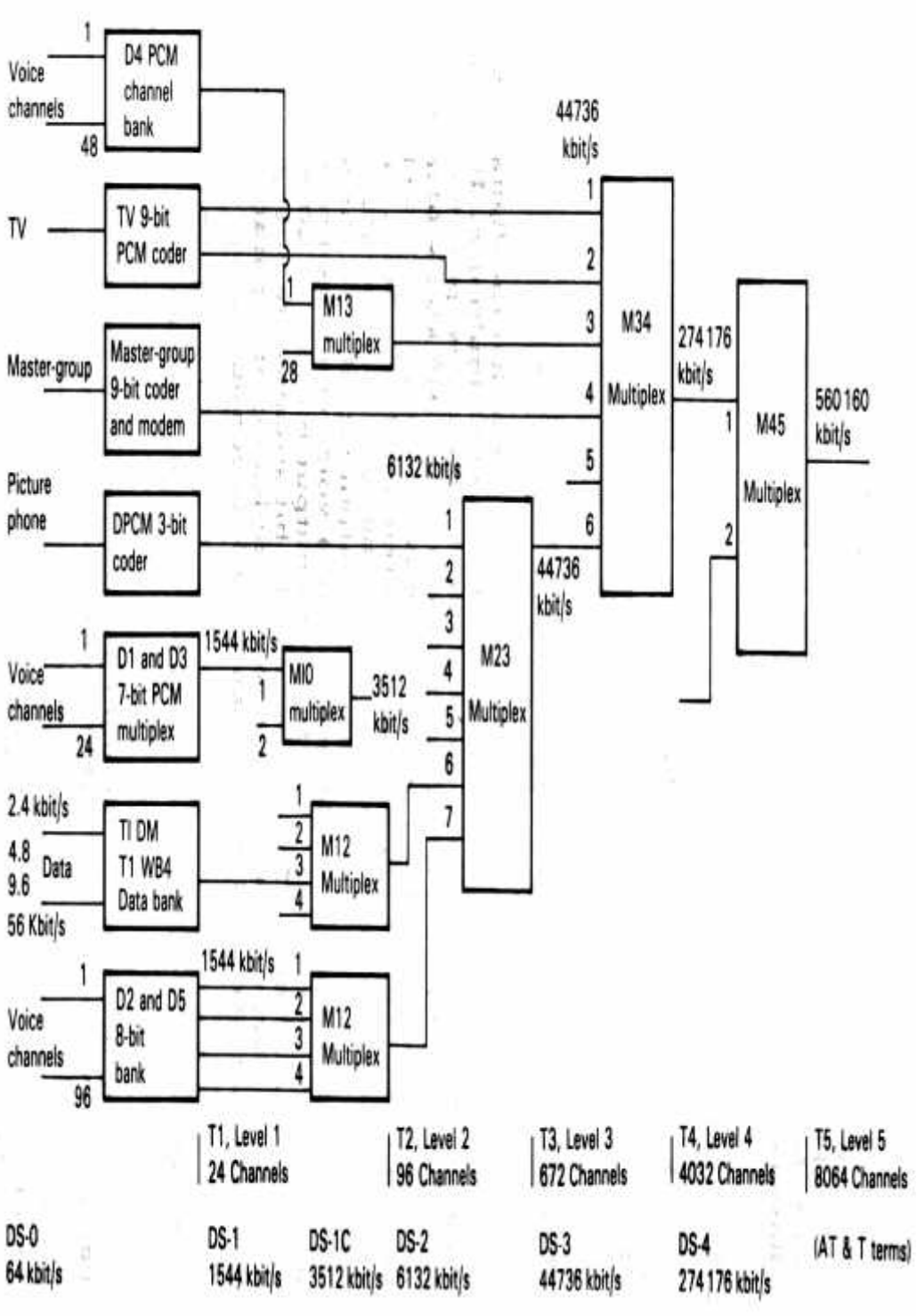


Fig.3.2 North American digital hierarchy

3.2 PCM Hierarchy Adopted In India:

Please refer fig.3.3. India adopts E System basing on first level bit stream of 2048 kbps which can go up to fifth level bit stream of 564992 kbps & 7680 speech channels. The multiplexing of different orders is discussed in the following paragraphs.

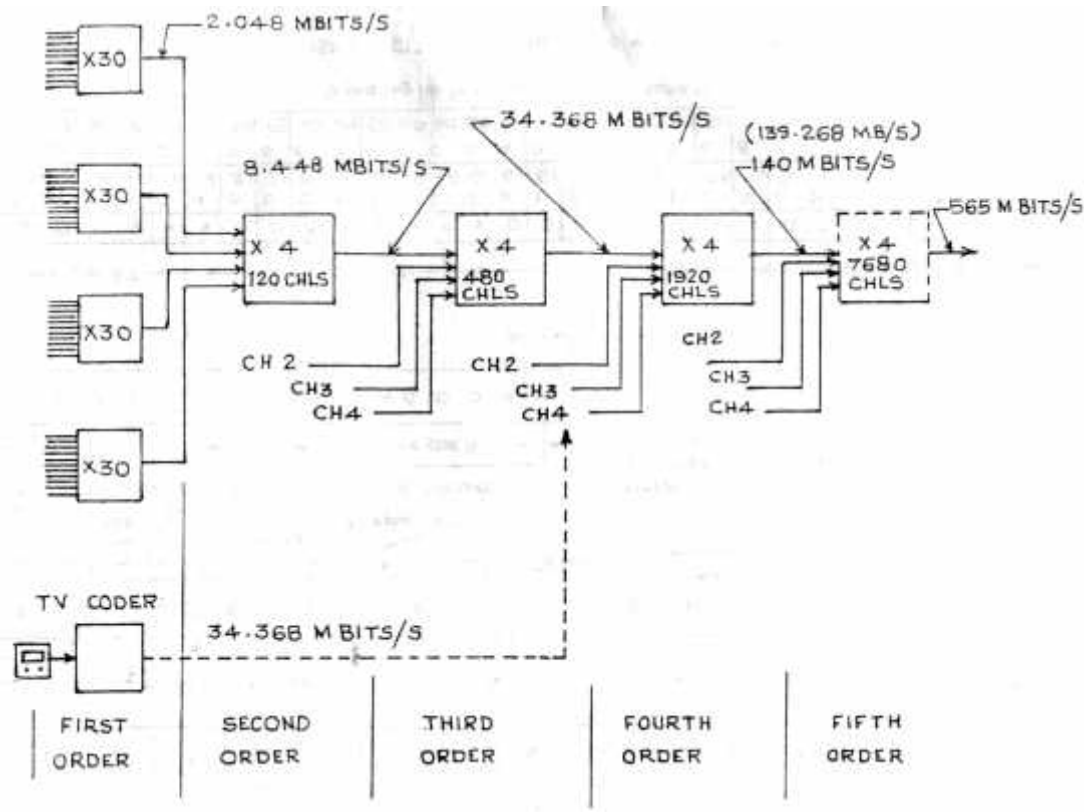


Fig. 3.3. PCM Hierarchy adopted in India

3.3 Basics of PDH Multiplexing

PDH multiplexing from II order onwards involves two basic operations irrespective of hierarchical level. These are : Bit interleaving and Justification.

Bit-interleaving

A digital multiplexer can be considered as a parallel to serial converter. It accepts a set of inputs (or messages often called as tributaries) applied in parallel and interlaces the inputs in to a single output signal having specific time intervals allocated to each message serially.

In 30 channel PCM, the signal E1 is formed by byte interleaving. But in higher order multiplexing, i.e. forming E2 out of 4 E1s or E3 out of 4 E2s or E4 out of 4 E3s, multiplexed signal is formed by bit-interleaving. In bit-interleaved multiplexing, one bit is taken at a time from each tributary to produce a multiplexed signal.

Four incoming tributaries are shown in fig.3.4(a) and multiplexed signal formed by bit-interleaving is shown in fig.3.4(b)

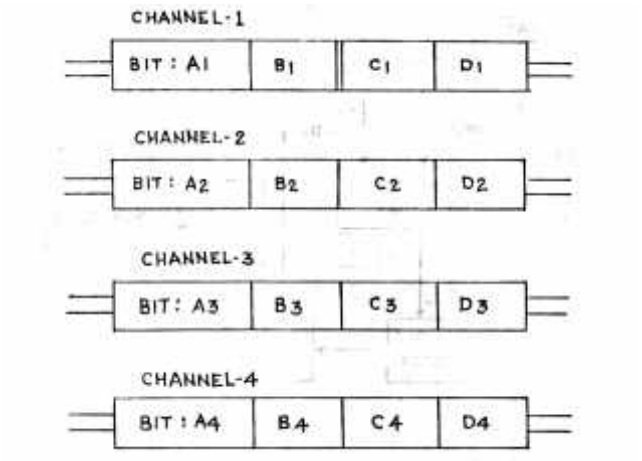


Fig.3.4 (a) Incoming tributaries

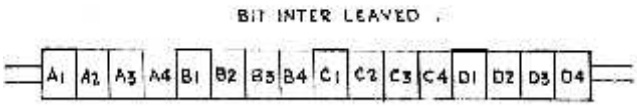


Fig.3.4(b) Multiplexed signal formed by Bit-interleaving

Justification

In PDH, we are multiplexing tributaries whose clock can vary independent of one another, but the range of variation is restricted within a certain specified limits. Multiplexing of such tributaries involves a more complex process known as Justification, in which different tributary bit rates are permitted to be properly related to the multiplex equipment clock.

Consider the case as shown in Fig.3.5, of one input tributary signal entering its corresponding channel in the multiplexer. The multiplexer clock is running slightly faster than the incoming signal, and there will be periodically a surplus time slot in the transmitted signal that will contain either repetition of one of the incoming digits, or a random digit. Either way there will be a digital error at the system output. The idea behind the Justification, or pulse shifting systems is to identify the time slots containing these errors, transmit to the receiving terminals, the information on them and arrange for their deletion from the received signal. Justification can be considered as the process of changing the digit rate of a digital signal in a controlled manner so that it can accord with a digit rate different from its own inherent rate, usually without loss of information (ITU-T definition 4022, in recommendation G.702.)

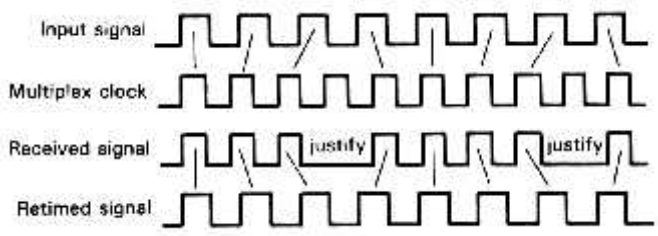


Fig.3.5 Positive Pulse Stuffing Or Positive Justification

Positive Justification:

Let the bit rate at the output of the multiplexer be F Kb/s. and the input data stream be f Kb/s. In a positive justification system, the multiplexer output bit rate F is made higher than the sum of the maximum bit rates of the input tributaries, i.e.,

$$F > 4f \qquad (4.1)$$

ITU-T systems and most practical multiplex systems restrict justification operations to a pre assigned time slots in order to simplify the system design. With this pre assigned, range the allowable range of digit for the tributary inputs can be made according to the equation (4.2).

$$4f_{max} - 4f_{min} = 4j \qquad (4.2)$$

Where as “j” is the number of justifiable time slots/sec/tributary.

In a positive justification system such as that shown in fig. 3.5, the time slots in the outgoing multiplex signal will become available at a rate exceeding that of the total incoming data bit rates as given by equation 4.2. As this represents a bit rate difference, or a frequency difference between output (or multiplexed clock frequency) and input signals, it may represented as a phase change per unit time of one of the signals with respect to the other. If the reference signal is considered to be the multiplex clock signal, the input signal will be continuously shifting against this reference. This shift will continue until such time as the system decides that it has gone far enough and justification is required. At this point a message is sent to the receiving terminal by means of justification service digits, informing it that the next time slot will be justified. On receipt of this information and the justified signal, the receive terminal deletes the next justifiable time slot from the signal and the original input tributary is restored.

To overcome the problems of transmission channel errors effecting the transmitted justification service digit, and causing a false deletion or a spurious insertion of information in a time slot at receive end, which in turn would cause an error and possibly loss of frame alignment, the justification service digits are transmitted in triplicate. The code 111 is for positive justification, and 000 for no justification. On corruption of one of these 3 digits, the majority of the bits in the code produce the decision. That is if 110 is received it will be interpreted as 111, but if 100 is received, it is interpreted as 000 and no justification will result.

Please refer fig.3.6 showing positive justification process in II order multiplexing. Consider one of the 4 tributaries which may enter in to this multiplex equipment and let it be input number 1. The level 1 bit stream (2048 kbps) entering the input is detected by the phase locked loop which extracts the timing information “f” from the bit stream and permits the bit stream to be entered into the buffer store, or elastic store. The stored bits are read out from the elastic store with the timing of the internal clock whose frequency is the multiplex clock frequency (F) divided by 4. This frequency (F/4) is slightly higher than the external clock frequency (f)., since it has to accommodate, in the multiplex output frame structure, the

justification control bits, justification bit and frame alignment signal etc., i.e., all overhead bits. As a result of this the reading of the pulses would appear to occur at a faster rate than the rate at which the pulses are stored, resulting in a gradual reduction of the stored bits in the elastic store. This is not quite so, for the read pulse is effectively muted by the positions where the overhead bits would occur, and thus another input pulse during this muting period is read into the store. The threshold detector supervises this, and when the number of stored bits is reduced to a pre determined value by the remaining difference in frequency

Of the two clocks after the read muting has been taken into account, the threshold detector informs the stuffing control to inhibit reading, as a result, as a result bits with zero state are stuffed into designated time slots known as "justifiable digit time slots" contained in the digit stream, to make up the differences in the clock frequency.

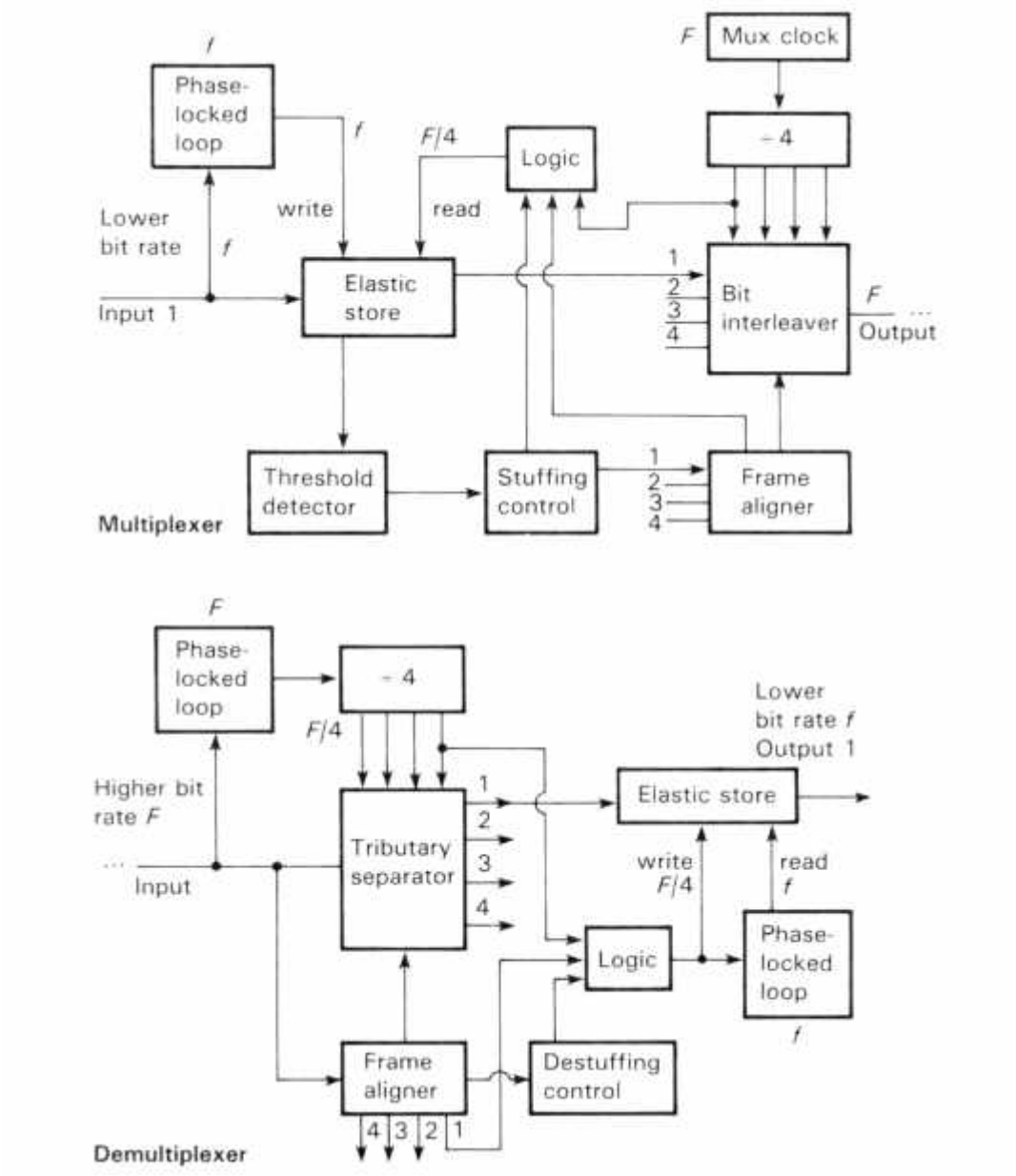


Fig.3.6 Block Diagram Concepts Of Positive Justification Or Positive Pulse Stuffing In II Order Multiplex System

If the store is filling or is filled when a fixed justifiable time slot occurs, the time slot is used. If the store is near empty, the time slot is ignored. Information concerning the status of the bits of the bits (that is justification or no justification) is also inserted in to pre determined time slots in the digital bit stream together with the other service bits and transmitted to the remote end. At the receiving end another elastic store is provided.

Writing into this store is inhibited by the de stuffing control at the justified positions in order to remove the null bits inserted during stuffing or justification.

As the removal of justifications causes an abrupt change in the receiving clock, a second phase locked loop is provided for smoothing and reading out the pulses in the elastic store. This phase locked loop also has been designed to permit proper operation over the required range of variations in the digit rates. ITU-T recommendations G.742 provides the details of second order digital multiplex equipment operating at 8448 kbps respectively using positive justification. ITU-T recommendations G.751 provides the details of third order and fourth order digital multiplex equipment operating at 34368 kbps and 139264 kbps respectively.

We shall now examine II, III and IV order multiplexing in PDH based on E-Hierarchy (2048 kbps)

3.4 II-Order Digital MUX

Integration of four 2 Mbps (2.048 Mbps) tributaries to an 8.448 Mbps stream in II-order digital MUX and the retrieval of tributaries are discussed in this section.

Refer to Fig. 3.7(a). An 8.448 Mbps clock is divided by four to supply a 2.112 Mbps clock for all the four tributaries. Each 2.112 Mbps clock is made out-of-phase by a quarter with respect to the previous one. These clock signals are used for reading data out of the 8-bit buffer memory. Only one channel is shown in the figure 3.7.

Frame structure of E2 (8.448 Mbps signal) is shown in fig.3.7(b).

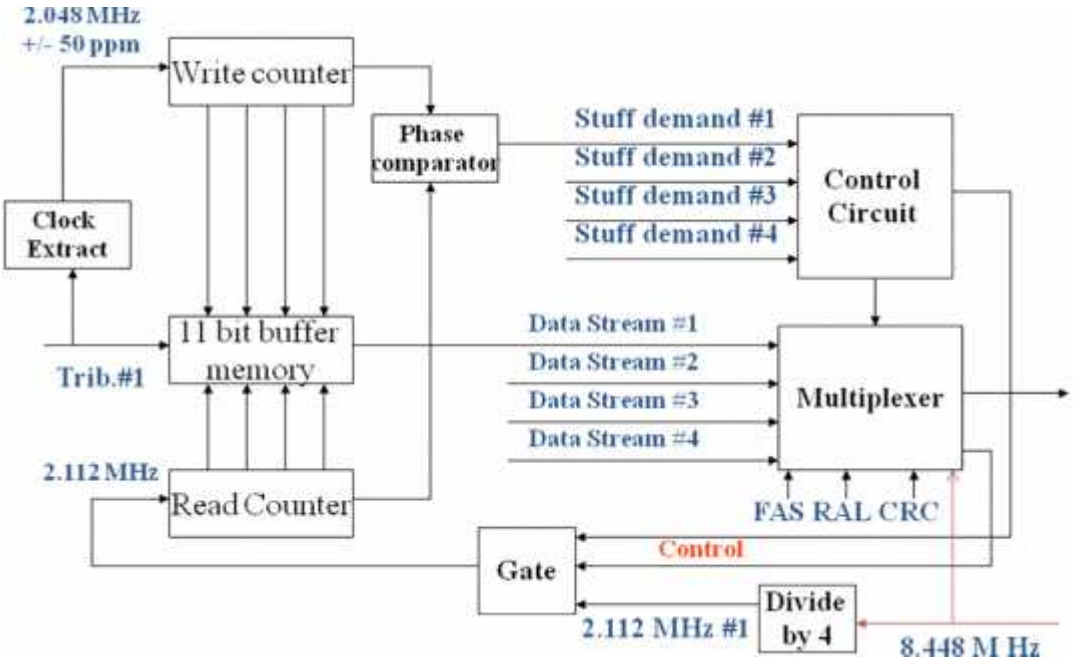
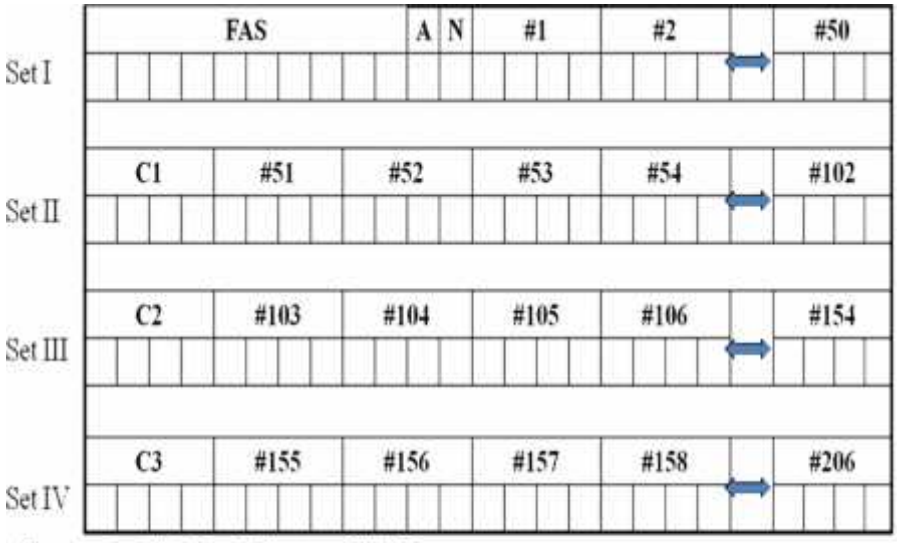


Fig.3.7(a) Block diagram of II order multiplexing

A gate through which the 2112 kHz clock signal passes is controlled by a multiplexer and a stuffing circuit. When overhead bits such as frame alignment signal, remote alarm bit, future use bit, justification control bit, and justification bit are inserted into the 8 Mb data stream, the pulses corresponding to these bits in the 2112 kHz clock signal are stopped. This results in an interrupted 2112 kHz clock, and is designated as the 2 Mb transmit read clock. Because the outputs of both transmit read counter and transmit write counter are compared, the 2 Mb transmit read clock has the same nominal information rate as the incoming data.

The 11-bit buffer memory is assigned to each 2 Mb tributary. The tributary data is called "2Mb data" and is written into the 11-bit buffer memory with a 2 Mb transmit write clock (2048 kHz ± 50ppm) that is extracted from the same tributary data. The information is loaded and unloaded at different rates. The loading (writing) rate is constant while the unloading (reading) rate, even though it has a higher bit rate than the loading rate, is interrupted.

The 2 Mb transmit write clock and 2 Mb interrupted read clock have a relatively low accuracy (30 ppm for read clock). In order to compensate for these variations, a phase comparator with a set threshold is used to detect the phase difference between the two clocks. Once the phase difference reaches the set threshold, the read clock is close to re-reading a previous bit. To avoid this, the phase comparator sends a stuff demand signal to the stuffing circuit when the phase difference reaches a set threshold. Upon its reception, the stuffing circuits sends "111" as the justification control bits (JCB) of the following frame. After the JCBs are sent, the stuffing circuit controls the rate so as to stop the 2112 kHz clock pulse for the time-slot # 155 (TS-155) of that tributary. It may be noted from Fig. 12.4 that each time-slot carries four bits---one bit for each tributary. TS-155 has data if the JCBs are 000, and justification bit if JCBs are 111. This rule applies to each bit of TS-155 as per JCBs of the corresponding tributary.



Frame size: 212 Bits X 4 sets = 848 Bits

FAS: Frame Alignment Signal (1111010000) A: Remote Alarm (1-Alarm) N: Resvd

#1 to #206 (excl #155): Each a set of 4 bits; 1 bit from each Tributary

C1 to C3: Justification Control bits (1st bit of each for Trib.1 etc. – 111 > Justification)

#155: Justification Bits of each tributary

Fig.3.7(b) Frame structure of E2 (8.448 Mbps signal)

Retrieval of tributaries

Refer to Fig. 3.7(c). The demultiplexer locates the synchronization word in the incoming 8Mbps signal, recovers the 8.448 Mbps clock, and converts the input signal into four parallel streams of 2.112 Mbps each. The 2.112 Mbps data stream is written into an elastic store with the help of a write clock at 2.112 MHz (Rx clock/4).

The write clock is a 2.112 MHz perforated clock. The perforations are made at specific durations corresponding to FAS bit position, JC and justification bit slots. Since the clock is interrupted, the data is effectively written into the elastic store at a nominal rate of 2.048 Mbps even though the input to the elastic store is at a higher rate.

It may please be noted that the operation done here is the reverse of what was done at the multiplexer. In the multiplexer, data was read from the elastic store by providing perforations in the read clock.

The read clock for the elastic store is obtained from a 2.048 MHz VCXO which is phase-locked to the 2.112 MHz clock. The data can then be taken to the 2 Mbps interface for HDB-3 coding and onward transmission.

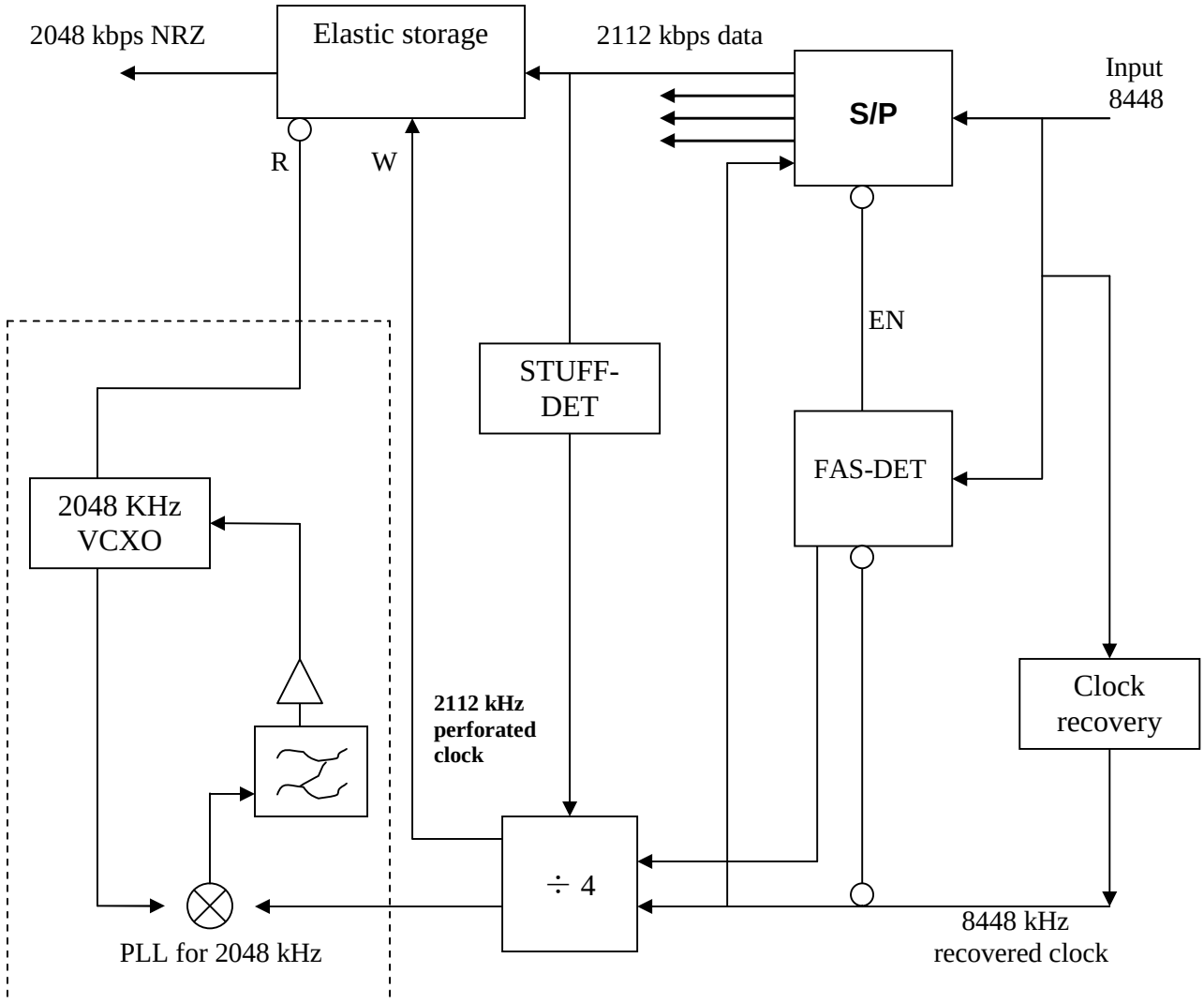


Fig. 3.7(c) Retrieval of tributaries in II- order MUX.

3.5 III-Order Digital MUX

Block diagram of III order digital MUX is shown in fig. 3.8(a) and E3 (34.368 Mbps) frame structure is shown in fig.3.8(b). Each frame has 1536 bits. Incoming tributaries are at 8.448 Mbps rate.

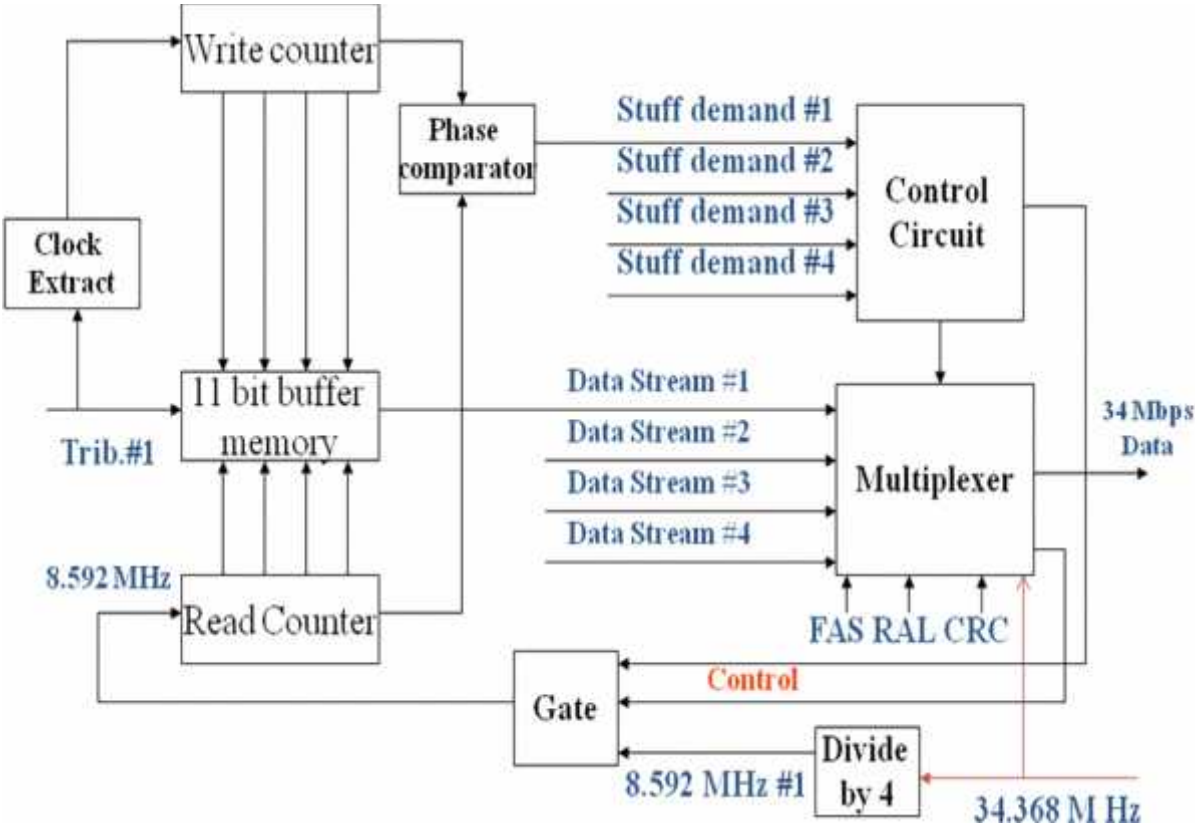


Fig.3.8(a) III Order Multiplexing Block diagram

Bit stream integration process is similar to that in II-order MUX. Only the frame size and clock rates are different. The data read in clock is 8.592 MHz. Incoming data is at 8.448 Mbps ± 30 ppm. Each frame has 378 time-slots with 4 bits per slot; FAS and service digits are the first twelve bits of a frame; justification bits are in TS-284.

It may be noted that TS-284 is also used for remote loopback at 8 Mb level (other than data and justification bits). If JC1, JC2 and JC3, are 000; the bit in TS-284 carries data; if they are 111, the bit in TS-284 carries remote loopback information. A ‘0’ indicates request for loopback and a ‘1’ indicates no request.

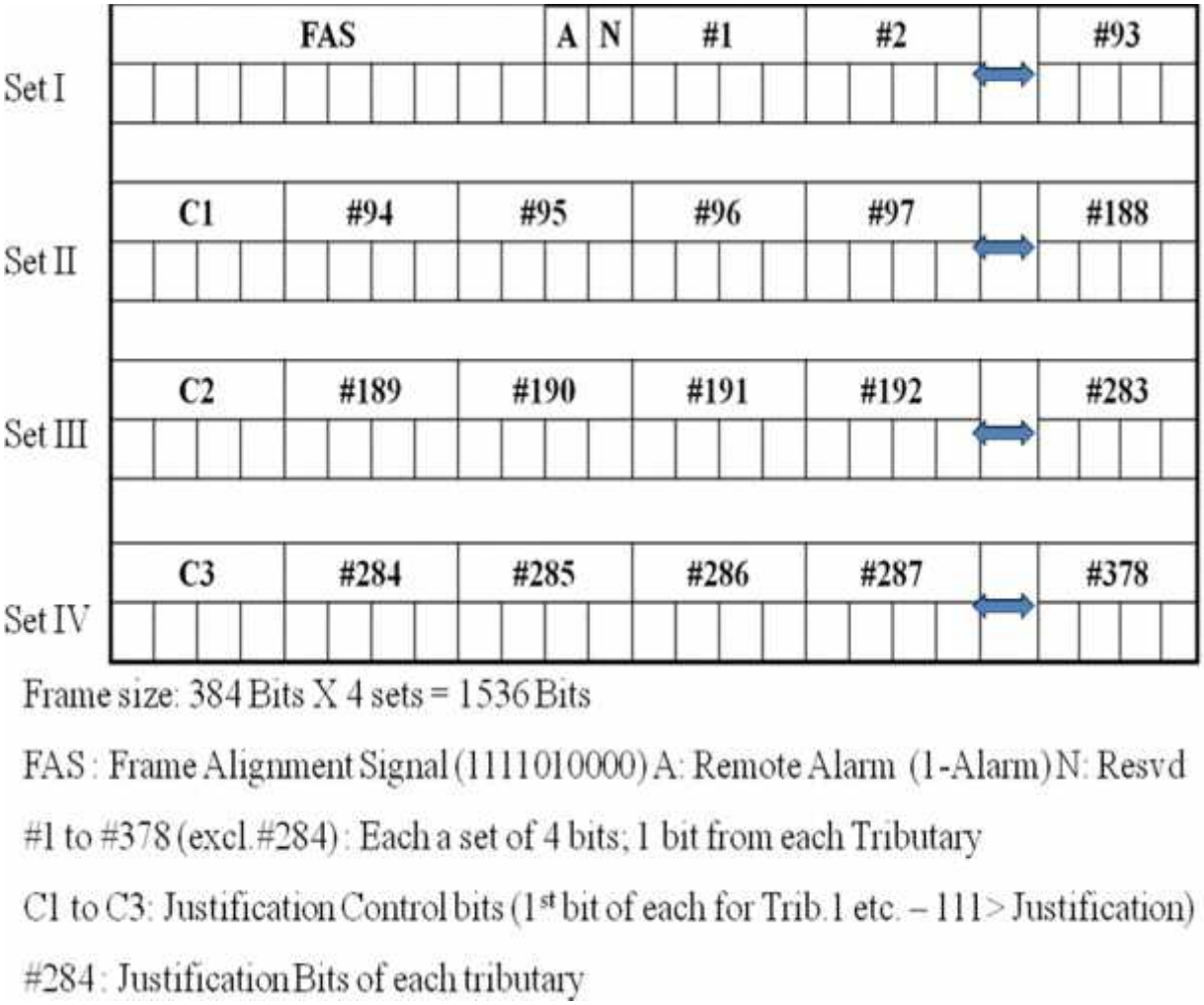


Fig.3.8(b) Frame structure of E3 (34.368 Mbps) signal

Retrieval of tributaries

Refer to Fig. 3.8(c). The demultiplexer locates the synchronization word in the incoming 34.368 Mbps signal, recovers the 34.368 Mbps clock, and converts the input signal into four parallel streams of 8.592 Mbps each. The 8.592 Mbps data stream is written into an elastic store with the help of a write clock at 8.592 MHz (Rx clock/4).

The write clock is a 8.592 MHz perforated clock. The perforations are made at specific durations corresponding to FAS bit position, JC and justification bit slots. Since the clock is interrupted, the data is effectively written into the elastic store at a nominal rate of 8.448 Mbps even though the input to the elastic store is at a higher rate.

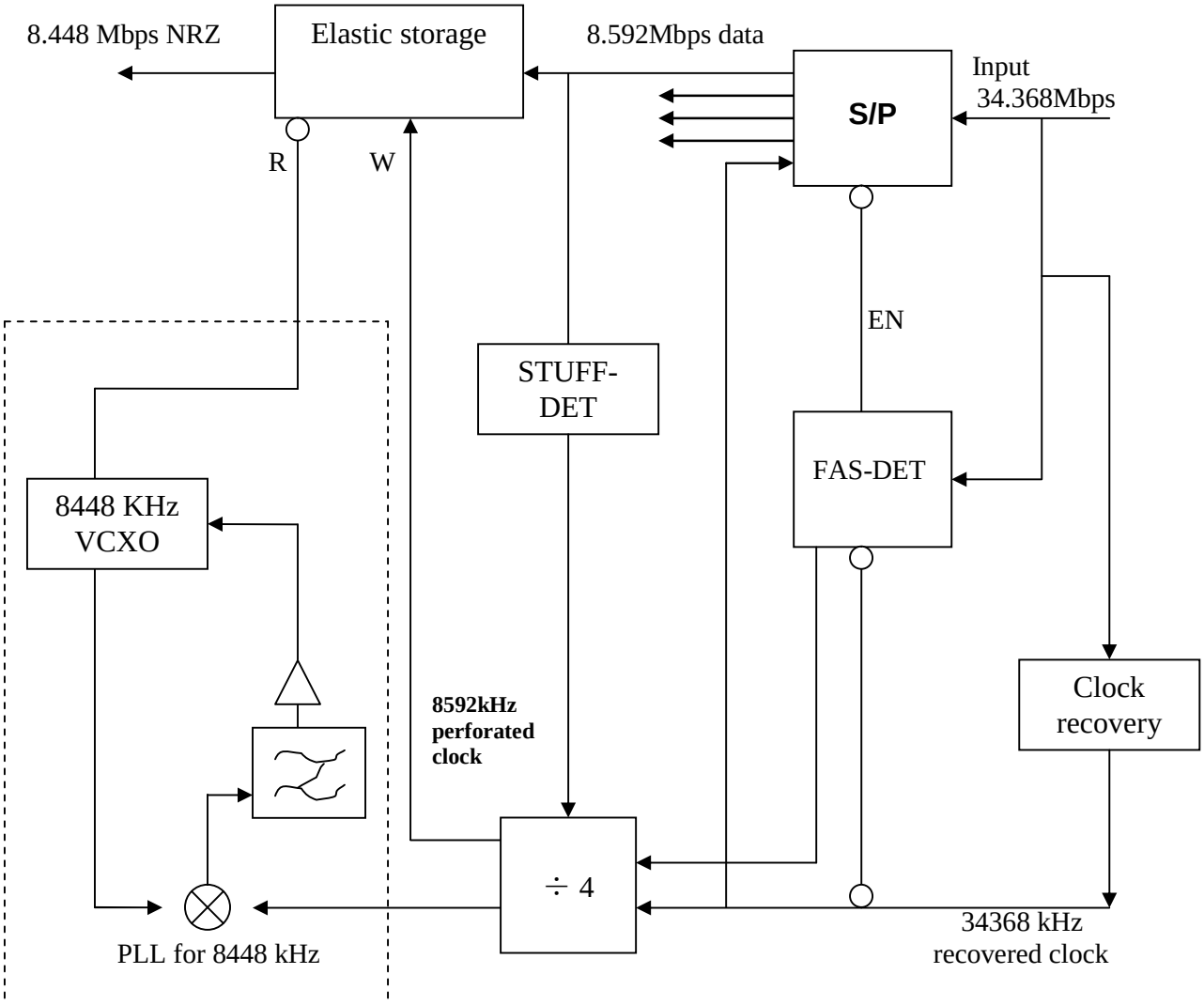


Fig. 3.8(c) Retrieval of tributaries in III order MUX.

It may please be noted that the operation done here is the reverse of what was done at the multiplexer. In the multiplexer, data was read from the elastic store by providing perforations in the read clock.

The read clock for the elastic store is obtained from a 8.448 MHz VCXO which is phase-locked to the 8.592 MHz clock. The data can then be taken to the E2 (8.448 Mbps) interface for further processing.

3.6 IV Order Digital MUX

Block diagram of IV order digital MUX is shown in fig. 3.9(a) and E4 (139.264 Mbps) frame structure is shown in fig.3.9(b). Each frame has 2928 bits. Incoming tributaries are at 34.368 Mbps rate.

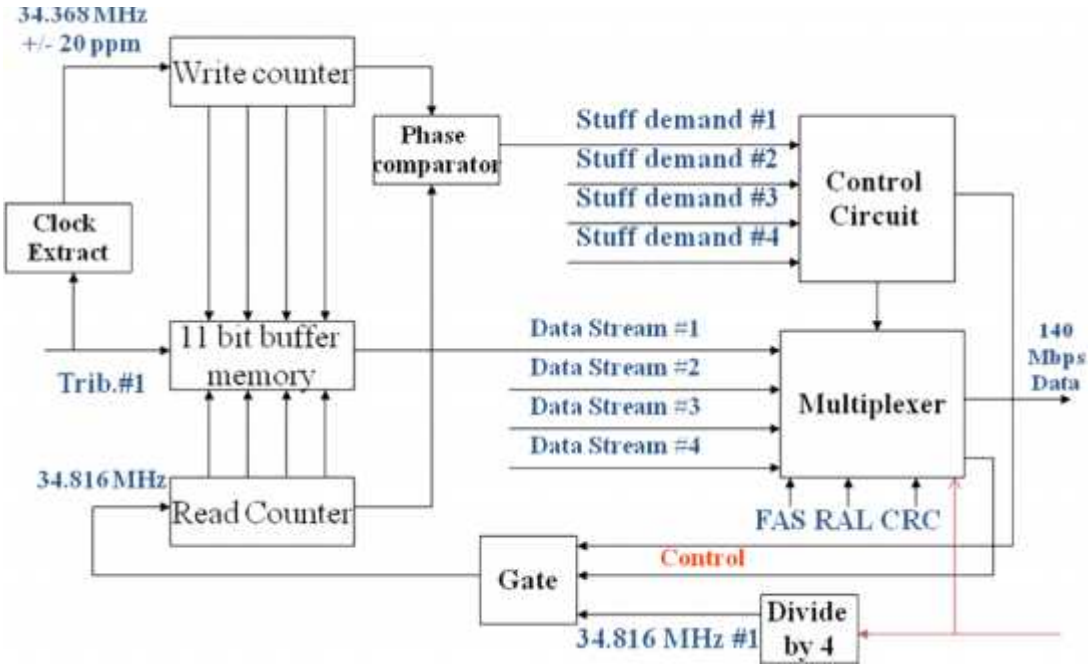
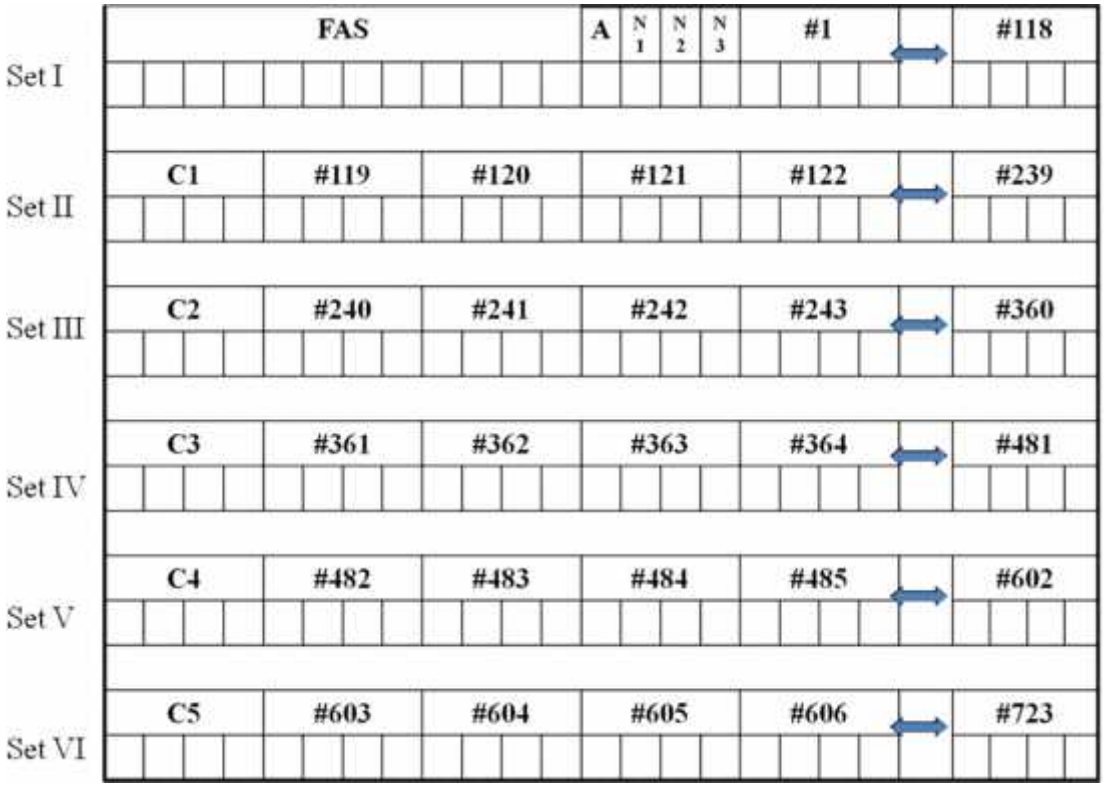


Fig. 3.9(a) Block diagram of IV Order Digital Multiplexing

Bit stream integration process is similar to that in III-order MUX. Only the frame size and clock rates are different. The data read in clock is 34.816 MHz. Incoming data is at 34.368 Mbps ± 30 ppm. Each frame has 2928 time-slots with 4 bits per slot; FAS occupies the first twelve bits of a frame; alarm and national bits occupy the next 4 bits. Justification bits are in TS-603. JCBs are 5 per tributary, facilitating majority decision.



Note:

Frame size: 122 Bits X 4 sets i.e. 488 Bits /Set & 4 Sets : 2928 Bits

FAS : Frame Alignment Signal (111110100000)

A&N Bits: A: Remote Alarm (1-Alarm) ; N1: Parity ; N2&N3: Resvd

#1 to #723 (excl.#603) : Each one, a set of 4 bits; 1 bit from each Tributary

C1 to C5: Justification Control bits (11111> Justification; 00000 > None)

#603 : Justification Bits of each tributary

Fig. 3.9(b) Frame structure of E4 (139.264 Mbps) signal

It may be noted that TS-603 is also used for remote loopback at 34.368 Mbps level (other than data and justification bits). If JC1 to JC5 are 00000, the bit in TS-603 carries data; if they are 11111, the bit in TS-603 carries remote loopback information. A ‘0’ indicates request for loopback and a ‘1’ indicates no request.

Retrieval of tributaries

Refer to Fig. 3.9(c). The demultiplexer locates the synchronization word in the incoming 139.264 Mbps signal, recovers the 139.264 Mbps clock, and converts the input signal into four parallel streams of 34.816 Mbps each. The 34.816 Mbps data stream is written into an elastic store with the help of a write clock at 34.816 MHz (Rx clock/4).

The write clock is a 34.816 MHz perforated clock. The perforations are made at specific durations corresponding to FAS bit position, JC and justification bit slots. Since the clock is interrupted, the data is effectively written into the elastic store at a nominal rate of 34.368 Mbps even though the input to the elastic store is at a higher rate.

It may please be noted that the operation done here is the reverse of what was done at the multiplexer. In the multiplexer, data was read from the elastic store by providing perforations in the read clock.

The read clock for the elastic store is obtained from a 34.368 MHz VCXO which is phase-locked to the 34.816 MHz clock. The data can then be taken to the E3 (34.368 Mbps) interface for further processing.

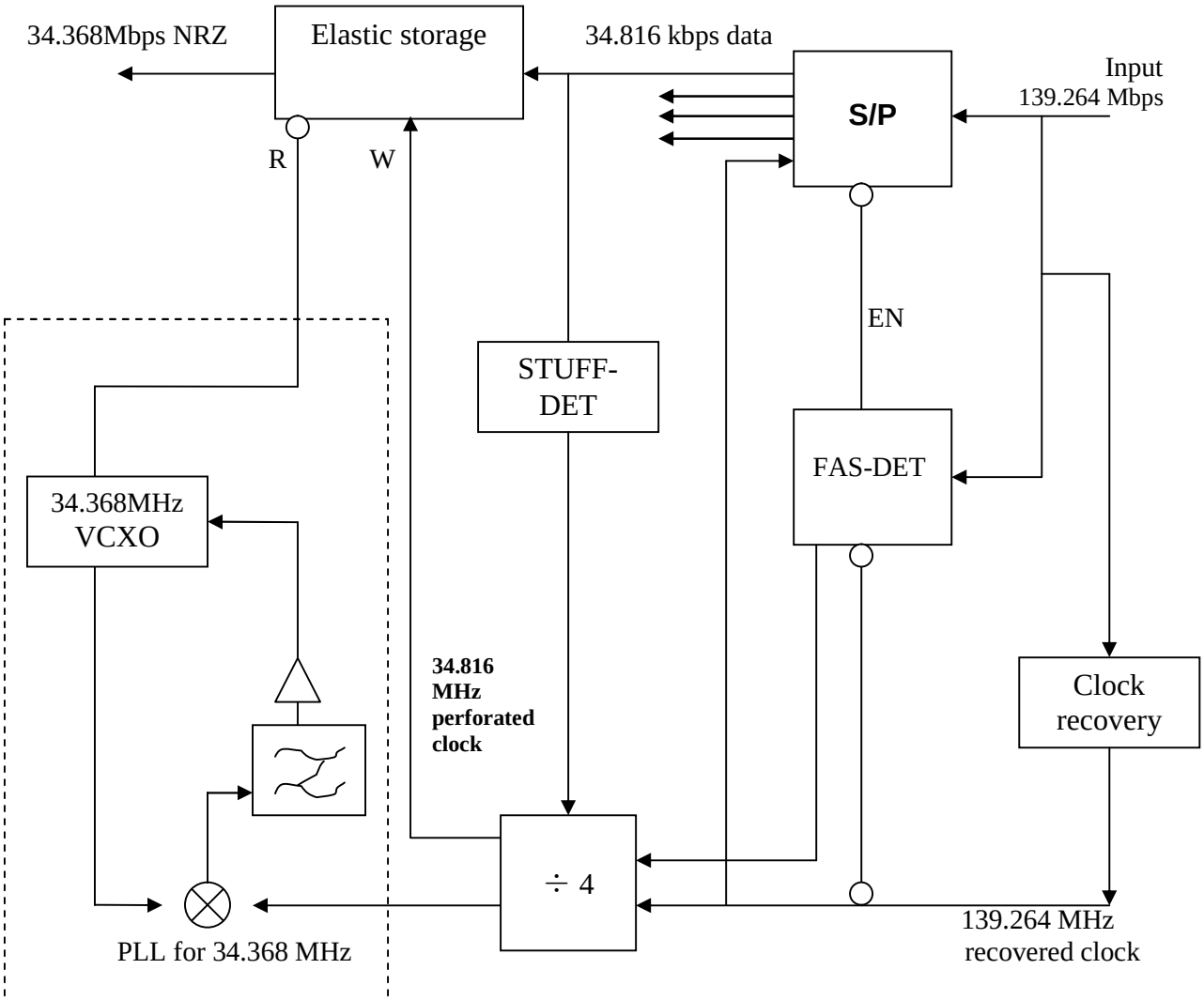


Fig. 3.9(c) Retrieval of tributaries in IV order MUX.

Objective:

1. In E2 with bit rate of 8448 Kbps has ---------- channel capacity
2. In E3 with bit rate of 34368 Kbps has ----------channel capacity
3. In E4 with bit rate of 139264 Kbps has ---------- channel capacity
4. In T1 with bit rate of 1544 Kbps has ---------- channel capacity
5. PDH multiplexing from 2nd order onwards involves ----------interleaving
6. PDH multiplexing from ---------- order onwards involves Justification
7. A sub-frame of 2nd order digital multiplexing system is having ---------- number of bits.
8. In the 2 nd order MUX system frame repetition frequency is----------.
9. No. of justification control bits used per tributary in the 2 nd order MUX system is--------.
10. In the 2 nd order digital multiplexing system a frame is divided into ----------of sub-frames.
11. For the fourth order digital multiplexing system the bit rate is 139.264 Mb/s with a tolerance value of----------.
12. In E2 Frame structure TS ----------occupies Justification Bits
13. PDH E1 employs _____ interleaving.

Subjective:

1. Write the PDH Hierarchy Adopted in INDIA?
2. What are the Basics of PDH Multiplexing System?
3. Write short notes on :
   a. Bit interleaving.
   b. Byte interleaving
4. What is Justification Write the Process employed in Justification?
5. Explain the Frame structure with block diagram of E2 (8.448 Mb/s)?
6. Explain the Frame structure with block diagram of E3 (34.368 Mb/s)?

CHAPTER 4

JITTER & WANDER IN PDH NETWORKS

4.1 Jitter & Wander

Jitter and wander are defined respectively as the short term and long term variations of the significant instant of a digital signal from their ideal positions in time. The significant instant may be taken as the midpoint or any fixed arbitrary point, which is clearly identifiable on each of the pulses.

4.1.1 Jitter: Please refer Fig.4.1 showing pictorial representation of jitter

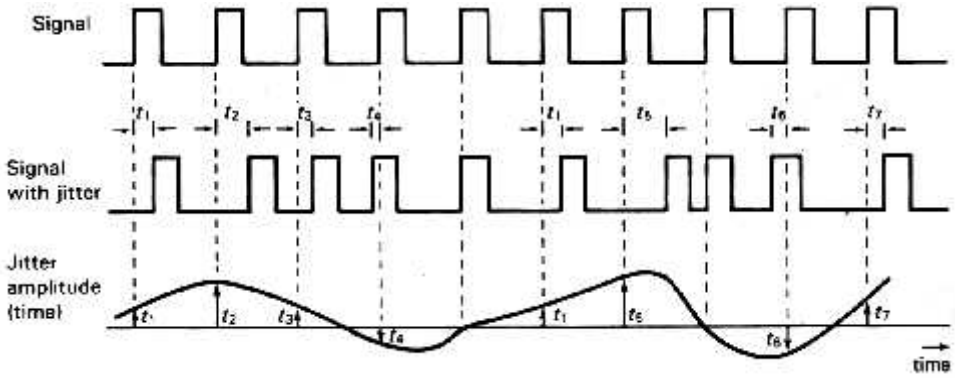


Fig.4.1 Pictorial Representation Of Jitter And Its Effect On Digital Signal

The jitter waveform represents jitter as a continuous time function with properties independent of the digital signal, which it affects. Jitter signal considered to be most significant, occupies the frequency range from a few tens of Hz to several KHz. The unit of jitter is unit interval (UI). The unit interval is defined as per ITU-T recommendation G.701 definition 2018, as “The nominal difference in time between the consecutive significant instants of an isochronous signal”. This means that, if

The instantaneous jitter amplitude is 1 microsecond in a 100 KHz square wave

The period of frequency = 1second / 100 KHz = 10 « sec

For a timing signal to differentiate between what is a mark and what is space, the Unit Interval between the significant instants = 5 μ sec

Jitter Amplitude = 1μ sec / 5 μ sec = 0.2 UI.

4.1.2 Sources of Jitter: In a digital transmission system, jitter may take place due to a variety of sources. The majority of these sources fall in the categories as listed below:

1. Very low frequency jitter:
   a) Variations in the propagation delays.
   b) Slowly changing temperature delays.
2. Low frequency jitter: Inherent instabilities of clock sources.
3. Noise induced jitter:
   a) Phase noise in crystal controlled oscillator circuits used in clocks through out the system.

b) Noise in logic circuits.

4. Multiplex induced jitter: Insertion and removal of justification bits and framing digits.
5. Jitter on the regenerated bit streams: Inter symbol interference
6. Regenerator Jitter: Imperfect timing recovery at the regenerators.

4.1.3 Effects of Jitter

The accumulation of jitter should be prevented. The equipment should be so designed that its tolerance limits should be able to accommodate, the jitter generated by the preceding equipment and system. If it is not done, the accumulated jitter can cause the following impairments. ITU -T recommendation G.823.

1. An increase in the probability of introducing digital errors into digital signals at points of signal regeneration caused by the timing signals being displaced from their optimum positions in time.
2. The introduction of uncontrolled slips into digital signals as a result of the digital store capacity designed to cater for other effects being used up, thus causing store spillage and, for the opposite effect, store depletion. Spillage and depletion occur in certain types of terminal equipment incorporating buffer stores and phase comparators. Eg: Jitter reducers and certain digital multiplex equipment.
3. A degradation of digitally encoded analog information as a result of phase modulation of the reconstructed samples in the digital to analog conversion device at the end of the connection. The timing jitter in this case which affects the regularity of the spacing between samples of the reconstructed PAM signals is sometimes known as absolute jitter. Encoded PCM speech is fairly tolerant to this type of effect, but digitally encoded television is much more sensitive.

4.2 ITU-T Recommendations regarding control of jitter and wander

The jitter and wander in digital transmission systems should be kept within the specified limits to ensure that the quality of encoded analog information is not significantly impaired. It this is not done, the samples in the digital to analog conversion are impaired and the result is a corrupted output.

The control of jitter to contain the digital error rate to within that recommended is achieved by limiting the alignment error in every re timing process. This may be achieved by designing the clock recovery circuitry to have a jitter bandwidth comparable to that of the incoming jitter bandwidth. The absolute jitter magnitude is usually not significant in the occurrence of jitter induced errors.

The control of slips to within that recommended can only be achieved if the jitter generation and accumulation in all equipments through out the network are considered. This means that there is the requirement for overall jitter control and jitter performance specification.

As the control of jitter means ‘the control of jitter to within specified limits’, there is a need to specify these limits in such a way that overall control can be realized. The specification of the limits are thus made for different interconnecting elements such as digital radio links or

individual pieces of equipment such as multiplex equipment, digital exchanges etc., the network in its totality under different network configurations, and international connecting networks.

Also this jitter control philosophy should ensure that the error and slip objectives, etc. would be met for any network element experiencing jitter on its input, irrespective of its location in the network or from where the signal originates in the network. Further more, these objectives must continue to be met as the network expands and its configuration changes.

The ITU-T recommendation G.823 is concerned with the control of jitter and wander within digital networks that are based on the 2048 kbps hierarchy. These recommendations contain:

1. Network limits for the maximum output jitter at any hierarchical interface
2. Jitter limits appropriate to digital equipments

Let us examine them.

4.2.1 Network limits for the maximum output jitter at any hierarchical interface:

The basic philosophy in this case is to specify the maximum network limit that should not be exceeded at any hierarchical interface and to provide a consistent frame of work for the specification of individual digital equipments. In addition to this, guidelines and information, but not limits are provided so that jitter accumulation studies and measurements can be made.

Table 4.1 below gives the ITU-T recommendation G.823 for limits of the maximum permissible levels of jitter at hierarchical interfaces within a digital network.

It may please be noted that:

1. These specified limits are for the co directional interface only.
2. The frequency values shown in parentheses apply only to certain national interfaces.

These limits should be met for all operating conditions and regardless of the amount of equipment preceding the interface.

Parameter Value		Network limit of pk-pk jitter		Measurement filter bandwidth		
Digit rate of 1 UI		B1 UI measured f1-f4	B2 UI measured f3-f4	Band-pass filter having a lower cut-off frequency f1 or f3 and an upper cut off frequency f4		
Kbit/s	ns			f1 Hz.	f3 k Hz.	f4 k Hz.
64 (Note 1)	15600	0.25	0.05	20	3	20
2048	488	1.5	0.2	20	18 (700 Hz.)	100
8448	118	1.5	0.2	20	3 (80 kHz.)	400
34368	29.1	1.5	0.15	100	10	800
139 264	7.18	1.5	0.075	200	10	3500

Table. 4.1 Maximum permissible jitter at hierarchical interface based on the 2048 kbit/s hierarchy (tolerable input jitter)

In operational networks, signals at an interface can contain jitter up to the maximum permissible network limit. This is important in the design of equipments incorporating jitter reducers where this jitter, together with any additional jitter generated in the system prior to the jitter reducer, needs to be accommodated.

4.2.2 Jitter limits appropriate to digital equipments:

For individual digital equipments, the jitter performance is specified in three ways.

- Maximum output jitter in the absence of input jitter (intrinsic jitter).
- Jitter and wander tolerance of digital input ports (tolerable input jitter).
- Jitter transfer characteristic.

Maximum Output Jitter In The Absence Of Input Jitter:

As it is necessary to restrict the amount of jitter which an individual item of equipment can generate, ITU-T Recommendations defining the maximum permissible levels of jitter generated in the absence of any input jitter are provided when dealing with specific systems. These limits never exceed the maximum permitted network limit. Measurement is shown in fig.4.2

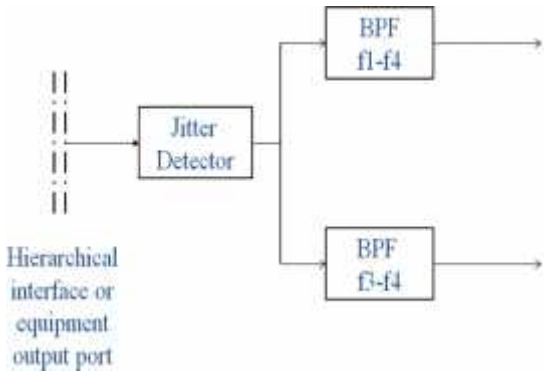


Fig.4.2 Output jitter in absence of input jitter

Limits are tabulated in table 4.2

Data Rate (kbps)	1 UI (ns)	NW Limits of pk-to-pk Jitter		Measurement filter bandwidth		
		B1 UI Measured f1-f4	B2 UI Measured f3-f4	BPF having lower cut-off frequency f1 or f3 and upper cut-off frequency f4		
				f1 Hz	f3 kHz	f4 kHZ
64	15600	0.05	0.01	20	3	20
2048	488	0.25	0.06	20	18	100
8448	118	0.25	0.06	20	3	400
34368	29.1	0.25	0.05	100	10	800
139264	7.18	0.25	0.025	200	10	3500

Table 4.2 Output jitter limits in absence of input jitter

Jitter tolerance Of Digital Input Port:

Figure 4.3 gives input jitter tolerance in a graphical way. Table 4.3 gives the values of f1, f2, f3, f4 and A0, A1, A2. These limits are used to insure that, under the worst conditions, the input ports of equipments are capable of accommodating these levels of jitter when connected to any recommended hierarchical interface within the network.

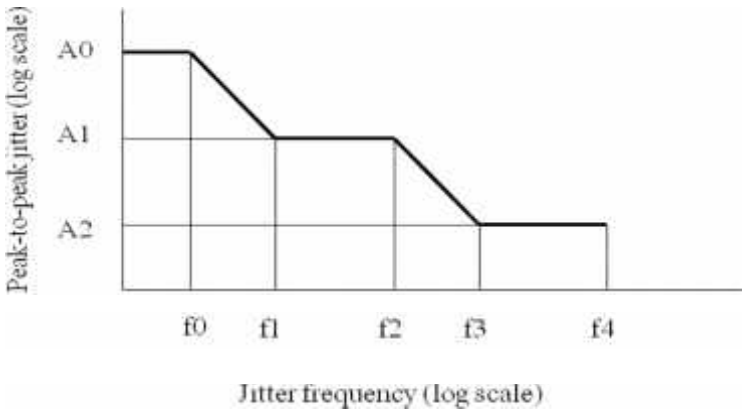


Fig.4.3 Graphical presentation of input jitter tolerance

Data Rate (kbps)	1 UI (ns)	Peak-to-peak jitter (in UI)			Frequency					PRBS for testing
		A0	A1	A2	f0 Hz	f1 Hz	f2 kHz	f3 kHz	f4 kHz	
64	15600	1.15	0.25	0.05	1.2 X 10^{-5}	20	0.6	3	20	$2^{11} - 1$
2048	488	36.9	1.5	0.2		20	2.4	18	100	$2^{15} - 1$
8448	118	152	1.5	0.2		20	0.4	3	400	$2^{15} - 1$
34368	29.1	Under study	1.5	0.15	Under study	100	1.0	10	800	$2^{23} - 1$
139264	7.18		1.5	0.075		200	500	10	3500	$2^{23} - 1$

Fig. 4.3 Interpretation of input jitter tolerance curve

Jitter Transfer Characteristic:

Jitter present at the input port of an equipment may in many cases be partially transmitted to the output port. In passing through the equipment the higher jitter frequencies are usually attenuated, whereas the lower frequency jitter may not be. The jitter transfer characteristic provided in the ITU-T recommendations take the form of a mask which indicates the permissible jitter gain versus frequency for particular items of equipment or systems. Table 4.4 gives jitter transfer characteristic. 'P' indicates positive justification

Digital Rate, kbit/s	Jitter gain, dB	Frequency		Roll off after cut off, dB/decade
		Lowest	Cut off f_2	
8448 (P)	0.5	As low as possible	40 Hz	20
34368 (P)	0.5	As low as possible	100 Hz	20
139 264 (4X34368, P)	0.5	As low as possible	300 Hz	20
139 264 (16 X 8448, P)	0.5	As low as possible	100 Hz	20

Table.4.4 Jitter Transfer characteristics

4.3 Jitter Limits For Digital Sections:

To provide the jitter limits for digital sections it is necessary to introduce a hypothetical reference digital section (HRDS) whose lengths have been chosen to be 50 km or 280 km. These are representative digital sections likely to be encountered in real operational networks, and are sufficiently long to permit a realistic performance specification for digital radio systems. The model is homogeneous in that it does not include other digital equipments such as MULDEXes.

Figure 4.4 shows this HRDS, and the jitter specifications in Table 4.5 relate to it. The jitter transfer function recommended (ITU-T Recommendation G.823) limits the maximum gain to a value of 1 dB with the lower frequency limit of 5 Hz. being acceptable. For line sections at 2048 kbit/s complying with the alternative national interface option as indicated by the figures in parentheses in table 4.5, a jitter gain of 3 dB is acceptable. The output jitter in the absence of input jitter for any valid signal condition should not exceed the limit provided in Table. 4.3

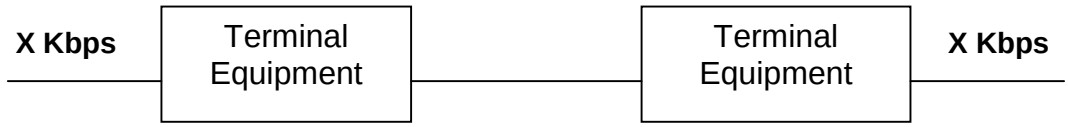


Fig.4.4 Hypothetical reference Digital Section

Bit rate k bit/s	HRDS Length, km	Maximum output pk-pk jitter for digital section up to the length of a HRDS		Measurement filter bandwidth		
		Low frequency limit (f_1-f_4) UI	High frequency limit (f_3-f_4) UI	Band-pass filter having a lower cut off frequency f1 or f3 and an upper cut off frequency f4		
				f1 KHz	f3 KHz	F4 KHz
2048	50	0.75	0.2	20	18 (700 Hz)	100
8448	50	0.75	0.2	20	3 (80 KHz)	400
34368	50	0.75	0.15	100	10	800
34368	280	0.75	0.15	100	10	800
139 264	280	0.75	0.075	200	10	3500

Table 4.5 The maximum output jitter in the absence of input jitter for a digital section up to the length of a HRDS (intrinsic jitter)

In parentheses of table 4.4, a jitter gain of 3 dB is acceptable.

4.4 Jitter Measurement Methods:

ITU-T Recommendations G.823 & O.151.

- **Oscilloscope:** Used for measuring the peak to peak value of the phase jitter for repetitive sources such as the timing signal.
- **Calibrated Phase Detector:** Used for clock timing signals or for repetitive bit streams, where the reference signal is either at the same rate or is a sub multiple of the input bit streams.
- **Digital Processing Oscilloscope:** This technique provides a time and amplitude quantized histogram estimator for the probability density function of the transition times of a digital signal, which unlike many commercial jitter measuring techniques permits measurements at all hierarchical levels and intermediate data rates. In addition this technique also provides a detailed description of the jitter phenomena, which permits measurements to be made on either a single transition in a periodic data sequence, or on an ensemble of all transitions. This method also provides the means for separate identification and study of uncorrelated and pattern dependent jitter contributions to be made. The jittered signal is displayed on the

Digital Processing Oscilloscope (DPO) using a jitter free reference signal for the trigger input.

ITU-T Recommended Test Set Ups:

Fig. 4.5(a) shows the test set up for measuring timing jitter, which is derived from Recommendations O.171, and figure 4.5(b) shows the test set up for measuring output jitter from a hierarchical interface for an equipment output port G.823

- **Test Signal Source:**

Fig.4.5 (b) is effectively the jitter measuring circuit shown in the test set up of Fig.4.5 (a). The tests made on digital equipment may be made with either a jittered or non-jittered digital signal. To transmit this signal a pattern generator, clock generator and modulation source as shown in Fig.4.5 (a) are required. The modulation source may be provided within the clock generator and/or patter generator or it may be provided separately as shown. The clock generator is able to be phase modulated from the modulation source and the peak to peak deviation of the modulated signal indicated. The clock generator outputs comprising the modulated clock signal and a timing reference signal are required to be not less than 1 volt peak to peak into 75 ohms. The modulated clock signal is used to drive a pattern generator, which usually is able to provide a frame alignment signal and justification control bits if the pattern test signal is to enter the input of a digital demultiplexer.

For use at digit rates of 64 kbit/s, the pattern generator is to provide a pseudo-random patter of ($2^{11} - 1$) bit length in accordance with ITU-T Recommendation O.152. For levels, 1,2 and 3 of both hierarchies, as shown in figure 4.1, except for 34368 kbit/s, a pseudo random pattern ($2^{15} - 1$) bit length is recommended. For 34368 kbit/s of and 139 264 kbit/s, a pseudo random pattern of ($2^{23} - 1$) bit length is recommended. Both of these pseudo random patterns are generated in accordance with Recommendation O.151. In addition to these patterns, a 1000 1000 repetitive pattern, two freely programmable 8 bit patterns capable of being alternated at a low rate such as between 10 Hz. and 100 Hz. Or a freely programmable 16 bit pattern, is available from the primary generator.

It is normally assumed that live traffic on transmission systems consists of essentially random digit sequences and, for this reason, test patterns normally consist of pseudo random binary sequences (PRBS), suitably encoded and of a length adequate to give a reasonable distribution of power within the band widths of any timing recovery filters in the system. Preliminary studies on the relationships between test pattern jitter and live traffic jitter have revealed that jitter arising from the use of pseudo random test sequences is dependent not only upon the sequence length, but also upon which of the set of allowable generator configurations (see section 5.1.13) are chosen for a given sequence length. It is therefore possible that, for a given sequence length, some generator configurations will be better than others for live traffic simulations. The test pattern sequences most often used are pseudo random binary maximal length [($2^{15} - 1$) bits], encoded into the appropriate interface code. Every sequence of ($2^n - 1$) contains (0.5) x (2^n) –1 zeros and (0.5) X (2^n) ones. Every complete sequence will also contain all possible n-bit combinations of ones and zeros except the (n) zeros combination and the (n-1)

ones combination. Thus, for moderate values of n, a sequence generated will for practical purposes approximate to a random binary sequence. The 2^{15} sequence frequently used for testing 2 and 8 Mbit/s systems does on some sequences exhibit a tendency for bunching of the longer runs of zeros and even after HDB3 coding the effects of this bunching can be detected on a regenerative repeater. On live systems, traffic jitter usually varies from day to day, with changes in the traffic carried.

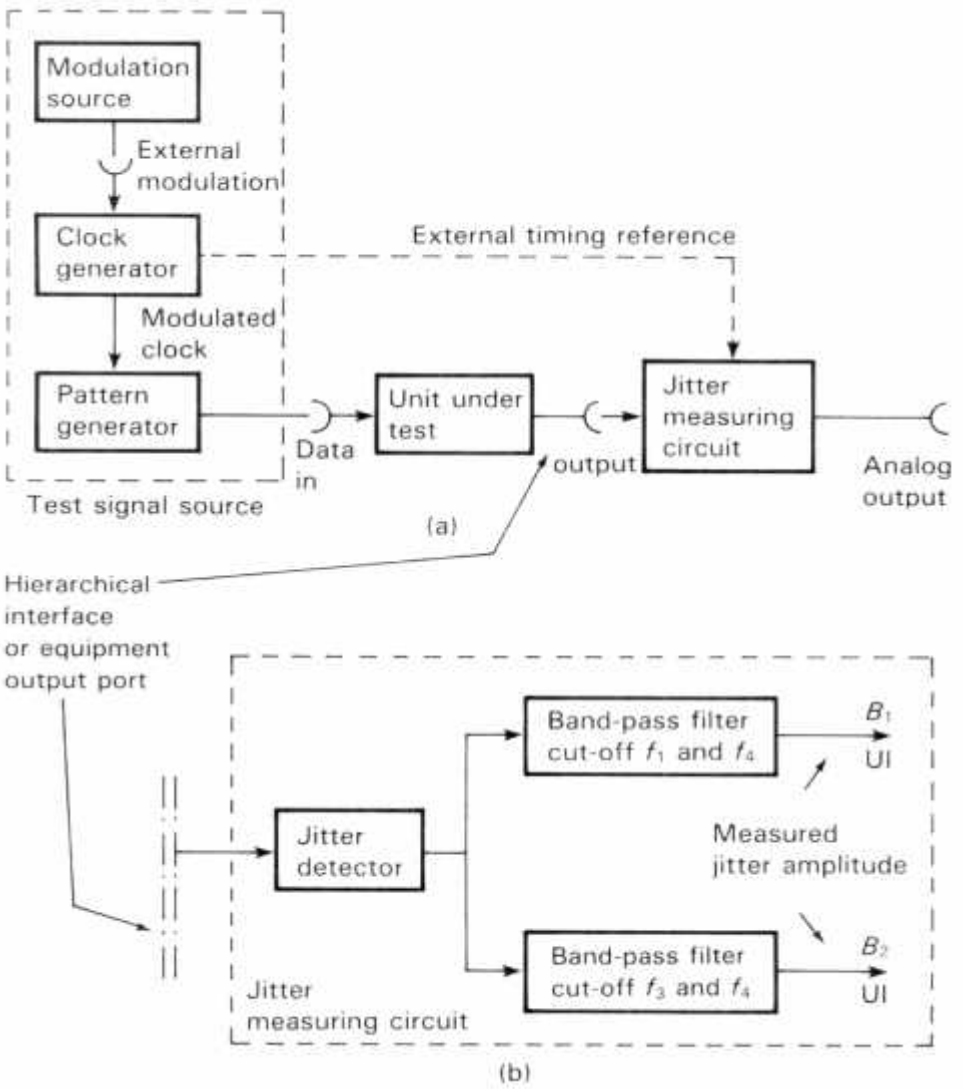


Fig.4.5 ITU-T Measurement Arrangements For Jitter

4.5 Jitter accumulation in PDH networks

In PDH networks, we have regenerative repeaters placed at regular intervals. At these repeaters, output signal is retimed under the control of a timing signal derived from the incoming signal. We study here the accumulation of

- pattern-dependent jitter
- random pattern jitter
- alternate repetitive pattern jitter on such networks.

Accumulation of pattern-dependent jitter

The most significant component of jitter in a regenerator is the waiting-time jitter which is pattern dependant. If this jitter is truly random, the total rms jitter J_N on a link with N regenerative repeaters is

$$\boldsymbol{J}_N \cong J \times \sqrt[4]{N} \text{ for large value of } N,$$

Where J = rms jitter of single regenerator due to controlled source.

Since the pattern-dependent jitter is not random, the above expression is modified as

$$\boldsymbol{J}_N \cong J_1 \times \sqrt{2N} \text{ for large values of } N.$$

Based on operational experience,

$$0.4 \text{ UI} \leq J_1 \leq 1.5 \text{ UI}.$$

Use of PLL in the timing recovery circuit modifies the expression further as

$$\boldsymbol{J}_N \cong J_1 \times \sqrt{2NA},$$

Where A is a factor dependent on the number of repeaters and the damping factor of PLL.

From the above expressions, the following inferences can be drawn:

- Pattern-dependent jitter accumulates more rapidly than non-pattern-dependent jitter as the number of regenerators increased.
- The amplitude of jitter produced by a chain of regenerators increases without limit as the number of regenerators is increased

Accumulation of random jitter

The jitter produced by random signals is itself random. Its amplitude has a Gaussian probability distribution function. Hence, for a given standard deviation (rms amplitude), the probability of exceeding any chosen peak-to-peak amplitude can be calculated. Normally, the probability of exceeding peak-to-peak value of 1.5 UI is very low.

Accumulation of Jitter due to alternate repetitive patterns

When the signal being transmitted is composed of two repetitive patterns alternating at low frequency, the jitter appears as a low frequency repetitive wave with amplitude proportional to the number of regenerators.

The maximum peak-to-peak jitter is given by

$$J_{NP} = \text{N x PSJ},$$

Where PSJ stands for pattern sensitive jitter, produced by a single regenerator when it is subjected to alternating repetitive patterns.

This situation is unlikely in normal operations, but to rule out the slightest possibility, digital scramblers are used.

Jitter accumulation in MULDEX pairs over entire network

To conclude, waiting-time jitter is a significant contribution from a MULDEX equipment. Accumulation is in between $\sqrt[4]{N}$ times to $\sqrt{2N}$ times Jitter on single hop where N is the number of hops (i.e. number of MULDEX pairs).

4.7 Methods Of Minimizing Jitter:

Two basic methods are commonly used. The first is to take steps to prevent the generation and systematic accumulation of the jitter by the use of scramblers. These devices effectively cause the signal to become random and so reduce the effect of any pattern dependent jitter causing mechanisms. The second method is to reduce the magnitude of the jitter already present by using a re timing circuit which has a bandwidth which is less than that of the signal bandwidth. This circuit is known as a 'jitter reducer'. As mentioned above, the jitter frequencies which are below the jitter reducer's cut off frequency are not reduced and may cause, in some circuits, an uncontrolled slip, due to the jitter amplitude at these frequencies accumulating and becoming large enough to affect digital equipments which are not transparent to jitter. The choice of buffer stores with sufficient capacity at the input of digital equipments in the practical situation alleviates this problem.

Scramblers:

Scrambler and de-scrambler are shown in fig.4.6.

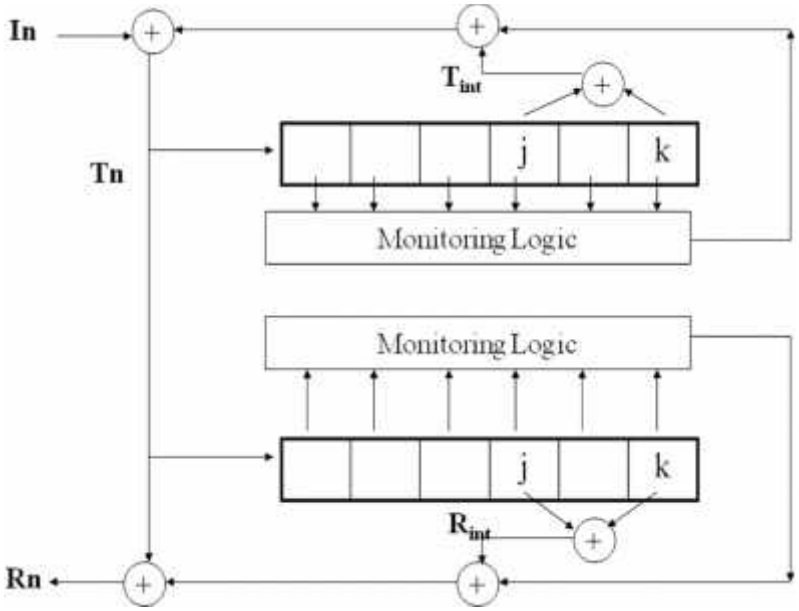


Fig.4.6 Scrambler and de-scrambler

Exclusive-OR operation, bit by bit, on incoming stream and it's delayed versions removes patterns if any. Converse operations at receiving end retrieve the original transmitted sequence. The reader may please take a test sequence with repetitive pattern and check that pattern is removed in the sequence sent to receiver. It can also be verified that the finally retrieved sequence is replica of input sequence.

Advantages of using scrambler-descrambler as an integral part of a digital transmission system are listed as below.

- Ensure that the accumulation of jitter is not correlated with the signal.
- Reduce the effects of low frequency jitter accumulation.
- Reduce the effects of cross talk levels on symmetric pair cable produced by synchronous systems, by suppressing discrete spectral components of periodic bit patterns.

One disadvantage of using them is that they cause error extension effects. That is, any transmission error, which, under non-scrambled conditions would cause only one error in a system, will cause further errors when the system is in the scrambled condition. This is due to the way the scrambler operates and to the use that it makes of a feedback path. The feedback path, feeds any error appearing on it back into the scrambling circuit's input, thus compounding the error.

Jitter-reducer

Jitter-reducer is shown in fig.4.7. Clock recovered from incoming sequence using normal PLL is subjected to High Q PLL recovery. Jitter on the initially recovered clock and later version cancel each other.

On N-hop PDH link, use of jitter-reducer reduces jitter according to the equation :

$J_N = 2.N.J.(f_c.BW/2)^{1/2}$

f_c is cut-off frequency of de-jitter circuit

BW is bandwidth of regenerator equipment

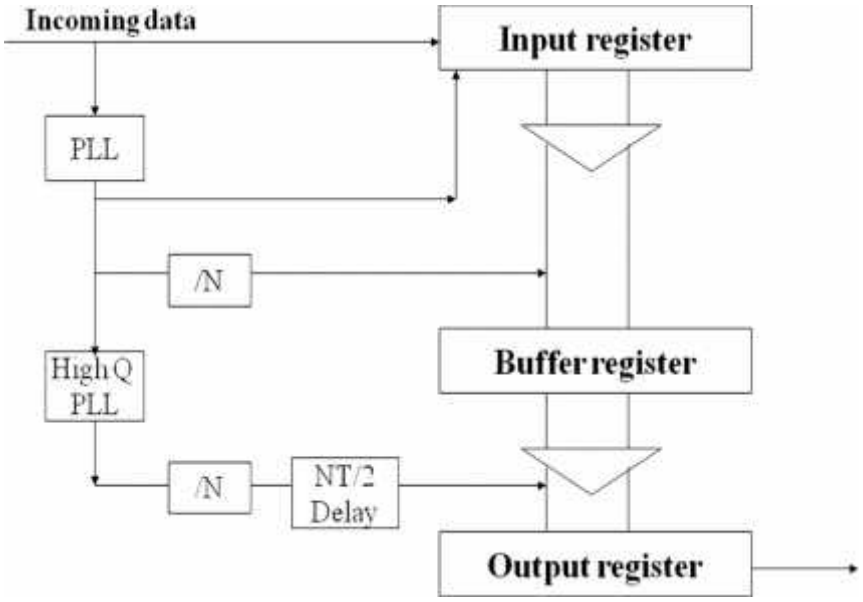


Fig.4.7 Jitter-reducer

Objective:

1. Jitter is defined as the ----------term variations of the significant instant of a digital signal from their ideal position in time

2. Wander is defined as the ----------term variations of the significant instant of a digital signal from their ideal position in time

3. The unit of Jitter is ----------

4. Multiplex induced jitter is due to adjustment of ----------

5. Inter symbol interference may arise due to ----------

6. Imperfect timing recovery at regenerator leads to ----------jitter

7. Jitters can be reduced by the use of ----------

Subjective:

1. Define Jitter and Wander in the Transmission system?

2. Explain the significance of Jitter in Data communication system?

3. What are the ITU-T recommendations regarding control of Jitter and Wander?

4. Write shot notes on :
   a. Jitter Transfer Characteristic.
   b. Jitter Tolerance.
   c. Scramblers

References

Chapter 3 and 4 of this notes are prepared referring the book – 'Digital Microwave Communication Systems' - by P.V.Sreekanth, (2003), Universities Press (Orient Longman)