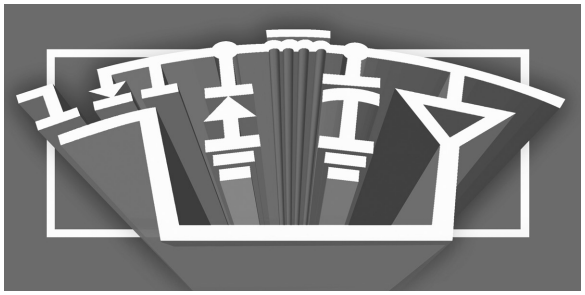

Power Supply Design Seminar

Designing an LLC Resonant Half-Bridge Power Converter

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Designing an LLC Resonant Half-Bridge Power Converter

Hong Huang

ABSTRACT

While half-bridge power stages have commonly been used for isolated, medium-power applications, converters with high-voltage inputs are often designed with resonant switching to achieve higher efficiency, an improvement that comes with added complexity but that nevertheless offers several performance benefits. This topic provides detailed information on designing a resonant half-bridge converter that uses two inductors (LL) and a capacitor (C), known as an LLC configuration. This topic also introduces a unique analysis tool called first harmonic approximation (FHA) for controlling frequency modulation. FHA is used to define circuit parameters and predict performance, which is then verified through comprehensive laboratory measurements.

INTRODUCTION

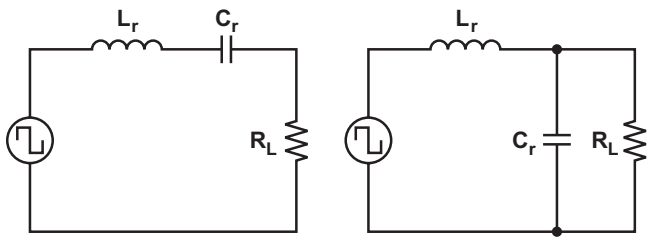
Higher efficiency, higher power density, and higher component density have become common in power-supply designs and their applications. Resonant power converters—especially those with an LLC half-bridge configuration—are receiving renewed interest because of this trend and the potential of these converters to achieve both higher switching frequencies and lower switching losses. However, designing such converters presents many challenges, among them the fact that the LLC resonant half-bridge converter performs power conversion with frequency modulation instead of pulse-width modulation, requiring a different design approach.

This topic presents a design procedure for the LLC resonant half-bridge converter, beginning with a brief review of basic resonant-converter operation and a description of the energy-transfer function as an essential requirement for the design process. This energy-transfer function, presented as a voltage ratio or voltage-gain function, is used along with resonant-circuit parameters to describe the relationship between input voltage and output voltage. Next, a method for determining parameter values is explained. To demonstrate how a design is created, a step-by-step example is then presented for a converter with 300 W of output power, a 390-VDC input, and a 12-VDC output. The topic concludes with the results of bench-tested performance measurements.

A. Brief Review of Resonant Converters

There are many resonant-converter topologies, and they all operate in essentially the same way: A square pulse of voltage or current generated by the power switches is applied to a resonant circuit. Energy circulates in the resonant circuit, and some or all of it is then tapped off to supply the output. More detailed descriptions and discussions can be found in this topic's references.

Among resonant converters, two basic types are the series resonant converter (SRC), shown in Fig. 1a, and the parallel resonant converter (PRC), shown in Fig. 1b. Both of these converters regulate their output voltage by changing the frequency of the driving voltage such that the impedance of the resonant circuit changes. The input voltage is split between this impedance and the load. Since the SRC works as a voltage divider between the input and the load, the DC gain of an SRC is always



a. Series resonant converter. *b. Parallel resonant converter.*

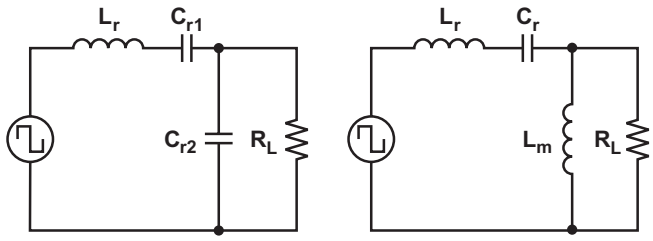
Fig. 1. Basic resonant-converter configurations.

lower than 1. Under light-load conditions, the impedance of the load is very large compared to the impedance of the resonant circuit; so it becomes difficult to regulate the output, since this requires the frequency to approach infinity as the load approaches zero. Even at nominal loads, wide frequency variation is required to regulate the output when there is a large input-voltage range.

In the PRC shown in Fig. 1b, the load is connected in parallel with the resonant circuit, inevitability requiring large amounts of circulating current. This makes it difficult to apply parallel resonant topologies in applications with high power density or large load variations.

B. LCC and LLC Resonant Converters

To solve these limitations, a converter combining the series and parallel configurations, called a series-parallel resonant converter (SPRC), has been proposed. One version of this structure uses one inductor and two capacitors, or an LCC configuration, as shown in Fig. 2a. Although this combination overcomes the drawbacks of a simple SRC or PRC by embedding more resonant frequencies, it requires two independent physical capacitors that are both large and expensive because of the high AC currents. To get similar characteristics without changing the physical component count, the SPRC can be altered to use two inductors and one capacitor, forming an LLC resonant converter (Fig. 2b). An advantage of the LLC over the LCC topology is that the two physical inductors can often be integrated into one physical component, including both the series resonant



a. LCC configuration. *b. LLC configuration.*

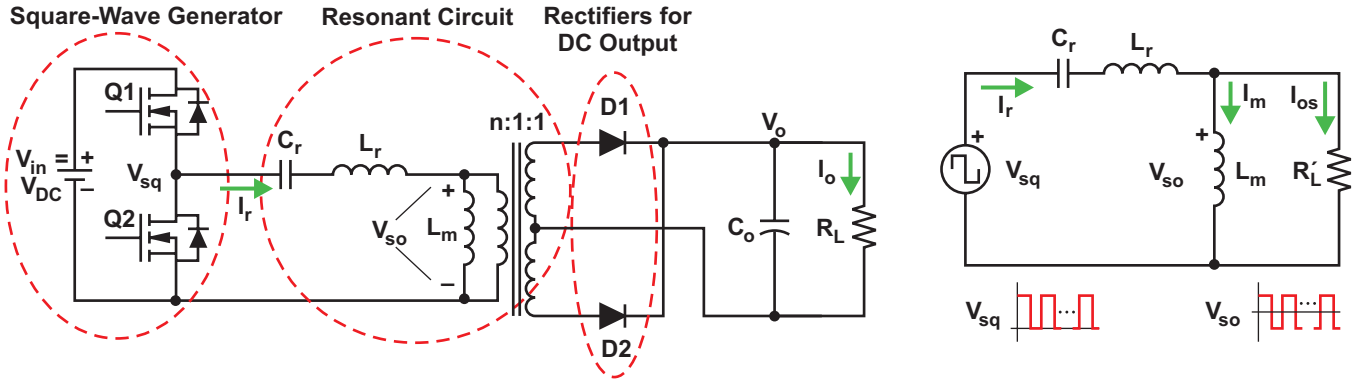
Fig. 2. Two types of SPRC.

inductance, L_r, and the transformer's magnetizing inductance, L_m.

The LLC resonant converter has many additional benefits over conventional resonant converters. For example, it can regulate the output over wide line and load variations with a relatively small variation of switching frequency, while maintaining excellent efficiency. It can also achieve zero-voltage switching (ZVS) over the entire operating range. Using the LLC resonant configuration in an isolated half-bridge topology will be described next, followed by the procedure for designing this topology.

II. LLC Resonant Half-Bridge Converter

This section describes a typical isolated LLC resonant half-bridge converter; its operation; its circuit modeling with simplifications; and the relationship between the input and output voltages, called the voltage-gain function. This voltage-gain function forms the basis for the design procedure described in this topic.



a. Typical configuration. *b. Simplified converter circuit.*

Fig. 3. LLC resonant half-bridge converter.

A. Configuration

Fig. 3a shows a typical topology of an LLC resonant half-bridge converter. This circuit is very similar to that in Fig. 2b. For convenience, Fig. 2b is copied as Fig. 3b with the series elements interchanged, so that a side-by-side comparison with Fig. 3a can be made. The converter configuration in Fig. 3a has three main parts:

1. Power switches Q1 and Q2, which are usually MOSFETs, are configured to form a square-wave generator. This generator produces a unipolar square-wave voltage, V_{sq}, by driving switches Q1 and Q2, with alternating 50% duty cycles for each switch. A small dead time is needed between the consecutive transitions, both to prevent the possibility of cross-conduction and to allow time for ZVS to be achieved.
2. The resonant circuit, also called a resonant network, consists of the resonant capacitance, C_r, and two inductances—the series resonant inductance, L_r, and the transformer's magnetizing inductance, L_m. The transformer turns ratio is n. The resonant network circulates the electric current and, as a result, the energy is circulated and delivered to the load through the transformer. The transformer's primary winding receives a bipolar square-wave voltage, V_{so}. This voltage is transferred to the secondary side, with the transformer providing both electrical isolation and the turns ratio to deliver the required voltage level to the output. In Fig. 3b, the load R'_L includes the load R_L of Fig. 3a together with the losses from the transformer and output rectifiers.
3. On the converter's secondary side, two diodes constitute a full-wave rectifier to convert AC input to DC output and supply the load R_L. The output capacitor smooths the rectified voltage and current. The rectifier network can be implemented as a full-wave bridge or center-tapped configuration, with a capacitive output filter. The rectifiers can also be implemented with MOSFETs forming synchronous rectification to reduce conduction losses, especially beneficial in low-voltage and high-current applications.

B. Operation

This section provides a review of LLC resonant-converter operation, starting with series resonance.

Resonant Frequencies in an SRC

Fundamentally, the resonant network of an SRC presents a minimum impedance to the sinusoidal current at the resonant frequency, regardless of the frequency of the square-wave voltage applied at the input. This is sometimes called the resonant circuit's selective property. Away from resonance, the circuit presents higher impedance levels. The amount of current, or associated energy, to be circulated and delivered to the load is then mainly dependent upon the value of the resonant circuit's impedance at that frequency for a given load impedance. As the frequency of the square-wave generator is varied,

the resonant circuit's impedance varies to control that portion of energy delivered to the load.

An SRC has only one resonance, the series resonant frequency, denoted as

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}. \quad (1)$$

The circuit's frequency at peak resonance, f_{c0}, is always equal to its f_0. Because of this, an SRC requires a wide frequency variation in order to accommodate input and output variations.

f_{c0}, f_0, and f_p in an LLC Circuit

However, the LLC circuit is different. After the second inductance (L_m) is added, the LLC circuit's frequency at peak resonance (f_{c0}) becomes a function of load, moving within the range of $f_p \le f_{c0} \le f_0$ as the load changes. f_0 is still described by Equation (1), and the pole frequency is described by

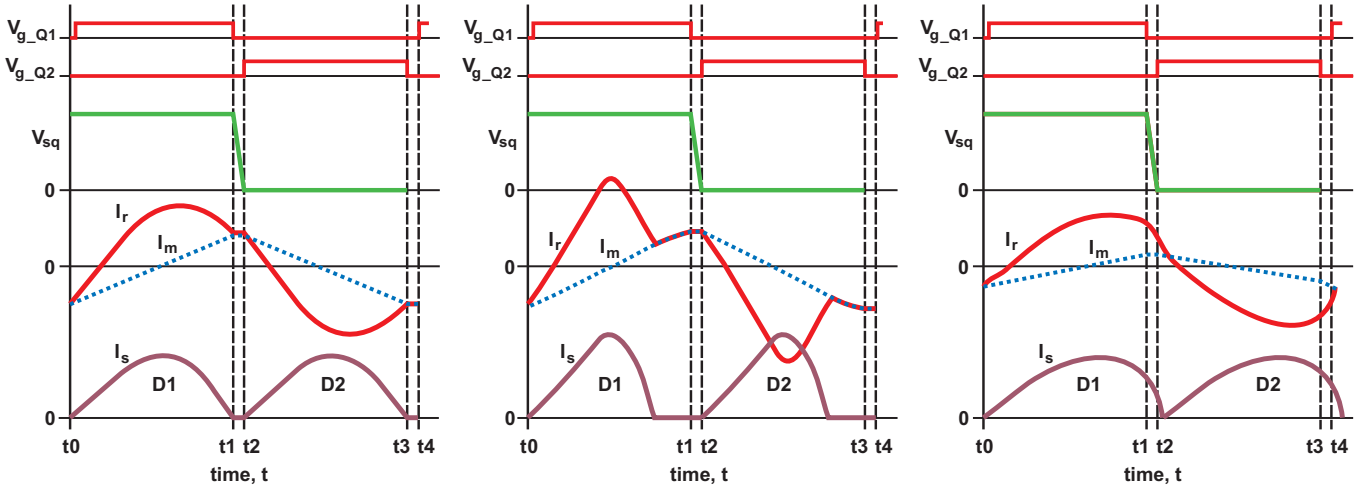
$$f_p = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}}. \quad (2)$$

At no load, $f_{c0} = f_p$. As the load increases, f_{c0} moves towards f_0. At a load short circuit, $f_{c0} = f_0$. Hence, LLC impedance adjustment follows a family of curves with $f_p \le f_{c0} \le f_0$, unlike that in SRC, where a single curve defines $f_{c0} = f_0$. This helps to reduce the frequency range required from an LLC resonant converter but complicates the circuit analysis.

It is apparent from Fig. 3b that f_0 as described by Equation (1) is always true regardless of the load, but f_p described by Equation (2) is true only at no load. Later it will be shown that most of the time an LLC converter is designed to operate in the vicinity of f_0. For this reason and others yet to be explained, f_0 is a critical factor for the converter's operation and design.

Operation At, Below, and Above f_0

The operation of an LLC resonant converter may be characterized by the relationship of the switching frequency, denoted as f_{sw}, to the series resonant frequency (f_0). Fig. 4 illustrates the typical waveforms of an LLC resonant converter with the switching frequency at, below, or above the series resonant frequency. The graphs show, from top to bottom, the Q1 gate (V_{g_Q1}), the Q2 gate (V_{g_Q2}), the switch-node voltage (V_{sq}), the resonant circuit's current (I_r), the magnetizing current (I_m), and the secondary-side diode current (I_s). Note that the primary-side current is the sum of the magnetizing current and the secondary-side current referred to the primary; but, since the magnetizing current flows only in the primary side, it does not contribute to the power transferred from the primary-side source to the secondary-side load.



a. At f_0. *b. Below f_0.* *c. Above f_0.*

Fig. 4. Operation of LLC resonant converter.

Operation at Resonance (Fig. 4a)

In this mode the switching frequency is the same as the series resonant frequency. When switch Q1 turns off, the resonant current falls to the value of the magnetizing current, and there is no further transfer of power to the secondary side. By delaying the turn-on time of switch Q2, the circuit achieves primary-side ZVS and obtains a soft commutation of the rectifier diodes on the secondary side. The design conditions for achieving ZVS will be discussed later. However, it is obvious that operation at series resonance produces only a single point of operation. To cover both input and output variations, the switching frequency will have to be adjusted away from resonance.

Operation Below Resonance (Fig. 4b)

Here the resonant current has fallen to the value of the magnetizing current before the end of the driving pulse width, causing the power transfer to cease even though the magnetizing current continues. Operation below the series resonant frequency can still achieve primary ZVS and obtain the soft commutation of the rectifier diodes on the secondary side. The secondary-side diodes are in discontinuous current mode and require more circulating current in the resonant circuit to deliver the same amount of energy to the load. This additional current results in higher conduction losses in both the primary and the secondary sides. However, one characteristic that should be noted is that the primary ZVS may be lost if the switching frequency becomes too low. This will result in high switching losses and several associated issues. This will be explained further later.

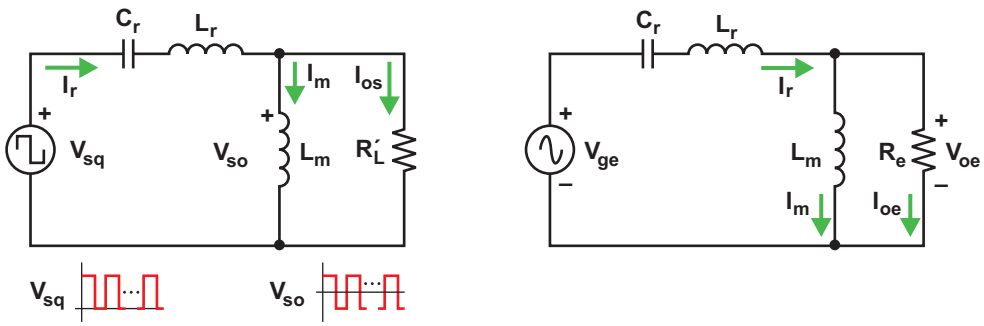
Operation Above Resonance (Fig. 4c)

In this mode the primary side presents a smaller circulating current in the resonant circuit. This reduces conduction loss because the resonant circuit's current is in continuous-current mode, resulting in less RMS current for the same amount of load. The rectifier diodes are not softly commutated and reverse recovery losses exist, but operation above the resonant frequency can still achieve primary ZVS. Operation above the resonant frequency may cause significant frequency increases under light-load conditions.

The foregoing discussion has shown that the converter can be designed by using either $f_{sw} \geq f_0$ or $f_{sw} \leq f_0$, or by varying f_{sw} on either side around f_0. Further discussion will show that the best operation exists in the vicinity of the series resonant frequency, where the benefits of the LLC converter are maximized. This will be the design goal.

C. Modeling an LLC Half-Bridge Converter

To design a converter for variable-energy transfer and output-voltage regulation, a voltage-transfer function is a must. This transfer function, which in this topic is also called the input-to-output voltage gain, is the mathematical relationship between the input and output voltages. This section will show how the gain formula is developed and what the characteristics of the gain are. Later the gain formula obtained will be used to describe the design procedure for the LLC resonant half-bridge converter.



a. Nonlinear nonsinusoidal circuit. *b. Linear sinusoidal circuit.*

Fig. 5. Model of LLC resonant half-bridge converter.

Traditional Modeling Methods Do Not Work Well

To develop a transfer function, all variables should be defined by equations governed by the LLC converter topology shown in Fig. 5a. These equations are then solved to get the transfer function. Conventional methods such as state-space averaging have been successfully used in modeling pulse-width-modulated switching converters, but from a practical viewpoint they have proved unsuccessful with resonant converters, forcing designers to seek different approaches.

Modeling with Approximations

As already mentioned, the LLC converter is operated in the vicinity of series resonance. This means that the main composite of circulating current in the resonant network is at or close to the series resonant frequency. This provides a hint that the circulating current consists mainly of a single frequency and is a pure sinusoidal current. Although this assumption is not completely accurate, it is close—especially when the square wave's switching cycle corresponds to the series resonant frequency. But what about the errors?

If the square wave is different from the series resonance, then in reality more frequency components are included; but an approximation using the single fundamental harmonic of the square wave can be made while ignoring all higher-order harmonics and setting possible accuracy issues aside for the moment. This is the so-called first harmonic approximation (FHA) method, now widely used for resonant-converter design. This method produces acceptable design results as long as the converter operates at or close to the series resonance.

The FHA method can be used to develop the gain, or the input-to-output voltage-transfer function. The first steps in this process are as follows:

- Represent the primary-input unipolar square-wave voltage and current with their fundamental components, ignoring all higher-order harmonics.
- Ignore the effect from the output capacitor and the transformer's secondary-side leakage inductance.
- Refer the obtained secondary-side variables to the primary side.
- Represent the referred secondary voltage, which is the bipolar square-wave voltage (V_{so}), and the referred secondary current with only their fundamental components, again ignoring all higher-order harmonics.

With these steps accomplished, a circuit model of the LLC resonant half-bridge converter in Fig. 5a can be obtained (Fig. 5b). In Fig. 5b, V_{ge} is the fundamental component of V_{sq}, and V_{oe} is the fundamental component of V_{so}. Thus, the nonlinear and nonsinusoidal circuit in Fig. 5a is approximately transformed into the linear circuit of Fig. 5b, where the AC resonant circuit is excited by an effective sinusoidal input source and drives an equivalent resistive load. In this circuit model, both input voltage V_{ge} and output voltage V_{oe} are in sinusoidal form with the same single frequency—i.e., the fundamental component of the square-wave voltage (V_{sq}), generated by the switching operation of Q1 and Q2.

This model is called the resonant converter's FHA circuit model. It forms the basis for the

design example presented in this topic. The voltage-transfer function, or the voltage gain, is also derived from this model, and the next section will show how. Before that, however, the electrical variables and their relationships as used in Fig. 5b need to be obtained.

Relationship of Electrical Variables

On the input side, the fundamental voltage of the square-wave voltage (V_{sq}) is

$$v_{ge}(t) = \frac{2}{\pi} \times V_{DC} \times \sin(2\pi f_{sw} t), \quad (3)$$

and its RMS value is

$$V_{ge} = \frac{\sqrt{2}}{\pi} \times V_{DC}. \quad (4)$$

On the output side, since V_{so} is approximated as a square wave, the fundamental voltage is

$$v_{oe}(t) = \frac{4}{\pi} \times n \times V_o \times \sin(2\pi f_{sw} t - \varphi_V), \quad (5)$$

where φ_V is the phase angle between V_{oe} and V_{ge}, and the RMS output voltage is

$$V_{oe} = \frac{2\sqrt{2}}{\pi} \times n \times V_o. \quad (6)$$

The fundamental component of current corresponding to V_{oe} and I_{oe} is

$$i_{oe}(t) = \frac{\pi}{2} \times \frac{1}{n} \times I_o \times \sin(2\pi f_{sw} t - \varphi_i), \quad (7)$$

where φ_i is the phase angle between i_{oe} and v_{oe}, and the RMS output current is

$$I_{oe} = \frac{\pi}{2\sqrt{2}} \times \frac{1}{n} \times I_o. \quad (8)$$

Then the AC equivalent load resistance, R_e, can be calculated as

$$R_e = \frac{V_{oe}}{I_{oe}} = \frac{8 \times n^2}{\pi^2} \times \frac{V_o}{I_o} = \frac{8 \times n^2}{\pi^2} \times R_L. \quad (9)$$

Since the circuit in Fig. 5b is a single-frequency, sinusoidal AC circuit, the calculations can be made in the same way as for all sinusoidal circuits. The angular frequency is

$$\omega_{sw} = 2\pi f_{sw}, \quad (10)$$

which can be simplified as

$$\omega = \omega_{sw} = 2\pi f_{sw}. \quad (11)$$

The capacitive and inductive reactances of C_r, L_r, and L_m, respectively, are

$$X_{C_r} = \frac{1}{\omega C_r}, \; X_{L_r} = \omega L_r, \text{ and } X_{L_m} = \omega L_m. \quad (12)$$

The RMS magnetizing current is

$$I_m = \frac{V_{oe}}{\omega L_m} = \frac{2\sqrt{2}}{\pi} \times \frac{n \times V_o}{\omega L_m}. \quad (13)$$

The circulating current in the series resonant circuit is

$$I_r = \sqrt{I_m^2 + I_{oe}^2}. \quad (14)$$

With the relationships of the electrical variables established, the next step is to develop the voltage-gain function.

D. Voltage-Gain Function

Naturally, the relationship between the input voltage and output voltage can be described by their ratio or gain:

$$M_{g\_DC} = \frac{n \times V_o}{V_{in}/2} = \frac{n \times V_o}{V_{DC}/2} \quad (15)$$

As described earlier, the DC input voltage and output voltage are converted into switching mode, and then Equation (15) can be approximated as the ratio of the bipolar square-wave voltage (V_{so}) to the unipolar square-wave voltage (V_{sq}):

$$M_{g\_DC} \approx M_{g\_sw} = \frac{V_{so}}{V_{sq}} \quad (16)$$

The AC voltage ratio, M_{g_AC}, can be approximated by using the fundamental components, V_{ge} and V_{oe}, to respectively replace V_{sq} and V_{so} in Equation (16):

$$\begin{aligned} M_{g\_DC} &= \frac{n \times V_o}{V_{in}/2} \approx M_{g\_sw} \\ &= \frac{V_{so}}{V_{sq}} \approx M_{g\_AC} = \frac{V_{oe}}{V_{ge}} \end{aligned} \quad (17)$$

To simplify notation, M_g will be used here in place of M_{g_AC}. From Fig. 5b, the relationship between V_{oe} and V_{ge} can be expressed with the electrical parameters L_r, L_m, C_r, and R_e. Then the input-to-output voltage-gain or voltage-transfer function becomes

$$M_g = \frac{V_{oe}}{V_{ge}} = \left| \frac{jX_{L_m} \parallel R_e}{(jX_{L_m} \parallel R_e) + j(X_{L_r} - X_{C_r})} \right| = \left| \frac{(j\omega L_m) \parallel R_e}{(j\omega L_m) \parallel R_e + j\omega L_r + \frac{1}{j\omega C_r}} \right|, \quad (18)$$

where $j = \sqrt{-1}$.

Equation (18) depicts a connection from the input voltage (V_{in}) to the output voltage (V_o) established in relation to M_g with LLC-circuit parameters. Although this expression is only approximately correct, in practice it is close enough to the vicinity of series resonance. Accepting the approximation as accurate allows Equation (19) to be written:

$$V_o = M_g \times \frac{1}{n} \times \frac{V_{in}}{2}. \quad (19)$$

In other words, output voltage can be determined after M_g, n, and V_{in} are known.

Normalized Format of Voltage-Gain Function

The voltage-gain function described by Equation (18) is expressed in a format with absolute values. It is difficult to give a general description of design issues with such a format. It would be better to express it in a normalized format. To do this, the series resonant frequency (f_0) can be selected as the base for normalization. Then the normalized frequency is expressed as

$$f_n = \frac{f_{sw}}{f_0}. \quad (20)$$

Further, to combine two inductances into one, an inductance ratio can be defined as

$$L_n = \frac{L_m}{L_r}. \quad (21)$$

The quality factor of the series resonant circuit is defined as

$$Q_e = \frac{\sqrt{L_r / C_r}}{R_e}. \quad (22)$$

Notice that f_n, L_n, and Q_e are no-unit variables.

With the help of these definitions, the voltage-gain function can then be normalized and expressed as

$$M_g = \left| \frac{L_n \times f_n^2}{[(L_n + 1) \times f_n^2 - 1] + j[(f_n^2 - 1) \times f_n \times Q_e \times L_n]} \right|. \quad (23)$$

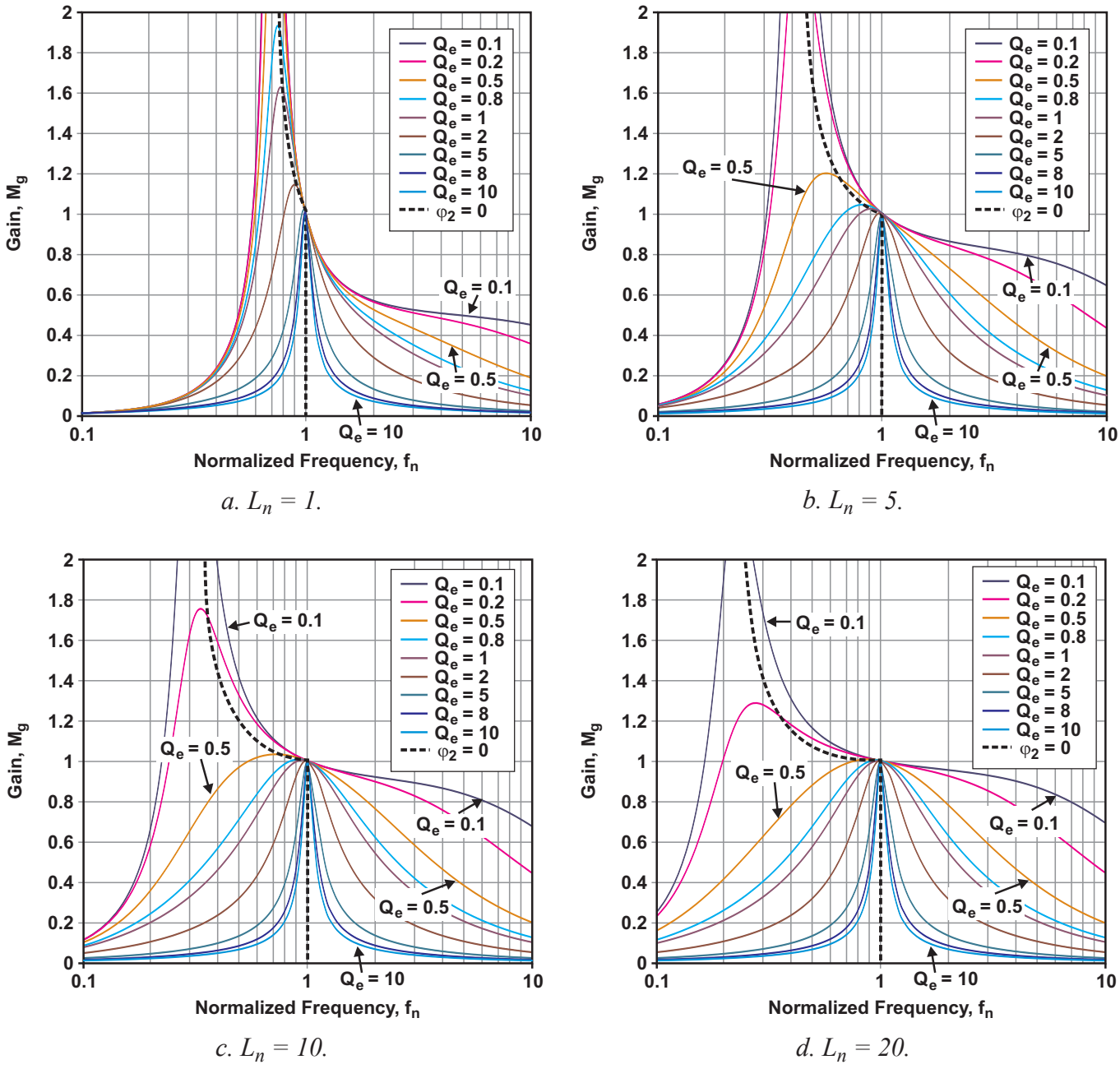
The relationship between input and output voltages can also be obtained from Equation (23):

$$V_o = M_g \times \frac{1}{n} \times \frac{V_{in}}{2} = M_g(f_n, L_n, Q_e) \times \frac{1}{n} \times \frac{V_{DC}}{2}, \quad (24)$$

where $V_{in} = V_{DC}$.

Behavior of the Voltage-Gain Function

The voltage-gain function expressed by Equation (23) and the circuit model in Fig. 5b form the basis for the design method described in this topic; therefore it is necessary to understand how M_g behaves as a function of the three factors f_n, L_n, and Q_e. In the gain function, frequency f_n is the control variable. L_n and Q_e are dummy variables, since they are fixed after their physical parameters are determined. M_g is adjusted by f_n after a design is complete. As such, a good way to explain how the gain function behaves is to plot M_g with respect to f_n at given conditions from a family of values for L_n and Q_e.



a. L_n = 1. *b. L_n = 5.*

c. L_n = 10. *d. L_n = 20.*

Fig. 6. Plots of voltage-gain function (M_g) with different values of L_n.

Figs. 6a to 6d illustrate several possible relationships. Each plot is defined by a fixed value for L_n (L_n = 1, 5, 10, or 20) and shows a family of curves with nine values, from 0.1 to 10, for the variable Q_e. From these plots, several observations can be made.

The value of M_g is not less than zero. This is obvious since M_g is from the modulus operator, which depicts a complex expression containing both real and imaginary numbers. These numbers represent both magnitude and phase angle, but only the magnitude is useful in this case.

Within a given L_n and Q_e, M_g presents a convex curve shape in the vicinity of the circuit's resonant frequency. This is a typical curve that shows the shape of the gain from a resonant converter. The normalized frequency corresponding to the resonant peak (f_{n_c0}, or $f_{sw} = f_{c0}$) is moving with respect to a change in load and thus to a change in Q_e for a given L_n.

Changing L_n and Q_e will reshape the M_g curve and make it different with respect to f_n. As Q_e is a function of load described by Equations (9) and (22), M_g presents a family of curves relating frequency modulation to variations in load.

Regardless of which combination of L_n and Q_e is used, all curves converge and go through the point of $(f_n, M_g) = (1, 1)$. This point is at $f_n = 1$, or $f_{sw} = f_0$ from Equation (20). By definition of series resonance, $X_{L_r} - X_{C_r} = 0$ at f_0. In other words, the voltage drop across L_r and C_r is zero, so that the input voltage is applied directly to the output load, resulting in a unity voltage gain of $M_g = 1$.

Notice that the operating point $(f_n, M_g) = (1, 1)$ is independent of the load; i.e., as long as the gain (M_g) can be kept as unity, the switching frequency will be at the series resonant frequency (f_0) no matter what the load current is. In other words, in a design whose operating point is at $(f_n, M_g) = (1, 1)$ or its vicinity, the frequency variation is narrowed down to minimal. At $(f_n, M_g) = (1, 1)$, the impedance of the series resonant circuit is zero, assuming there are no parasitic power losses. The entire input voltage is then applied to the output load no matter how much the load current varies. However, away from $(f_n, M_g) = (1, 1)$, the impedance of the series resonant circuit becomes nonzero, the voltage gain changes with different load impedances, and the corresponding operation becomes load-dependent.

For a fixed L_n, increasing Q_e shrinks the curve, resulting in a narrower frequency-control band, which is expected since Q_e is the quality factor of the series resonant circuit. In addition, as the whole curve shifts lower, the corresponding peak value of M_g becomes smaller, and the f_n corresponding to that value moves towards the right and closer to $f_n = 1$. This frequency shift with increasing Q_e is due to an increased load. It is apparent from reviewing Equations (9) and (22) that an increase in Q_e may come from a reduction in R_L, as both L_m and L_r are fixed. For the same series resonant frequency, C_r is fixed as well. R_L is in parallel with L_m, so reducing R_L will reduce the effect of L_m and shift f_{c0} towards f_0. As a simple illustration, it is helpful to examine two extremes:

1. If R_L is open, then $Q_e = 0$, and $f_{c0} = f_p$ as described by Equation (2). f_{c0} sits to the far left of f_0, and the corresponding gain peak is very high and can be infinite in theory.
2. If R_L is shorted, then $Q_e = \infty$ and L_m is completely bypassed or shorted, making the effect of L_m on the gain disappear. The corresponding peak gain value from the L_m effect then becomes zero, and f_{c0} moves all the way to the right, overlapping f_0.

   Therefore, if R_L changes from infinite to zero, the resonant peak gain changes from infinite to unity, and the corresponding frequency at peak resonance (f_{c0}) moves from f_p to the series resonant frequency (f_0).

For a fixed Q_e, a decrease in L_n shrinks the curve; the whole curve is squeezed, and f_{c0} moves towards f_0. This results in a better frequency-control band with a higher peak gain. There are two reasons for this. First, as L_n decreases due to the decrease in L_m, f_p gets closer to f_0, which squeezes the curves from f_p to f_0. Second, a decreased L_n increases L_r, resulting in a higher Q_e. A higher Q_e shrinks the curve as just described.

At first glance, it appears that any combination of L_n and Q_e would work for a converter design and that the design could be made with f_n operating on either side of $f_n = 1$. However, as explained in the following section, there are many more considerations.

III. Design Considerations

As discussed earlier, f_n is the control variable in frequency modulation. Therefore the output voltage can be regulated by M_g through controlling f_n, as indicated by Fig. 6 and Equation (24), which can be rearranged as

$$V_o = M_g(f_n, L_n, Q_e) \times \frac{1}{n} \times \frac{V_{in}}{2}. \qquad (25)$$

Although this discussion has so far determined that the design should operate in the vicinity of the series resonance, or near $f_n = 1$, it is recommended that the optimum design be restricted to the area described by a1 through a4 in Fig. 7, for reasons to be explained.

A. What Does "In the Vicinity" Mean?

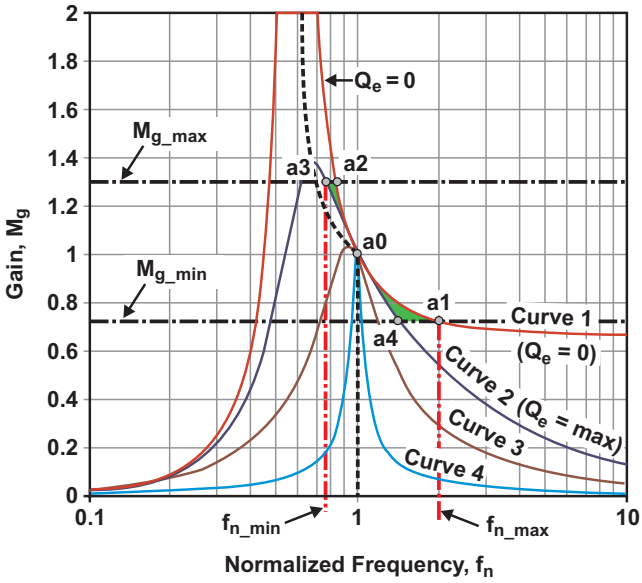
Obviously, "in the vicinity" is a loose designation; but, as stated before in the discussion of the FHA concept, if a pure sinusoidal current flowing through the resonant circuit is assumed, and if the circuit is made to operate at the exact location of f_0, then the design result is accurate. This can also be verified easily by a bench test or a computer simulation, but so far there is no verification in theory. A potential insight into such verification can be made through Equation (19). Assigning a value of 1 to M_g in Equation (19) as an indication of operation at $f_n = 1$ will remove the approximations made to Equation (17). A precise relationship is then achieved between the DC input and DC output as described by Equation (15).

A design that operates only at f_0 certainly cannot be made, but when it includes operating frequencies away from f_0, it starts to show errors when compared with bench-test measurements. So the common understanding in an FHA design approach is that it can help to create an initial design, with all design variables retaining their clear physical concepts and meanings, which is important in order for designers to understand the behavior of the LLC converter. However, it should be expected that some bench testing to optimize and finalize the design may be necessary. This could be an iterative process, but computer-based circuit simulation will save iteration cycles. As a matter of fact, computer simulation plays an important role in LLC-converter design after an initial design is made with the FHA approach.

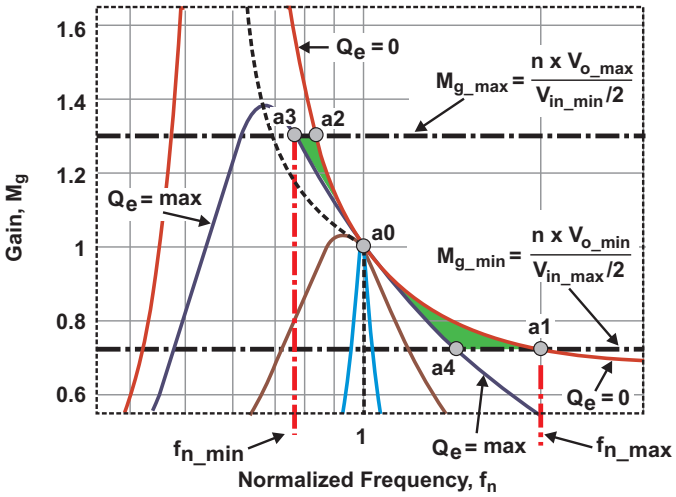
B. Basic Design Requirements

For a typical design of a power-supply converter, as is well-known, three basic requirements are almost always considered first—line regulation, load regulation, and efficiency.

Line regulation is defined as the maximum output-voltage variation caused by an input-voltage variation over a specified range, at a given output load current.



a. In the vicinity of series resonance (near $f_n = 1$).



b. Operation boundary set by a1 through a4.

Fig. 7. Recommended design area.

Load regulation is defined as the maximum output-voltage variation caused by a change in load over a stated range, usually from no load to maximum.

These two types of regulation are actually achieved through the voltage-gain adjustment—and in an LLC converter, the gain adjustment is made through frequency modulation. The recommended area of operation described in Fig. 7 shows a

relatively steep slope for the gain, which can narrow the range of the frequency modulation. As such, a design has to make the gain adequately adjustable in a range that meets the required regulating specifications.

Efficiency is one big benefit of using an LLC converter. The converter's switching losses can be reduced significantly by ensuring that primary-side ZVS is maintained over the whole operating range. As will be explained, ZVS cannot be achieved everywhere in the gain-plot area, but keeping the design within the recommended region will ensure ZVS.

Line Regulation

Achieving line regulation for the design of a power-supply converter can be based on Equation (25) and the recommended design areas in Fig. 7. A minimum and maximum output voltage, V_{o_min} and V_{o_max}, respectively, will be assumed. To simplify the discussion, it will also be assumed that all parasitic voltage drops—for example, from PCB traces, the MOSFET's R_{ds_on}, the diode's forward voltage, etc.—are already converted or lumped into a part of the output-voltage range. It will also be assumed that the design requires a maximum switching-frequency range; i.e., that it is limited within $f_{n\_min} \le f_n \le f_{n\_max}$. In reality, the frequency limits may need adjustment in order to adapt the line- and load-regulation requirements, or vice versa.

With these conditions and assumptions, to achieve line regulation (and load regulation as discussed later), M_g should be designed to meet the conditions described by Equation (26), which says that all possible M_g values must contain the value of both M_{g_min} and M_{g_max} within the f_n limits. For $I_o = 0$,

$$\{M_g \,|\, M_g > M_{g\_\infty}\} \supset \{M_{g\_min}, M_{g\_max}\}, \quad (26a)$$

and for $I_o > 0$,

$$\{M_g \,|\, M_g \ge 0\} \supset \{M_{g\_min}, M_{g\_max}\}, \quad (26b)$$

where

$$M_{g\_min} = \frac{n \times V_{o\_min}}{V_{in\_max}/2}, \quad (27)$$

$$M_{g\_max} = \frac{n \times V_{o\_max}}{V_{in\_min}/2}, \quad (28)$$

and

$$M_{g\_\infty} = \left|\frac{L_n}{L_n + 1}\right|. \quad (29)$$

M_{g_∞} is a special value of M_g that presents the gain value at no load when f_n is approaching infinity. In other words, at no load, the gain curve (M_g) is approaching an asymptotic horizontal line with its value described by Equation (29), which can be easily obtained from Equation (23) when the value of f_n approaches infinity.

M_{g_min} and M_{g_max} each form a horizontal line in Fig. 7. For the no-load condition ($I_o = 0$), the quality factor (Q_e) equals zero, shown in Fig. 7a as Curve 1. Since the gain curves are determined by L_n and Q_e, and $Q_e = 0$, L_n is the sole design factor at this stage. As such, a value for L_n needs to be selected that will provide a gain curve that meets the conditions of Equation (26). In other words, the value of L_n needs to make Curve 1 cross over the two horizontal lines defined by Equations (27) and (28) inside the frequency limits. This is depicted in Fig. 7 by design points a1 and a2.

Similarly, if the load condition is not zero ($I_o > 0$), then an appropriate curve can be selected by making Q_e correspond to the required maximum load and following the same process.

Load Regulation

Normal Load Operation

As illustrated in Fig. 7, the gain presents a family of curves. For a fixed L_n, each value for Q_e generates a different gain curve. A bigger Q_e makes the gain curve shift lower with a lower peak. As such, when load current increases, the gain curve moves away from its no-load shape (Curve 1) to a lower representation. In Fig. 7, Curve 2 corresponds to the maximum load current (Q_e = max) while still meeting the conditions of Equation (26) with the same L_n. This yields design points a3 and a4 in the recommended design area.

If the load is increased further, Curve 2 will be reshaped towards Curve 3. Horizontal line M_{g_max} will not be able to cross over with the gain curve,

so the conditions of Equation (26) cannot be met. Output-voltage regulation is then lost. When this happens, a design modification will be needed, such as adjusting L_n or the switching-frequency limits to reshape the gain curve.

Since Q_e is associated with the load current, it is appropriate to extend this discussion to include the possibility of overload and short-circuit conditions.

Overload Current

In the example, the recommended design area in Fig. 7 includes an overload because Q_{e_max} was defined to include a value for it. As stated earlier, any further increase in load causes Curve 2 to move towards Curve 3 or beyond, which places the design outside of the design area and towards the condition of a short circuit.

Load Short Circuit

Since a load short circuit causes a potentially excessive amount of current in the converter circuit, it is necessary to examine the gain plot of a load short circuit to know what happens and how to deal with it. The corresponding gain plot is shown by Curve 4 in Fig. 7a. f_{c0} will become f_0 when L_m is bypassed by a load short circuit, and this defines Curve 4 as the gain shape with a shorted output.

Curve 4 provides insight into possible solutions for protecting the LLC converter. One possibility is to increase the switching frequency to reduce the gain. Based on Figs. 6 and 7, if the switching frequency is increased to more than two times the series resonant frequency (f_0), the gain will be reduced to below 10%. If the frequency can be pulled up to ten times f_0, the gain becomes practically zero. From Equation (25) it can be seen that a zero gain transfers a zero percentage of input voltage to the load short circuit. In this way, the converter can be protected from a load short-circuit fault.

However, it is worth noting that the effectiveness of such a protection method depends on how quickly the short-circuit signal can be sent to the controller to activate the frequency increase. In the recommended design area, the gain will inevitably be forced to the left side of the resonant peak for some time until it eventually reaches Curve 4. This could cause several severe issues, including the possibility of a polarity reversal of the feedback control. Considering this, an independent overcurrent shutdown may be a preferable solution. However, if a frequency increase is still preferred, two other possible solutions are recommended. Either (1) add a separate high-speed control loop to rapidly initiate the frequency shift, or (2) shift the recommended design area to where the minimum switching frequency (f_{n_min}) is never less than the series resonant frequency (f_0)—i.e., to where $f_{n\_min} \geq 1$.

Zero-Voltage Switching (ZVS)

A major benefit of the LLC converter topology is its potential for significantly reduced switching losses, primarily achieved through primary-side ZVS; however, as stated earlier, it is ZVS considerations that drive the recommended design area to be only on the right side of the resonant gain curves in Fig. 7. This section discusses how ZVS is achieved and why it affects the design area.

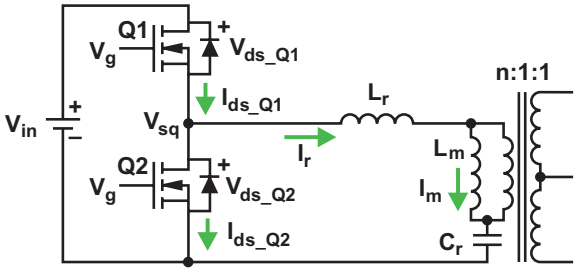
Achieving ZVS

To achieve ZVS, a MOSFET is turned on only after its source voltage, V_{ds}, has been reduced to zero by external means. One way of ensuring this

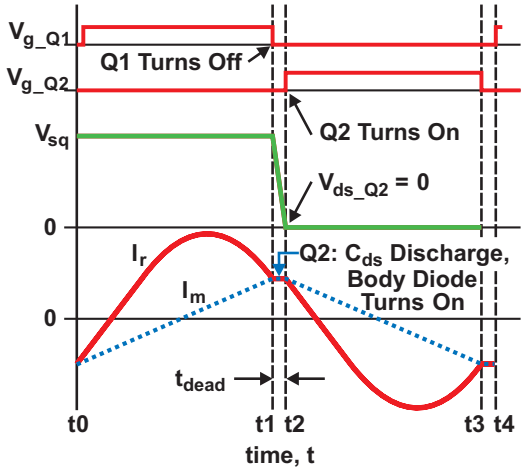
is to force a reversal of the current flowing through the MOSFET's body diode while a gate-drive turn-on signal is applied (see Fig. 8).

As shown in Fig. 8, when Q1 turns off at t1, the Q2 gate's turn-on drive signal is not applied until t2, such that there exists a dead time, t_{dead}, from t1 to t2. During t_{dead}, the current in the resonant circuit (I_r) is diverted from Q1 to Q2, first discharging Q2's drain-to-source capacitance, C_{ds}, to make its voltage zero, and then forward biasing Q2's body diode. At t2, conduction through the Q2 body diode maintains zero V_{ds_Q2} (ignoring the Q2 body diode's forward-voltage drop) until the Q2 gate's turn-on drive signal is applied. So the critical condition is when Q1 turns off. A nonzero current (I_r) should still continue in its same direction as when Q1 was on, normally accomplished by external circuit inductance. And, of course, the same conditions are necessary for a Q1 ZVS turn-on.

Since there is inductive impedance, the circuit's current lags behind its applied voltage. To achieve ZVS, the designer must determine the conditions



a. LLC resonant circuit.



b. ZVS timing waveform.

Fig. 8. ZVS operation.

where the input impedance, Z_{in} (shown in Fig. 9a), can be inductive, making the circuit's I_r lag behind its V_{ge}.

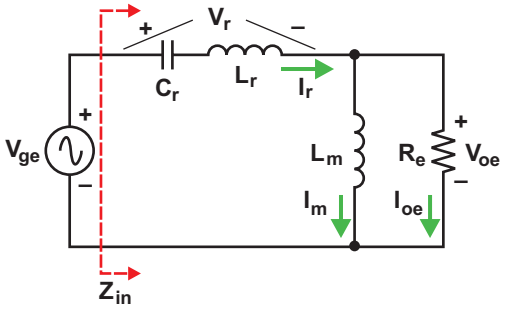
Z_{in} can be expressed in its polar form:

$$Z_{in} = |Z_{in}| e^{j\varphi_z}, \tag{30a}$$

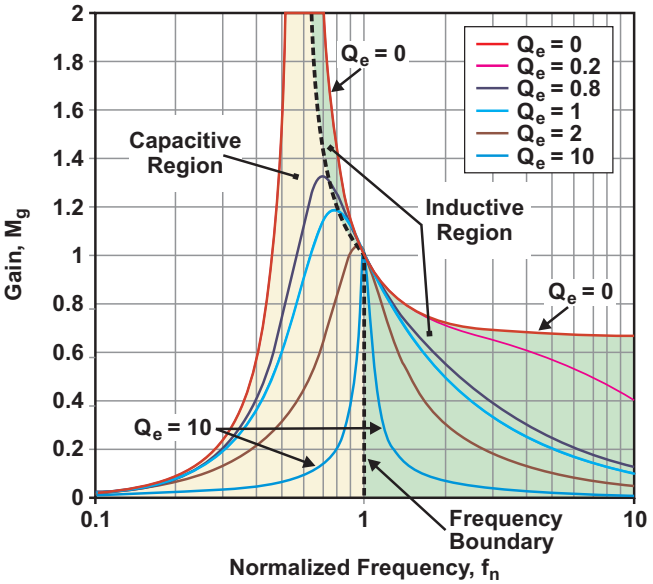
where φ_z is the phase angle between I_r and V_{ge}. From Equation (30a), it is apparent that Z_{in} varies in relation to φ_z ($-\pi/2 \le \varphi_z \le \pi/2$):

- When $\varphi_z > 0$, the impedance is inductive.
- When $\varphi_z < 0$, the impedance is capacitive.
- When $\varphi_z = 0$, the impedance is resistive.

The φ_z angle is a function of frequency, or switching frequency in this case. As such, a frequency boundary formed by the locus of the resonant peaks corresponds to $\varphi_z = 0$ and is the dividing line between the capacitive and inductive regions (see Fig. 9b). Therefore, ZVS can be

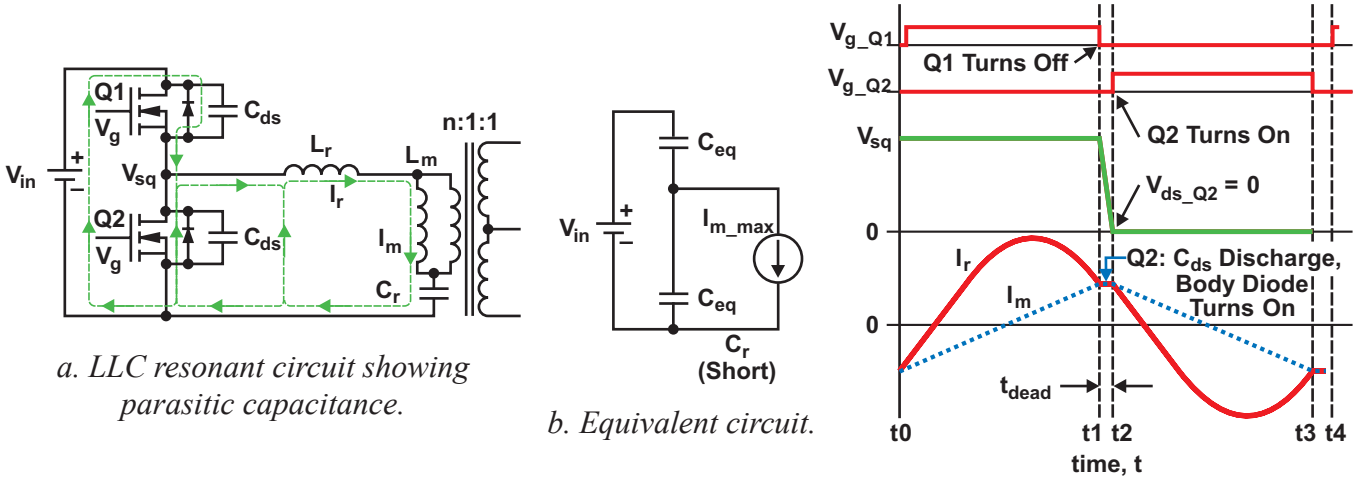


a. Input impedance.



b. Gain regions.

Fig. 9. LLC resonant circuit.



a. LLC resonant circuit showing parasitic capacitance.

b. Equivalent circuit.

c. ZVS timing waveform.

Fig. 10. Obtaining sufficient inductive energy for ZVS.

achieved only when the converter's input phase angle is greater than zero:

$$\varphi_z = \angle(|Z_{in}|e^{j\varphi_z}) > 0 \qquad (30b)$$

All resonant peaks corresponding to f_{c0} are in the capacitive region, although the boundary line is very close to the peaks. To distinguish resonant peaks from the gain values on the resonant boundary, the gain values on the frequency boundary are defined as attainable peak-gain values, denoted as M_{g_ap}. Practically, though, M_{g_ap} is usually very close to M_{g_peak}, where

$$M_{g\_peak} = M_g\big|_{f=f_{c0}} \qquad (31)$$

and f_{c0} is the frequency when the maximum value of M_g is achieved from Equation (18) or (23) during a frequency sweep from zero to infinity with a given L_m, L_r, C_r, and R_e.

From Fig. 7, it is clear that the recommended operating area, a1 through a4, is in the inductive region; so the design example should achieve ZVS. Although this is true, it is worth pointing out that the recommendation is only a condition necessary to ensure ZVS. There must also be sufficient inductive energy for the converter to operate with ZVS.

Ensuring Sufficient Inductive Energy

To realize sufficient inductive energy for ZVS, it is necessary to understand how ZVS is achieved in the inductive region. Fig. 10 can be used to describe the ZVS mechanism. During the dead-time interval between t1 and t2 (t_{dead}), the resonant circuit's current (I_r) equals the magnetizing current (I_m). I_m is by nature sinusoidal. In t_{dead}, I_m is circulating through the capacitances (C_{ds}) of Q1 and Q2 before Q2's body diode begins to conduct. In t_{dead}, the magnetic-field energy associated with I_m converts into the electric-field energy of the two capacitances; i.e., it charges up the C_{ds} of Q1 and discharges the C_{ds} of Q2 before Q2's body diode can turn on. C_r is much larger than $C_{ds} \times 2$, so any energy-conversion effect from C_r can be ignored. An equivalent circuit in t_{dead} can then be derived as shown in Fig. 10b. C_{eq} is used since parasitic capacitances exist in addition to $C_{ds} \times 2$. Hence, in order for the body diode of Q2 to be turned on within t_{dead}, the conditions in Equations (32a) and (32b) must be met:

$$\frac{1}{2}(L_m + L_r) \times I_{m\_peak}^2 \geq \frac{1}{2}(2C_{eq}) \times V_{in}^2 \qquad (32a)$$

$$t_{dead} \geq 16 \times C_{eq} \times f_{sw} \times L_m \qquad (32b)$$

Why the Capacitive Region Is Not Used

As already discussed, ZVS cannot be achieved in the capacitive region; and, without it, switching losses become high and the efficiency benefit of using an LLC converter is lost. Several additional issues arise if operation is allowed in the capacitive region:

- This region yields hard switching on the primary side, since ZVS is lost.
- Because of hard switching and a capacitive current, the primary-side MOSFET's body diodes present reverse-recovery losses, and these diodes are usually of a type with slow reverse recovery. The slow reverse recovery may allow severe shoot-through of the two primary MOSFETs, resulting in high current and causing the MOSFETs to fail.
- Even if the MOSFETs can be selected to tolerate shoot-through current caused by power dissipation from the reverse recovery, high current spikes are still present, leading to high EMI noise.
- The frequency relationship is reversed, which changes the feedback control to positive.

C. Selecting Design Parameters f_{sw}, n, L_n, and Q_e

With a better understanding of the gain behavior, it is now possible to move ahead and create the design. Thus far, all discussion has been based on knowing the values of f_{sw}, n, L_n, and Q_e and their potential effect on circuit operation; but, at the beginning of a design, nothing is known about these variables, so where does the designer start?

Selecting the Switching Frequency (f_{sw})

Acceptable switching frequency is usually defined for particular applications. For example, most off-line AC/DC applications require a switching frequency below 150 kHz for normal operation, and usually between 100 and 150 kHz as a rule of thumb. This is usually because conduction EMI testing starts at 150 kHz. Maintaining the switching frequency below the EMI test's lower boundary helps the application to pass the test. Therefore, circuit components corresponding to such a frequency range are usually well-developed, more available, and less expensive.

If a different frequency range is required for unique applications, there are several factors that may need consideration. As is well-known, the lower the switching frequency is, the bulkier the converter, and the less important switching losses and ZVS efficiency become. Conduction losses become dominant, making the LLC converter less attractive. A higher switching frequency makes the benefits of the LLC converter more pronounced, particularly in comparison with hard-switched converters. If the switching frequency is very high, additional factors may have to be considered, such as component availability and the associated additional cost; additional board-layout concerns; and additional switching losses despite MOSFET ZVS, such as magnetic-core losses. Also, the parasitic capacitance, C_w, of the transformer windings may begin to change the nature of the resonant gain curves, as shown in Fig. 11.

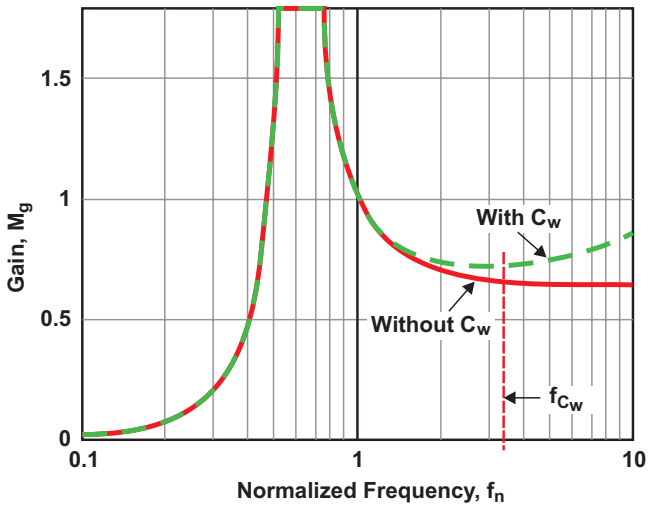


Fig. 11. Effect of transformer windings' parasitic capacitance (C_w) on gain function at high frequency.

Selecting the Transformer Turns Ratio (n)

As shown in Fig. 7, the gain magnitude in the recommended design area can be greater or smaller than unity. This provides flexibility in selecting the transformer turns ratio. Initially the gain can be set at unity ($M_g = 1$) for the output voltage at its middle value between V_{o_min} and V_{o_max}. This middle value can be called the output voltage's nominal value, V_{o_nom}, although the middle value may not necessarily always be the nominal value. Similarly, the input voltage's nominal value can be called V_{in_nom}. Then the transformer turns ratio

may be initially designed based on Equation (25):

$$n = M_g \times \frac{V_{in}/2}{V_o} = \frac{V_{in\_nom}/2}{V_{o\_nom}}\Bigg|_{M_g=1} \quad (33)$$

Selecting L_n and Q_e

Recall that in order to achieve line and load regulation across the operation range, the design must meet the conditions of Equation (26), which defines two horizontal lines crossing over two gain curves within frequency limits. Designing circuit parameters to select L_n and Q_e values that satisfy Equation (26) will be discussed next.

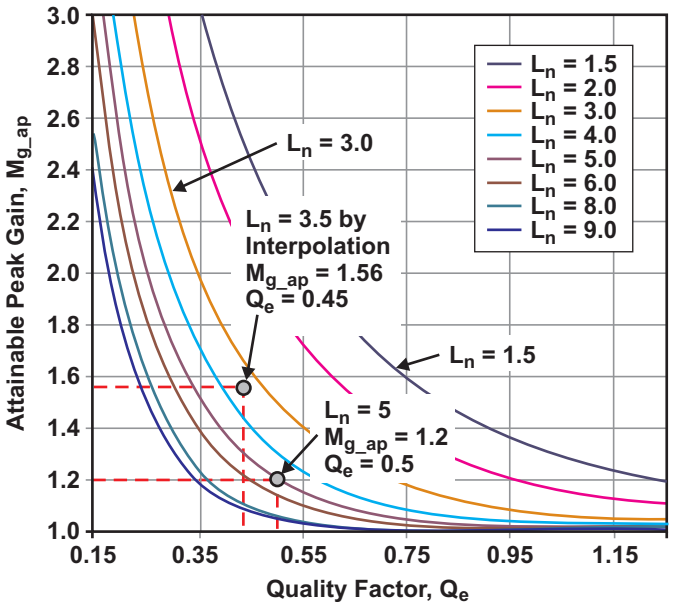
How Are the Proper L_n and Q_e Selected?

First, recall the discussion on Fig. 7. The most critical point for normal operation is the point a3. This point corresponds to Q_{e_max}, determined by the maximum load current. This point should be designed to avoid operation that would enter the capacitive region. Since a required maximum gain (M_{g_max}) can be determined from Equation (28), M_{g_max} can be plotted to the gain curves to obtain point a3 by finding the cross point between the M_{g_max} line and the gain curves. Because the gain curves are dependent on L_n and Q_e, several gain curves may need to be drawn to find a proper point a3. This is certainly one way to make the initial selection of L_n and Q_e, but it is a difficult way and most likely will require some wild guess.

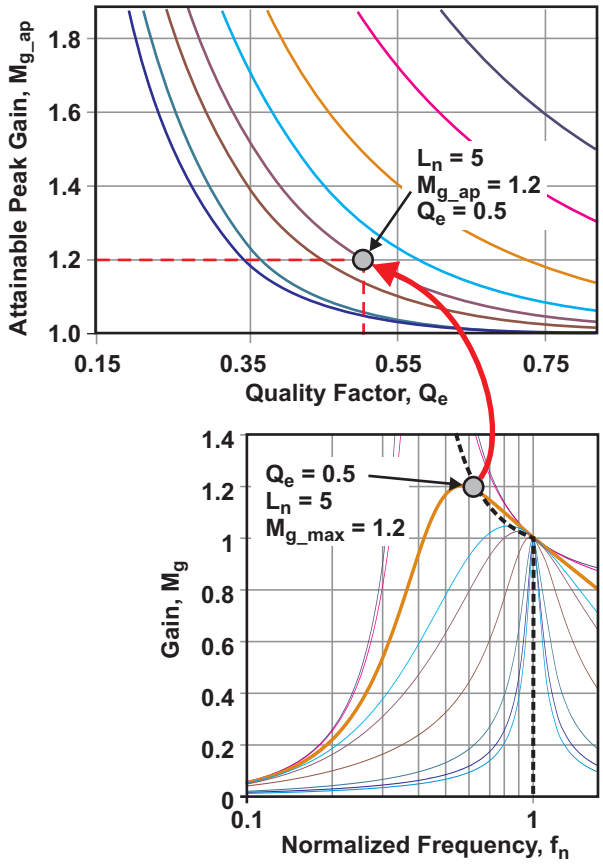
A more desirable approach is to create a common tool to represent the gain curves that can be shared and reused by different designs. Since the attainable peak gain (M_{g_ap}) corresponding to Q_{e_max} is the highest gain of concern for a design, gain-curve plots can be created beforehand to show M_{g_ap} with different values of L_n and Q_e. Then L_n and Q_e can be selected to achieve $M_{g\_ap} > M_{g\_max}$ based on a common tool—the M_{g_ap} curves. How this method is used will be described after a discussion of how the M_{g_ap} curves are obtained.

How Are the M_{g_ap} Curves Obtained?

The created M_{g_ap} curves are shown in Fig. 12a. The horizontal axis is Q_e and the vertical axis is M_{g_ap} with respect to a family of fixed values for L_n. Fig. 12b is used to illustrate how Fig. 12a is formed.



a. Peak-gain curves.



b. Obtaining peak-gain curves.

Fig. 12. Using peak-gain curves in a design.

From a plot of gain curves, for example from Fig. 6b, which is partially copied to the lower half of Fig. 12b, one attainable peak-gain value, M_{g_ap} = 1.2, can be located at the curve with (L_n, Q_e) = (5, 0.5). This point can be plotted to Fig. 12a at (M_{g_ap}, Q_e) = (1.2, 0.5). (Note that L_n = 5 at this point.) Because all curves in Fig. 6b have a fixed L_n = 5, that figure can be used to repeat the process with different Q_e values. Then a peak-gain curve can be formed as a function of Q_e with a fixed L_n = 5, shown in Fig. 12a. The process can be repeated for different L_n values of interest, producing the results in Fig. 12a.

How Are M_{g_ap} Curves Used in a Design?

With M_{g_max} already determined for a particular design from Equation (28), M_{g_max} can be plotted as a horizontal line on Fig. 12a. Any M_{g_ap} values above this line are greater than M_{g_max}, so the designed converter should operate in the inductive region. For example, for M_{g_max} = 1.2, any values of M_{g_ap} can be selected that are greater than 1.2, as shown in Fig. 12a. Then the selected value meets the maximum-gain requirement. From the selected M_{g_ap} value, L_n and Q_e values can then be selected. For example, selecting a value from the curve of L_n = 5 provides the L_n value right away. Since a gain value greater than M_{g_max} needs to be selected, Q_e would have to be less than 0.5, based on Fig. 12a. Similarly, a smaller L_n provides more gain and L_n can be selected by interpolating as shown in Fig. 12a. For example, if a value of 0.45 is selected for Q_e, the corresponding M_{g_ap} value with L_n = 3.5 would be 1.56 > M_{g_max} = 1.2, which satisfies the design requirements.

What L_n and Q_e Values Are Best if They Are All Greater than M_{g_max}?

Different applications may require the selection of unique values for L_n and Q_e to achieve an optimal design. However, LLC converters have some things in common that can be used to guide the selection:

- A smaller L_n can make the peak gain higher for a fixed Q_e, keeping the design's operation out of the capacitive region. Since L_n is a ratio of the magnetizing inductance (L_m) to the series resonant inductance (L_r), a smaller L_n usually results from a smaller L_m, and vice versa. Equation (13) indicates that a smaller L_m will introduce higher magnetizing current. This can help ZVS but will increase conduction losses.
- A smaller Q_e makes the peak gain higher while associated gain curves have a larger frequency variation for a given gain adjustment. A large Q_e results in a very low peak gain, which may not meet the design requirements.
- With these considerations in mind and from design practice, a good start is to select a value for L_n around 5 and for Q_e around 0.5 so that the corresponding gain curves will be neither too flat nor too steep.
- Reiteration is usually needed after an initial selection.

D. Peak-Gain Curves from a Bench Test

The attainable peak-gain curves shown in Fig. 12a were made from the gain function described by Equation (23), but Equation (23) was developed with approximations. These approximations allow errors in the peak-gain curves, causing accuracy concerns. To test the accuracy, a comparison was made between the gain function of Equation (23) and a bench test with a 135-kHz series resonant frequency. The peak-gain values were found to differ from those shown in Fig. 12a and from the gain curves shown in Fig. 6.

The comparison results are plotted in Fig. 13a. The solid line shows the result based on Equation (23), and the discrete points (▼) show the results from the bench test. This comparison supports the argument that the FHA-based gain function of Equation (23), while diverging for frequencies away from resonance, is accurate enough and acceptable in the vicinity of series resonance.

One other interesting observation is that the peak gain and attainable peak gain from the test are much larger than those obtained from the FHA-based gain function. Certainly this is good for a design, as it yields more design margin before operation enters the capacitive region. From this viewpoint, computer-based circuit simulation should be conducted to supplement an FHA design if more accuracy is desired prior to hardware implementation.

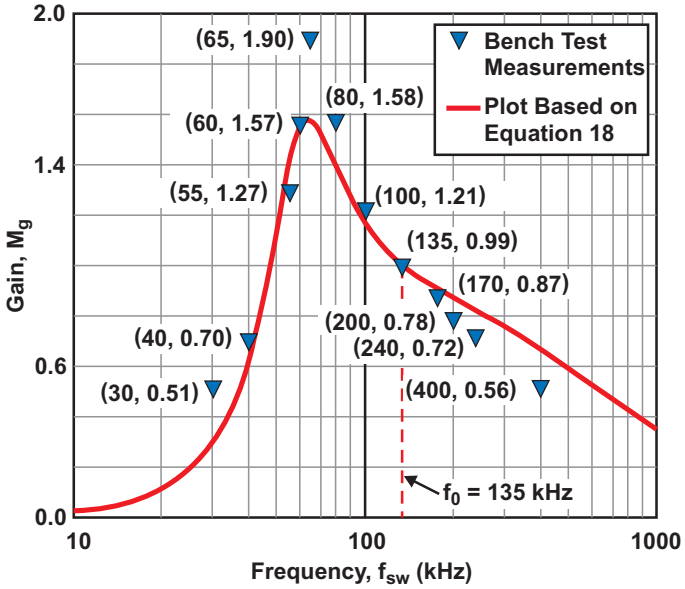
In practice, to reduce the potential effect of inaccuracy, peak-gain curves may be regenerated by experiment and/or by computer-based circuit simulation to replace the curves from Equation (23). Fig. 13b shows the peak-gain curves resulting from the experiment. Compared to Fig. 12a, Fig. 13b presents higher gain values. For example, for $L_n = 5$ and $Q_e = 0.5$, the attainable peak gain from Fig. 13b is $M_{g\_ap} = 1.65$, versus 1.2 from Fig. 12a.

E. Resonant-Network Design Flow

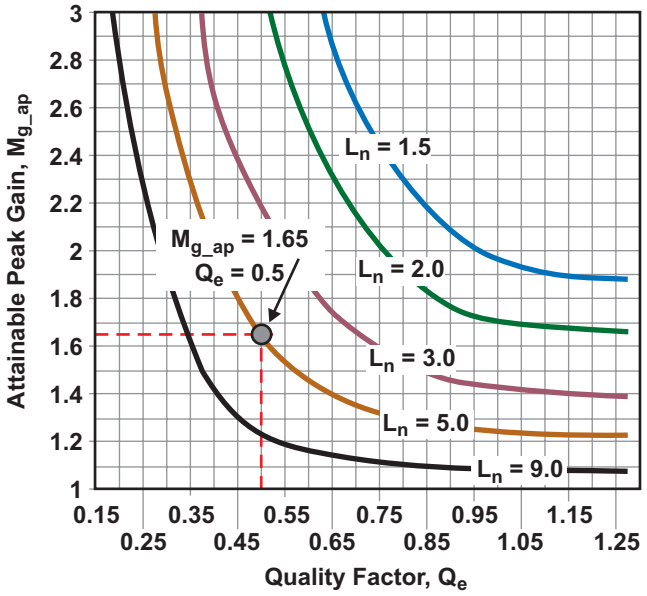
The design procedure that has been described can be summarized as follows:

- First, terminal voltages V_{o_min} and V_{in_max}, used in Equation (27), and V_{o_max} and V_{in_min}, used in Equation (28), must be taken from the converter specifications.
- Second, the transformer turns ratio (n) can be obtained from Equation (33). Then the two horizontal lines represented by M_{g_min} and M_{g_max} can be calculated. From the converter's load specifications, the load current with its corresponding resistance (R_L) can be obtained at any specified load condition. Then the AC equivalent load resistance (R_e) in the FHA circuit model can be determined from Equation (9).
- Third, two proper gain curves must be found that will cross over the two horizontal lines represented by M_{g_min} and M_{g_max} within selected or specified frequency limits. It is obvious that this can be done by selecting proper values for L_n and Q_e. After L_n and Q_e are obtained, the resonant circuit's parameters (C_r, L_r, and L_m) can be calculated based on Equations (22), (1), and (21), respectively:

$$C_r = \frac{1}{2\pi f_{sw} R_e Q_e}\Bigg|_{f_{sw} = f_0} \tag{34}$$



a. Comparison of FHA-based gain function and bench test.



b. Peak-gain curves from test.

Fig. 13. Peak-gain curves from experiment.

$$L_r = \left.\frac{1}{(2\pi f_{sw})^2 C_r}\right|_{f_{sw}=f_0} \quad (35)$$

$$L_m = L_n L_r \quad (36)$$

The design method can also be summarized with the flowchart shown in Fig. 14.

IV. Design Example

This section will demonstrate step-by-step how to use the described method to design an LLC resonant half-bridge converter. The design is oriented to applications with low output voltage, such as the ATX12 power supplies used in computers and servers, where energy conservation is important.

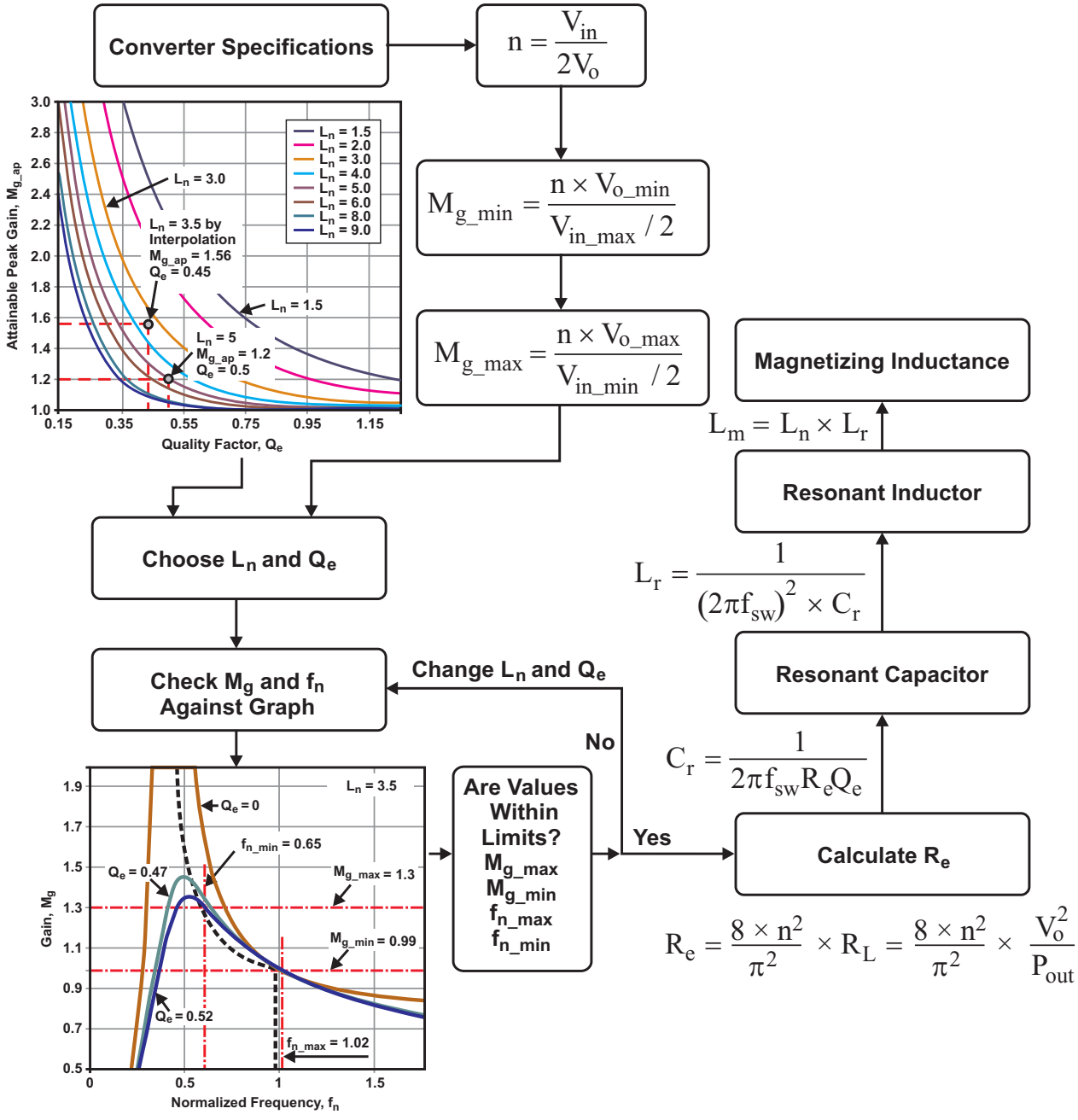


Fig. 14. Flowchart of resonant-network design.

The converter's electrical specifications are as follows:

- Input voltage: 375 to 405 VDC
- Rated output power: 300 W
- Output voltage: 12 VDC
- Rated output current: 25 A
- Output-voltage line regulation (I_o = 1.0 A): ≤ 1%
- Output-voltage load regulation (V_{in} = 390 V): ≤ 1%
- Output-voltage peak-to-peak ripple (V_{in} = 390 V and I_o = 25 A): ≤ 120 mV
- Efficiency (V_{in} = 390 V and I_o = 25 A): ≥ 90%
- Switching frequency (normal operation): 70 to 150 kHz

A. Block Diagram of Proposed Converter Circuit

A block diagram of the proposed circuit is shown in Fig. 15. For clarity, some auxiliary functions are not included. For the LLC resonant-mode controller, the UCC25600 can be a good choice. This eight-pin device has built-in, state-of-the-art, efficiency-boosting features and high-level protection features that provide a cost-effective solution. The step-by-step design demonstration will focus mainly on the power stage. For those interested in how to use and program the UCC25600, please refer to its data sheet (Reference [1]).

B. Design Steps

1. Determine Transformer Turns Ratio (n)

The transformer turns ratio is determined by Equation (33):

$$n = M_g \times \frac{V_{in}/2}{V_o} = \frac{V_{in\_nom}/2}{V_{o\_nom}}\bigg|_{M_g=1}$$

From the specifications, the nominal values for input voltage and output voltage are 390 V and 12 V, respectively, so the turns ratio can be calculated as

$$n = \frac{V_{in\_nom}/2}{V_{o\_nom}} = \frac{(390\ \text{V})/2}{12\ \text{V}} = 16.25 \Rightarrow 16.$$

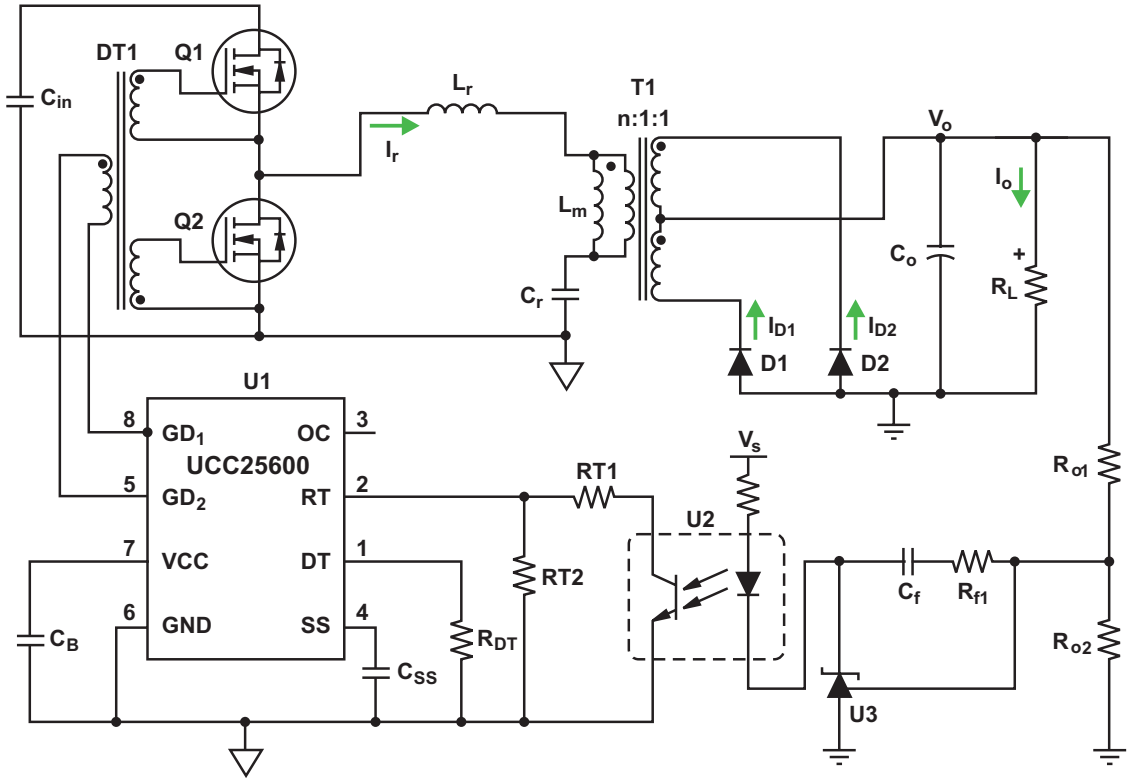


Fig. 15. Proposed circuit for the design example.

2. Determine M_{g_min} and M_{g_max}

M_{g_min} and M_{g_max} can be determined by using Equations (27) and (28), respectively:

$$M_{g\_min} = \frac{n \times (V_{o\_min} + V_F)}{V_{in\_max}/2}$$

$$= \frac{16 \times [12\ V \times (1-1\%) + 0.7\ V]}{(405\ V)/2} = 0.99$$

$$M_{g\_max} = \frac{n \times (V_{o\_max} + V_F + V_{loss})}{V_{in\_min}/2}$$

$$= \frac{16 \times [12\ V \times (1+1\%) + 0.7\ V + 1.05\ V]}{375/2}$$

$$= 1.18$$

In these calculations, 1% is used to adjust output voltage from the line and load regulation. V_F = 0.7 V is assumed for the secondary-side diode's forward-voltage drop. V_{loss} = 1.05 V is assumed for the voltage drop due to power losses. If the efficiency is assumed to be 92% (> 90% as required by the specifications), then 8% of the total power would be power losses. If all losses are referred to the output voltage, then 8% loss at 25 A would drop the output voltage to

$$\frac{\frac{300\ W}{92\%} \times 8\%}{25\ A} = 1.05\ V.$$

This is added to M_{g_max} to maintain voltage-load regulation.

To keep operation within the inductive region with an overload-current capability of 110%, M_{g_max} is increased from 1.18 to 1.18 × 110% = 1.30.

3. Select L_n and Q_e

From Fig. 12a, if the values L_n = 3.5 and Q_e = 0.45 are selected, the corresponding M_{g_ap} = 1.56, which is greater than M_{g_max} = 1.30. A curve for L_n = 3.5 is not shown in Fig. 12a, but it can be obtained by interpolating the curves of L_n = 3 and L_n = 4.

4. Determine the Equivalent Load Resistance (R_e) in Fig. 5b

R_e is determined from Equation (9). At full load,

$$R_e = \frac{8 \times n^2}{\pi^2} \times \frac{V_o}{I_o} = \frac{8 \times 16^2}{\pi^2} \times \frac{12\ V}{25\ A} = 99.7\ \Omega.$$

At 110% overload,

$$R_e = \frac{8 \times n^2}{\pi^2} \times \frac{V_o}{I_o} = \frac{8 \times 16^2}{\pi^2} \times \frac{12\ V}{25\ A \times 110\%} = 90.6\ \Omega.$$

5. Design Resonant Circuit's Parameters

The resonant circuit's parameters are determined from Equations (34), (35), and (36). A switching frequency of 130 kHz may be selected initially for the series resonant frequency, and then the resonant circuit's parameters can be calculated at full load:

$$C_r = \frac{1}{2\pi \times Q_e \times f_0 \times R_e}$$

$$= \frac{1}{2\pi \times 0.45 \times 130 \times 10^3\ Hz \times 99.7\ \Omega}$$

$$= 27.3\ nF \Rightarrow 12\ nF \times 2 + 3.3\ nF$$

$$L_r = \frac{1}{(2\pi \times f_0)^2 C_r}$$

$$= \frac{1}{(2\pi \times 130 \times 10^3\ Hz)^2 \times 27.3 \times 10^{-9}\ F}$$

$$= 54.9\ \mu H \Rightarrow 60\ \mu H$$

$$L_m = L_n \times L_r = 3.5 \times 60 = 210\ \mu H$$

6. Verify the Resonant-Circuit Design

The design parameters are as follows:

- Series resonant frequency:

$$f_0 = \frac{1}{2\pi \times \sqrt{L_r \times C_r}}$$

$$= \frac{1}{2\pi \times \sqrt{60 \times 10^{-6}\ H \times 27.3 \times 10^{-9}\ F}}$$

$$= 124.4\ kHz$$

- Inductance ratio:

$$L_n = \frac{L_m}{L_r} = \frac{210\ \mu H}{60\ \mu H} = 3.5$$

- Quality factor at full load:

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_e}$$

$$= \frac{\sqrt{(60\times10^{-6}\ H)/(27.3\times10^{-9}\ F)}}{99.7\ \Omega} = 0.47$$

- Quality factor at 110% overload:

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_e}$$

$$= \frac{\sqrt{(60\times10^{-6}\ H)/(27.3\times10^{-9}\ F)}}{90.6\ \Omega} = 0.52$$

Plot the gain curves corresponding to the design parameters (Fig. 16). The plot shows that the initial design meets the requirements of both Equation (26) and the following frequency specifications:

- The frequency at series resonance is f_0 = 124.4 kHz.
- The frequency at (M_{g_min}, f_{sw_max}) is $f_{n\_max} \times f_0$ = 1.02 × 124.4 kHz = 126.9 kHz.
- The frequency at (M_{g_max}, f_{sw_min}) with an overload (Q_e = 0.52) is $f_{n\_min} \times f_0$ = 0.65 × 124.4 kHz = 80.7 kHz.

7. Determine the Primary-Side Currents

The primary-side RMS load current (I_{oe}) with a 110% overload is determined from Equation (8):

$$I_{oe} = \frac{\pi}{2\sqrt{2}} \times \frac{I_o}{n} = 1.11 \times \frac{25\ A \times 110\%}{16} = 1.91\ A$$

The RMS magnetizing current (I_m) at f_{sw_min} = 80.7 kHz is determined from Equation (13):

$$I_m = 0.901 \times \frac{nV_o}{\omega L_m}$$

$$= 0.901 \times \frac{16 \times 12\ V}{2\pi \times 80.7 \times 10^3\ Hz \times 210 \times 10^{-6}\ H}$$

$$= 1.63\ A$$

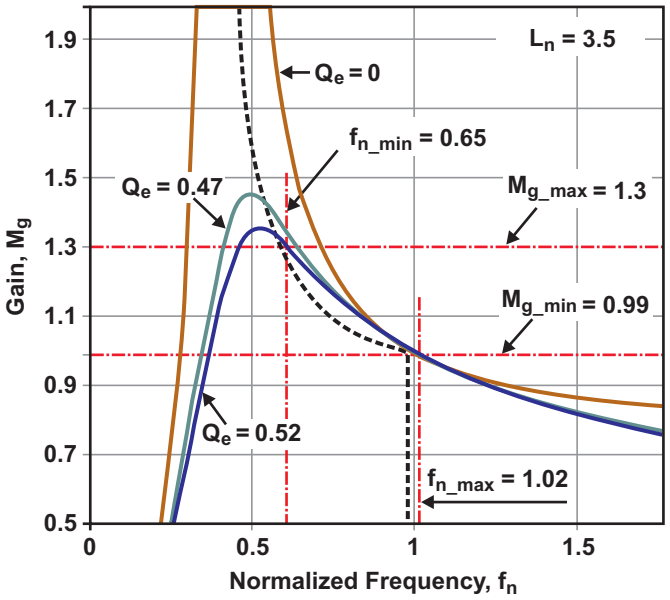


Fig. 16. Verification of resonant-circuit design.

The resonant circuit's current (I_r) is determined from Equation (14):

$$I_r = \sqrt{I_m^2 + I_{oe}^2} = \sqrt{(1.63\ A)^2 + (1.91\ A)^2} = 2.51\ A$$

This is also the transformer's primary winding current at f_{sw_min}.

8. Determine the Secondary-Side Currents

The total secondary-side RMS load current is the current referred from the primary-side current (I_{oe}) to the secondary side:

$$I_{oe\_s} = n \times I_{oe} = 16 \times 1.91\ A = 30.6\ A$$

Since the transformer's secondary side has a center-tapped configuration, this current is equally split into two transformer windings on the secondary side. The current of each winding is then calculated as

$$I_{sw} = \frac{\sqrt{2} \times I_{oe\_s}}{2} = \frac{\sqrt{2} \times 30.6\ A}{2} = 21.6\ A.$$

The corresponding half-wave average current is

$$I_{sav} = \frac{\sqrt{2} \times I_{oe\_s}}{\pi} = \frac{\sqrt{2} \times 30.6\ A}{\pi} = 13.8\ A.$$

9. Select the Transformer

The transformer can be built or purchased from a catalog. The specifications for this example are:

- Turns ratio (n): 16
- Primary terminal voltage: 450 VAC
- Primary winding's rated current, I_{wp}: 2.6 A
- Secondary terminal voltage: 36 VAC
- Secondary winding's rated current, I_{ws}: 21.6 A (center-tapped configuration)
- Frequency at no load: 127 kHz
- Frequency at full load: 80 kHz
- Insulation between primary and secondary sides: IEC60950 reinforced insulation

10. Select the Resonant Inductor

The inductor can be built or purchased from a catalog, with these specifications:

- Series resonant inductance, L_r: 60 µH
- Rated current, I_{L_r}: 2.6 A
- Terminal AC voltage:

$$V_{L_r} = \omega L_r \times I_r = 2\pi \times 80.7 \times 10^3 \times 60 \times 10^{-6} \times 2.6$$

$$= 75.7\ \text{V} \Rightarrow 100\ \text{V}$$

- Frequency range: 80 to 127 kHz

11. Select the Resonant Capacitor

The resonant capacitor (C_r) must have a low dissipation factor (DF) due to its high-frequency, high-magnitude current. Capacitors such as electrolytic and multilayer X7R ceramic types usually have high DF and therefore are not preferred. NP0 capacitors can be used due to their low DF, but their capacitance range presents limitations. Capacitors often used for LLC converters are made with metalized polypropylene film. These capacitors present very low DF and are capable of handling high-frequency current.

Before a capacitor is selected, its voltage rating has to be derated with regard to the switching frequency in use. Fig. 17 shows an example where a 12-nF capacitor rated at 600 V_{RMS} can be used only up to 300 V_{RMS} with a 100-kHz switching frequency.

The selected capacitor (C_r) must meet these additional specifications:

- Rated current, I_{C_r}: 2.6 A
- AC voltage, calculated from the circuit in Fig. 9a:

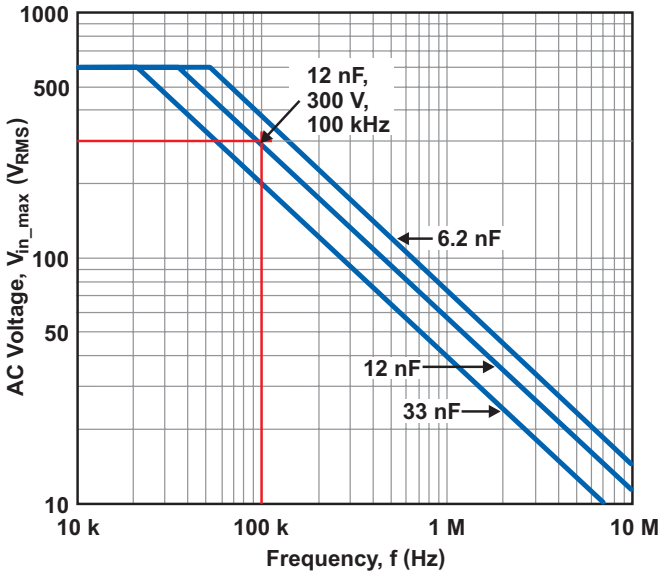


Fig. 17. Voltage derating from frequency.

$$V_{C_r} = X_{C_r} \times I_r = \frac{I_r}{\omega \times C_r}$$

$$= \frac{2.6\ \text{A}}{2\pi \times 80.7 \times 10^3\ \text{Hz} \times 27.3 \times 10^{-9}\ \text{F}} = 187.9\ \text{V}$$

- RMS voltage:

$$V_{C_r\_RMS} = \sqrt{\left(\frac{V_{in\_max}}{2}\right)^2 + V_{C_r}^2}$$

$$= \sqrt{\left(\frac{405\ \text{V}}{2}\right)^2 + (187.9\ \text{V})^2} = 276.3\ \text{V}$$

- Corresponding peak voltage:

$$V_{C_r\_peak} = \frac{V_{in\_max}}{2} + \sqrt{2} \times V_{C_r}$$

$$= \frac{405\ \text{V}}{2} + \sqrt{2} \times 187.9\ \text{V} = 467.4\ \text{V}$$

12. Select the Primary-Side MOSFETs

Specify the MOSFET parameters required for the converter. Each MOSFET sees the input voltage as its maximum applied voltage:

$$V_{Q1\_peak} = V_{Q2\_peak} = V_{in} = 405\ \text{V} \Rightarrow 500\ \text{V}$$

Each MOSFET conducts half of the resonant network's current in steady state after the resonant capacitor's voltage has been established. However, during the initial start-up and transient, the current in each MOSFET can be as high as the resonant current (I_r) with a 110% overload:

$$I_{Q1\_RMS} = I_{Q2\_RMS} = I_r = 2.51\ A$$

MOSFET switching losses are minimized by ZVS; therefore, the MOSFETs' conduction losses may become the main concern for the design. This suggests that MOSFETs with a low R_{ds_on} should be used, but with the recognition that there is usually a trade-off between R_{ds_on} and C_{ds}.

13. Design for ZVS

The converter's input phase angle must be greater than zero, as described by Equation (30b). Based on Step 6, this requirement has been met.

The conditions under which the converter has sufficient inductive energy and sufficient switching dead time for ZVS are described by Equations (32a) and (32b), respectively. To check these conditions, it can be assumed that C_{eq} is mainly from the MOSFETs' C_{ds}. For typical 500-V MOSFETs, C_{ds} is around 200 pF. If it is assumed that C_{eq} = 200 pF and that the worst-case minimum magnetizing current (I_{m_min}) is

$$I_{m\_min} = 0.901 \times \left.\frac{n \times V_o}{2\pi \times f_{sw} \times L_m}\right|_{\substack{f_{sw} = \\ 127\ kHz}}$$

$$= 0.901 \times \frac{16 \times 12\ V}{2\pi \times 127 \times 10^3 \times 210 \times 10^{-6}}$$

$$= 1.03\ A,$$

then, to verify Equation (32a),

$$\frac{1}{2}(L_m + L_r) \times I_{m\_peak}^2$$

$$= \frac{1}{2}(210 \times 10^{-6}\ H + 60 \times 10^{-6}\ H) \times (\sqrt{2} \times 1.03\ A)^2$$

$$= 286.5 \times 10^{-6}\ \text{joules},$$

and

$$\frac{1}{2}(2C_{eq}) \times V_{in}^2 = 200 \times 10^{-12}\ F \times (405\ V)^2$$

$$= 32.8 \times 10^{-6}\ \text{joules}.$$

These calculations verify that Equation (32a) is true:

$$\frac{1}{2}(L_m + L_r) \times I_{m\_peak}^2 \geq \frac{1}{2}(2C_{eq}) \times V_{in}^2$$

To meet the requirements of Equation (32b), the dead time should be designed as

$$t_{dead} \geq 16 \times 200 \times 10^{-12}\ F \times 127 \times 10^3\ Hz$$

$$\times 210 \times 10^{-6}\ H = 85.0 \times 10^{-9}\ s.$$

A t_{dead} of 100 ns will meet the requirement.

14. Select the Rectifier Diodes

The diodes' voltage rating is determined as

$$V_{DB} = \frac{V_{in\_max}/2}{n} \times 2$$

$$= \frac{(405\ V)/2}{16} \times 2 = 25\ V \Rightarrow 30\ V.$$

The diodes' current rating is determined as

$$I_{sav} = \frac{\sqrt{2} \times I_{oe\_s}}{\pi} = \frac{\sqrt{2} \times 30.6\ A}{\pi} = 13.8\ A.$$

15. Select the Type of Output Filter and Specify the Capacitors

In an LLC converter, the output filter may consist of capacitors alone instead of the LC filter seen in most pulse-width-modulated converters, although a small second-stage LC filter can be an option. If the filter has only capacitors, they should be chosen to allow conduction of the rectifier current through all AC components.

The rectifier's full-wave output current is expressed as

$$I_{rect} = I_{sw} = \frac{\pi}{2\sqrt{2}} \times I_o.$$

Then, for the load current (I_o), the capacitor's RMS current rating at about 100 kHz is calculated as

$$I_{C_o} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times I_o\right)^2 - I_o^2} = \sqrt{\frac{\pi^2}{8} - 1} \times I_o$$

$$= 0.482 \times I_o = 0.482 \times 25\ A = 12.1\ A.$$

Usually a single capacitor will not allow such a high RMS current, so several capacitors connected in

parallel are often used and may offer a lower profile. Aluminum solid capacitors with conductive-polymer technology have a high current rating and a low equivalent series resistance (ESR), making them a good choice.

The ripple voltage is a function of the amount of AC current that flows in and out of the capacitors with each switching cycle, multiplied by the capacitors' ESR. Since all electric current, including the load's DC current, can be assumed to flow in and out of the filter capacitors, this is a very good estimate of the ripple voltage. To meet the specification for a 120-mV ripple voltage, the maximum ESR should be

$$ESR_{max} = \frac{V_{o\_pk\text{-}pk}}{I_{rect\_peak}} = \frac{V_{o\_pk\text{-}pk}}{\left(\frac{\pi}{4} \times I_o\right) \times 2}$$

$$= \frac{0.12\ V}{\frac{\pi}{2} \times 25\ A} = 3.05\ m\Omega.$$

Any capacitance value can be used as long as combined capacitors meet the following specifications:

- Voltage rating: 16 V
- Ripple-current rating: 12.1 A at 100 kHz
- ESR: < 3 mΩ

16. Verify the Design with a Bench Test

To verify the design's performance, a physical converter needs to be built and bench tested. Generally, one or more design iterations may be needed to meet all specifications and to optimize the design. The final design used the following parameters:

- Transformer turns ratio: n = 17:1:1
- Resonant network's parameters: L_m = 280 µH, L_r = 60 µH, and C_r = 24 nF

Detailed design files and test results can be found in Reference [2]. Physical EVM boards are also available from TI. Several critical test waveforms are shown in Fig. 18 for immediate reference.

V. Computer Simulation and FHA

For designing an LLC resonant half-bridge converter, it is strongly recommended that a computer-based circuit-simulation method be used along with the FHA method. Using the two methods together is effective and provides a good balance. The FHA method is very effective for initiating a design because it provides a functional connection between a frequency-modulated switching-mode converter and established sinusoidal AC circuit design and analysis, giving designers insight into the converter's operation. Computer-based circuit simulation, on the other hand, compensates the FHA method with accurate design values. The combined design approach can significantly reduce the number of design iterations, shortening the time from starting a design to realizing its final product.

VI. Conclusion

This topic has presented comprehensive considerations for designing an isolated LLC resonant half-bridge converter. It has been shown that the FHA method is especially effective for initiating a new design of this type. A step-by-step design example has also been presented to demonstrate how to use this method.

VII. Acknowledgments

The author would like to express sincere gratitude to Richard Garvey, Bob Mammano, Bing Lu, and Bob Neidorff for their valuable discussions during the preparation of this topic.

VIII. References

[1] "8-Pin High-Performance Resonant Mode Controller," UCC25600 Data Sheet, TI Literature No. SLUS846

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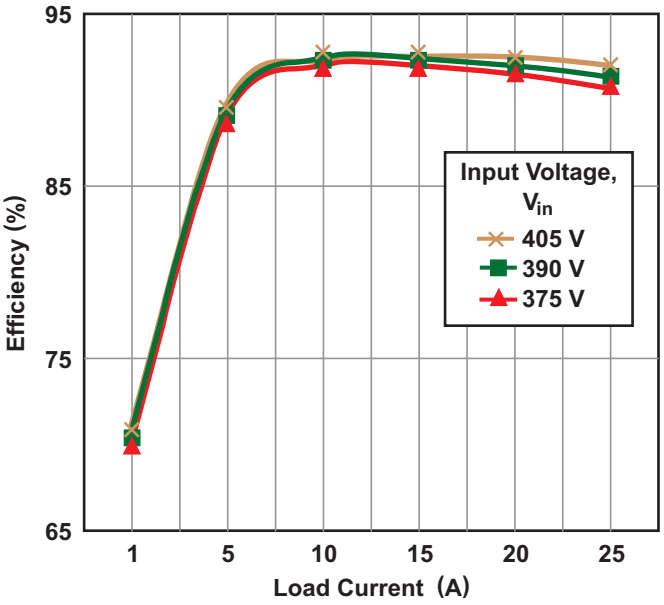
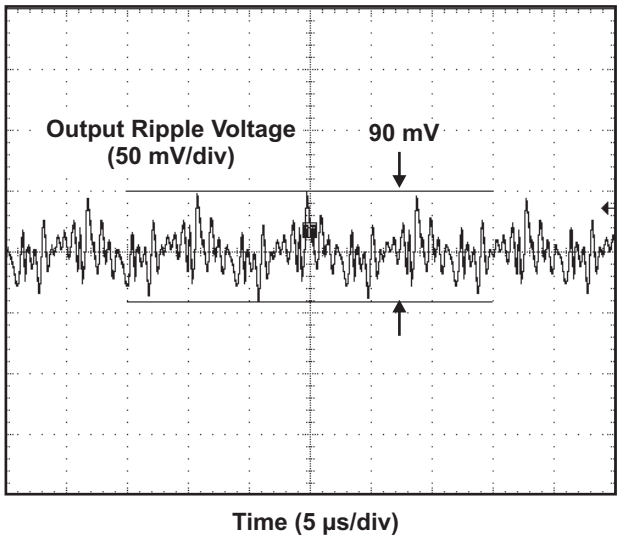
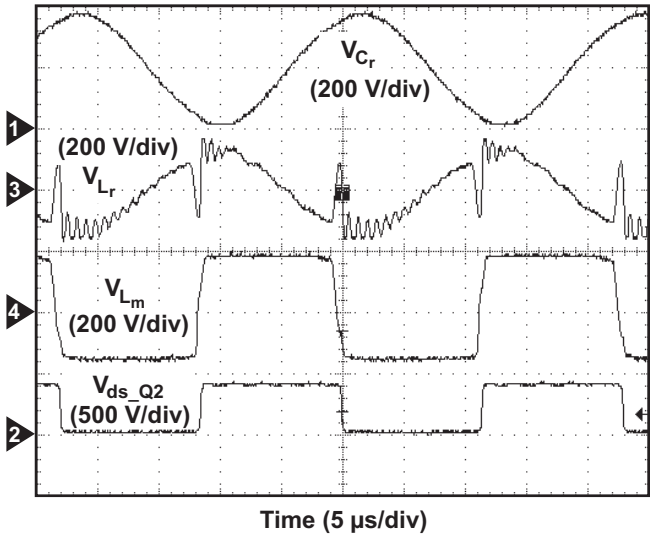


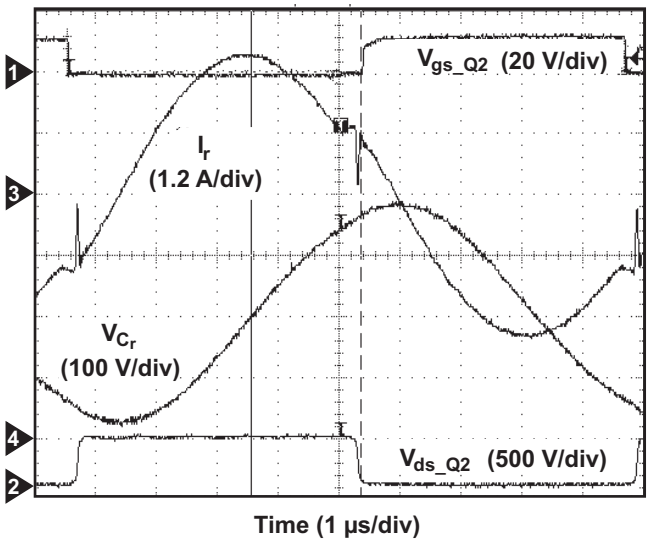
a. Efficiency.



b. Output ripple voltage (full load).



c. Voltage waveforms in resonant network (full load).



d. Resonant network's current and voltage (full load).

Fig. 18. Critical test waveforms of the design.

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