APPLICATION NOTE U-165

Lisa Dinwoodie

Design Review: Isolated 50 Watt Flyback Converter Using the UCC3809 Primary Side Controller and the UC3965 Precision Reference and Error Amplifier

UNITRODE

Design Review: Isolated 50 Watt Flyback Converter Using the UCC3809 Primary Side Controller and the UC3965 Precision Reference and Error Amplifier

By Lisa Dinwoodie

ABSTRACT

The flyback power stage is a popular choice for single and multiple output dc-to-dc converters at power levels of 150 Watts or less. Without the output inductor required in buck derived topologies, such as the forward or push-pull converter, the component count and cost are reduced. This application note will review the design procedure for the power stage and control electronics of a flyback converter. In these isolated converters, the error signal from the secondary still needs to cross the isolation boundary to achieve regulation. By using the UC3965 Precision Reference with Low Offset Error Amplifier on the secondary side to drive an optocoupler and the UCC3809 Economy Primary Side Controller on the primary side, a simple and low cost 50 Watt isolated power supply is realized.

INTRODUCTION

The flyback converter reviewed in this application note, and available as a demonstration board ("demo board"), is specifically designed to interface with the voltage ranges used in the telecommunications industry. The primary goal of this 5V, 50 Watt power supply is an efficient design which meets all the specifications while maintaining low cost. This goal is achieved by using the UCC3809 on the primary side for fixed frequency current mode control and using the error amplifier and precision reference of the UC3965 on the secondary side. Each of these 8-pin integrated circuits requires minimal external parts resulting in an economical yet effective design. The demo board schematic is shown in Figure 1 and the list of materials is tabulated on page 17.

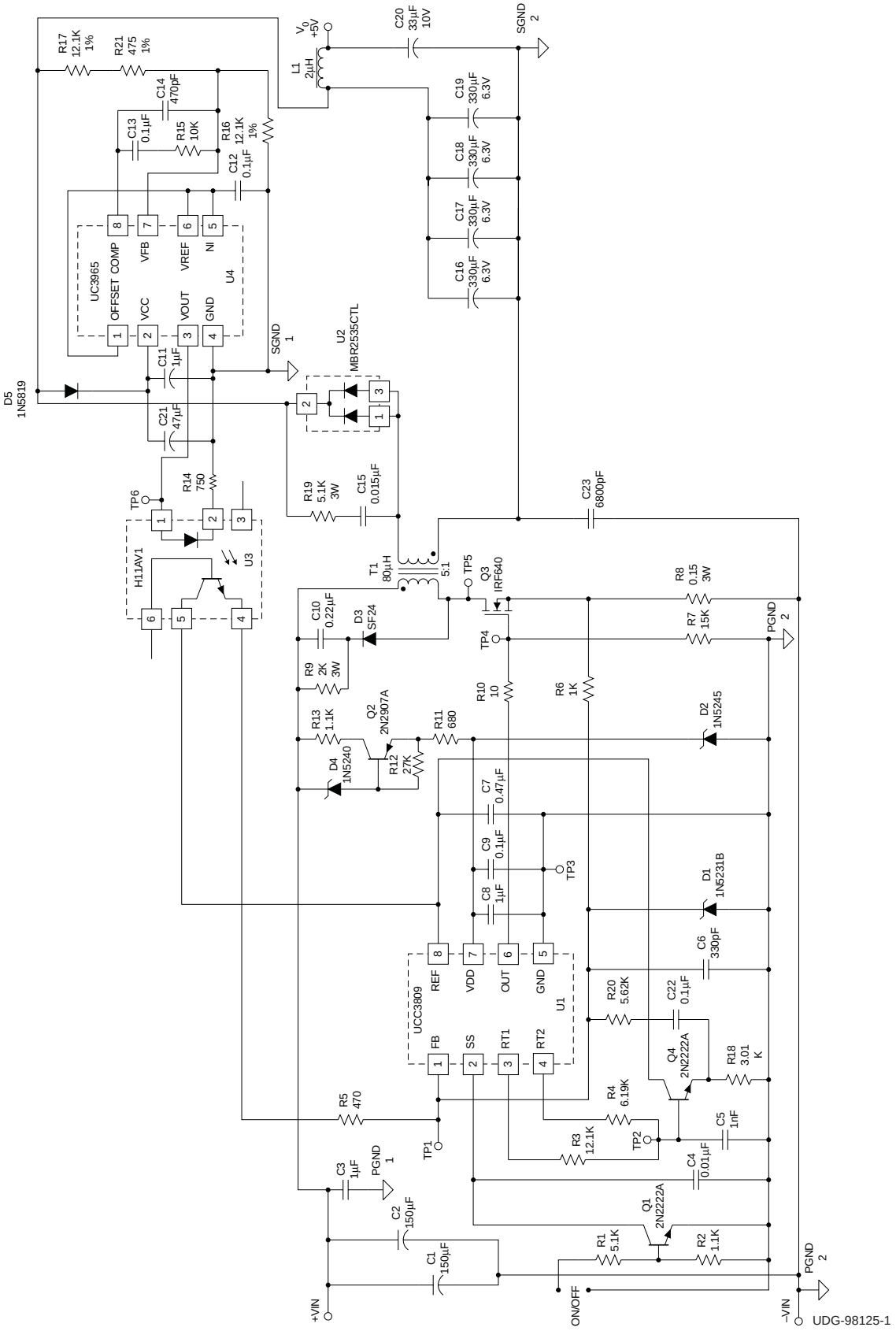

Figure 1. Schematic diagram of the –48V to +5V flyback converter available as a demo board.

POWER SUPPLY SPECIFICATIONS

Input Voltage Range:	–72VDC to –32VDC (–48VDC nominal)
Output Voltage:	+5VDC
Load:	0A to 10A
Regulation:	±2% Over Load, Line, and Temperature
Isolation:	1500VRMS

DESIGNING THE POWER STAGE

Flyback Topology

There are many standard power converter topologies available to choose from, each with its advantages and disadvantages [1]. After careful consideration, taking into account factors such as low power, simplicity, isolation, input and output ripple currents, and low cost, the flyback configuration was chosen. The basic flyback converter topology is shown in Figure 2.

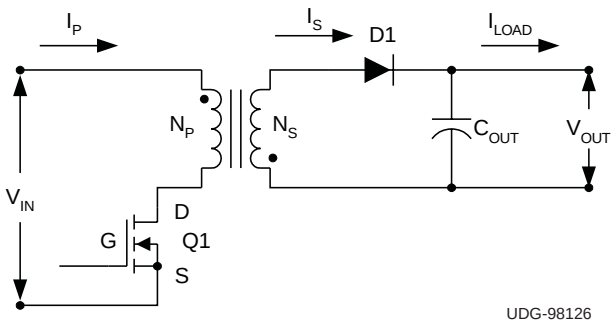

Figure 2. Flyback converter circuit configuration.

Control Method

Voltage mode control was past over in favor of current mode control because current mode control responds immediately to line voltage changes and provides inherent over current protection for the switching device. Traditional peak current mode control compares the amplified output voltage error with the primary inductor current signal. Using the UCC3809 pulse width modulator (PWM) as the controller, the amplified output voltage error and the primary inductor current ramp are summed and compared to a 1V threshold. The inner current control loop contains a small current sense resistor which senses the primary inductor current. The resistor transforms this current waveform into a voltage signal that is fed directly into the primary side PWM comparator. This inner loop determines the response to input voltage changes. The outer voltage control loop involves comparing a portion of the output voltage to a reference voltage at the input of the secondary side error amplifier. This divided down output voltage drives the inverting input to the error amplifier in the UC3965 which then drives an internal inverting output buffer. The resulting output then drives an optocoupler. The optocoupler output is also fed directly into the primary side PWM comparator. As the output voltage increases above the desired level, the optocoupler is driven harder on, forcing the PWM comparator to shut off the gate drive to the switching element. This outer loop determines the response to load changes.

Peak current mode control requires simpler compensation, has pulse-by-pulse current limiting, and has better load current regulation. Because the secondary currents are already quite large, continuous conduction mode (CCM) was chosen. Primary and secondary RMS currents can be up to two times higher for discontinuous mode than for CCM. Discontinuous conduction mode would require using a transistor with a higher current rating. Because the output ripple current is less than it would be if discontinuous mode were used, the output capacitors are smaller.

Continuous conduction mode has the disadvantage of requiring a higher magnetizing inductance to stay in CCM throughout the entire operating range and a right-half-plane zero in its transfer function. Feedback loop stabilization will be discussed in a later section.

Maximum Duty Cycle and Turns Ratio

Now that the topology (flyback) and control method (peak current mode control) have been decided upon, the next decision to be made is what the maximum duty cycle, D_{max}, should be. The duty cycle is the ratio of on-time of Q1, Figure 2, to total period, or $D = t_{on}/ T$. In a CCM flyback converter the maximum duty cycle will determine the turns ratio of the transformer and impact the maximum voltage stress on the switching element. For this design, a maximum duty cycle of 45% was selected. Limiting the duty cycle increases the number of controller ICs to chose from because many available today have maximum duty cycle limitations of 50%.

The DC transfer function of a CCM flyback converter is:

$$\frac{V_O + V_D}{V_{IN(\min)} - V_{Rds(on)}} = \frac{1}{N} \bullet \left(\frac{D_{\max}}{1 - D_{\max}} \right) \quad (1)$$

where V_O equals the output voltage, 5V,

V_D = forward voltage drop across rectifier D1, assumed to be 0.8V,

V_{IN} = 32 to 72V, $V_{IN(min)}$ = 32V,

$V_{Rds(on)}$ = on voltage drop across MOSFET Q1, equal to $R_{ds(on)} \bullet I_{RMS(primary)}$, assumed to be 1V,

N = turns ratio, equal to N_P/N_S,

N_S = number of transformer secondary turns,

N_P = number of transformer primary turns,

D = duty cycle.

Maximum duty cycle, 0.45, occurs at minimum input voltage. Substituting these values into (1) gives us a turns ratio of 4.37. The turns ratio is inversely proportional to the peak primary current, I_{PEAK}, but directly proportional to the voltage stress on the switching element. So the peak currents will not become unreasonably high and the voltage stress on the MOSFET will be kept as low as possible, the turns ratio is rounded up only to the next integer value, 5, or simply five primary turns for every one secondary turn. Recalculating equation (1) results in an actual D_{max} of 48%.

Switching Frequency

Because the magnetic components and filters will be smaller, the tendency is to have as high a switching frequency as possible. Unfortunately, the decision is not quite that clear cut. Core losses, gate charge currents, and switching losses increase with higher switching frequencies; peak currents and, consequently, I^2R losses increase with lower switching frequencies. A compromise must be reached between component size, current levels, and acceptable losses. Synchronization with other systems and backward compatibility may also be deciding factors. For this design, a fixed frequency (f_{sw}) of 70kHz was chosen. At D_{max} equal to 48%, $t_{on(max)}$ becomes 6.9µs.

Transformer Design [2]

The transformer in a flyback converter is actually a coupled inductor with multiple windings. Transformers provide coupling and isolation whereas inductors provide energy storage. The energy stored in the air gap of the inductor is equal to:

$$E = \frac{L_P \bullet (I_{PEAK})^2}{2} \quad (2)$$

where E is in Joules, L_P is the primary inductance in Henries, and I_{PEAK} is the peak primary current in Amperes. When the switch is on, D1 (from Figure 2) is reverse biased due to the dot configuration of the transformer. No current flows in the secondary windings and the current in the primary winding ramps up at a rate of:

$$\frac{\Delta I_L}{\Delta t} = \frac{V_{IN(\min)} - V_{Rds(on)}}{L_P} \quad (3)$$

where $V_{IN(min)}$ and $V_{Rds(on)}$ were defined previously and Δt is equal to $t_{on(max)}$ at $V_{IN(min)}$. The output capacitor, C_{OUT}, supplies all of the load current at this time. Because the converter is operating in the continuous conduction mode, ΔI_L is the change in the inductor current which appears as a positive slope ramp on a step. The step is present because there is still current left in the secondary windings when the primary turns on. When the switch turns off, current flows through the secondary winding and D1 as a negative ramp on a step, replenishing C_{OUT} and supplying current directly to the load.

Based on (3), the primary inductance can be calculated given an acceptable current ripple, ΔI_L. For the demo board design, ΔI_L was set to equal one-half the peak primary current. For a CCM flyback design, the peak primary current is calculated based upon (4).

$$I_{PEAK} = \left(\frac{I_{OUT(\max)}}{N} \right) \bullet \left(\frac{1}{1 - D_{\max}} \right) + \frac{\Delta I_L}{2} \quad (4)$$

By replacing ΔI_L with ½(I_{PEAK}), $I_{OUT(max)}$ with 10A, D_{max} with 0.48, and N with 5 as detailed earlier, the peak primary current is calculated to be 5.16A and ΔI_L calculates to 2.58A. The root mean square, RMS, current of a ramp on a step waveform is defined in (5) and calculates to be 2.74A for this application.

$$I_{rms} = \sqrt{\frac{t_{on(\max)}}{T} \bullet \left((I_{PEAK})^2 - \Delta I_L \bullet I_{PEAK} + \frac{(\Delta I_L)^2}{3} \right)} \quad (5)$$

Using (3), L_P calculates to approximately 80µH. Due to cost considerations and a switching frequency of 70kHz, the core material was chosen to be manganese zinc ferrite 3C85 from Philips. Be-

cause the inductor (a.k.a. the flyback transformer) is driven in one quadrant of the B-H plane only, a larger core is required in a flyback design. Because this converter is operating in the continuous conduction mode at a relatively low frequency, the maximum peak flux density, B_{max}, is limited by the saturation flux density, B_{sat}. Taking all this into consideration, the minimum core size is determined by (6).

$$AP = \left(\frac{L_P \bullet I_{PEAK} \bullet I_{rms} \bullet 10^4}{420 \bullet k \bullet B_{max}} \right)^{1.31} \quad (6)$$

where AP = the core area product in cm^4,

k = winding factor, equal to 0.2 for a continuous mode flyback,

$B_{max} \approx B_{sat}$, or 0.33 Telsa for 3C85 material at 100°C.

The result of (6) is compared to the product of the winding area, Aw (cm^2), and effective core area, Ae (cm^2), listed in the core manufacturer's data sheet. For this design, a Philips EFD30 core met the minimum criteria.

The minimum number of primary turns is determined by:

$$N_P = \frac{L_P \bullet I_{PEAK} \bullet 10^4}{B_{max} \bullet Ae} \quad (7)$$

Based upon this result and the predetermined turns ratio, the number of secondary turns is established. With a turns ratio of 5 and N_P equal to 20, N_S is calculated to be 4.

The energy stored in the flyback transformer is actually stored in an air gap in the core.This is because the high permeability of the ferrite material can't store much energy without saturating first. By adding an air gap, the hysteresis curve of the magnetic material is actually tilted, requiring a much higher field strength to saturate the core. The size of the air gap is calculated using (8).

$$gap = \frac{\mu_o \bullet \mu_r \bullet (N_P)^2 \bullet Ae \bullet 10^{-2}}{L_P} \quad (8)$$

In (8), the gap is measured in centimeters, μ_o is the permeability of free space equal to $4\pi \bullet 10^{-7}$ H/m, and μ_r is equal to the relative permeability of the gap material (in this case the gap material is air, μ_r =1). This gap is calculated to be 0.043cm and is evenly distributed between the center post and two outer legs of the EFD30 core.

The primary windings are two strands of 21AWG magnet wire in parallel, the first layer wound closest to the core, the second layer over the secondary windings. The secondary windings consist of four strands of 18AWG magnet wire in parallel, filling a single layer for maximum coupling.

Using a primary inductance of 80µH and a maximum duty cycle of 48% means the converter will not stay in continuous mode control over the entire operating range because of the relationship expressed in (9).

$$P_{O(min)} = \frac{\left(V_{IN(min)} - V_D\right) \bullet V_{IN(min)} \bullet \left(t_{on(max)}\right)^2}{2.5 \bullet T \bullet L_P} \quad (9)$$

According to (9), at the 32V minimum input voltage the converter will enter discontinuous mode at an output load current of less than 3.33A. To remain in CCM would require a much larger transformer, 264.5µH at 48% duty cycle. Increasing the primary inductor value requires a much larger core, such as the E41/17/2 core set from Philips. This would require 60% more circuit board space than the present core.

Another approach to guarantee remaining in continuous mode is to reduce the maximum duty cycle to approximately 26% and continue to use an 80µH flyback inductor.Unfortunately, the result of this would be considerably higher peak currents. Higher peak currents result in an increase of all the I^2R losses, and a larger core would be needed anyway to satisfy the core area product limit which is dependent upon the peak primary current as expressed in (6).

It is far better to design for continuous mode and to transition into discontinuous mode than the other way around. Discontinuous mode is actually unavoidable at zero load. A continuous mode feedback control loop has the ability to maintain stability while in discontinuous mode. However, a control loop designed for discontinuous operation does not take into account the already eluded to right-half-plane zero present in continuous mode. The existing demo board design has the fortuitous advantage of showing the user waveforms for both operating modes dependent upon input voltage and load current (see Figures 16 and 17).

MOSFET Selection

The switching element in a flyback converter must have a voltage rating high enough to handle the maximum input voltage and the reflected secondary voltage, not to mention any leakage inductance induced spike that is inevitably present. Approximate the required voltage rating of the MOSFET using (10).

$$V_{ds} = \left[\left(V_{IN(\max)} + V_L\right) + \left(\frac{N_P}{N_S}\right) \bullet \left(V_O + V_D\right)\right] \bullet 1.3 \quad (10)$$

where V_{ds} = the required drain to source voltage rating of the MOSFET,

V_L = the voltage spike due to the leakage inductance of the transformer, estimated to be thirty percent of $V_{IN(max)}$,

and the additional 1.3 factor includes an overall thirty percent margin.

For the flyback converter presented, the required minimum voltage rating of the MOSFET calculates to be 160V. An IRF640 N-channel power MOSFET was chosen. This device has a voltage rating of 200V, a continuous DC current rating of 18A, and an $R_{ds(on)}$ of only 0.18Ω. By consulting the typical gate charge vs. gate-to-source voltage waveform in the manufacturer's data book, calculating the average current required to drive the gate capacitor of the FET is possible:

$$I_{gate} = Q_{\max} \bullet f_{sw} \quad (11)$$

Q_{max} is the total gate charge in Coulombs, estimated to be 70nC based upon a gate to source voltage of 15V and a drain to source voltage of 160V. According to (11), the average supply current of the controller, I_{VDD}, needs to increase by 4.9mA to switch the gate at the selected operating frequency.

This FET will experience both switching and conduction losses. The conduction losses will be equal to the I^2R losses, as shown by (12).

$$P_{cond} = \left(I_{rms}\right)^2 \bullet R_{ds(on)} \quad (12)$$

Switching losses are the result of overlapping drain current and drain to source voltage at turn on and turn off [3]. At turn on the drain current begins to flow through the FET device when the gate voltage has reached the V_{gs} threshold. This drain current will continue to rise until reaching its final value. Meanwhile, the drain to source voltage will remain at V_{ds}, calculated earlier in (10). This voltage starts to fall only after the "Miller" capacitor begins to charge. The charging time, t_{ch}, for the "Miller" capacitor is a function of the gate resistor, R_g (R10 in Figure 1), and the gate to drain "Miller" charge, Q_{gd}, as shown in (13).

$$t_{ch} = \frac{Q_{gd} \bullet R_g}{VDD - V_{gs(th)}} \quad (13)$$

In (13), VDD is the bias voltage of the UCC3809 and $V_{gs(th)}$ is the gate threshold voltage of the FET. The whole process repeats itself in reverse at turn off. The power dissipation of the FET's output capacitance, C_{oss}, also contributes to the switching losses in the form of $\frac{1}{2}CV^2f$. The total switching losses are estimated based on equation (14).

$$P_{SW} = \frac{C_{oss} \bullet \left(V_{ds}\right)^2 \bullet f_{sw}}{2} + V_{ds} \bullet I_{PEAK} \bullet t_{ch} \bullet f_{sw} \quad (14)$$

The total FET losses are the sum of the conduction losses (12) and the switching losses (14), calculated to be 3.3W for the IRF640 FET used on the demo board. Without appropriate heatsinking, this device would have a junction to ambient thermal resistance of 62°C/W, resulting in a junction temperature rise of 206°C above ambient. Heat sinking is obviously required to prevent the junction temperature, T_j, from exceeding 150°C and avert device failure due to excessive heating. The IRF640 has a junction to case thermal resistance, θ_{jc}, of 1°C/W, using a silicone elastomer heat sink pad provides a case to heat sink thermal resistance, θ_{cs}, of 1.26°C/W. A heat sink which provides a maximum thermal resistance, θ_{sa}, of 35°C/W must be chosen for a use in an ambient temperature, T_a, of 25°C, as shown in (15a) and (15b).

$$T_j = \left(P_{cond} + P_{sw}\right) \bullet \left(\Theta_{jc} + \Theta_{cs} + \Theta_{sa}\right) + T_a \quad (15a)$$

$$\Theta_{sa} = \frac{T_j - T_a}{P_{cond} + P_{sw}} - \left(\Theta_{jc} + \Theta_{cs}\right) \quad (15b)$$

Diode Selection

Schottky rectifiers have a lower forward voltage drop than typical PN devices, making it the rectifier of choice when considering reducing converter losses and improving overall efficiency. Selecting the appropriate Schottky for a specific application depends mainly on the working peak reverse voltage rating, the peak repetitive forward current, and

the average forward current rating of the device. If the maximum working peak reverse voltage is exceeded the reverse leakage current will rise above its specified limit. The peak reverse voltage that the device will be subjected to is equal to the reflected maximum input voltage minus the voltage drop across the FET added to the output voltage. The maximum average forward current rating of the device must not be exceeded if the junction temperature of the device is to remain within its safe operating range. Because all current to the output capacitor and load must flow through the diode, the average forward diode current is equal to the steady-state load current. The peak repetitive forward current is equal to the reflected primary peak current. An MBR2535CTL Schottky rectifier from Motorola met the requirements for the demo board design. This device is a common cathode dual Schottky with a forward voltage drop of 0.47V and a working peak reverse voltage rating of 35V, exceeding the 20V requirement of the demo board design. The average rectified forward current rating is specified at 12.5A per leg, 25A total, and the peak repetitive forward current is rated for 25A per leg, or a total of 50A. The demo board requirement is 10A total average forward current and 26A total peak repetitive forward current.

Power loss in the Schotty is the summation of conduction losses and the reverse leakage losses. Conduction losses are calculated using the forward voltage drop and the average forward current. The MBR2535CTL will have conduction losses equal to 4.7W. Reverse leakage losses, which are dependent upon the reverse leakage current, the blocking voltage, and the on-time of the FET, are calculated to be 0.05W. Heat sink selection is once again based upon the required thermal resistance of the heat sink to air interface in order to maintain a junction temperture of less than 125°C.

Input and Output Capacitors

The input capacitors are chosen based upon their ripple current rating and their rated voltage. The input current waveform is shown in Figure 3. The shaded regions represent the current actually supplied by the input capacitors during the switch's on- and off-times. The RMS value of this ripple current is calculated by adding the RMS current of the ramp on a step shaded waveform during t_{ON} with the RMS value of the average input current during t_{OFF}. Because this example uses a duty cycle that is very close to 50%, this RMS current is almost equal to the primary RMS current calculated in (5).The actual capacitor value is not that critical as long as the minimum capacitance gives an acceptable ripple voltage determined by the following equation:

$$C_{\min} = \frac{I_{rms}}{8 \bullet f_{sw} \bullet \Delta V} \qquad (16)$$

In (16), I_{rms} is equal to the RMS current, calculated from Figure 3, and ΔV is equal to the acceptable ripple voltage. Two United Chemi-Con SXE series 150µF capacitors in parallel met the requirements for the demo board design when derated for ambient temperature and frequency. The small 1µF ceramic capacitor is added at the converter input to provide a shorter path for high frequency ripple.

The output capacitors are also chosen based upon their low equivalent series resistance (ESR), ripple current and voltage ratings, and (16). The ripple current that the output capacitor experiences is a result of supplying the load current during the FET conduction time and its charging current during the FET off-time, as illustrated by the shaded regions in Figure 4. During the conduction time of the FET, the secondary windings of the transformer are not conducting. The discharging of the output capacitor supplies the 10A load current. During the FET

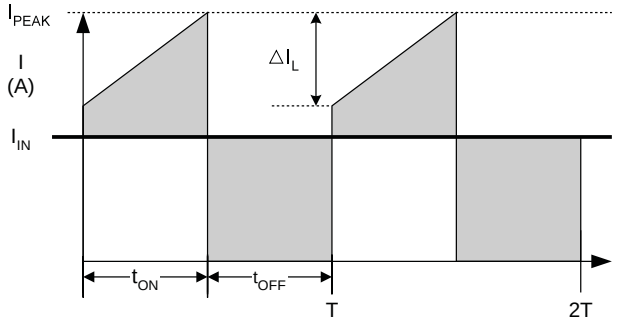

Figure 3. Input capacitor current waveform.

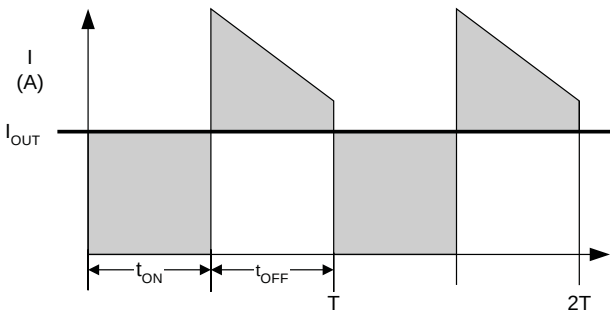

Figure 4. Output capacitor current waveform.

off-time, the secondary windings are conducting and the secondary peak current is charging the output capacitor and delivering the 10A current to the load. The RMS current is calculated to be approximately 14A. Four Sanyo OSCON 6SH330M 330µF capacitors in parallel met the requirements for the demo board design when derated for ambient temperature and frequency.

SETTING UP THE UCC3809

The UCC3809 was selected as the primary side controller for this application because of its flexibility, low cost, and built in features such as programmable maximum duty cycle, full cycle programmable soft start, undervoltage lockout, and low operating current.

VDD Bias/UVLO

The employment of a constant current biasing scheme, as shown in Figure 5, minimizes transformer design costs by eliminating the need for a bootstrap winding. It also avoids any high power dissipation that would be present in a single bias resistor. This is especially true with a wide input voltage range, such as seen in the telecommunications industry. The current biasing scheme supplies enough current for the gate drive, determined by (11), in addition to the maximum I_{VDD} current required to operate the internal functions of the IC.

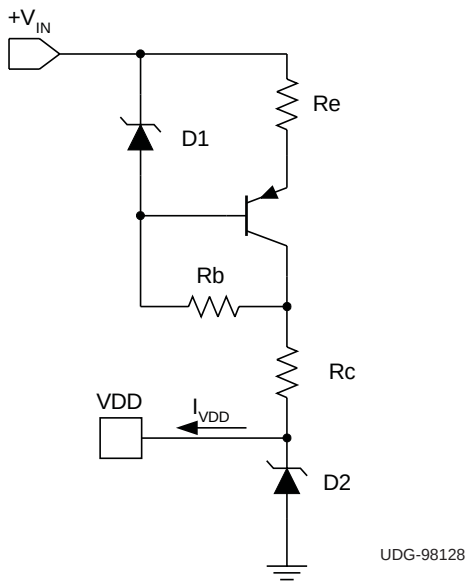

Figure 5. Constant current biasing.

The zener diode, D1, minus the V_{BE} drop of the small signal PNP transistor, sets up a constant voltage across the emitter resistor, Re, resulting in a constant emitter current. The selection of the collector resistor, Rc, ensures the transistor remains in the active mode throughout the entire range of V_{IN} while maintaining VDD above the under voltage lockout level. All of these components have minimal power dissipation and are surface-mountable if desired. Although the internal shunt regulator can sink up to 25mA, D2 was added to minimize the power dissipation in the IC.

The UCC3809 is available with two different undervoltage lockout (UVLO) levels and hysteresis options. Off-line users can take advantage of the wider hysteresis option available in the –2 device while the tighter hysteresis of the –1 is optimized for dc-to-dc converter use. UVLO insures that the IC bias is within specification before enabling the output stage. This guarantees the output drive is capable to fully turn on the MOSFET once the UVLO threshold has been reached. The output drive and reference voltage are actively held low during power-up and the I_{VDD} starting current is less than 100µA until VDD crosses the turn-on threshold. As VDD crosses the turn-off threshold during power-down, REF and the output drive are pulled low.

Decoupling

Both VDD and REF should be decoupled with good quality, low ESR/ESL, ceramic capacitors placed as close to the VDD or REF pin as possible and returned directly to the GND pin for the best high frequency performance. Because the reference voltage provides the bias to many of the internal circuits of the IC, its decoupling capacitor should be at least 0.47µF for adequate filtering.

Soft Start and Shutdown

The soft start feature enables the IC to start up in a controlled manner. While the IC is in UVLO, the SS pin is held low. Once the UVLO threshold has been crossed, an internal 6µA current source charges the external soft start capacitor (C4, Figure 1). As the capacitor voltage ramps up from 1V to 2V, the output duty cycle linearly increases to a level required for output voltage regulation. The soft start capacitor is chosen so that there is a delay of approximately 3 milliseconds before VOUT ramps up to its full potential. Pulling the SS pin below 0.5V will shut down the output and pull REF low. This feature is easily implemented using a small signal NPN and a pull-down resistor to accept a logic level command signal.

Output Driver

The totem pole output stage of the UCC3809 has the ability to source 0.4A and sink 0.8A. Placing a small resistor (R10, Fig. 1) in series with the IC output and the gate of the FET will damp any oscillations caused by the parasitic wiring inductance and the FET's input capacitance. To insure the MOSFET gate does not get charged to its turn-on threshold during device start up, a pull-down resistor (R7, Fig. 1) is added to the gate drive. The output stage provides a low resistance during overshoot and undershoot, eliminating the need for Schottky diodes on the output.

Oscillator

The data sheet gives a complete description of the operation of the internal oscillator and optional synchronization schemes. The external RT1 resistor (R3, Fig. 1) and the internally generated voltage across it control the charge current of CT (C5, Figure 1). When the CT voltage is equal to 2/3 of the reference voltage, sensed through RT2 (R4, Figure 1), the oscillator initiates a discharge cycle. The discharge current is set by RT2 and the CT voltage is sensed through RT1. When CT has discharged to 1/3 of the reference voltage, the charging cycle begins again.

The demo board requires 48%, or 6.9µs, of unrestrained on-time during its full range of operation. The duty cycle clamp is set at 66%, or 9.5µs, so that within the range of normal operation, the output regulation is not sacrificed because of hitting the duty cycle clamp. This clamp will effectively prevent the transformer from saturating when the input voltage is less than the minimum operating range, such as during start-up, brown-outs, and shut down, without inhibiting normal operation. For 100kHz switching frequency, the recommended capacitor for CT is approximately 1nF, and the internal capacitance of the IC is estimated to be 27pF. Setting t_{on} of the duty cycle clamp to 9.5µs, and CT equal to 1nF, RT1 is determined by:

$$RT1 = \frac{t_{on}}{0.74 \bullet (CT + 27pF)} \qquad (17)$$

RT2 is then selected to satisfy the switching frequency period. The oscillator frequency is approximated by the following equation:

$$f_{sw} = \frac{1}{0.74 \bullet (CT + 27pF) \bullet (RT1 + RT2)} \qquad (18)$$

For good noise immunity, the timing components must be placed as close as possible to the IC pins. The CT-RT1-RT2 junction (TP2 on the demo board) should be used to look at the oscillator waveform instead of putting a probe directly onto pins 3 and 4 of the IC. The probe will add stray capacitance to the oscillator and alter the switching frequency if placed directly on the IC pins.

Current Limiting

Selection of the current sense resistor is accomplished by dividing the FB 1V threshold value by the peak primary current at the desired current limit point, typically 120% of I_{PEAK}.

$$R_{sense} = \frac{FB_{threshold}}{1.2 \bullet I_{PEAK}} \qquad (19)$$

This ground-referenced resistor must be a low inductance type and have a rated power level to meet the $(I_{RMS})^2 \bullet R_{sense}$ requirement. The closest standard value resistor that meets this requirement is used. The UCC3809/UC3965 demo board uses a 0.15Ω resistor for current sensing. This value resistor equates to a maximum primary side current limit point of 6.67A. This would lead to a worst case short circuit output current, I_{sc}, of 12.9A as calculated using (4), substituting I_{sc} for $I_{OUT(max)}$. Upon crossing the PWM comparator threshold, the internal PWM latch is reset, turning off the output driver until the beginning of the next oscillator charge cycle.

Current spikes caused by the leakage inductance of the flyback transformer and the reverse recovery of the diode could trip the current sense latch and prematurely shut off the output. This unwanted spike can be suppressed by adding a small RC filter for effective leading edge blanking (Figure 6). Usually adding a few hundred nanoseconds of blanking time is enough to ignore (or "blank") any unwanted current spikes. An internal 250Ω NMOS FET discharges the high frequency capacitor used in this filter during the PWM off-time.

Slope Compensation [4]

Sensing peak inductor current instead of average inductor current results in a loop response that is less than ideal. Adding slope compensation to the current sense signal cancels this error by maintaining a constant average current independent of duty cycle. Slope compensation is required for open loop stability in a current mode system with 50% or greater duty cycles, but will benefit any current mode application at the cost of a few small parts.

The UCC3809 demo board resistively divides the oscillator sawtooth at the CT node and superimposes it onto the current sense signal using an emitter follower configuration as detailed in [4].

The first step in implementing slope compensation is to calculate the flyback inductor down slope on the secondary side in amps per second:

$$S(L) = \frac{di}{dt} = \frac{V_{sec}}{L_{sec}} \quad (20)$$

where $V_{sec} = V_O + V_D$ and $L_{sec} = L_P/N^2$. Then transform this slope to the primary side and calculate the equivalent slope voltage at the sense resistor in volts per second:

$$VS(L)' = \frac{S(L)}{N} R_{sense} \quad (21)$$

Next, calculate the oscillator slope at the timing capacitor, CT, in volts per second:

$$VS(osc) = \frac{\Delta V_{osc}}{t_{on(\max)}} \quad (22)$$

ΔV_{osc} is equal to the CT peak to peak voltage, 1.67V for the UCC3809. Because the oscillator waveform has a valley voltage greater than zero, an AC coupling capacitor is required (Fig. 6). Using superpositioning and neglecting the coupling and LEB capacitors, the voltage ramp equation at the FB pin can be derived (23).

$$V(ramp) = \frac{VS(L)' \bullet R_{SC}}{R_{LEB} + R_{SC}} + \frac{VS(osc) \bullet R_{LEB}}{R_{LEB} + R_{SC}} \quad (23)$$

The value of the R_{SC} resistor (Figure 6) is dependent upon the amount of slope compensation to be added. By equating a portion (M) of the inductor downslope to the resistively divided oscillator charge slope, R_{SC} can be determined.

$$\frac{VS(osc) \bullet R_{LEB}}{R_{LEB} + R_{SC}} = M \bullet \left(\frac{VS(L)' \bullet R_{SC}}{R_{LEB} + R_{SC}} \right) \quad (24)$$

$$R_{SC} = \frac{R_{LEB} \bullet VS(osc)}{VS(L)' \bullet M} \ \Omega \quad (25)$$

To guarantee current loop stability at 100% duty cycle, a minimum compensation of ½ the inductor down slope (M = 0.5) must be added. By adding slope compensation equal to the down slope of the inductor current (M = 1), any current perturbation will be eliminated in one cycle. The demo board incorporates approximately 80% slope compensation by using 5.62KΩ and 1KΩ resistors for R_{SC} and R_{LEB}, respectively.

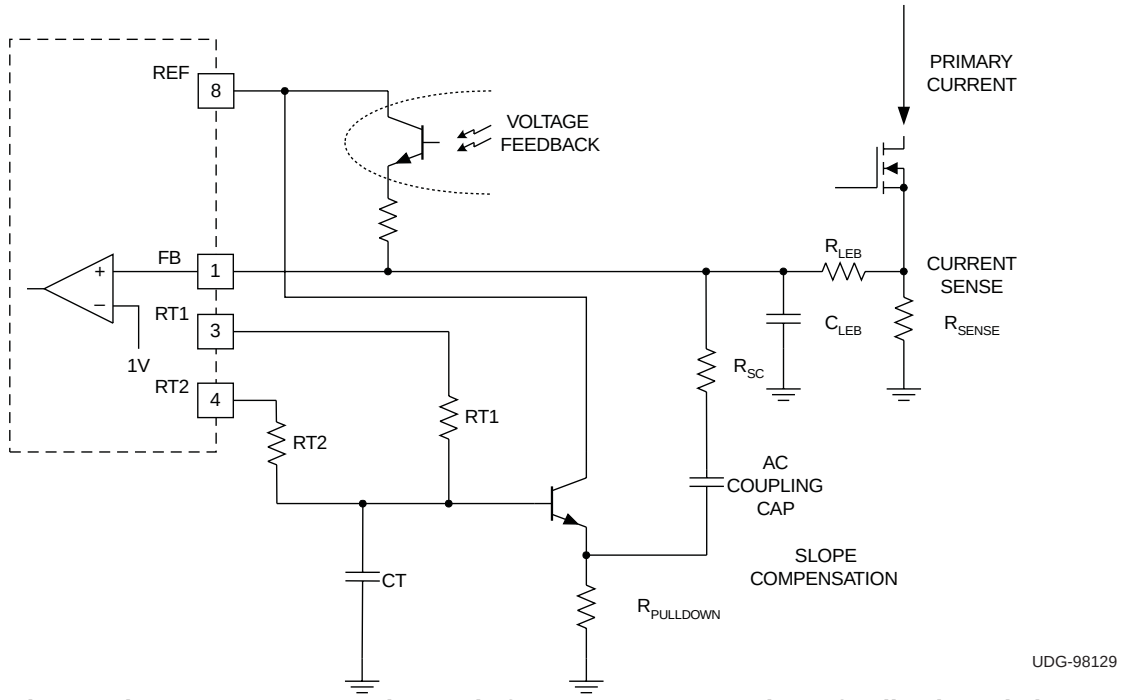

Figure 6. The FB pin serves as a summing node for current sense, voltage feedback, and slope compensation.

Voltage Feedback

The FB pin of the UCC3809 sums the voltage feedback signal to the current sense signal and any added slope compensation. The voltage feedback signal is from an optocoupler, which is driven from an error amplifier on the secondary side of the converter.The signal from the optocoupler is designed to trip the 1V threshold of the UCC3809 internal comparator when the output voltage exceeds its specified limit.

SETTING UP THE SECONDARY SIDE ERROR AMPLIFIER, UC3965

Because the flyback converter in this design is input-output isolated, the error amplifier needed to sense the output voltage is on the secondary side. The designers of the UCC3809 considered this when designing the circuit and omitted the error amplifier from this IC. Utilizing the UC3965 Precision Reference and Low Offset Error Amplifier satisfies the requirement for a secondary side error amplifier and has an on-board precision reference needed for accurate regulation.

Biasing, UVLO, and Decoupling

Because the UVLO threshold of the UC3965 is 4.1V, the secondary side IC can be biased from the 5V output bus. To prevent the ripple voltage from tripping the under voltage lockout, a 47µF decoupling capacitor is used. A Schottky diode in series with the input pin is required to prevent the decoupling capacitors from discharging with the output capacitors during the FET on-time.

Output Voltage Sensing

The precision reference of the UC3965 is tied to the non-inverting input of the device's internal error amplifier. The output voltage of the converter is resistively divided and compared to this reference at the inverting input. This error amplifier has a low 1mV input offset voltage that insures accurate regulation of V_o. The error amplifier drives the inverting input of an internal buffer whose output is then used to drive an optocoupler diode. As the output voltage increases beyond its desired value, the voltage difference at the error amplifier increases. This results in less drive at the inverting input of the internal buffer, increasing its output drive to the optocoupler. If the application does not require input-output isolation, this buffer could be used to drive the PWM directly.

Loop Compensation [5] [6]

As previously alluded to, a continuous current mode flyback will contain a right-half-plane (RHP) zero in its transfer function. What exactly does this mean? Basically, any increase in load current will require the primary peak inductor current to increase. The duty cycle must increase to accomplish this. In a flyback converter, the inductor current flows to the output only when the FET is off and the diode is conducting. Increasing the duty cycle increases the FET conduction time but decreases the diode conduction time. Ironically, the result of this is the average diode current, the current that supplies the load, actually decreases. This is a temporary situation; as the inductor current rises, the diode current eventually reaches its proper value. The condition where the average diode current must actually decrease before it can increase is referred to as a right-half-plane zero. To complicate matters, this zero contributes a phase lag, not a phase lead as a normal zero would. This zero moves in frequency as a function of load and input voltage, as shown in (26), making it impossible to cancel out by the insertion of a pole.

$$f_{RHPZERO} = \frac{N \bullet V_{IN}^{\,2}}{2 \bullet \pi \bullet R_{OUT} \bullet L_P \bullet (V_{IN} + N \bullet V_{OUT})} \quad (26)$$

The easiest way to deal with a right-half-plane zero is to roll off the loop gain at a relatively low frequency using simple dominant pole compensation. Unfortunately, the result of this is poor dynamic response.

The primary goal of the compensation network is to provide good line and load regulation and dynamic response. These objectives are best met by providing high gain at low frequencies for good DC regulation and high bandwidth for good transient response. Optimum closed loop performance can only be achieved by first knowing what the transfer characteristic of the PWM and switching circuit looks like. Constructing a Bode plot of the known poles and zeroes in the power stage does this. Bode plots give a visual interpretation of the gain versus frequency and phase versus frequency characteristics of a system. In the gain plot, the gain shown at each frequency represents the amount by which the feedback loop will reduce a disturbance at that frequency.

Besides the RHP zero, the output capacitor and the load contribute a pole at a frequency determined by (27), and the output capacitor alone will contribute a zero based upon its ESR and capacitance as shown in (28).

$$f_{pole} = \frac{1+D}{2 \bullet \pi \bullet R_{OUT} \bullet C_{OUT}} \quad (27)$$

$$f_{zero} = \frac{1}{2\pi \bullet ESR \bullet C_{OUT}} \quad (28)$$

The control to output gain [7] is calculated using (29):

$$GAIN = 20 \bullet \log \bullet \left[\frac{I_{sc} \bullet R_{OUT} \bullet V_{IN}}{V_C \bullet (1-D) \bullet (2 \bullet N \bullet V_O + V_{IN})} \right] \quad (29)$$

In this equation, the output short circuit current, I_{sc}, was calculated previously. V_c is the control voltage, equal to 2.5V in the UC3965. In addition to the control to output gain, the optocoupler will also contribute a gain based upon its current transfer ratio and a phase lag due to its large collector to base capacitance. Because the optocoupler data sheet usually does not include any frequency dependent curves, the bandwidth was measured in the lab using a network analyzer. The gain contribution from the optocoupler averaged 7dB and the expected pole was not evident in scans run up to 60kHz. The closed loop gain of the inner current loop is equal to the inverse of the sense resistor, $1/R_{sense}$, or 16dB. By adding all of these factors together, a Bode plot of the uncompensated system can be realized.

Once the frequency response of the uncompensated system is determined, the next step is to determine what compensation is needed around the error amplifier for optimum performance. As stated earlier, optimum performance requires a high gain at low frequencies for good DC regulation and high bandwidth for good transient response. The crossover frequency, f_c, is the frequency at which the gain magnitude equals 0dB. High bandwidth is achieved by having the highest possible f_c. Because of the RHP zero, the highest possible crossover frequency is limited to $f_{RHPZERO}/\pi$.The phase margin, or the amount the phase lag measures at f_c less 180°, should be at least 45° for good transient response with little overshoot.The magnitude of the gain at the frequency where the phase plot measures –180° is referred to as the gain margin. If the slope of the gain plot is –2, or –40dB/decade, at low frequencies, it must transition to a –20dB/decade slope, also known as a –1 slope, one decade before crossing the 0dB point.If the slope remains at the –2 slope the resultant gain margin would be too small causing severe underdamped oscillations at f_c.

With all these tricks of the trade in mind, the compensation network is designed around the error amplifier.A certain amount of juggling is inevitable but, in general, the scheme shown in Figure 7 will handle most compensation requirements. There is a pole at the origin which contributes a –1 slope in the gain plot, a low frequency zero, f_{EAZERO} (30), flattens out the slope so the midrange gain is equal to R_f/R_i. A high frequency pole, f_{EAPOLE} (31), helps suppress any high frequency noise from propagating through the system. R_d forms a voltage divider with R_i and provides a DC offset.

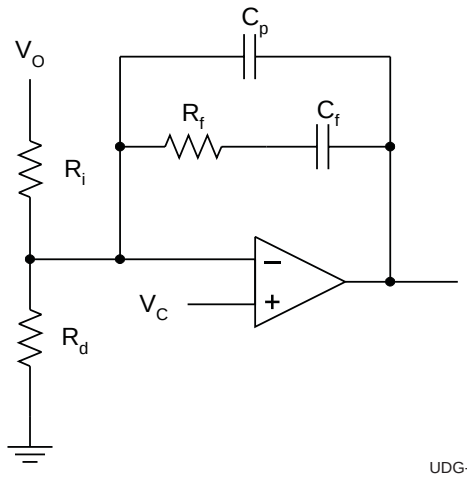

Figure 7. Error amplifier compensation network.

By combining the Bode plots of the PWM and power stage with the error amplifier compensation, a plot of the entire system is realized.

$$f_{EAZERO} = \frac{1}{2 \bullet \pi \bullet R_f \bullet C_f} \quad (30)$$

$$f_{EAPOLE} = \frac{1}{2 \bullet \pi \bullet R_f \bullet C_p} \quad (31)$$

The following graphs show examples of Bode plots before and after compensation.

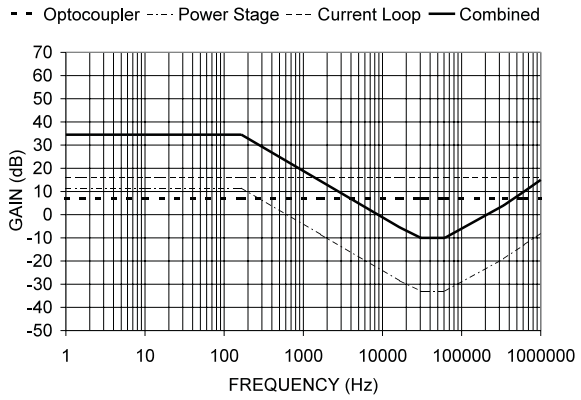

Figure 8. Gain Bode plot without compensation.

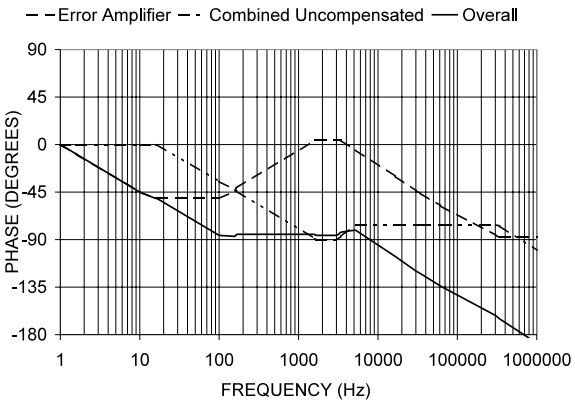

Figure 11. Phase bode plot with compensation.

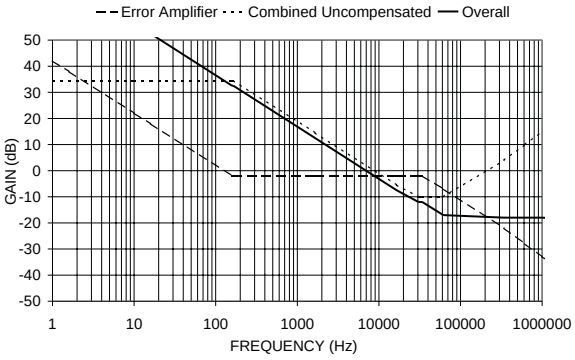

Figure 9. Gain Bode plot with compensation.

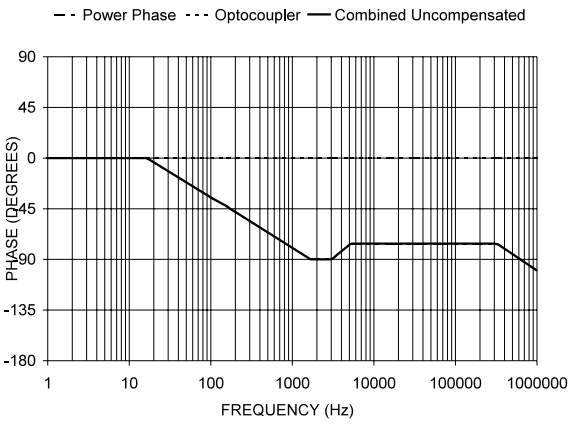

Figure 10. Phase Bode plot without compensation.

SNUBBERS AND CLAMPS [7]

Transformer leakage inductance imposes high transients in the switch, requiring a switching device with an excessive voltage rating. The primary side of the demo board utilizes a passive polarized voltage clamp (Figure 12) to suppress the voltage overshoot during the turn-off transition of the FET. This circuit limits the peak switch voltage, reducing the power dissipation in the switching device. The total dissipated energy remains the same, but it is now divided between the clamp resistor and the FET.

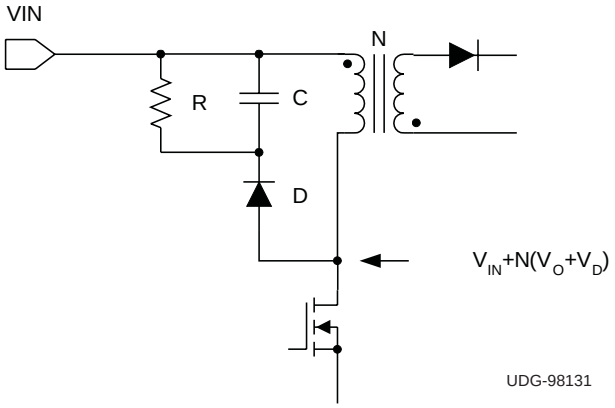

Figure 12. RCD clamp on the primary side suppresses voltage overshoot across the FET.

The parasitic inductance of the transformer is discharged into the capacitor during each switching cycle. The value of the capacitor is selected based upon the amount of energy that this leakage inductance stores plus the initial energy stored in the capacitor from the input voltage and the reflected output voltage. Equation 32 determines the minimum capacitor value.

$$C = \frac{L_L \bullet (I_{PEAK})^2}{\Delta V_c \bullet (\Delta V_c + 2V)} \quad (32)$$

In the above equation, ΔV_c is equal to the acceptable change of voltage across the capacitor, usually between 40 and 60V. L_L is equal to the leakage inductance of the transformer. I_{PEAK} is equal to the peak current in the inductor at the time of turn-off. V is equal to the DC bias across the capacitor. This DC bias is a result of the DC path through the resistor and diode and the secondary side voltage reflected to the primary:

$$V = N \bullet (V_O + V_D) \quad (33)$$

The resistor is selected such that the RC time constant is much longer than the switching period. This resistor must not only dissipate the energy stored in the leakage inductance, but also the voltage due to the DC bias of the capacitor:

$$P_R = \frac{L_L \bullet (I_{PEAK})^2 \bullet f_{sw}}{2} + \frac{V^2}{R} \quad (34)$$

The resistor used on the demo board must dissipate 2.4W of power. The diode is selected based upon the charging current of the capacitor.

The secondary side of the converter requires an RC snubber across the diode (Figure 13) to damp the high frequency ringing on the 5V bus due to the parasitic inductance of the transformer and parasitic capacitance of the Schottky.

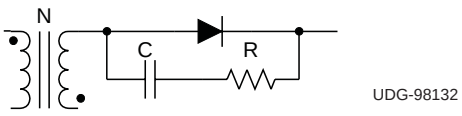

Figure 13. RC snubber on the secondary side dampens parasitic oscillations.

The capacitor is chosen such that, when placed across the Schottky, the oscillating frequency, f_{osc}, is reduced by approximately half. The leakage inductance, L_{SL} and parasitic capacitance, C_p can be determined by simultaneously solving (35a) and (35b).

$$f_{osc} = \frac{1}{2 \bullet \pi \bullet \sqrt{L_{SL} \bullet C_p}} \quad (35a)$$

$$\frac{f_{osc}}{2} = \frac{1}{2 \bullet \pi \bullet \sqrt{L_{SL} \bullet (C_p + C)}} \quad (35b)$$

In (35b), C is the capacitor that was added to reduce the oscillation frequency. The appropriate value of the resistor is selected to provide critical damping to the oscillation:

$$R = \sqrt{\frac{L_L}{(C_p + C)}} \quad (36)$$

Because the time constant of this RC snubber is much less than the switching period but much longer than the voltage rise time, the power dissipated by the resistor is dependent upon the energy stored in the capacitor. Since the capacitor charges and discharges each cycle, the power the resistor must dissipate is equal to:

$$P_R = C \bullet V^2 \bullet f_{sw} \quad (37)$$

In (37), C is the RC snubber capacitor value. V is equal to the drain to source voltage reflected to the secondary side added to the output voltage plus the voltage drop across the diode. This snubber circuit will prevent the anode of the diode from ringing below the reverse voltage rating of the Schottky device.

LC FILTER

The voltage ripple on the output will occur at the switching frequency and is required to be less than 50mV peak to peak. To meet the output noise specification, an LC filter was added to the converter output. The unfiltered ripple, V_R, will be equal to the peak secondary current multiplied by the ESR of the output capacitor bank. The amount of attenuation needed to filter the ripple, V_R, to an acceptable level is determined by (38)

$$ATTEN_{db} = -20 \bullet \log \bullet \left(\frac{V_R}{0.05} \right) \quad (38)$$

An LC filter will produce a gain plot with a –40dB/decade slope. The selected LC filter should have a pole that results in a minimum gain derived from (38) at the switching frequency. The pole frequency will occur at:

$$f_{pole} = \frac{1}{2 \bullet \pi \bullet \sqrt{LC}} \quad (39)$$

The demo board employs a 2µH iron powder toroid and a 33µF electrolytic capacitor for a pole frequency of 20kHz and a minimum gain of –8dB.

EXPERIMENTAL RESULTS

The oscilloscope traces refer to the test points (TP) indicated and are referenced to the appropriate ground, either primary or secondary.

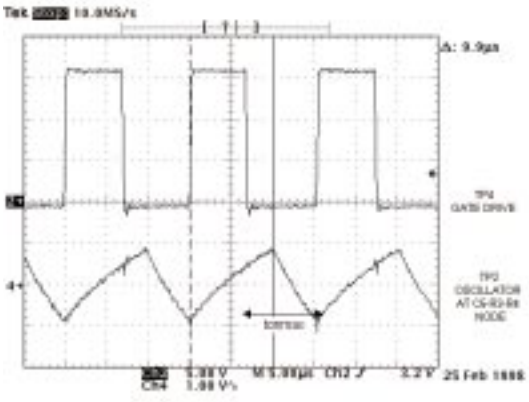

Figure 14. The UCC3809 gate drive and oscillator.

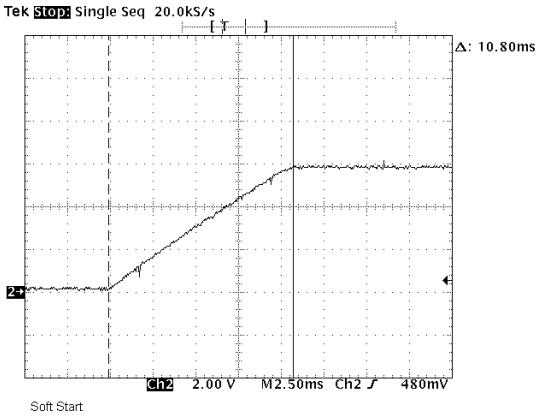

Figure 15. Soft start capacitor charging waveform.

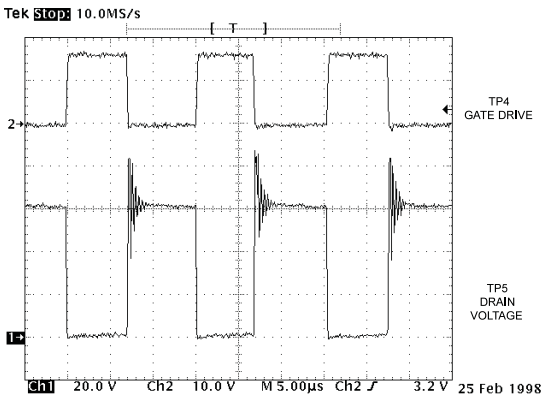

Figure 16. Gate and drain in continuous conduction mode.

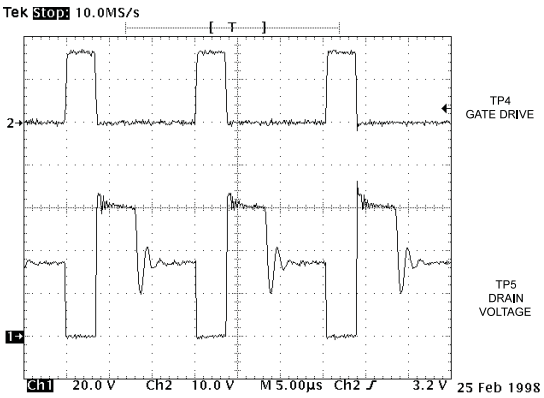

Figure 17. Gate and drain in discontinuous conduction mode.

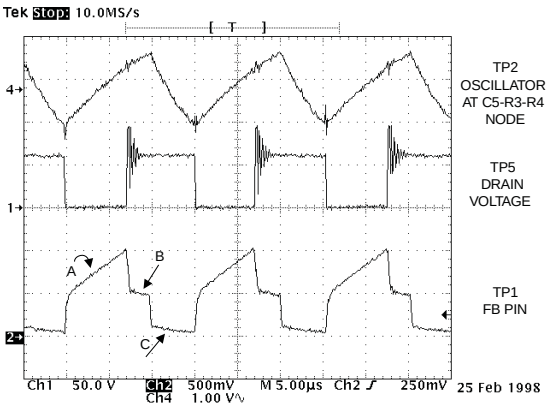

Figure 18. The FB pin in continuous conduction mode.

In Figure 18, the FB pin is shown in the bottom trace. Region A is the summation of the current sense and voltage feedback , at 1V the gate is turned off, resulting in the drain establishing a voltage with respect to the source. Region B results from the FB pin still sensing the voltage feedback during the remaining oscillator charge time. Region C is where the internal 250Ω on resistance FET is turned on during the PWM off time, discharging all external capacitance at that node.

Efficiency measurements performed yielded the following results.

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	n
31.763	1.830	58.126	5.019	9.211	46.225	0.795
31.954	1.809	57.805	5.014	9.178	46.022	0.796
48.014	1.178	56.560	5.017	9.202	46.168	0.816
48.073	1.172	56.342	5.015	9.185	46.060	0.818
72.038	0.780	56.190	5.015	9.187	46.071	0.820

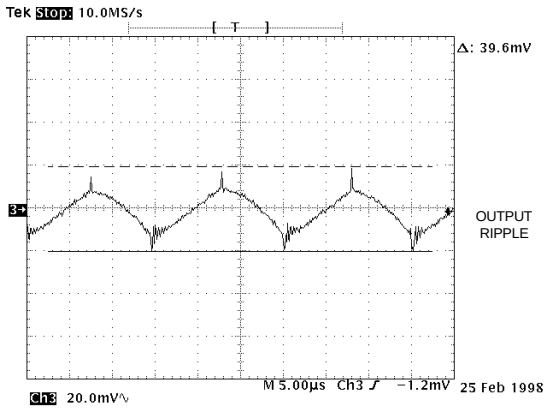

Figure 19. Output voltage ripple waveform.

ALTERNATE OUTPUT VOLTAGES

A user may require an output voltage different from the 5V discussed thus far. By working through this design review and substituting the required output voltage level, new peak currents and maximum duty cycles can be determined. These changes will be reflected in the selection of appropriate components such as the MOSFET, sense resistor, diode, and output capacitors. The transformer would be redesigned for the optimum turns ratio, wire sizes, and core requirements for the given design.

Table 1. Demonstration board parts list.

Reference Designator	Description	Manufacturer	Part Number
C1, C2	150mF, 80V, Aluminum Capacitor	United Chemi-Con	SXE80VB151M12X20LL
C3	1µF, 100V, Ceramic Capacitor	KEMET	C340C105K1R5CA
C4, C22	0.01µF, 50V, Ceramic Capacitor		
C5	1nF, 50V, Ceramic Capacitor		
C6	330pF, 50V, Ceramic Capacitor		
C7	0.47µF, 50V, Ceramic Capacitor		
C8	1µF, 50V, Ceramic Capacitor		
C9, C12	0.1µF, 50V, Ceramic Capacitor		
C10	0.22µF, 100V, Ceramic Capacitor	KEMET	C330C224K1R5CA
C11	1µF, 35V, Tantalum Capacitor		
C14	0.22µF, 50V, Ceramic Capacitor		
C15	0.015µF, 50V, Ceramic Capacitor		
C16, C17, C18, C19	330µF, 6.3V, Aluminum Capacitors	SANYO	OSCON 6SH330M
C20	33µF, 10V, Tantalum Capacitor		
C21	47µF, 25V, Aluminum Electrolytic	Panasonic	ECE-A1AFS470
C23	6800pF, 50V, Ceramic Capacitor		
D1	ZENER, 5.1V		1N5231
D2	ZENER, 15V		1N5245
D3	2A, 200V, Ultra Fast		SF24
D4	ZENER, 10V		1N5240
D5	1A Schottky		1N5819
L1	2.5µH, 11A	Coiltronics, Inc.	CTX08-14017
Q1, Q4	small signal NPN		MPS2222A
Q2	small signal PNP		MPS2907A
Q3	200V, 18A, N-Channel MOSFET	Motorola or IR	IRF640

Reference Designator	Description	Manufacturer	Part Number
R1	5.1K, ¼W, 5%		
R2, R13	1.1K, ¼W, 5%		
R3	12.1K, ¼W, 5%		
R4	6.19K, ¼W, 5%		
R5	470, ¼W, 5%		
R6	1.0K, ¼W, 5%		
R7	15K, ¼W, 5%		
R8	0.15, 3W, 5%	RCD	RSF2B0.15 ohm 5%
R9	2K, 3W, 5%	RCD	RSF2B2K ohm 5%
R10	10, ¼W, 5%		
R11	680, ¼W, 5%		
R12	27K, ¼W, 5%		
R14	750, ¼W, 5%		
R16, R17	12.1K, ¼W, 1%		
R18	3.01K, ¼W, 5%		
R19	5.1, 3W, 5%	RCD	RSF2B5.1 ohm 5%
R20	5.62K, ¼W, 5%		
R21	475, ¼W, 1%		
T1	80μH, N = 5	Coiltronics, Inc.	CTX08-13916
U1	PWM Controller	Unitrode	UCC3809
U2	25A, 35V Power Schottky Rectifier	Motorola	MBR2535CTL
U3	Optocoupler	Motorola	H11AV1
U4	Error Amplifier, Reference	Unitrode	UC3965
Heatsink	For TO-220	AAVID	529802 B 0 25 00

SUMMARY

The UCC3809/UC3965 demo board is an example of a 50 Watt continuous current mode flyback converter that includes features such as a duty cycle clamp, slope compensation, input to output isolation, and primary and secondary snubbers, just to name a few. A detailed step by step approach is given for power stage component selection, transformer design, loop compensation, and component power dissipation calculations. The features of the UCC3809 and the UC3965 offer design flexibility for a wide range of applications in simple to use 8-pin packages.

REFERENCES

[1] Abraham I. Pressman, *Switching Power Supply Design,* McGraw-Hill, Inc., 1991.

[2] Lloyd H. Dixon, Jr., *Filter Inductor and Flyback Transformer Design for Switching Power Supplies*, Unitrode Power Supply Design Seminar Manual SEM-1100, 1996.

[3] Bill Andreycak, *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits*, Unitrode Application Note U-137, Unitrode Applications Handbook IC# 1051, 1997.

[4] Bill Andreycak, *Practical Considerations in Current Mode Power Supplies*, Unitrode Application Note U-111, Unitrode Applications Handbook IC# 1051, 1997.

[5] Lloyd H. Dixon, Jr., *Control Loop Cookbook*, Unitrode Power Supply Design Seminar Manual SEM-1100, 1996.

[6] Lloyd H. Dixon, Jr., *Closing the Feedback Loop*, Unitrode Power Supply Design Seminar Manual SEM-700, 1990.

[7] Philip C. Todd, *Snubber Circuits: Theory, Design, and Application*, Unitrode Power Supply Design Seminar Manual SEM-900, 1993.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.