DIGITAL ELECTRONICS: ECE 213

Topic: Sequential Circuits, Latches and Flip flops

UNIT IV: Introduction to Sequential Circuits

Lecture No.: 26

Prepared By: Irfan Ahmad Pindoo

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Introduction to Sequential Circuits

- Sequential circuits are those in which the output depends not only on the present inputs, but also on the previous output state and/or the previous inputs.

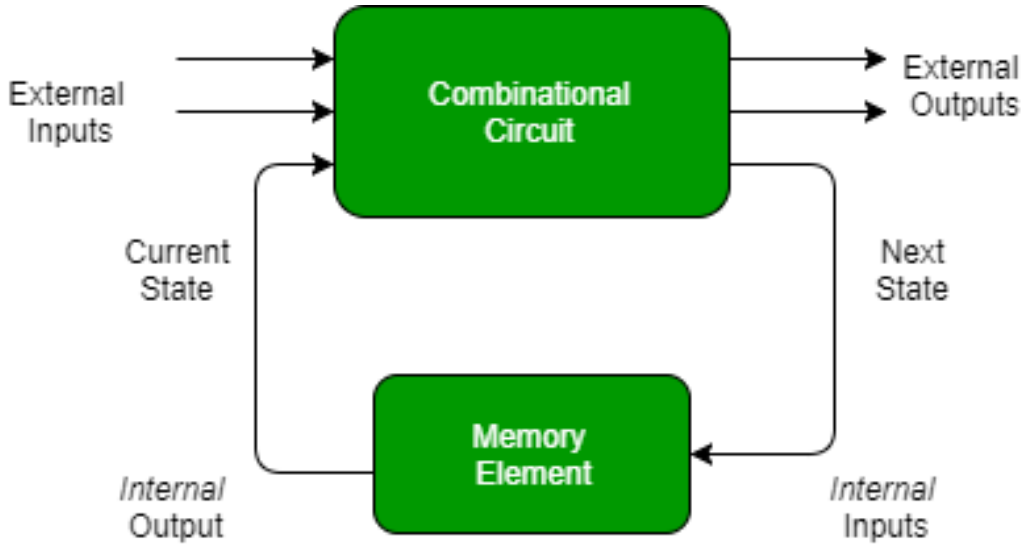


Figure: Sequential Circuit

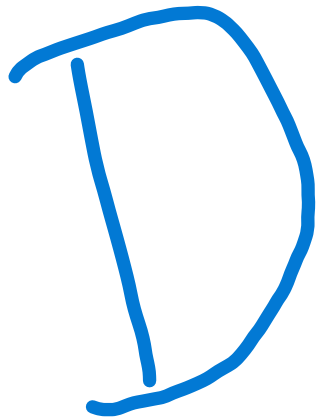
Difference between Combinational and Sequential Circuits

Combinational Circuits	Sequential Circuits
The output depends only upon the present inputs	output depends not only on the present inputs, but also on the previous output state and/or the previous inputs
No feedback	Feedback available from output to input
No ability to store	Ability to store
Easier to design, use and handle	not easier to design, use and handle
No clock signal	Clock signals are required for triggering purposes
Faster	slower than combinational circuits
Elementary building block: Logic gates	Elementary building block: Flip flops
Examples: Adder, Subtractor, Magnitude comparator, Multiplexer, Decoder, etc.	Examples: Latches, flip flops, counters, registers,etc.

QUICK QUIZ (POLL)

Which of the following is NOT the combinational circuit?

a) magnitude comparator
b) multiplexer
c) parity generator circuit
d) Flip flop



Basic Storage Element: Latch

- A storage element in a digital circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit), until directed by an input signal to switch states.
- Storage elements that operate with **signal levels** (rather than signal transitions) are referred to as latches; those controlled by a **clock transition** are flip-flops.
- Because they are the building blocks of flip-flops, so, we will consider the fundamental storage mechanism used in latches before considering flip-flops.

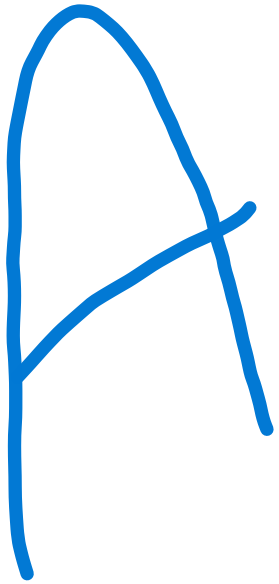
SR Latch

- The SR latch is a circuit with two cross-coupled NOR gates or two cross-coupled NAND gates, and two inputs labeled S for set and R for reset.
- The latch has two useful states:
  1. When output Q = 1 and Q'= 0, the latch is said to be in the set state.
  2. When Q = 0 and Q'= 1, it is in the reset state.
- Outputs Q and $Q'$are normally the complement of each other. Otherwise, the device will enter an unpredictable or undefined state or a metastable state.

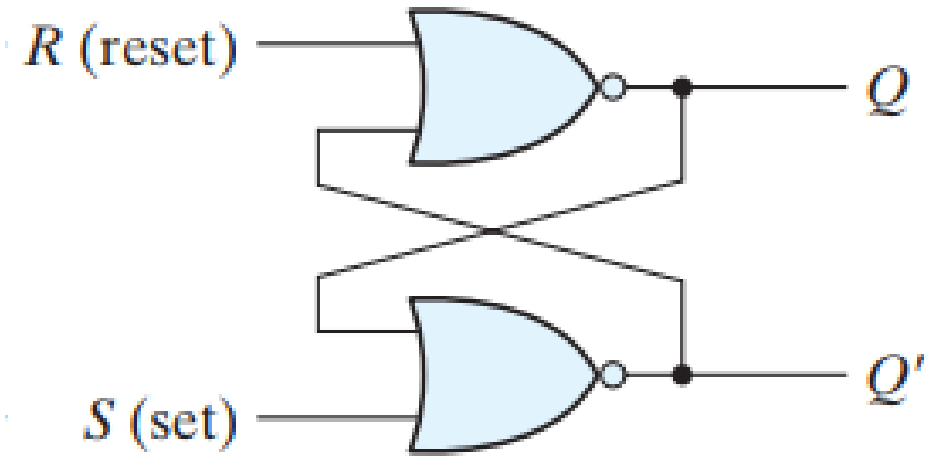
QUICK QUIZ (POLL)

What is the output state in SR latch at Q = 1 and Q'= 0

a) set
b) reset
c) memory
d) indeterminate



SR NOR Latch



S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

QUICK QUIZ (POLL)

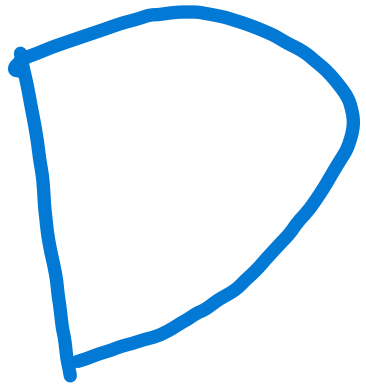
Which of the following state is invalid/indeterminate in SR NOR latch?

a) S=1, R= 0

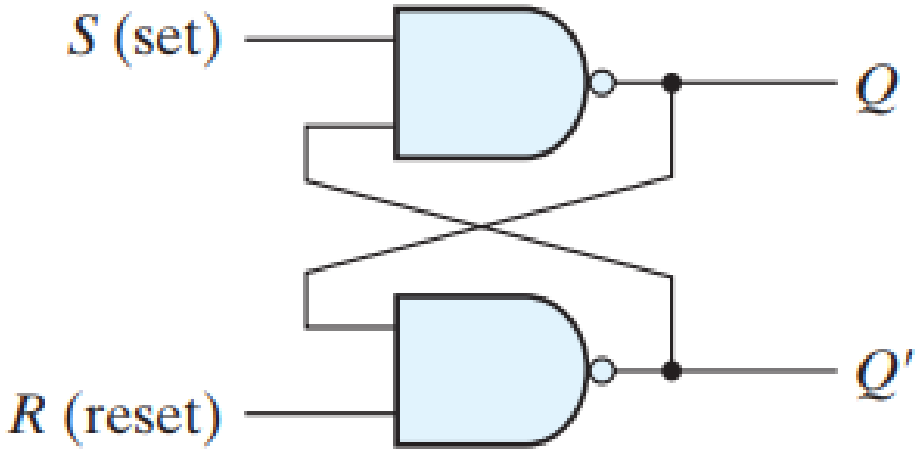
b) S=0, R= 1

c) S=0, R= 0

d) S=1, R= 1



SR NAND Latch



S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

- Because the NAND latch requires a 0 signal to change its state, it is sometimes referred to as an $S'R'$ latch.
- The primes (or, sometimes, bars over the letters) designate the fact that the inputs must be in their complement form to activate the circuit.

QUICK QUIZ (POLL)

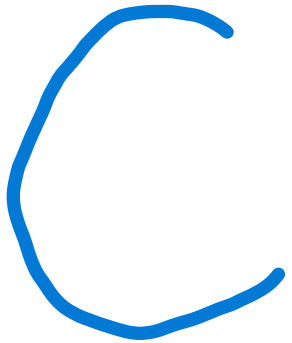
Which of the following state is invalid/indeterminate in SR NAND latch?

a) S=1, R= 0

b) S=0, R= 1

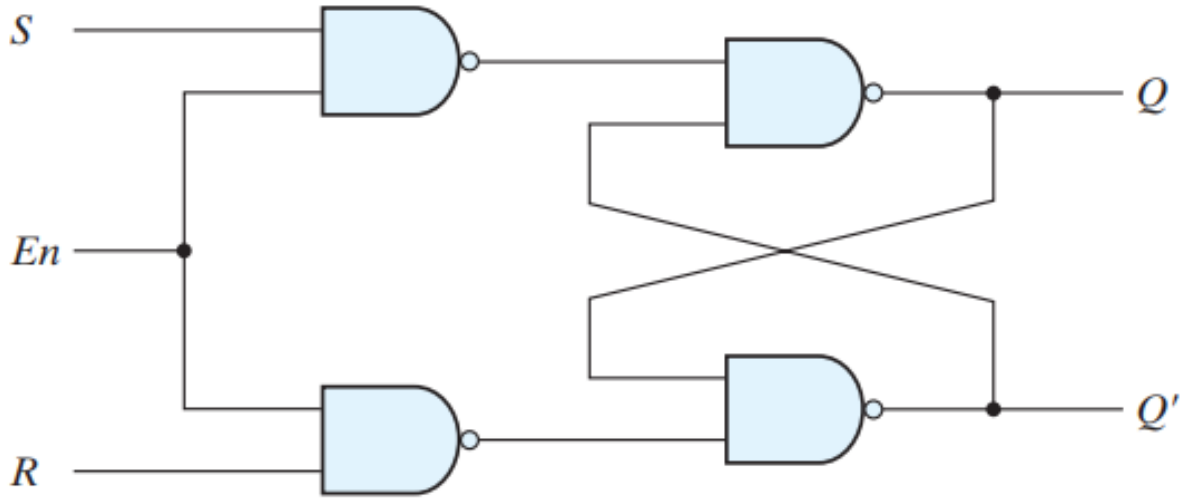
c) S=0, R= 0

d) S=1, R= 1



SR Latch with control input

- The operation of the basic SR latch can be modified by providing an additional input signal that determines (controls) when the state of the latch can be changed by determining whether S and R can affect the circuit.



(a) Logic diagram

En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

QUICK QUIZ (POLL)

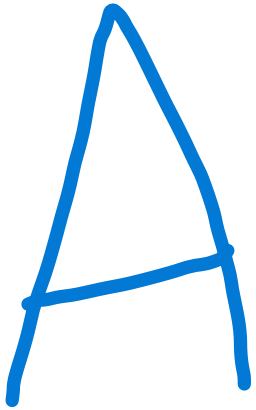
What is the output state in SR enabled NAND based latch at S=1, R= 0, and En=0?

a) Q= set

b) Q=reset

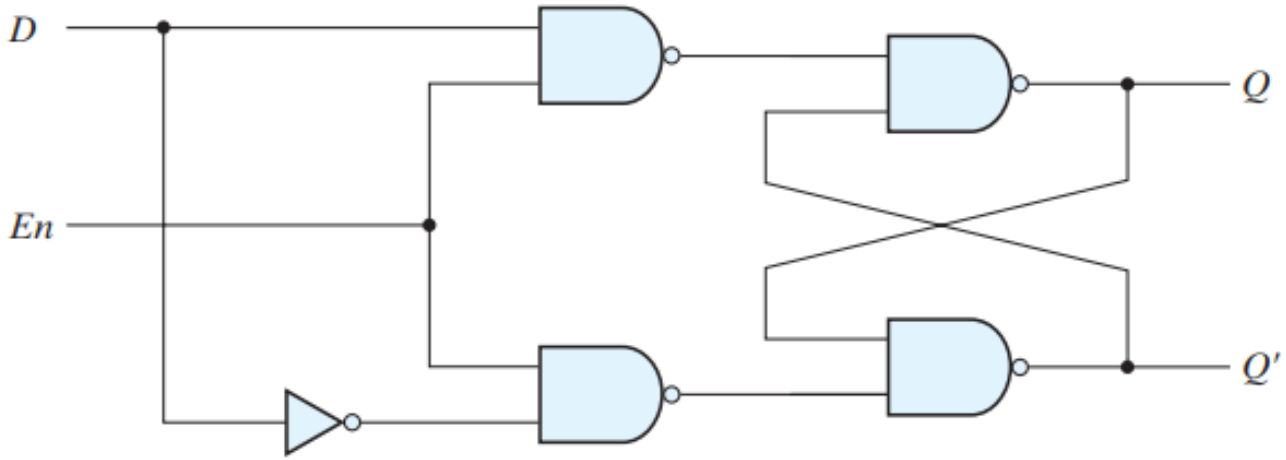
c) Q=memory

d) Q=indeterminate



D Latch (Transparent Latch)

- One way to eliminate the undesirable condition of the indeterminate state in the SR latch is to ensure that inputs S and R are never equal to 1 or 0 at the same time. This is done in the D latch.



(a) Logic diagram

En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

D Latch (Transparent Latch)

- The D latch receives that name from its ability to hold *data* in its internal storage. It is suited for use as a temporary storage.
- The binary information present at the data input of the D latch is transferred to the Q output when the enable input is asserted.
- The output follows changes in the data input as long as the enable input is asserted. This situation provides a path from input D to the output, and for this reason, the circuit is often called a transparent latch.
- When the enable input signal is de-asserted, the binary information that was present at the data input at the time the transition occurred is retained (i.e., stored) at the Q output until the enable input is asserted again.

QUICK QUIZ (POLL)

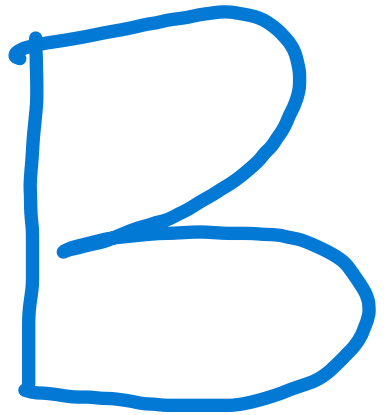
In D flip-flop, D stands for _____

a) Distant

b) Data

c) Desired

d) Delay



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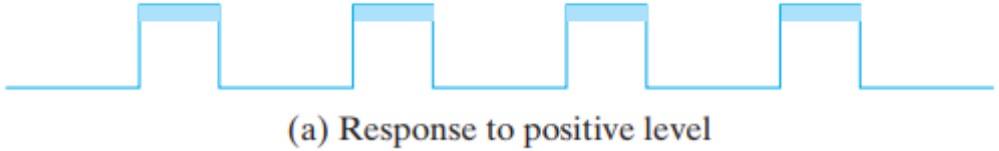
Flip Flop

- A flip flop is an electronic circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying inputs.
- Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.



(a) Response to positive level

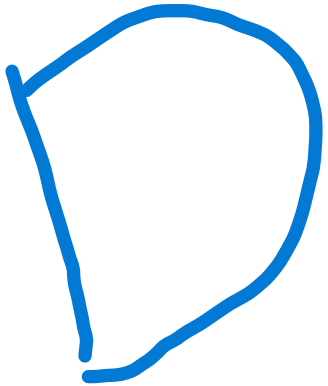
(b) Positive-edge response

(c) Negative-edge response

QUICK QUIZ (POLL)

Flip flops are:

a) Level sensitive
b) Positive edge triggered
c) Negative edge triggered
d) Both b and c



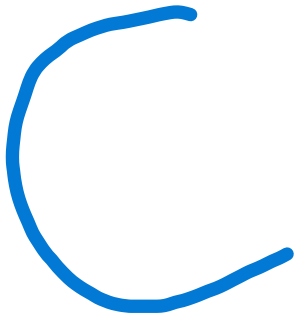
Difference between Latch and Flip Flop

Latch	Flip flop
Level sensitive	Edge sensitive
A latch doesn’t contain any clock signal	A flip-flop contains a clock signal
The structure of Latches is built with logic gates	FFs are designed with latches by adding an extra clock signal.
Latches are responsive toward faults on enable pin	FFs are protected toward faults
Asynchronous	Synchronous
Faster	Slower

QUICK QUIZ (POLL)

Which of the following is synchronous sequential circuit

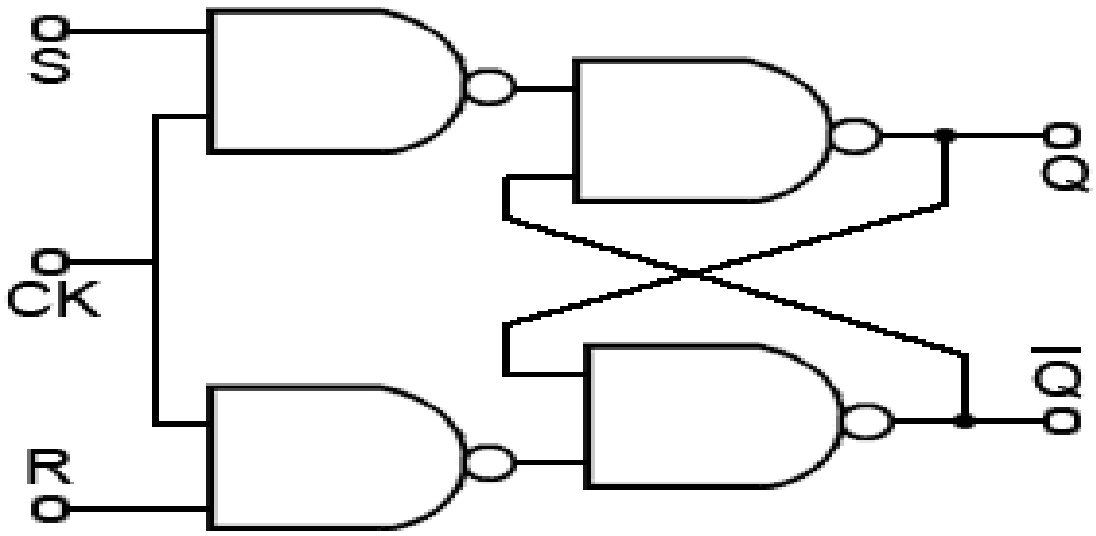
a) NAND based SR latch
b) NOR based SR latch
c) Clocked SR flip flop
d) D latch



Types of Flip Flop

- SR flip flop
- D flip flop
- JK flip flop
- T flip flop

SR Flip Flop



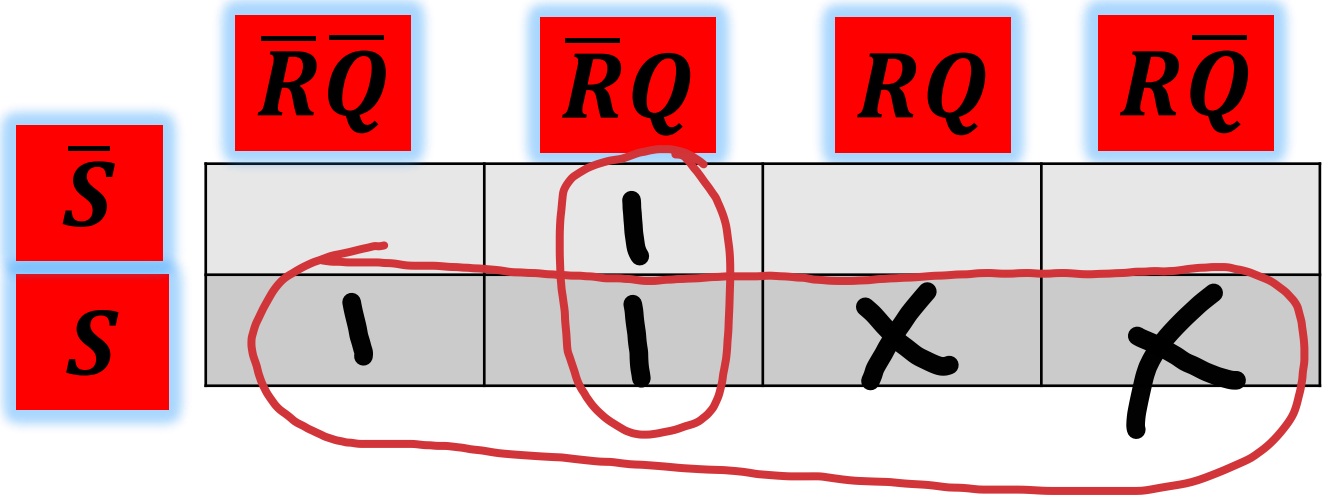
Characteristic Table:

CLK	S	R	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	×	Q_n	$\overline{Q_n}$
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	Invalid	
1	1	1	1	Invalid	

SR Flip Flop

Characteristic Table:

CLK	S	R	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	×	Q_n	$\overline{Q_n}$
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	Indeterminate	
1	1	1	1	Indeterminate	



Characteristic Eq^{n}

$Q_{n+1} = S + RQ_n$

QUICK QUIZ (POLL)

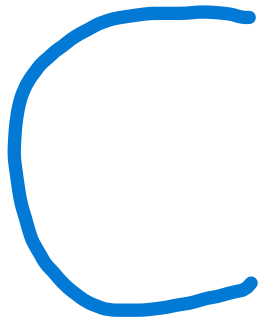
What would be the output state in clocked SR flip flop when S=1, R=0 and CLK=0?

a) SET

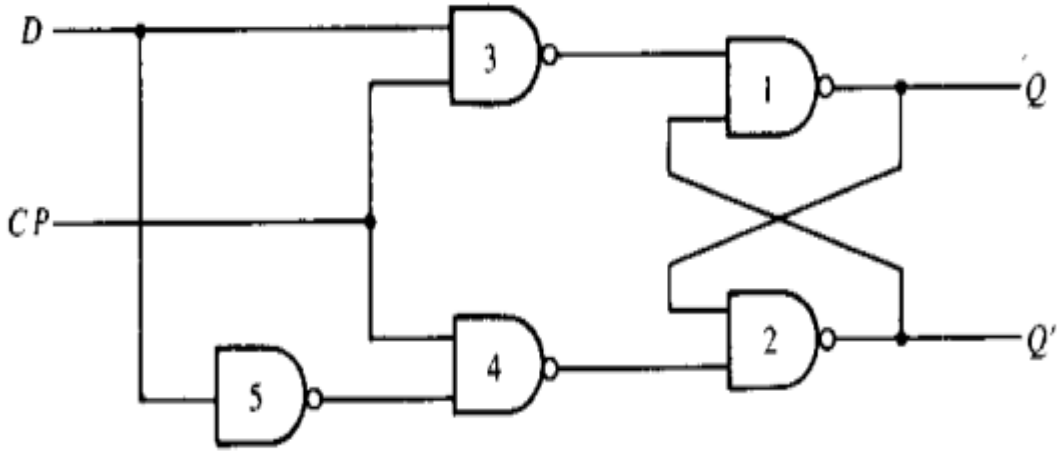
b) RESET

c) MEMORY

d) INVALID



D Flip Flop



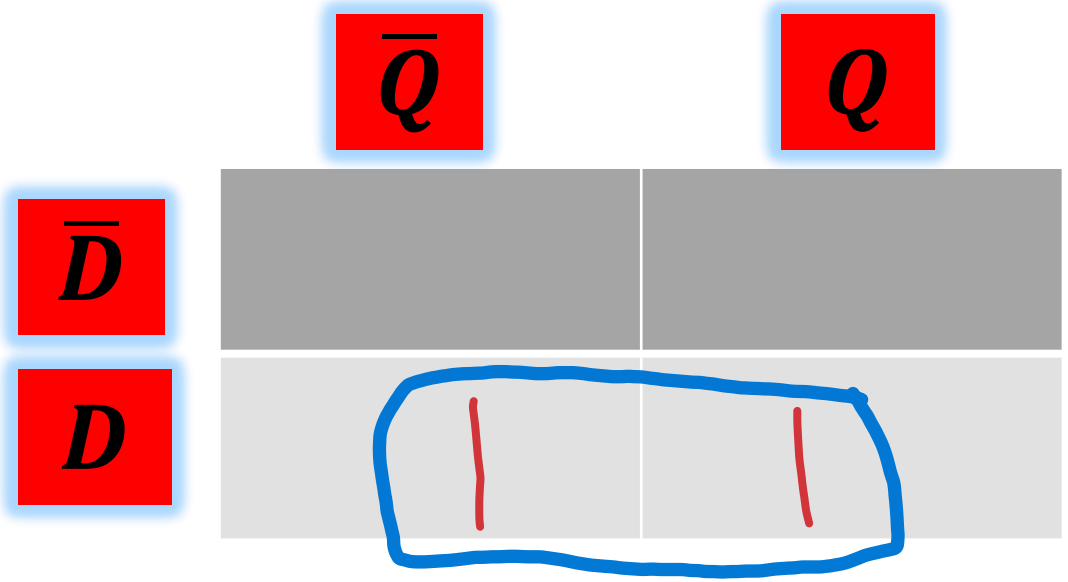
Characteristic Table:

CLK	D	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	Q_n	$\overline{Q_n}$
1	0	0	0	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0

D Flip Flop

Characteristic Table:

CLK	D	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	Q_n	$\overline{Q_n}$
1	0	0	0	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0

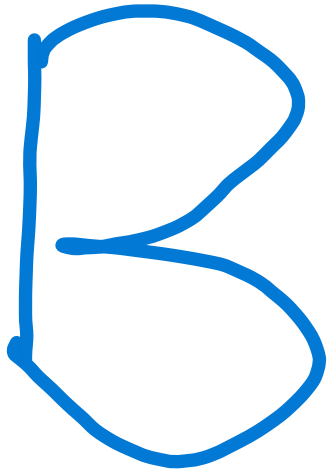


$$Q_{n+1} = D$$

QUICK QUIZ (POLL)

“The output is same as that of input, when clock is enabled”. This statement is true for

a) SR flip flop
b) D flip flop
c) JK flip flop
d) T flip flop



DIGITAL ELECTRONICS: ECE 213

Topic: Flip Flops and Race Around Condition

UNIT IV: Introduction to Sequential Circuits

Lecture No.: 28

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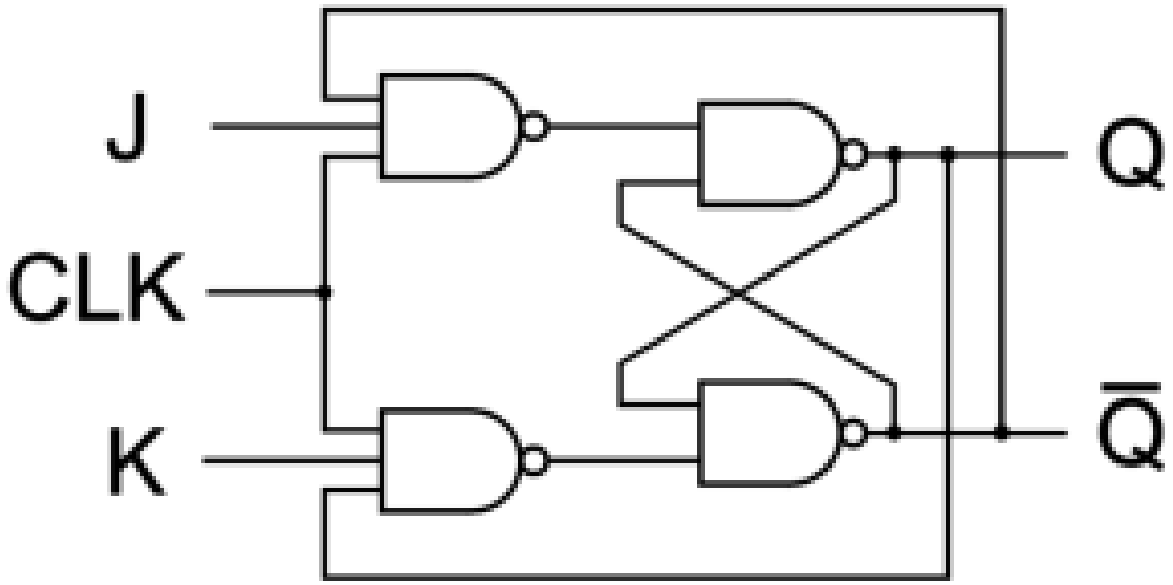
JK Flip Flop



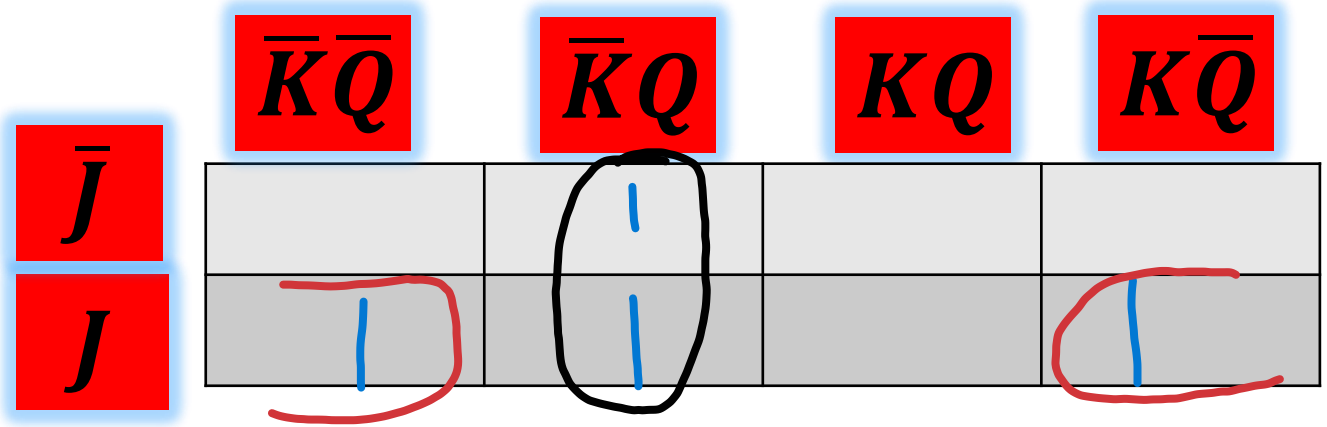
Characteristic Table:

CLK	J	K	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	×	memory	
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	0	1

JK Flip Flop

Characteristic Table:

CLK	J	K	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	×	Q_n	$\overline{Q_n}$
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	1	0
1	1	0	0	1	0
1	1	1	1	0	1



Chracteristic Eq^{n}

$$Q_{n+1} = \bar{J}\bar{Q}_n + \bar{K}Q_n$$

QUICK QUIZ (POLL)

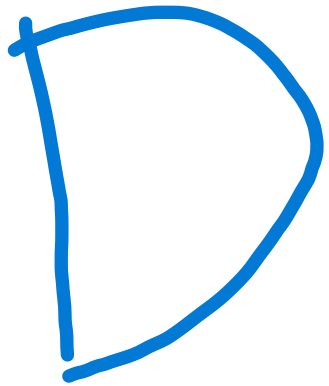
What would be the output state in clocked JK flip flop when J=1, K=1 and CLK=1?

a) SET

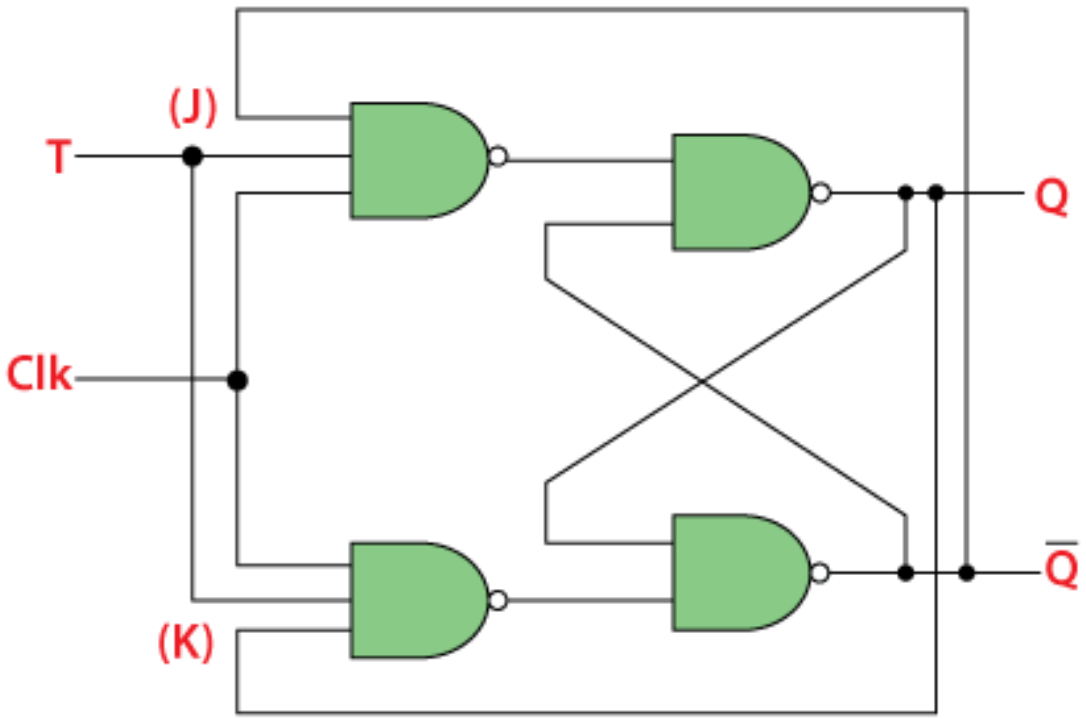
b) RESET

c) MEMORY

d) TOGGLE



Toggle – T Flip Flop



Characteristic Table:

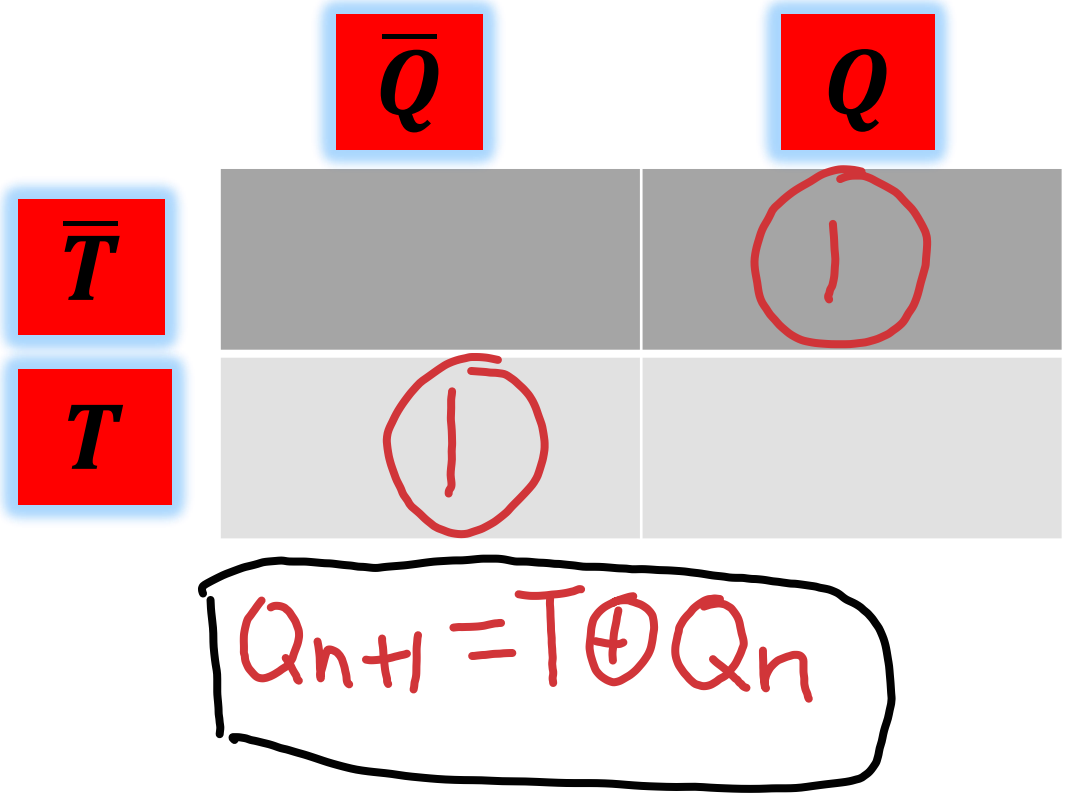
CLK	T	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	Q_n	$\overline{Q_n}$
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

XOR gate

T Flip Flop

Characteristic Table:

CLK	T	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	Q_n	$\overline{Q_n}$
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1



QUICK QUIZ (POLL)

In a J-K flip-flop, if J=K the resulting flip-flop is referred to as _____

a) D flip-flop

b) S-R flip-flop

c) T flip-flop

d) S-K flip-flop

QUICK QUIZ (POLL)

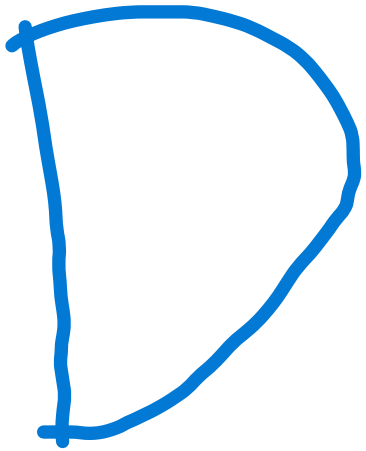
The flip-flops which has not any invalid states are _____

a) S-R, J-K, D

b) S-R, J-K, T

c) J-K, D, S-R

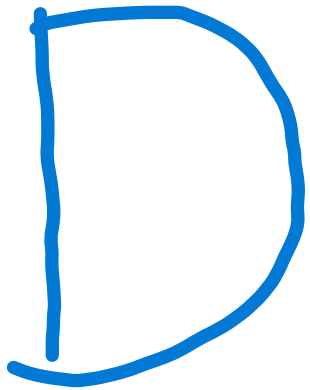
d) J-K, D, T



QUICK QUIZ (POLL)

The characteristic equation for a T flip flop resembles_____ logic gate

a) NOR
b) NAND
c) XNOR
d) XOR



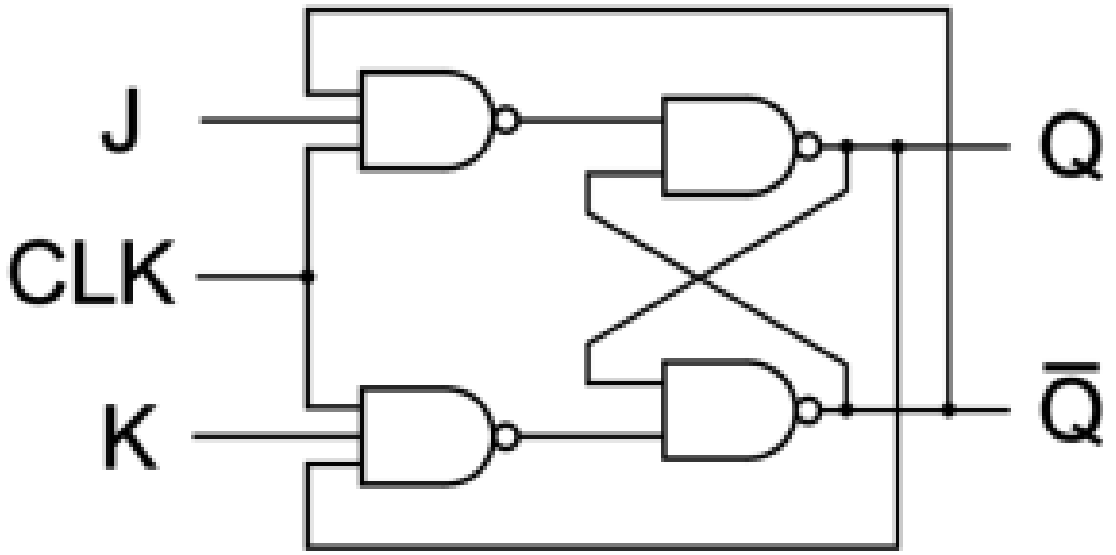
Race around condition in JK Flip Flop

Although, JK flip-flop resolves the invalid state condition of SR flip flop, which occurs when Set and Reset are both set to 1.

There arises a new problem in JK flip flop, when J and K inputs of the JK flip flop are provided with high input i.e., 1, then output continuously toggles into that region (output changes either from 0 to 1 or from 1 to 0, which creates a disturbance in output.

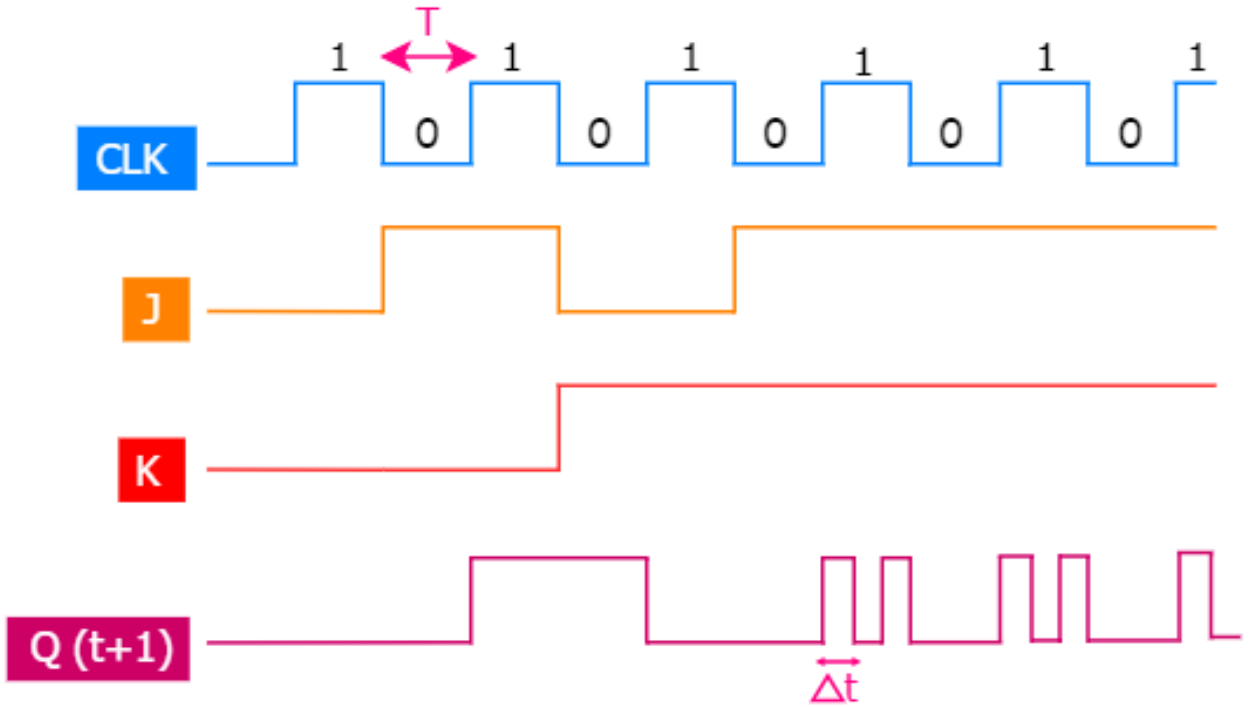
This situation is referred to as the race around the condition.

Race around condition in JK Flip Flop



Race around condition in JK Flip Flop

TIMING DIAGRAM:



DIGITAL ELECTRONICS: ECE 213

Topic: Flip Flops and Race Around Condition

UNIT IV: Introduction to Sequential Circuits

Lecture No.: 29

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School of Computer Science and Engineering

How can we eliminate race around condition?

There are three ways using which we can eliminate the race around condition in JK flip flop, which are discussed below:

1. Increasing the delay of flip-flop
2. Use of edge-triggered flip-flop
3. Use of master-slave JK flip-flop

How can we eliminate race around condition?

Increasing the delay of flip-flop

The propagation delay (delta t) should be made greater than the duration of the clock pulse (T). But it is not a good solution as increasing the delay will decrease the speed of the system.

Use of edge-triggered flip-flop

If the clock is High for a time interval less than the propagation delay of the flip flop then racing around condition can be eliminated. This is done by using the edge-triggered flip flop rather than using the level-triggered flip-flop.

Use of master-slave JK flip-flop

If the flip flop is made to toggle over one clock period then racing around condition can be eliminated. This is done by using Master-Slave JK flip-flop.

QUICK QUIZ (POLL)

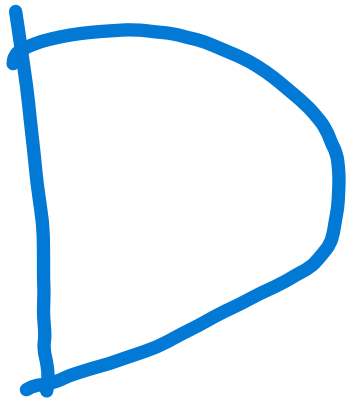
The condition for race around condition in JK flipflop is:

a) J=1, K=0 and CLK=0

b) J=1, K=0 and CLK=1

c) J=1, K=1 and CLK=0

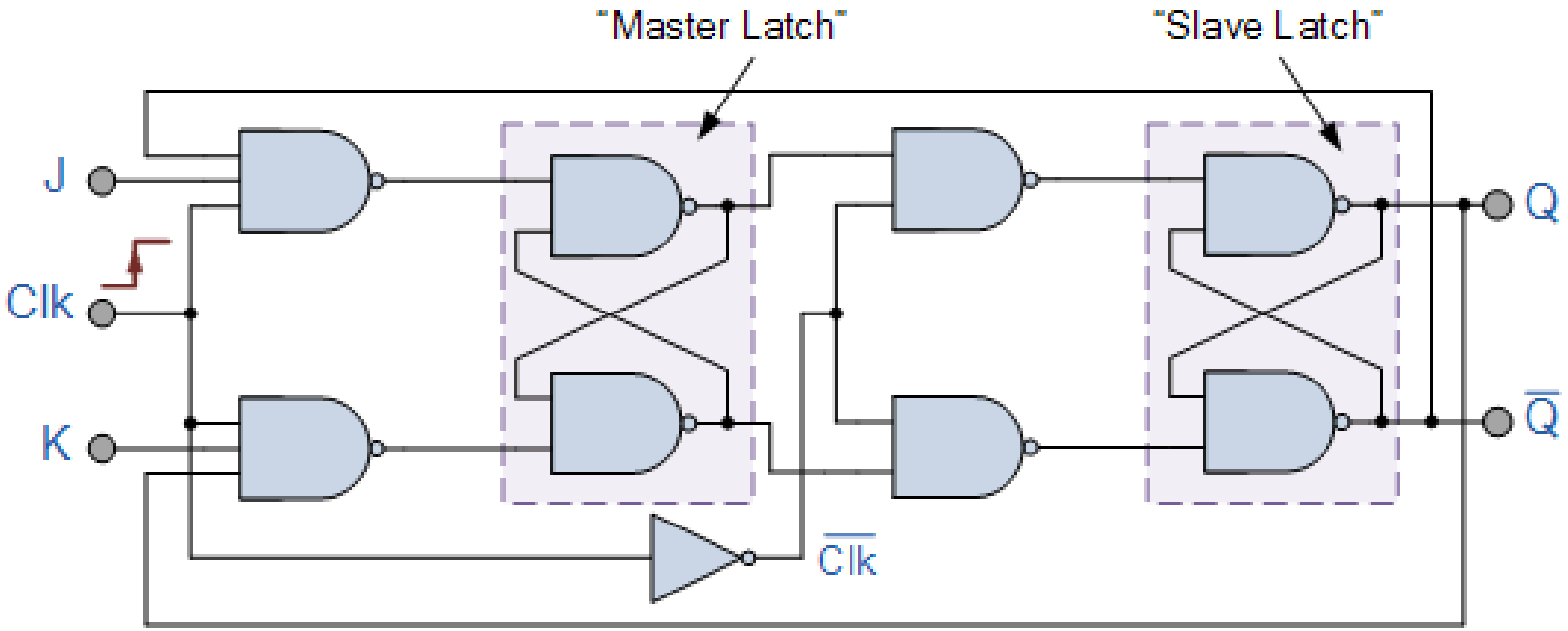
d) J=1, K=1 and CLK=1



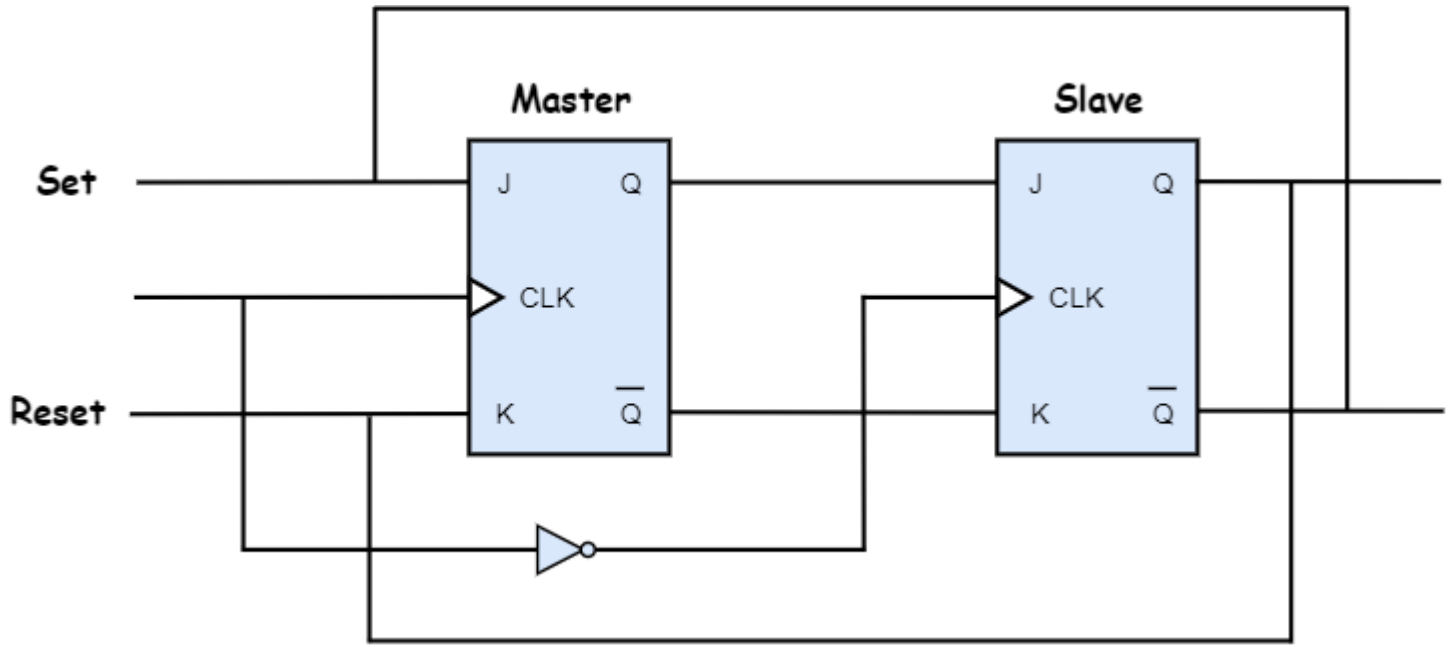
Master Slave JK Flip Flop

- The Master-Slave Flip-Flop is basically a combination of two JK flip-flops connected together in a series configuration. Out of these, one acts as the “master” and the other as a “slave”. The output from the master flip flop is connected to the two inputs of the slave flip flop whose output is fed back to inputs of the master flip flop.
- In addition to these two flip-flops, the circuit also includes an inverter. The inverter is connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip-flop. In other words if CP=0 for a master flip-flop, then CP=1 for a slave flip-flop and if CP=1 for master flip flop then it becomes 0 for slave flip flop

Master Slave JK Flip Flop



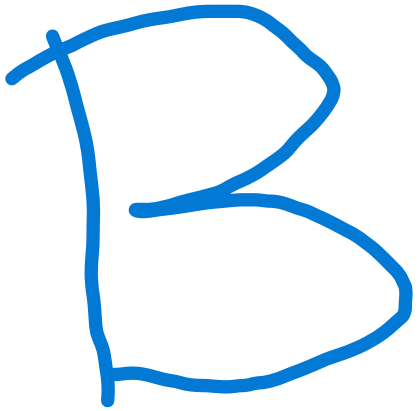
Master Slave JK Flip Flop



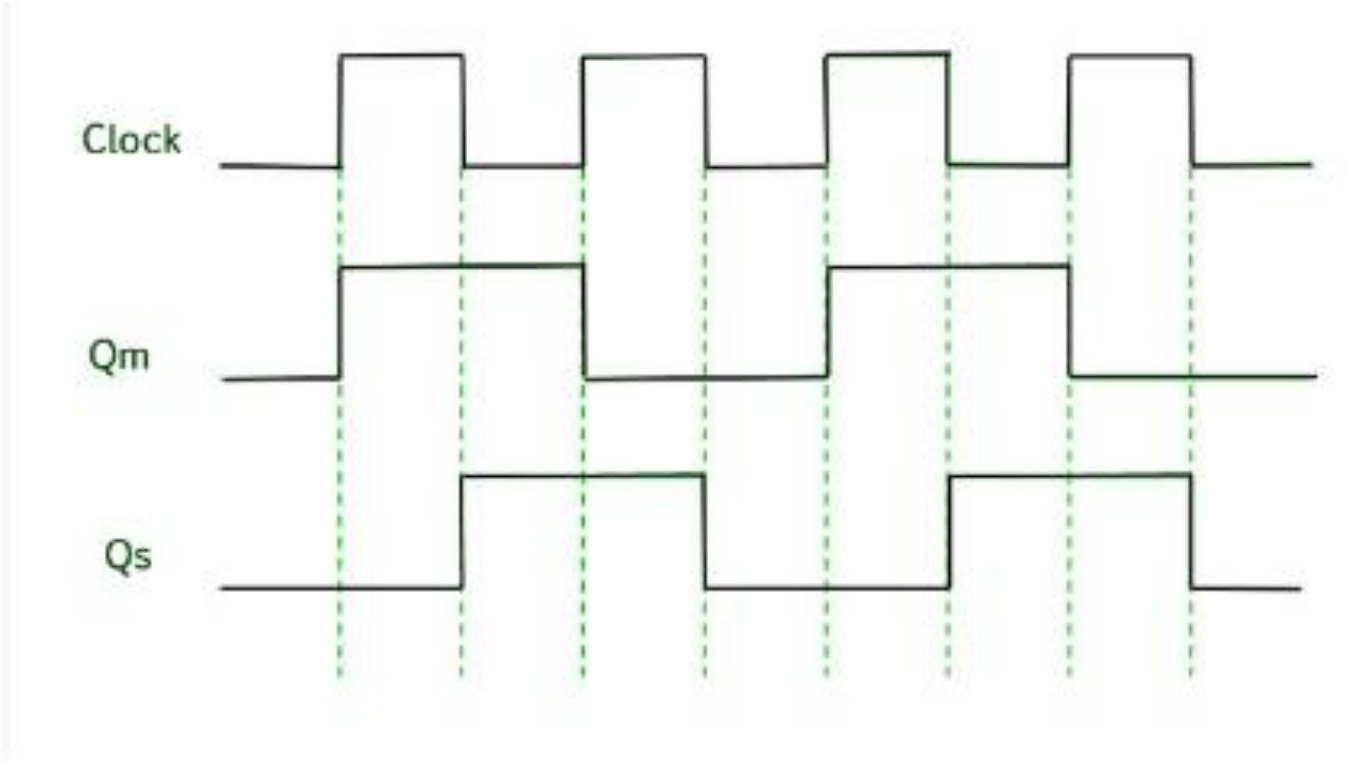
QUICK QUIZ (POLL)

Master-Slave configuration is designed by using?

a) SR Latch
b) JK flip flop
c) Multiplexer
d) Adder



Master Slave JK Flip Flop



QUICK QUIZ (POLL)

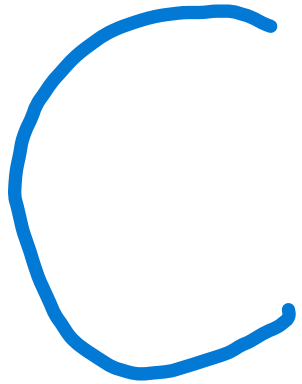
Master slave flip flop is also referred to as?

a) Level triggered flip flop

b) Pulse triggered flip flop

c) Edge triggered flip flop

d) Edge-Level triggered flip flop



DIGITAL ELECTRONICS: ECE 213

Topic: Sequential Circuits, Latches and Flip flops

UNIT IV: Introduction to Sequential Circuits

Lecture No.: 30

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Excitation Table

Suppose we want to know the sequence of the input combination which results in a definite output state.

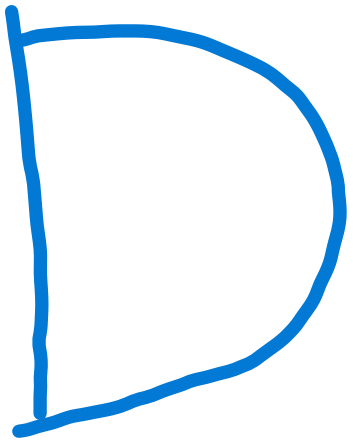
The information pertaining to this can be obtained by back-tracing (in terms of columns) the information presented by the characteristic table of the flip-flop.

QUICK QUIZ (POLL)

For the given outputs, the corresponding input states are calculated.

This statement is true for:

a) Truth table
b) Characteristic table
c) State table
d) Excitation table



Excitation Table: SR Flip Flop

Characteristic Table:

CLK	S	R	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	×	Q_n	$\overline{Q_n}$
1	0	0	0	**0**	**1**
1	0	0	1	**1**	**0**
1	0	1	0	**0**	**1**
1	0	1	1	**0**	**1**
1	1	0	0	**1**	**0**
1	1	0	1	**1**	**0**
1	1	1	0	**Indeterminate**	
1	1	1	1	**Indeterminate**	

Excitation Table:

Q_n	Q_{n+1}	S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

QUICK QUIZ (POLL)

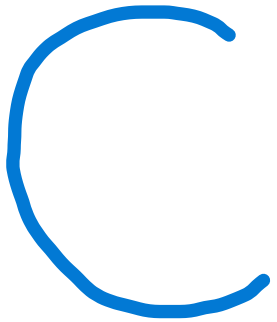
If Qn and Qn+1 values of SR flip flop are 1 and 0, the S and R values would be:

a) 1 and X

b) X and 1

c) 0 and 1

d) 1 and 0



Excitation Table: JK Flip Flop

Characteristic Table:

CLK	J	K	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	×	Q_n	$\overline{Q_n}$
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	0	1

Excitation Table:

Q_n	Q_{n+1}	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

QUICK QUIZ (POLL)

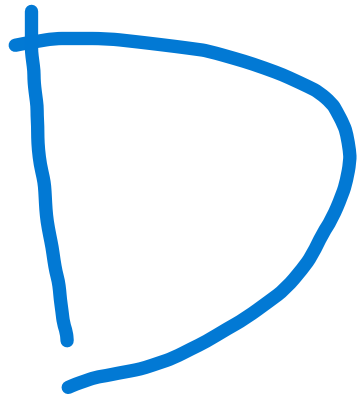
How many entries in the excitation table of JK flip flop consist of don’t cares:

a) 1

b) 2

c) 3

d) 4



Excitation Table: T Flip Flop

Characteristic Table:

CLK	T	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	Q_n	$\overline{Q_n}$
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

Excitation Table:

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Table: D Flip Flop

Characteristic Table:

CLK	D	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	Q_n	$\overline{Q_n}$
1	0	0	0	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0

Excitation Table:

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

QUICK QUIZ (POLL)

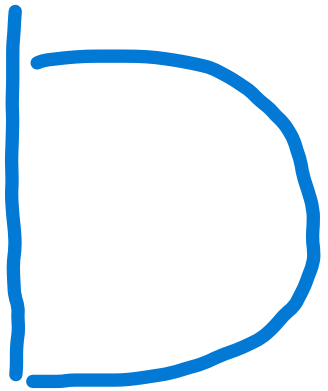
Which of the following flip flops gives maximum don’t cares in the excitation table?

a) SR flip flop

b) D flip flop

c) T flip flop

d) JK flip flop



Conversion of Flip flops

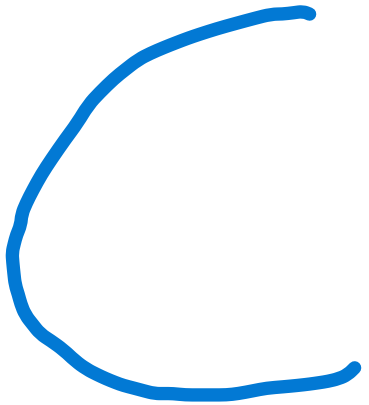
Steps to be followed:

1. Identify available and required flip flop.
2. Make characteristic table for required flip flop.
3. Make excitation table for available flip flop.
4. Write Boolean expression for available flip flop.
5. Design the circuit.

GATE Problem

An SR latch is a

a. Combinational circuit
b. Synchronous sequential circuit
c. One bit memory element
d. One clock delay element

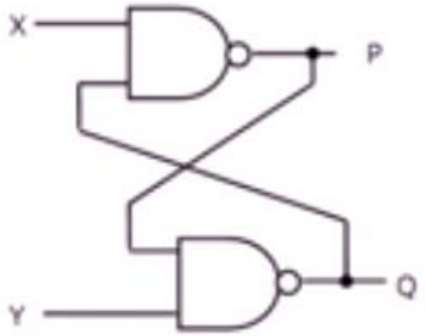


GATE Problem

The following binary values were applied to the X and Y inputs of the NAND latch shown in the figure in the sequence indicated below:

$X = 0, Y = 1;\quad X = 0, Y = 0;\quad X = 1, Y = 1.$

The corresponding stable P, Q outputs will be:



(A) P = 1, Q = 0; P = 1, Q = 0; P = 1, Q = 0 or P = 0, Q = 1

(B) P = 1, Q = 0; P = 0, Q = 1; or P = 0, Q = 1; P = 0, Q = 1

(C) P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 0 or P = 0, Q = 1

(D) P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 1