

(1)

Analog - Digital Interface Circuits - Abridged.

$$g_m = \sqrt{2} M_n C_{ox} \frac{W}{L} I_o$$

$$g_m = M_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})$$

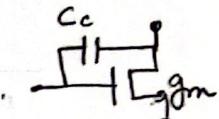
$$g_m = \frac{2 I_o}{V_{GS} - V_{th}}$$

$$Y_o = \frac{1}{\lambda I_o}$$

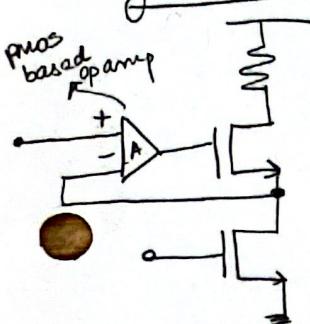
$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\varphi_F + V_{SB}}}$$

Overall gain = $-g_m Y_{out}$ low freq $\times \frac{(1 - s/\omega_z)}{(1 - s/\omega_{p1})(1 - s/\omega_{p2})}$

$$\omega_{p1} = \frac{1}{C_{node} \times R_{node}}$$

$$\omega_z = \frac{g_m}{C_c}$$


Gain boosting.

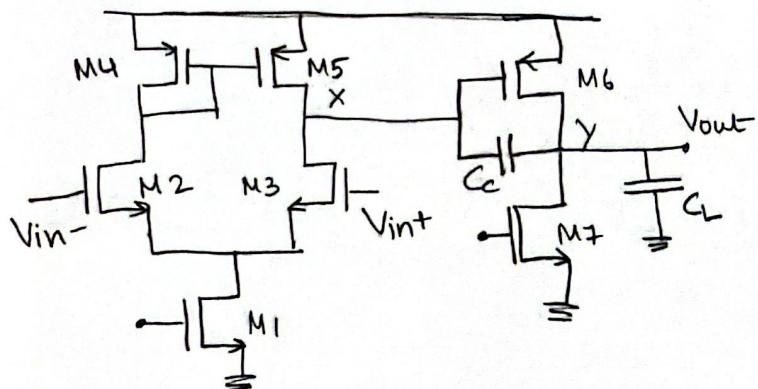


$$Y_{out} = (g_m Y_{o2}) Y_{o1} \times A.$$

$$\text{Cascode } Y_{out} = Y_{o1} + Y_{o2} + g_{m2} Y_{o1} Y_{o2}$$

$$\text{Diff amp gain } \left. \begin{array}{l} \\ \end{array} \right\} \text{ with PMOS load} \quad A_v = -g_{mN} (Y_{oN} \parallel Y_{op})$$

Opamps



$$\omega_{px} \approx - \frac{1}{(Y_{o5} \parallel Y_{o3})(g_{m6}(Y_{o6} \parallel Y_{o7})(C_L + C_{px}))} \quad \text{Miller comp.}$$

$$\omega_{py} \approx \frac{-g_{m6}}{C_L + C_{py}} \quad \omega_u = A_o / \omega_{pil} \quad \omega_u = g_{m3}/C_c$$

$\omega_{px} \downarrow \& \omega_{py} \uparrow \Rightarrow$ pole splitting.

→ Add resistor or buffer with C_c to kill reverse path & remove the zero from C_c

LHP pole \Rightarrow 

LHP zero \Rightarrow 

RHP pole \Rightarrow 

RHP zero \Rightarrow 

→ Typically choose $\omega_{p2} = 3\omega_u$ for good phase margin.

$$\Rightarrow C_{px} = \frac{1}{3} C_L \rightarrow \text{choose.}$$

⇒ For $\omega_{p2} = 3\omega_u$ we need $\frac{g_{m6}}{g_{m3}} = 4 \frac{C_L}{C_C}$ → gives I_1, I_2 ratio after choosing C_C .

$$\Rightarrow \frac{g_{m6}}{g_{m3}} \approx 10 \Rightarrow \frac{I_2}{I_1} \approx 10.$$

$$\text{generally } C_C = \frac{1}{3} C_L$$

Design flow

Given $C_L = 1\text{pF}$, $G = 1000$, $\omega_u = 1\text{G}\frac{\text{rad}}{\text{sec}}$, $\text{PM} > 60^\circ$

→ Choose $C_C = \frac{1}{3} \text{pF}$

$$\rightarrow \omega_u = \frac{g_{m3}}{C_C} \Rightarrow g_{m3} = \frac{1}{3} \text{mS}$$

$$\rightarrow V^* = 200\text{mV} \Rightarrow I_1 = \frac{g_m V^*}{2} = \frac{1}{3} \text{mA} \times 10^{-3} = 30\mu\text{A}$$

$$\Rightarrow I_2 = 0.3\text{mA}$$

⇒ Set the $\frac{W}{L}$ to get I_1 & I_2

⇒ Set L to get $G = 1000$.

Single stage Operational Transconductance Amplifier.

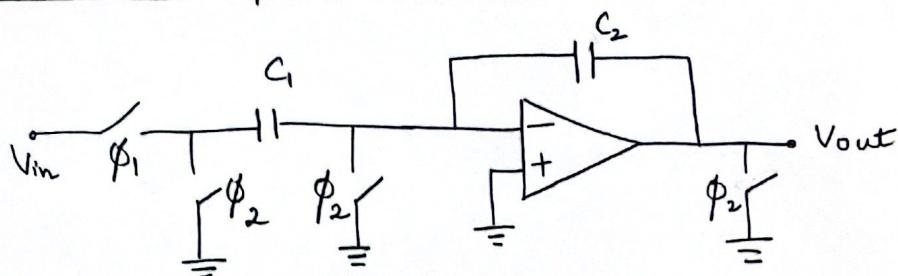
→ Low swing, complicated biasing, can't use unity gain feedback since CM of y_p & o_p are different

→ Single pole, High BW, very power efficient.

→ Could use CM feedback to fix o_p CM.

Switched Capacitor Circuits.

(3)

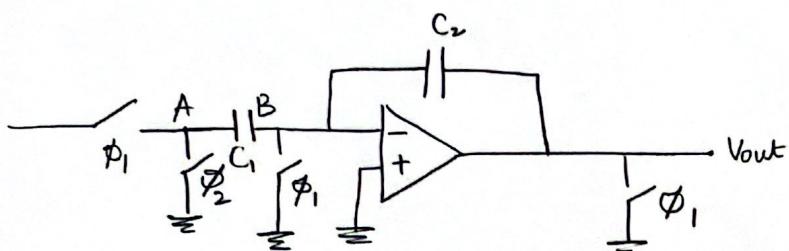


$$\text{Gain} = -\frac{C_1}{C_2}$$

$\phi_1 \xrightarrow{\text{ON}}$ gain phase.

$\phi_2 \xrightarrow{\text{ON}}$ reset phase.

Convert to sampling system.



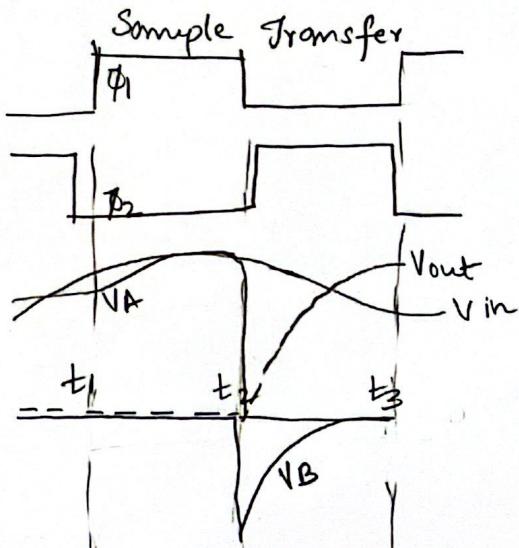
→ At the end of ϕ_1 ON, input charge $\propto c_1 = V_{in}(t_1) C_1$, $\propto c_2 = 0$.

$$\text{Total charge} = \propto c_1 + \propto c_2 = V_{in}(t_1) C_1$$

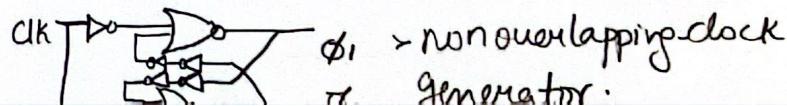
→ At ϕ_2 rising edge A is shorted \Rightarrow to maintain voltage drop across cap at $V_{in}(t_1)$, B falls to $-V_{in}(t_1)$. Op-amp takes time to respond.

⇒ -ve voltage on op amp -ve terminal \Rightarrow op-amp o/p is true, it pulls electrons out of C_2 & this pulls electrons from C_1 until C_1 is completely discharged & B is also at ground.

→ Total charge is on $C_2 \Rightarrow V_{out}(t_3) = \frac{V_{in}(t_1) C_1}{C_2}$ since B is ground.



- Sample & gain at the same time.
- Non inverting gain $= \frac{C_1}{C_2}$
- Samples i/p at t_1 .
- ϕ_1 & ϕ_2 must be non overlapping.
- parasitic caps at A & B do not affect it much.

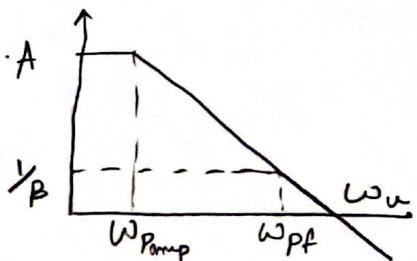


Feedback & RC circuits

$$V_{out} = V_s (1 - e^{-t/\tau}) \quad \text{in } t = 4.6\tau \text{ we settle to within } 1\%.$$

Where $\tau = \frac{1}{\omega_{pf}}$ → pole of feedback system A
in rad/sec.

$$\beta = \frac{C_2}{C_1} \text{ for switched cap.}$$



$$\omega_{pf} = \beta \omega_u.$$

$$\beta \leq 1$$

→ Slew rate of single stage diff pair

$$SR = \frac{I_B}{C_L} \rightarrow \text{branch current.}$$

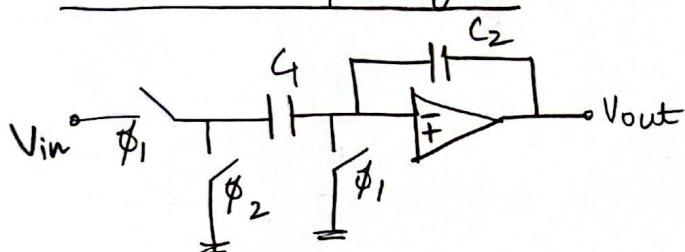
→ Slew rate of 2 stage opamp. (ignoring C_c)

while charging C_L $SR = \frac{I_{B2}}{C_L}$ since $I_{B2} > I_{B1}$

while discharging C_L $SR = \frac{I_{M6} - I_{B2}}{C_L}$

→ Without ignoring C_c :
$$SR = \frac{I_{B1}}{C_c}$$

Switched cap integrator



$$\frac{V_{out}}{V_{in}} = \frac{C_1}{C_2} \cdot \frac{z^{-1}}{1-z^{-1}}$$

ADC Basics & Characteristics.

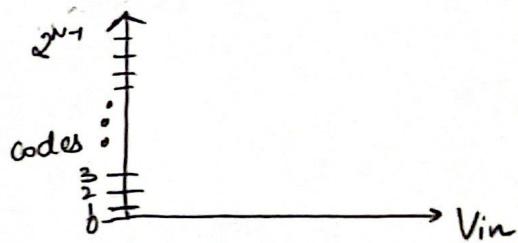
● $hSB = \frac{V_{Full\ scale.}}{2^N - 1} \rightarrow$ Voltage change associated with an LSB change in digital o/p.

DNL = Actual width(in LSB) - Ideal width (=1LSB)

- only defined at $2^N - 2$ codes since first & last codes don't have width
- ranges from -1 to ∞ . Often worst DNL is quoted.

$$\rightarrow INL(c) = \sum_{j=1}^c DNL(j)$$

→ Gain error & offset are other issues.



Quantization noise.

$$\overline{E_q^2} = \frac{LSB^2}{12} \rightarrow \text{noise power. It is evenly distributed from } -\frac{LSB}{2} \text{ to } \frac{LSB}{2}$$

$$V_{FS} = 2^N \text{ LSB}$$

$$\Rightarrow P_{signal} = \frac{(V_{FS}/2)^2}{2}$$

$$\Rightarrow \boxed{SNR = 6.02N + 1.76.}$$

$$SNR = 20 \log \left(\frac{V_{sig rms}}{2 V_{noise rms}} \right)$$

$$ENOB = \frac{SNR - 1.76}{6.02}$$

FFT

→ Coherent sampling \Rightarrow joining copies doesn't cause discontinuity.

→ For N sampled points we need

$$F_s = N F_{in}$$

must be 2^M for FFT

We could have $F_{in} = \frac{J}{N} F_s$

DFT review

$\tilde{x} = \tilde{x}[n+RN]$ is a periodic sequence with period N .

$$\tilde{x}[n] = \frac{1}{N} \sum_{k=0}^{N-1} \tilde{X}[k] e^{j \frac{2\pi}{N} kn}$$

Mag & Phase of these Fourier Coefficients give the spectrum.

→ Mag is symmetric around $\frac{N}{2}$ & phase is inverse symmetric around $\frac{N}{2}$.

→ $M_{N-k} = M_k$ & $\phi_{N-k} = -\phi_k$.

→ $N=0$ is DC \Rightarrow don't care. $N = \frac{N}{2}$ is $\frac{F_s}{2}$ \Rightarrow double counted.

→ Bin# = $k \Rightarrow$ Freq = $\frac{k F_s}{N}$

SNDR = $10 \log_{10} \frac{P_{fundamental}}{\sum \text{Power of all other bins except DC}}$. \rightarrow use only half of $\frac{N}{2}$ bin

THD = $10 \log_{10} \frac{P \text{ of harmonics (eg. 8 harmonics)}}{P \text{ of fundamental}}$

$$ENOB = \frac{SNDR - 1.76}{6.02}$$

SFDR = distance b/w fundamental & biggest harmonic.

$$SNDR = -10 \log \left\{ 10^{\frac{-SNR}{10}} + 10^{\frac{THD}{10}} \right\}$$

DNL Measurements

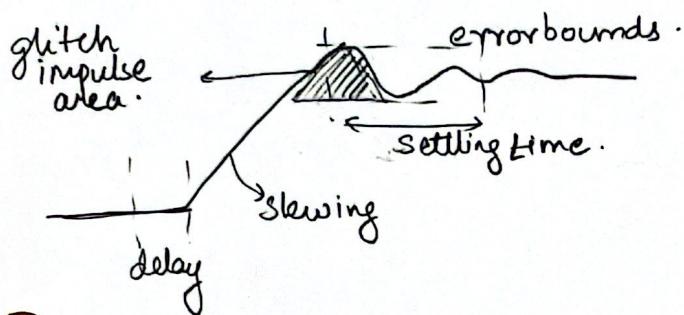
Code density test

$$DNL(i) = \frac{H(i)}{H(t)} - \frac{P(i)}{P(t)}$$

$H(i) \rightarrow$ no. of hits for code i
 $H(t) \rightarrow$ total hits for all codes.
 $P(i) \rightarrow$ nominal density $\Rightarrow \frac{1}{\text{no. of codes}}$

DAC specs

→ settling time, error bounds, slew rate, delay, GIA



ADC FOM

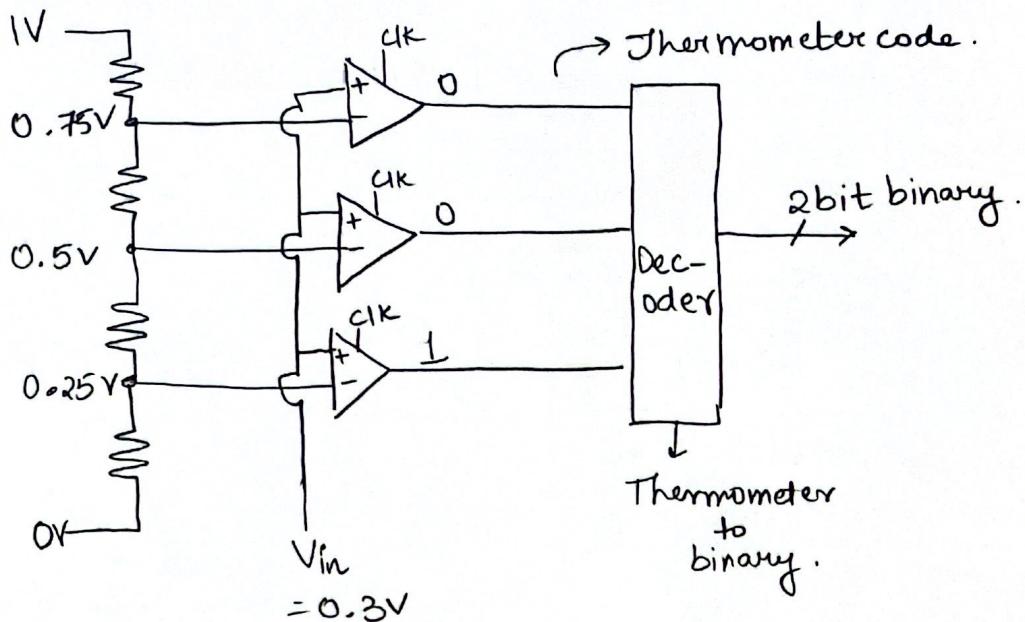
$$FOM = \frac{\text{Power}}{2 \times \text{Fin} \times 2^{\text{ENOB}}} \quad \text{measured at Fin.}$$

$$FOM_{Walden} = \frac{\text{Power}}{2 \times \text{Fin} \times 2^{2 \times \text{ENOB}}}$$

$$FOM_{Schreier} = 10 \log_{10} \frac{2^{2 \times \text{ENOB}} \times \text{BW}}{\text{Power}}$$

FLASH ADCs.

> N bits $\Rightarrow 2^N$ codes $\Rightarrow 2^N - 1$ comparators.



* Metastability.

$$P_{\text{error}} = \frac{2(2^N - 1) V_L}{V_R A_{\text{comp}}}.$$

$$A_{\text{comp}} = A_p A_L e^{t/t_r}$$

$$t_r = \frac{t_1 - t_2}{\ln 10}$$

$$t_r = C/g_m \text{ for crosscoupled CS comparator.}$$

→ Review strongARM latch from Razavi's paper.

$V_L \rightarrow$ min. diff. in voltages to detect logic

$V_R \rightarrow$ full scale analog input $= (2^N - 1)^{\text{LSB}}$

$A_{\text{comp}} \rightarrow$ Comparator gain.

$A_p \rightarrow$ Preamp gain.

$A_L \rightarrow$ Latch gain?

t_1, t_2 are times taken for two inputs V_1, V_2 to reach 100mV where $V_2 = 10V_1$.

(9)

Yield.

Yield due to nonmonotonicity.

$$P = P(V_{trip,j+1} - V_{trip,j} - 1 \text{ LSB} < -1 \text{ LSB}) \rightarrow \text{probability that a pair of comps. have nonmonotonicity.}$$

$\Rightarrow \text{Yield} = (1 - P)^{2^{N-2}}$

$$\sigma = \sqrt{2} \sigma_{\text{comp.}}$$

↳ comparator offset std. dev.

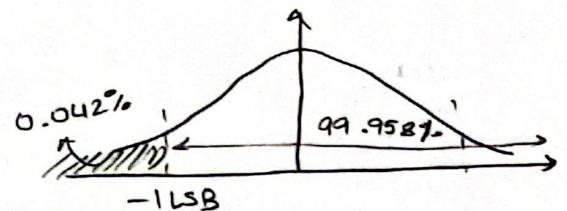
Eg: 8 bit ADC we need yield 90%.

Sol: $0.9 = (1 - P)^{254} \Rightarrow P = 0.00042 \Rightarrow 0.042\%$.

→ Use tables of MATLAB norminv fn. to set the cumulative distribution on the left of -1 LSB for $V_{trip,j+1} - V_{trip,j} - 1 \text{ LSB}$ to 0.042%

→ This gives -1 LSB is at -3.34σ

$$\Rightarrow \sigma = \frac{1 \text{ LSB}}{3.34} = 0.299 \text{ LSB.}$$



$$\Rightarrow \sigma_{\text{comp. required}} = \frac{0.299}{\sqrt{2}} \text{ LSB}$$

$$= 0.212 \text{ LSB.}$$

if $1 \text{ LSB} = 4 \text{ mV} \Rightarrow \boxed{\sigma_{\text{comp. required}} < 1 \text{ mV}} \rightarrow \text{very hard spec.}$

Yield due to DNL.

$$P = P(|V_{trip,j+1} - V_{trip,j} - 1 \text{ LSB}| > \text{DNL}_{\text{max}}).$$

$$\text{Yield} = (1 - P)^{2^{N-2}}$$

Offset & Mismatch.

$$\sigma^2(V_{TO}) = \frac{A_{VT}^2}{WL} + S_{V_{TO}}^2 D^2 \rightarrow \text{dominant}$$

\sim
dominant

$$\sigma^2(K) = \frac{A_K^2}{WL} + S_K^2 D^2$$

$$V_T = V_{TO} + K \underbrace{(\sqrt{|V_{BS}| + 2\varphi_F} - \sqrt{2\varphi_F})}_{\text{Body effect}}$$

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_B^2}{WL} + S_\beta^2 D^2 \quad A_{VT} \approx (4-8) \text{ mV}/\mu\text{m}$$

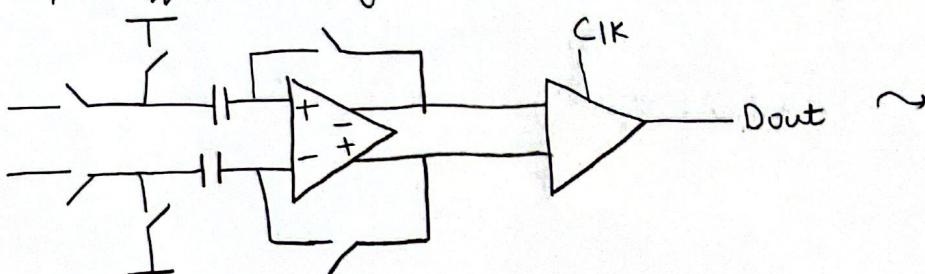
$$\frac{\sigma^2(I_D)}{I_D^2} = \frac{4\sigma^2(V_{TO})}{(V_{GS} - V_{TO})^2} + \frac{\sigma^2(\beta)}{\beta^2}$$

Preamplifier for offset cancellation.

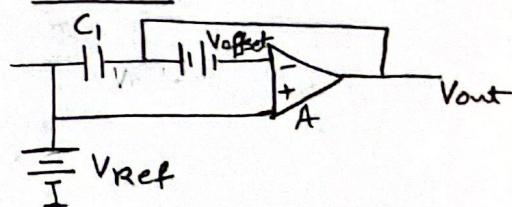
$$T_{\text{overall}} = \frac{T_{\text{comp}}}{A_{\text{preamp}}} \quad \text{mean } M_{\text{overall}} = \frac{M_{\text{comp}}}{A_{\text{preamp}}}.$$

Switched capacitor offset storage.

Input offset storage is better, since output offset storage limits the gain.



Single ended analysis when Φ_1 is closed.



$$(V_{\text{Ref}} - (V_{\text{out}} - V_{\text{offset}}))A = V_{\text{out}} \Rightarrow V_{\text{out}} = \frac{A}{A+1} (V_{\text{Ref}} + V_{\text{offset}}) \approx V_{\text{Ref}} + V_{\text{offset}}$$

$\Rightarrow V_{\text{offset}}$ is stored on the cap & cancels the "battery" offset during Φ_2 .

Sample and hold circuits.

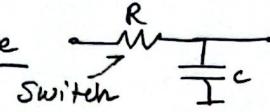
Jitter due to sampling clk.

$$V_j[n] = 2\pi f_0 A_0 t_j \cos(2\pi f_0 nT) \sim t_j \frac{dV(t)}{dt} \text{ at } t=nT$$

$$V_{j\text{rms}} = 2A_0\pi f \frac{t_{j\text{rms}}}{\sqrt{2}}$$

→ higher during crossovers in input $V(t)$.

$$\boxed{\text{SNR} = -20 \log_{10}(2\pi f_0 t_{j\text{rms}})} \quad f_0 \uparrow \Rightarrow \text{SNR} \downarrow.$$

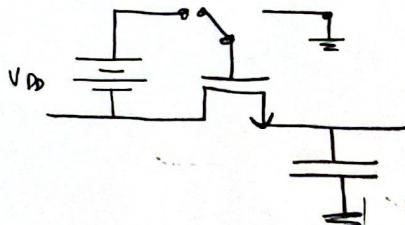
Capacitor noise  ⇒ mean sq. noise power = $\frac{K T}{C}$

$$R = \frac{1}{MnCoxWL(V_{gs} - V_t)}$$

here both V_{gs} & V_t depend on input & induce harmonic distortion.

→ Transmission gate could be used to make R more constant but synchronization is a huge problem.

→ Use Bootstrapped Sampling instead.



→ V_{gs} is now constant.

→ Circuit implementation is fairly complex.

→ Clock feedthrough is another issue but not as painful as charge injection.

Charge injection

When switch is turned off, channel charges flow into source & drain causing a transient spike in voltage.

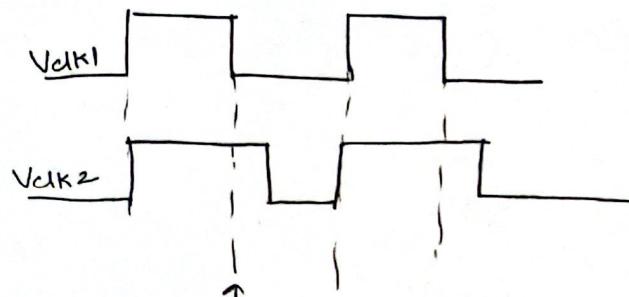
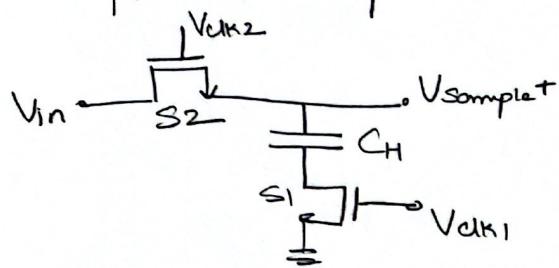
$$\text{Error voltage} = \frac{1}{2} \left(\frac{-Q}{C} \right) = -\frac{C_{ox}WL(V_{akhi} - V_{in} - V_{th})}{2C_H}$$

half of charge goes to D & $\frac{1}{2}$ to SINK.

- Solutions:
- ① Add dummy switch with opposite clocking to absorb these charges. Not great.
 - ② Differential SHA \Rightarrow charge injection has a CM component that is removed. Not great
 - ③ Bottom plate sampling \rightarrow Great!

Bottom plate sampling.

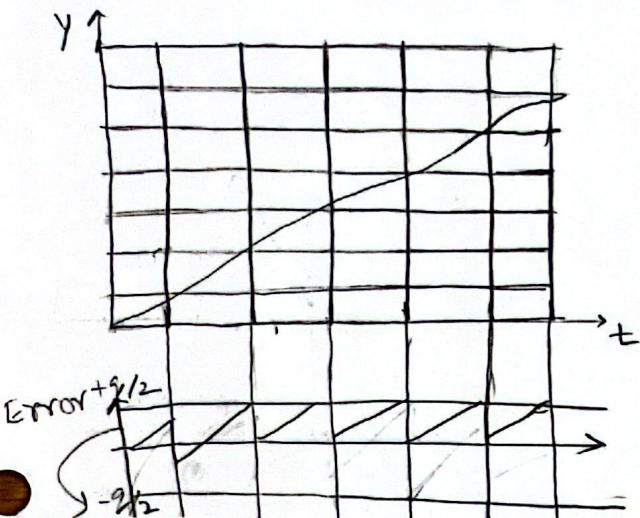
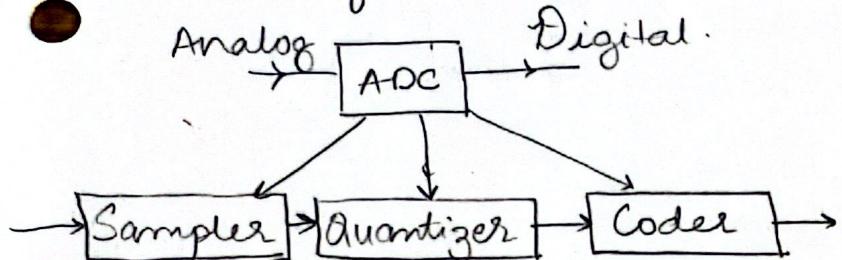
\rightarrow Fix the charge on the bottom plate of C_H so that charges cannot flow into cap.



> Once V_{clk1} opens, the charges on C_H cannot change $\Rightarrow V_{samplet}$ cannot change. The injection from S_1 is not a variable since source is at ground \Rightarrow constant injection (not an issue).

Sigma Delta Modulators

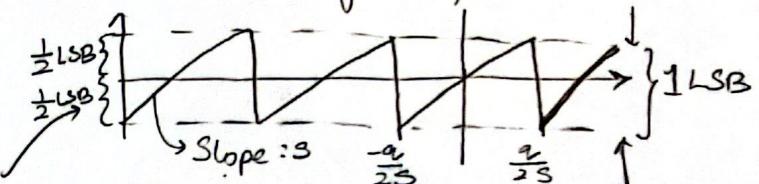
Basics of ADCs



Because Signal is using most of error is in 0 to $\pm \frac{q}{2}$. For a regular signal we can assume it is equally spread b/w $-\frac{q}{2}$ & $+\frac{q}{2}$ \Rightarrow sawtooth approximation.

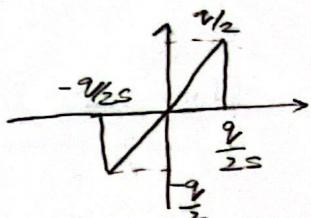
Let 1 LSB = q ; Slope = s ; \Rightarrow error signal is

$$e(t) = st, \quad -\frac{q}{2s} < t < \frac{q}{2s} \Rightarrow T = \frac{q}{s}$$



\Rightarrow The quantization error is equally probable within the range of $\pm \frac{1}{2}$ LSB

\rightarrow W.R. Bennett proved this more rigorously in 1948 and showed this assumption is

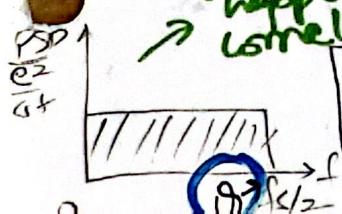


mean square value : $\overline{e^2(t)} = \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} e^2(t) dt$

$$= \frac{s}{q} \int_{-\frac{q}{2s}}^{\frac{q}{2s}} (st)^2 dt$$

More rigorous derivation is on pg. 14

What happens if correlated?



$$\overline{e^2(t)} = \frac{q^2}{12}$$

\Rightarrow rms quantization noise = $\frac{q}{\sqrt{12}}$
 \Rightarrow Total noise power is constant unlike 1 noise ... \Rightarrow constant

- Rigorous assumptions of $e(n)$
- (1) $e(n)$ is a sample sequence of a stationary RP
 - (2) $e[n]$ & $x[n]$ are uncorrelated
 - (3) probability density function $f_e(n)$ is uniform over $\pm \frac{q}{2}$
 - (4) $e(n)$ is a white noise process \Rightarrow its $\{e[n]\}$ are uncorrelated.

Assumption②

- > If noise is uncorrelated with input signal \Rightarrow input and sampling clock are not harmonically related. Then the error signal is spread evenly across all frequencies 0 to $f_s/2$.
- > If they are correlated total power is still $\frac{q^2}{12}$ but concentrated around harmonics.
- > Noise at frequencies above 0 to $f_s/2$ is folded back into 0 to $f_s/2$.

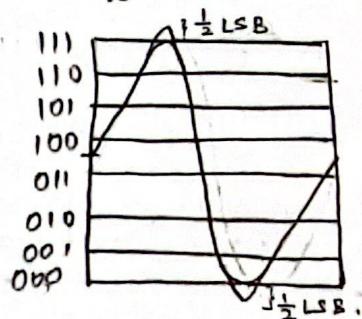
SNR calculation

Let input be a full scale sinusoid: $v(t) = q \frac{-2^N}{2} \sin(2\pi f t)$

$$\therefore \text{rms value} = \frac{q \cdot 2^N}{2\sqrt{2}}$$

$$\text{SNR} = 20 \log \frac{\text{rms of } v_p}{\text{rms of } q_{\text{noise}}}$$

$$= 20 \log \frac{q \cdot 2^N / 2\sqrt{2}}{q / \sqrt{12}} = 20 \log 2^N + 20 \log \sqrt{\frac{3}{2}}$$



$$\boxed{\text{SNR} = 6.02N + 1.76 \text{dB}}$$

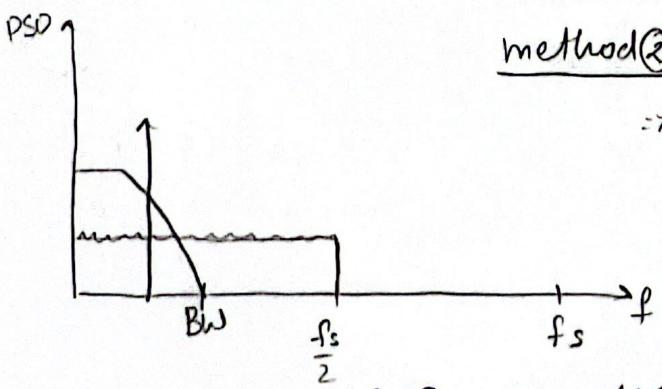
over dc to $f_s/2$.

→ SNR is only a function of N! How can we get more SNR?

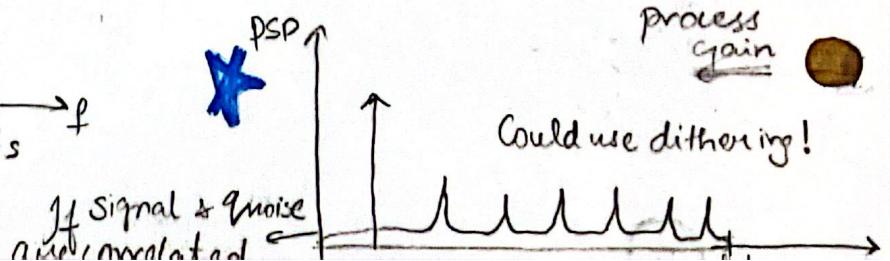
method ①: Increase N! Inherently limit each bit gives 6dB↑ in SNR.

method ②: We can use a filter ($BW < f_s/2$)

$$\therefore \text{SNR} = 6.02N + 1.76 + 10 \log \left(\frac{f_s}{2 \cdot BW} \right)$$



Q: Why noise is only upto $f_s/2$?

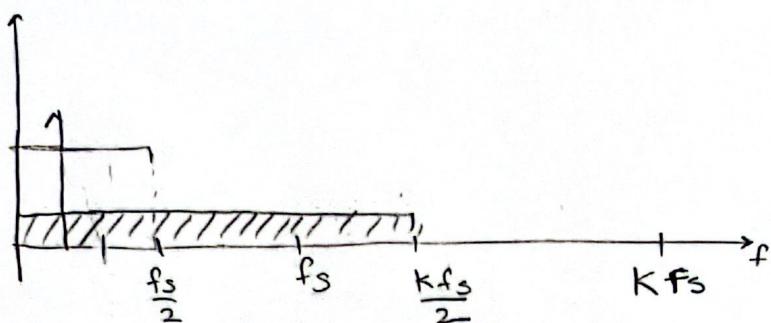


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"Increase SNR further?"

^{→ same as method ②}
Method ③ :- Recall that total noise power is fixed = $\frac{N^2}{12}$ and spread evenly from 0 to $\frac{f_s}{2}$. Increase f_s !

Oversampling

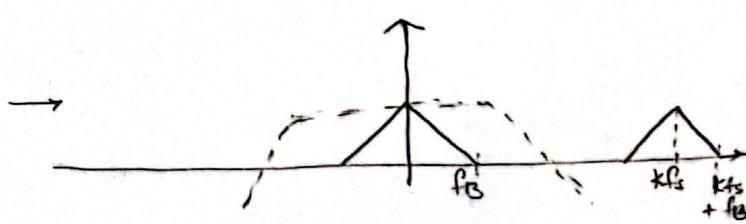
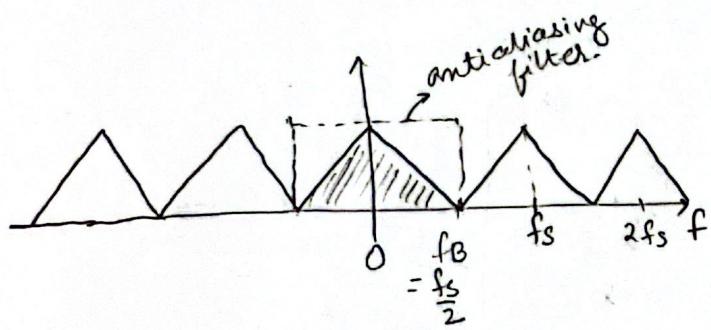
↳ Basically we are doing the exact same trick of method 2 where $BW = \frac{f_s}{2}$.



→ Oversampling by a factor of 2 \Rightarrow noise power \downarrow by half
 \Rightarrow 3dB improvement in ENOB.

→ For 1 bit \uparrow in ENOB $\Rightarrow 4 \times f_s$.

→ Also notice oversampling relaxes the requirements on the anti aliasing filter.



→ Drawbacks: 1 Gs/s 4bit ADC $\xrightarrow{\text{to}}$ 12bit ADC with oversampling

$\Rightarrow 4^8$ times $f_s = 65,536$ Gs/s!! Unrealistic!

Q: What is made off?: Speed for resolution!

lets go back to the ADC (Quantiser)

→ Any quantiser
ADC is nonlinear.
We can model it as a linear
System with a noise source
 $e[n]$

$$\rightarrow y[n] = x[n] + e[n]$$

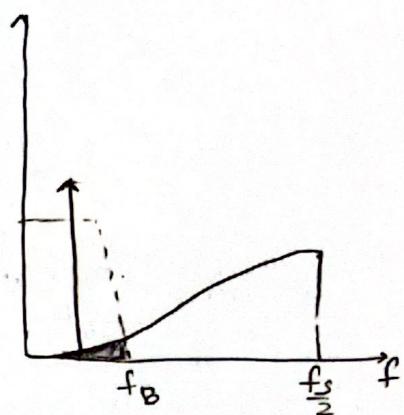
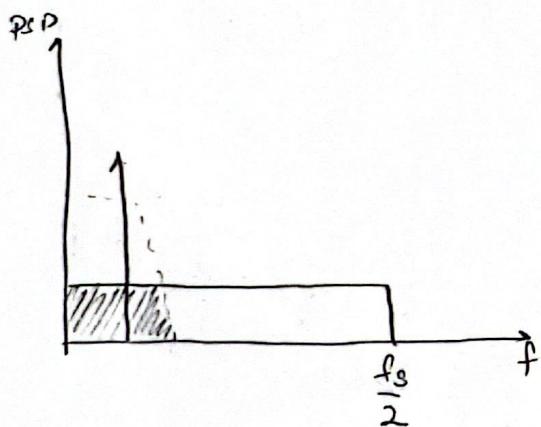
Z transform

$$Y(z) = X(z) + E(z)$$

In general

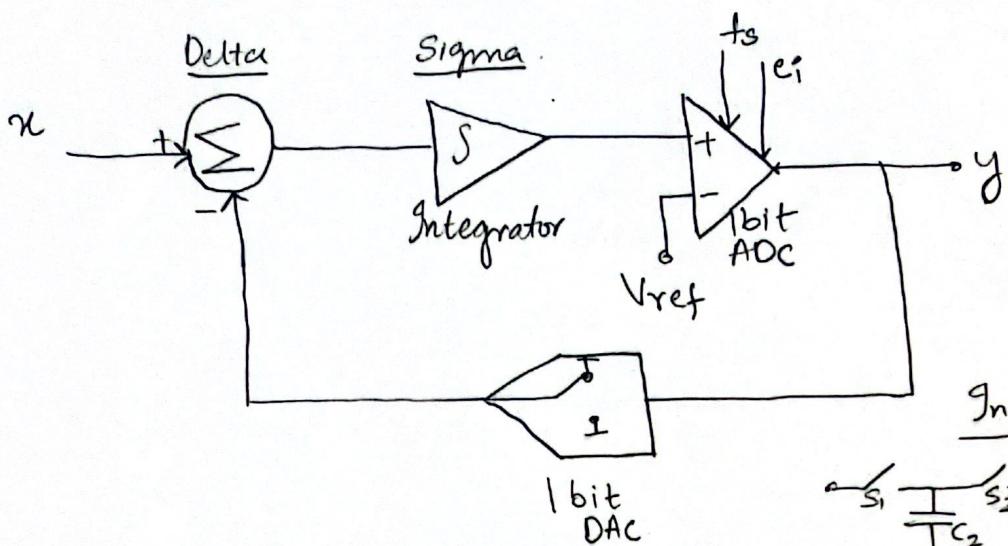
$$Y(z) = H_x(z) \cdot X(z) + H_e(z) + E(z)$$

→ The reason we can do this is that the signal and noise come from different sources. So we can design a different transfer function for the signal and noise to treat them differently. This is the key idea behind any noise reduction system (chopping, differentialamp) and that is what a sigma delta modulator is. It designs $H_e(z)$ to do noise shaping!

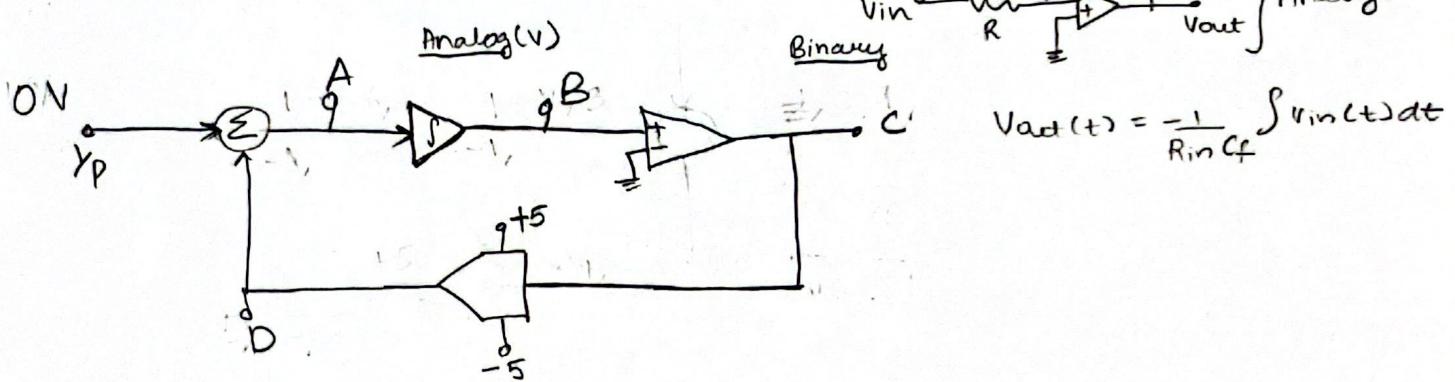


$\Sigma \Delta$ Modulators (ADCs)

15



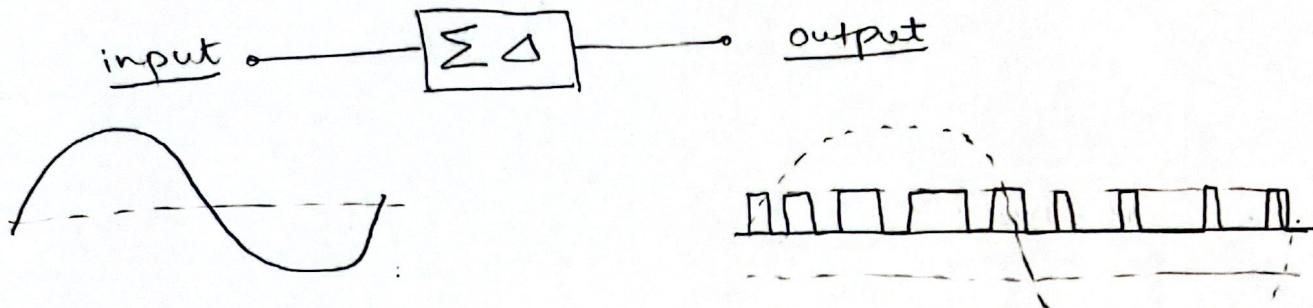
Time domain analysis (linear model)



v_p	A (v)	B (v)	C (1,0)	D (v)
0V	0, -5, 5, -5	0, -5, 0, -5	1, 0, 1, 0, 1, 0	5, -5, 5, -5,
2.5V	2.5, -2.5, -2.5, 2.5, 0, -2.5, 5, 7.5, -2.5, -2.5, 2.5, 0, -2.5, 5, 2.5, 0, -2.5	2.5, 0, -2.5, 5, 7.5, -2.5, 2.5, 0, -2.5, 1, 0, 1, 1, 1, 0, 1, 1, 1, 0, 1, 1	1, 1, 0, 1, 1, 1, 0, 1, 1, 1, 0, 1, 1, 1, 0, 1, 1, 1, 0, 1, 1	5, 5, -5, 5, 5, 5, 5, -5, 5, 5, 5, -5, 5, 5, -5, 5, 5, -5, 5, -5
-2.5V	-2.5, 2.5, -2.5, -2.5, -2.5, 2.5, 0, -2.5, 5, 2.5, 0, -2.5	2.5, 0, -2.5, 5, 7.5, -2.5, 2.5, 0, -2.5, 1, 0, 1, 1, 1, 0, 1, 1, 1, 0, 1, 1	1, 1, 0, 1, 1, 1, 0, 1, 1, 1, 0, 1, 1, 1, 0, 1, 1, 1, 0, 1, 1	5, 5, -5, 5, 5, 5, 5, -5, 5, 5, 5, -5, 5, 5, -5, 5, 5, -5, 5, -5

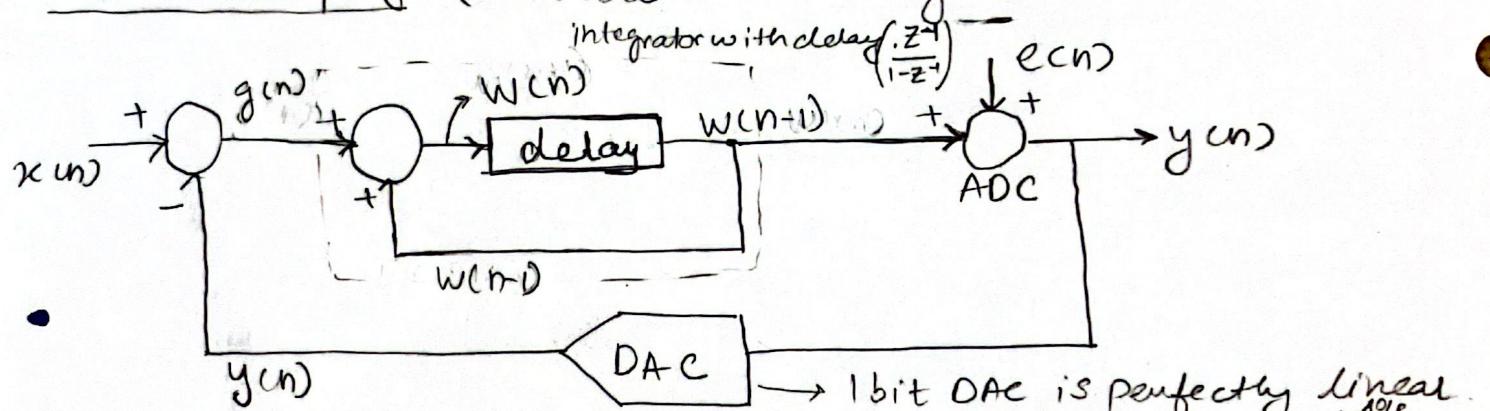
- Input is 0V \Rightarrow square wave output! } Density of 1's and 0's
 → Input is 2.5V \Rightarrow 75% duty cycle. } Represents input analog value!
 → Input is -2.5V \Rightarrow 25% duty cycle

Another way to think about it :- Average value at node D should be equal to input analog value, and this average value is a reflection of density of 1s and 0s.



→ Because of oversampling, the one bit ADC is able to capture the input signal.

Noise shaping (Discrete time analysis)



$$y(n) = w(n-1) + e(n)$$

$$\therefore w(n) = g(n) + w(n-1)$$

$$g(n) = x(n) - y(n)$$

$$g(n) = x(n) - w(n-1) - e(n)$$

$$\Rightarrow w(n) = x(n) - \cancel{w(n-1)} - e(n) + \cancel{w(n-1)}$$

$$\Rightarrow w(n) = x(n) - e(n)$$

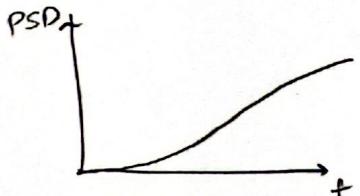
$$\Rightarrow y(n) = x(n-1) - e(n-1) + e(n)$$

$$\Rightarrow y(n) = x(n-1) + \underbrace{e(n) - e(n-1)}$$

Discrete time difference operation gives noise Shaping! Why?

$$y(n) = x(n-1) + \underbrace{e(n) - e(n-1)}$$

- If $e(n)$ is a low frequency signal $e(n) \approx e(n-1)$
⇒ Cancelled!
- If $e(n)$ is a high frequency signal $e(n) \stackrel{\text{maybe}}{\approx} -e(n-1)$
⇒ Add up!
- ⇒ Low frequency q. error is suppressed!
- Input is just delayed!



Taking Z transform

$$Y(z) = z^{-1} \cdot X(z) + (1-z^{-1}) E(z) \rightarrow \text{Bilinear to get C.T.}$$

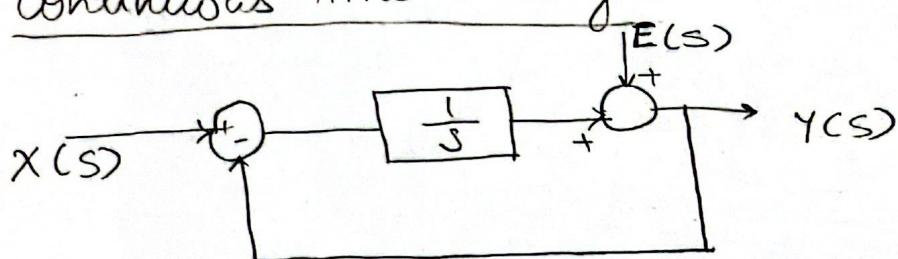
$$z = \frac{1 + \frac{T}{2}s}{1 - \frac{T}{2}s}$$

$$H_x(z) = z^{-1}$$

$$H_e(z) = 1 - z^{-1}$$

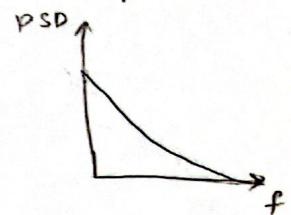
$T \rightarrow \text{sample time.}$

Continuous time analysis

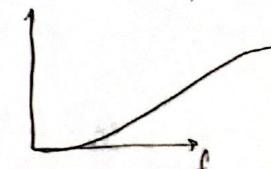


→ Notice here DAC nonlinear does not get shaped like the ADC. 1bit DAC is linear so no problem!

$$\frac{Y(s)}{X(s)} = \frac{\frac{1}{s}}{1 + \frac{1}{s}} = \frac{1}{s+1} \rightarrow \text{low pass}$$



$$\frac{Y(s)}{E(s)} = \frac{1}{1 + \frac{1}{s}} = \frac{s}{s+1} \rightarrow \text{high pass}$$



$$\Rightarrow Y(s) = \frac{1}{s+1} \cdot X(s) + \frac{s}{s+1} \cdot E(s) \rightarrow \text{Bilinear transform to get OT!}$$

$$s = \frac{2}{T} \left(\frac{z-1}{z+1} \right)$$

$$\underline{SNR} \quad H_e(z) \xrightarrow{z=e^{j2\pi f t}} H_e(s) \rightarrow P_{e,f} = P_E \cdot |H(s)|^2 \rightarrow \text{From } P_{e,f} \text{ we get SNR!} \rightarrow \text{Derivation in appendix}$$

from T.F calculate PSD & total power.

$$SNR = 6.02N + 1.76 - 10\log\left(\frac{\pi^2}{3}\right) + 30\log\frac{f_s}{2f_B}$$

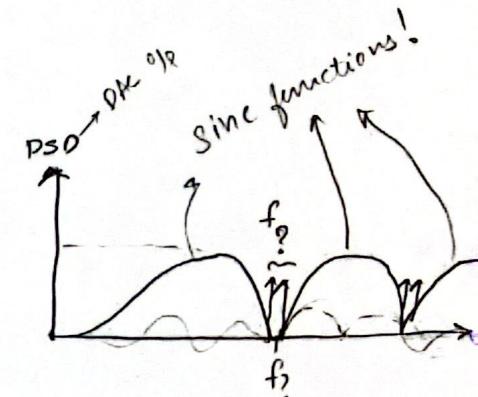
SNR could be worse if not oversampled

$$\text{If } \frac{f_s}{2f_B} = 2^x \Rightarrow 9.03x$$

\Rightarrow doubling sampling rate = 9dB improvement
= 1.5 bits!

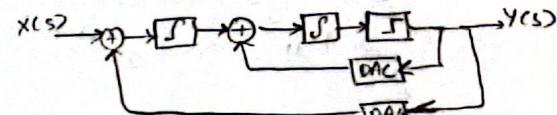
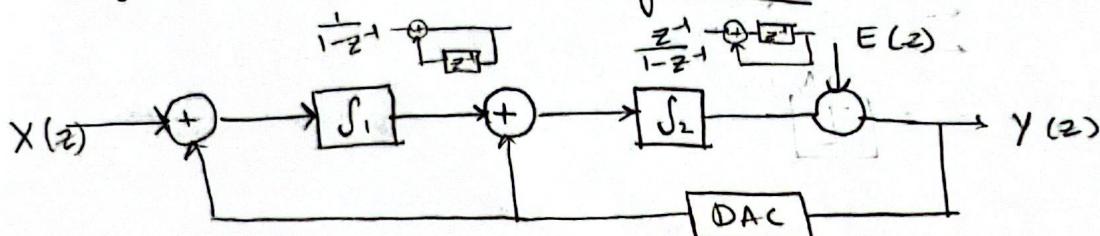
Limitations?

- > Speed (due to oversampling)
- > DAC nonlinearity?, integrator gain?
- > tones! $V_{in} = 0.001 \Rightarrow D/A has one 1 \times 999 \text{ os. in a period}$
 $\text{if } 1000T_s \Rightarrow \text{harmonics at } m \cdot \frac{f_s}{1000} \text{ within the signal B.W}$



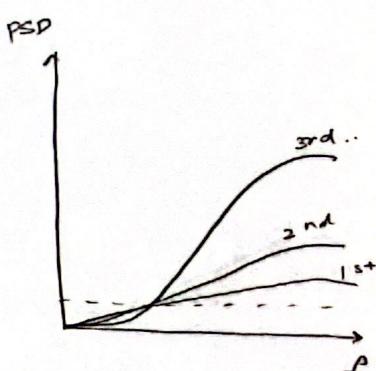
Improving the SNR? \rightarrow Many ways { Tradeoffs: Resolution, Bandwidth, circuit complexity, stability }

① Higher order :- 2 integrators



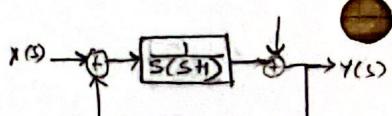
$$H_x(z) = z^{-1} ; \quad H_e(z) = (1-z^{-1})^2$$

$$SNR = 6.02N + 1.76 - 10\log\left(\frac{\pi^4}{5}\right) + 15.05x$$



\Rightarrow doubling sampling rate \rightarrow 15dB \rightarrow 2.5 bits!

L^{th} order $\Rightarrow (L+0.5)$ bits improvement!

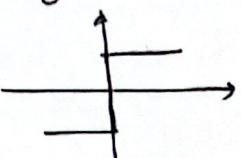


\Rightarrow But what are we ignoring here? Stability!

→ 2nd order $\Sigma\Delta$ has two poles \Rightarrow Need to consider Ph-Margin. 19

In reality this is where the model fails. The 1 bit ADC is Nonlinear. Therefore doing a stability analysis becomes difficult.

→ Why Nonlinear?

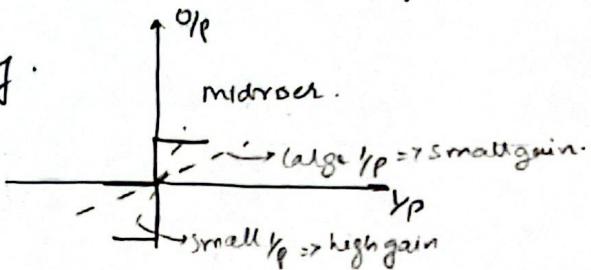


If ADC Y_p is 0 output is 1 \Rightarrow gain is ∞

If ADC Y_p is ∞ output is 1 \Rightarrow gain is 0

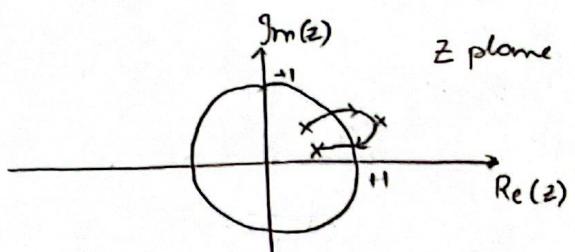
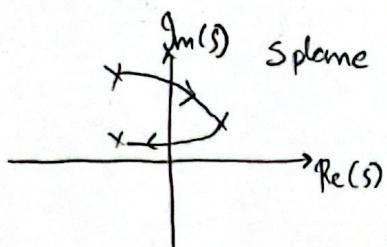
\Rightarrow ADC gain is a function of input.

→ It is like trying to fit a curve to a 1 bit quantiser.
The slope can be arbitrary.



→ Quantiser Y_p changes even if input is DC.

→ How Quantiser Y_p changes depends on input values. Therefore, pole locations depend on input.



→ System may temporarily become unstable but return to stable operation before the quantiser gets saturated.

→ If poles move outside unit circle when ADC input is small
 \Rightarrow high gain \Rightarrow signal levels rise \Rightarrow gain may fall \Rightarrow causes poles to move inside the unit circle.

② Higher bit ADC / DAC

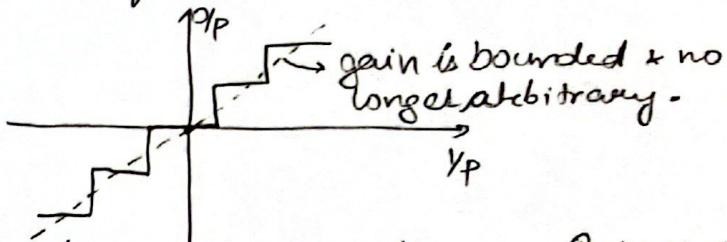
$$SNR = 6.02N + 1.76 - 10 \log\left(\frac{\pi^2}{3}\right) + 30 \log \frac{f_s}{2f_B}$$

↑
each bit \uparrow SNR by 6dB!

\Rightarrow 5 bit ADC & DAC can give 30dB \uparrow in SNR.

- Advantage : ① More closely follow the linearized model due to ADC becoming "more linear". 00 bit ADC is linear.
 ② Stability is better predicted for higher order.

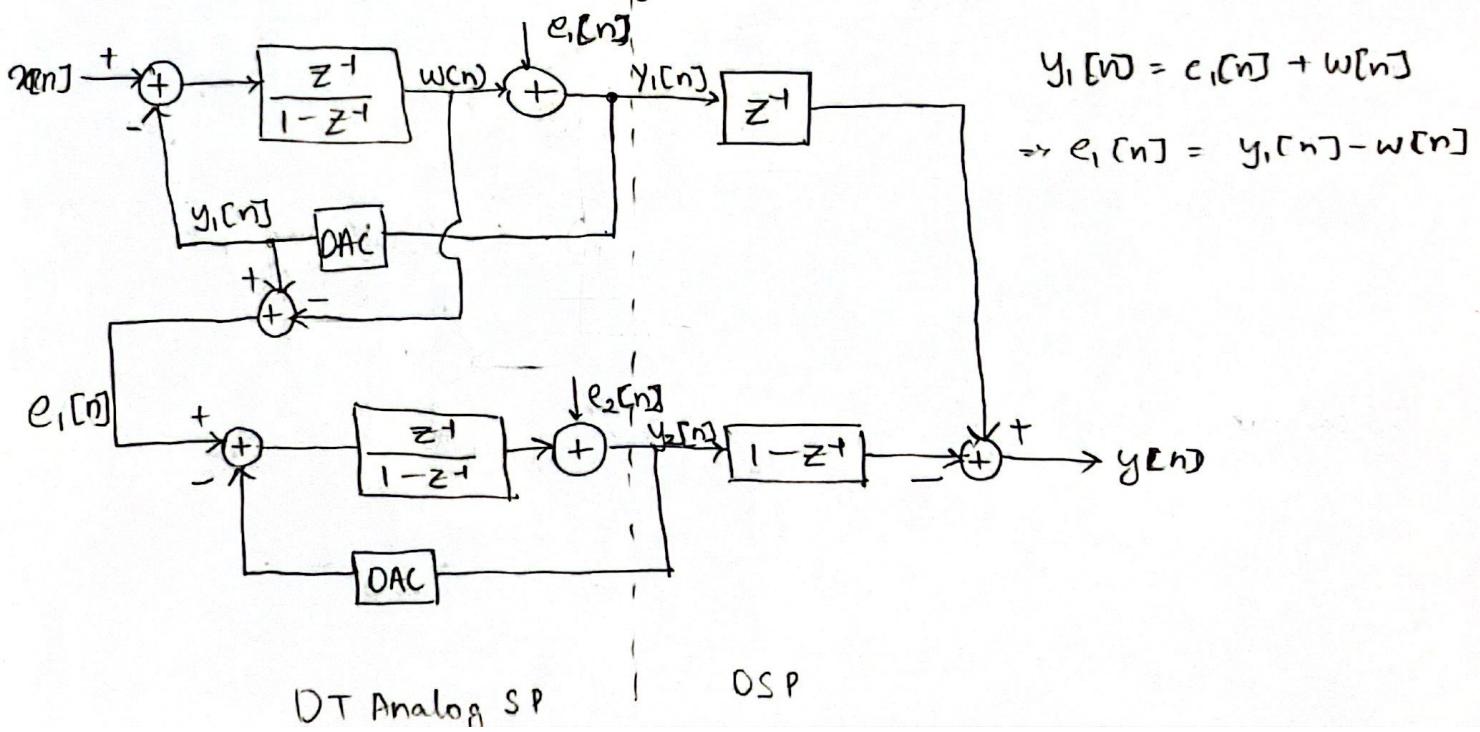
③ lower tones!?



- Disadvantage : ① DAC is higher bits & no longer perfectly linear. Quantization noise from DAC does not get noise shaped. \rightarrow Due to INL, DNL
 ② Implementing ^{high order} DAC is harder in VLSI/CMOS.

③ Multi-stage Sigma Delta Modulators (MASH)

- Constraints so far : ① Stability.
 ② Cannot go to higher order... } What can we do?



$$Y_1(z) = X(z)z^{-1} + E_1(z)(1-z^{-1})$$

$$Y_2(z) = E_1(z)z^{-1} + E_2(z)(1-z^{-1})$$

$$Y(z) = Y_1(z) \cdot z^{-1} - Y_2(z)(1-z^{-1})$$

$$= X(z) \cdot z^{-2} + E_1(z)(z^{-1}(1-z^{-1}))$$

$$-E_1(z)(z^{-1}(1-z^{-1})) - E_2(z)(1-z^{-1})^2$$

$$Y(z) = X(z) \cdot z^{-2} - E_2(z) \cdot (1-z^{-1})^2 \xrightarrow{\text{second order shaping!}} \text{Sign on noise is irrelevant}$$

Advantages

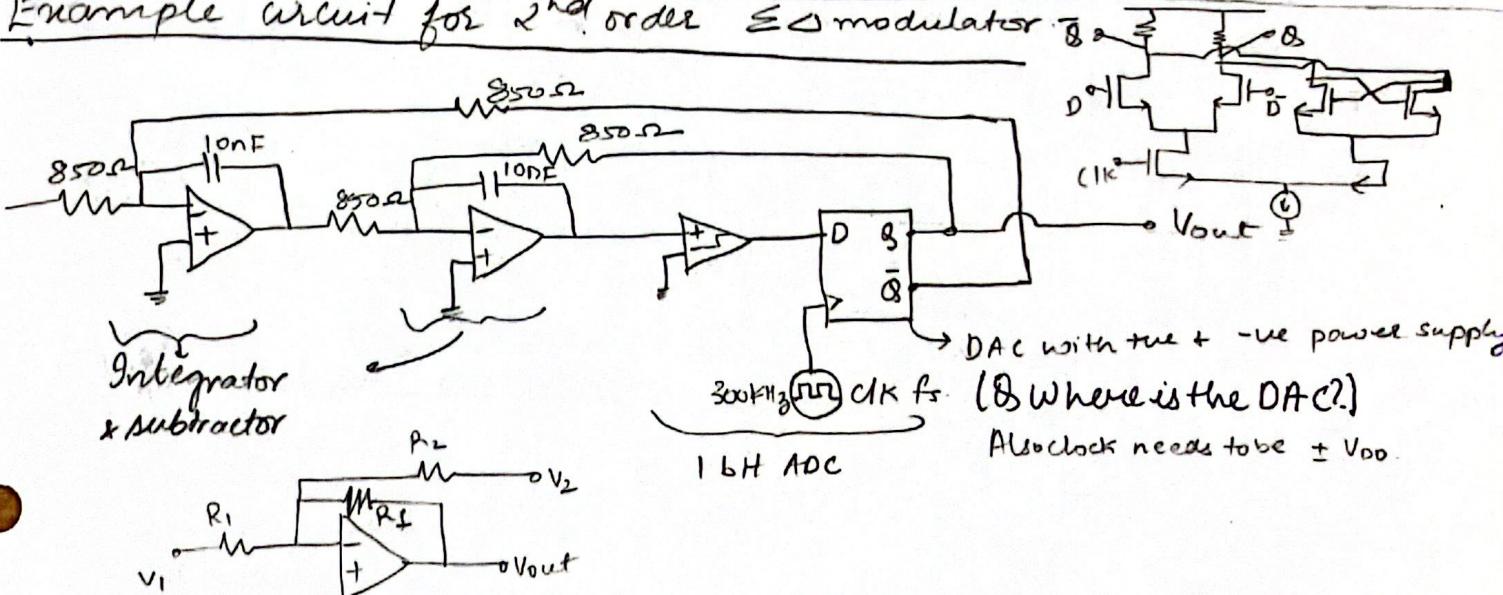
- > Stable.
- > lower order.

Q: Where do we need high resolution & low bandwidth?

Disadvantages

- > Mismatch b/w the 2 stages can cause problems!

Example circuit for 2nd order ΣΔ modulator

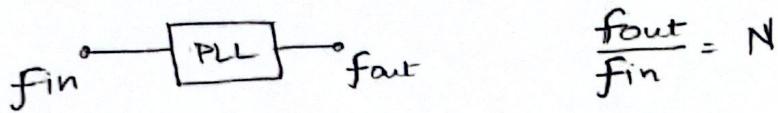


$$V_{out} = -\frac{R_f}{R_1} V_1 - \frac{R_f}{R_2} V_2$$

DAC with the + -ve power supply
300kHz CLK f. (Q: Where is the DAC?)
Also clock needs to be ± V_{dd}.

$\Sigma\Delta$ modulator for Frac-N PLL

PLL



If $f_{out} = 900 \text{ MHz}$ & channel spacing is 200 kHz .

$$\begin{aligned} &\Rightarrow 900.0 \text{ MHz} \\ &900.2 \text{ MHz} \\ &900.4 \text{ MHz} \end{aligned} \quad \left. \begin{array}{l} \text{What is the maximum } f_{in} \text{ I need?} \\ f_{in} = 200 \text{ kHz} \quad \text{Slow because PLL BW} = \frac{1}{10} f_{in}. \\ N \approx 4500 \quad \text{Noisy.} \end{array} \right.$$

$\text{noise} \propto N^2$
power

Solution? Fractional divide.

Large f_{in} & fractional N .

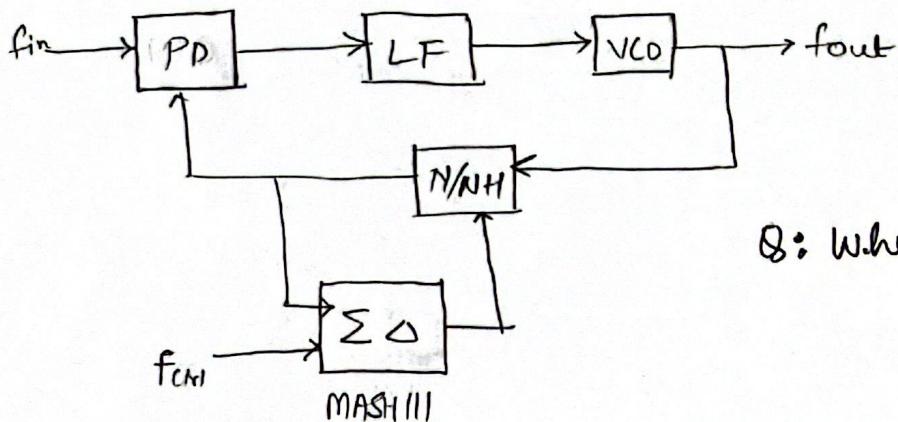
$$f_{in} = 20 \text{ MHz} \quad \& \quad N = 45.01 \Rightarrow 900.2 \text{ MHz.}$$

Problem? > If divider switches between 45 & 46 periodically, we get singletones (spurs at the output)

> Need to dither to remove spurs. \Rightarrow Need a "noisy" signal whose average value is "deterministic".

$\Rightarrow \Sigma\Delta$ modulator!

> Noise is shaped and removed by PLL bandwidth



Q: Where is the lowpass filter?

Appendix

* 13

Derivation of oversampling SNR

Variance or power of error signal $\sigma_e^2 = \frac{\Delta^2}{12}$
 & signal / p σ_x^2

$$\text{SNR} = 10 \log \frac{\sigma_x^2}{\sigma_e^2} \quad \left| \begin{array}{l} \text{Pey}(f) = \sigma_e(f) \cdot |H_e(f)|^2 \\ \text{P.S.D} \end{array} \right.$$

Since noise is white:

$$P.S.D \quad \sigma_e(f) = \frac{\sigma_e^2}{f_s} \Rightarrow \text{P.S.D of oversampled case is} \\ f_B \quad \text{Pey}(f) = \frac{\sigma_e^2}{f_s} \quad \text{this is higher}$$

$$\Rightarrow \text{In band noise power } \sigma_{ey}^2 = \int_{-f_B}^{f_B} \text{Pey}(f) df$$

$$= 2 \int_0^{f_B} \text{Pey}(f) df$$

$$= 2 \int_0^{f_B} \frac{\sigma_e^2}{f_s} df$$

$$\boxed{\sigma_{ey}^2 = \sigma_e^2 \left(\frac{2f_B}{f_s} \right)} \quad \text{l increase of Nyquist sampling.}$$

\Rightarrow In band power is lower!

$$\text{SNR} = 10 \log \frac{\sigma_x^2}{\sigma_{ey}^2} = 10 \log(\sigma_x^2) - 10 \log(\sigma_{ey}^2) + 10 \log \underbrace{\frac{f_s}{2f_B}}_{\text{process gain}}$$

If $\frac{f_s}{2f_B} = 2^\gamma$ \Rightarrow f_s is doubled $\Rightarrow \gamma++$

$$\text{SNR} = 10 \log(\sigma_x^2) - 10 \log(\sigma_{ey}^2) + \underbrace{3.01 \gamma}_{\text{double rate}} \\ \Rightarrow 3 \text{dB} \uparrow$$

$\sum \Delta$ modulator SNR

In band noise power

$$\bar{\sigma}_e^2 = \sigma_e^2 \left\{ \frac{\pi^2}{3} \cdot \left(\frac{2f_B}{f_s} \right)^3 \right\}$$

Similar to before.

$$H_c(z) = (1 - z^{-1})$$

$$P_{eq}(f) = P_e(f) \cdot |H_c(f)|^2$$

$$\bar{\sigma}_{eq}^2 = \int_{-f_B}^{f_B} P_{eq}(f) df$$

$$\Rightarrow SNR = 10\log(\bar{\sigma}_x^2) - 10\log(\bar{\sigma}_e^2) - 10\log\left(\frac{\pi^2}{3}\right) + 30\log\frac{f_s}{2f_B}$$

$$= 10\log(\bar{\sigma}_x^2) - 10\log(\bar{\sigma}_e^2) - 10\log\left(\frac{\pi^2}{3}\right) + 9.03 r.$$

\Rightarrow doubling sampling rate $= 9 dB \uparrow \Rightarrow \underline{1.5 \text{ bits improvement!}}$

Quantization error power $\bar{\sigma}_{eq}^2$, we know σ_{eq} is uniform across $-\frac{q}{2}$ to $\frac{q}{2}$.

$$\Rightarrow \bar{\sigma}_{eq}^2 = \frac{1}{q} \int_{-\frac{q}{2}}^{\frac{q}{2}} \sigma_{eq}^2 d\sigma_{eq} \rightarrow \bar{x}^n = \int x^n f_x(x) dx$$

$$= \frac{1}{q} \cdot \frac{\sigma_{eq}^2}{3} \Big|_{-\frac{q}{2}}^{\frac{q}{2}}$$

$$= \frac{1}{3q} \cdot \frac{2q^3}{8} = \frac{q^2}{12}$$