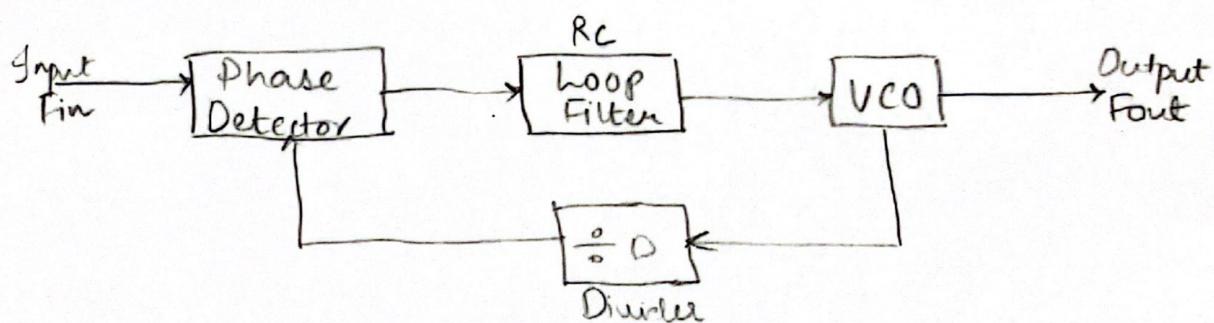


Phase locked loops.

→ Uses

- Power grid integration
- Rx-Tx clock synchronization
- Clock synchronization across the chip.
- Going from low freq. clock of oscillator to high freq. on chip.
- Modulate/Demodulate FM signals

Pll as a Feedback system

- Feedback factor is $\beta = \frac{1}{D}$
- $\frac{Y}{X} = \frac{A(s)}{1 + \beta A(s)}$, when $A(s)$ is large $\frac{Y}{X} = \frac{1}{\beta}$

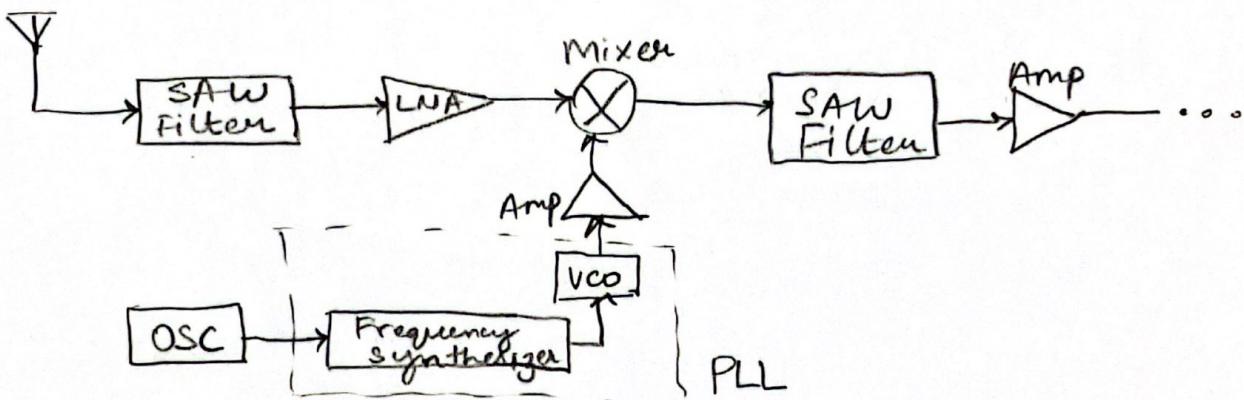
$$\Rightarrow \boxed{\frac{F_{out}}{F_{in}} = D}$$

Phase detector :- Measures phase difference between two signals and generates a corresponding voltage signal.

loop Filter :- A low pass filter that generates an average value of the voltage signal.

Voltage controlled oscillator :- Generates a frequency corresponding to the input voltage level.

TI GPS Handset [GPS - 1.5 GHz]



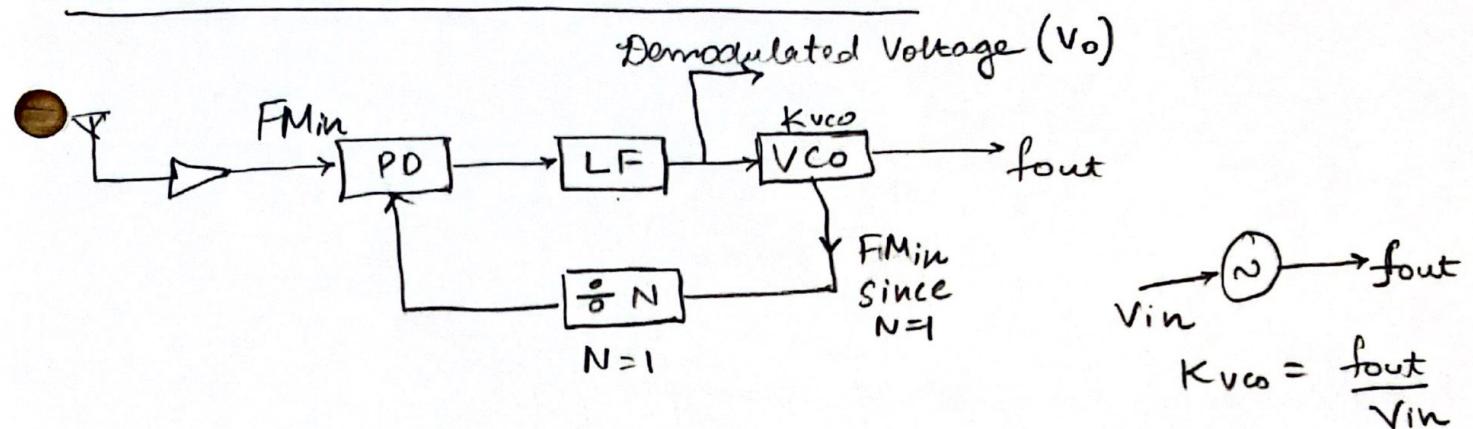
SAW :- An acoustic mechanical ~~frequency~~ filter since GPS is narrowband

Mixer :- Lowers the frequency.

Phh :- Generates the 1.5 GHz signal to pull out the GPS signal.

FM Demodulation and Modulation

13



$$\rightarrow \Rightarrow F_{VCO} = F_{Min}$$

$$\Rightarrow K_{VCO} = \frac{f_{out}}{V_{in}} = \frac{f_{out}}{V_o}$$

$$\Rightarrow V_o = \frac{f_{out}}{K_{VCO}}$$

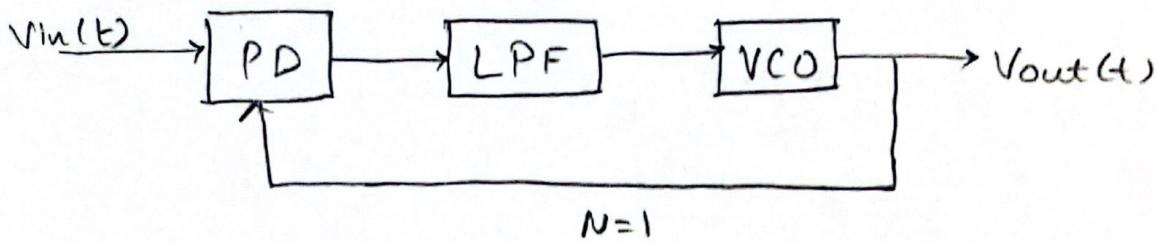
$$\Rightarrow \boxed{V_o = \frac{F_{Min}}{K_{VCO}}}$$

Voltage V_o indicates the frequency F_{Min}

\rightarrow For modulation you could vary N by the envelope/message signal frequency.

Clock Recovery.

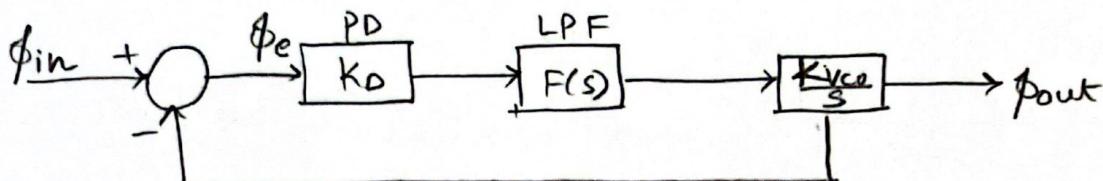
PLL Model.



Frequency is the rate of change of phase.

$$\omega = \frac{d\phi}{dt} \Rightarrow \phi = \int \omega dt$$

Modelling PLLs in phase is thereby easier.



$$\begin{aligned} & \text{For } VCO : \quad f_{out} = K_{VCO} V_{in} \\ & \frac{d\phi_{out}}{dt} = K_{VCO} V_{in} \\ & \Rightarrow \phi_{out} = \int K_{VCO} V_{in} \\ & \qquad \qquad \qquad = \frac{K_{VCO}}{s} V_{in} \end{aligned} \quad \left. \begin{array}{l} f_{out} = K_{VCO} V_{in} \\ \frac{d\phi_{out}}{dt} = K_{VCO} V_{in} \end{array} \right\} \Rightarrow \boxed{\frac{\phi_{out}}{V_{in}} = \frac{K_{VCO}}{s}} \frac{\text{rad}}{\text{sec/v}} \text{ or } \frac{\text{Hz}}{\text{V}}$$

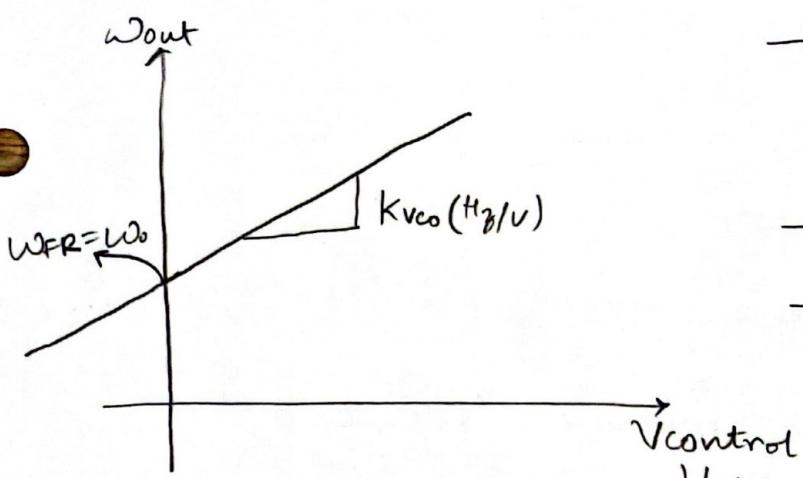
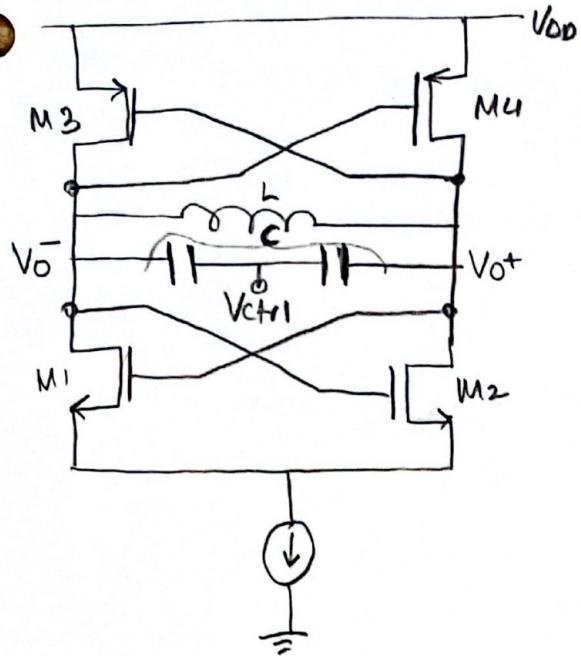
→ Therefore, PLLs have an inherent integration inside them → pole at 0 frequency (log scale-0).

→ At $\omega=0$ we get ∞ gain!

For opamps we do not get ∞ gain at $\omega=0$.

VCO - Implementation

15



- M1-M4 form 2 cross coupled inverters
- On their own they would form a latch
- Adding the L, C gives a resonance

$$\omega_{res} = \frac{1}{\sqrt{LC}}$$
- Capacitors here are varactors controlled by Vctrl.
- Only LC would give oscillations that die out, the transistors sustain these oscillations.
- Therefore Vctrl is translated to a frequency ω .

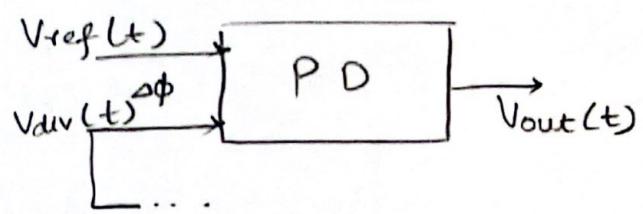
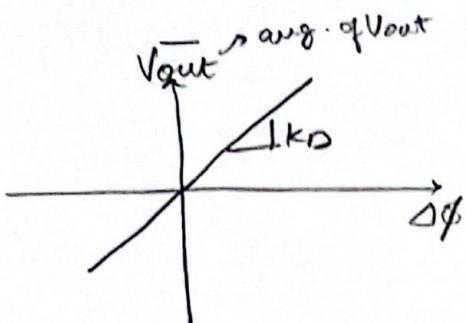
$$\rightarrow \omega_{out} = \omega_0 + K_{VCO} \cdot V_{control}$$

$$\begin{aligned} \rightarrow V_{out}(t) &= A \cos \omega_{out} \\ &= A \cos(\omega_0 t + K_{VCO} \int_{-\infty}^t V_{ctrl} dt) \\ \Rightarrow \phi_{excres} &= K_{VCO} \int_{-\infty}^t V_{ctrl} dt \end{aligned}$$

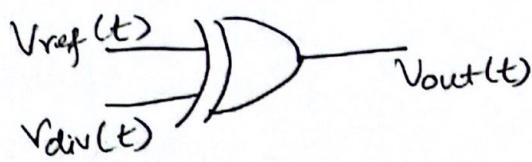
$$\phi_{excres} = \frac{K_{VCO}}{S} \cdot V_{ctrl}(t)$$

→ Each cross coupled pair gives a negative resistance of $-\frac{2}{g_m}$ to cancel the lossy resistors in the LC tank. This keeps the oscillations going!

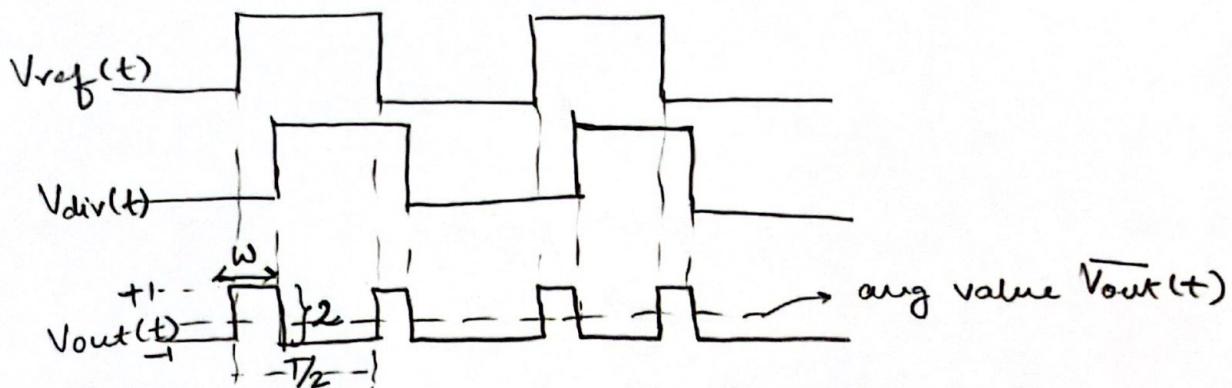
Phase Detector Implementation.



XOR gate



A	B	output
0	0	0
0	1	1
1	0	1
1	1	0

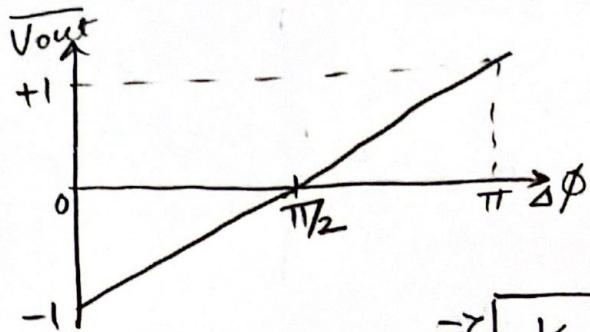


> Notice the XOR extracts the phase difference.

> $\overline{V_{out}} = 0$ if in phase.

→ In this case it is $\overline{V_{out}} = -1$ if in phase and +1 if out of phase

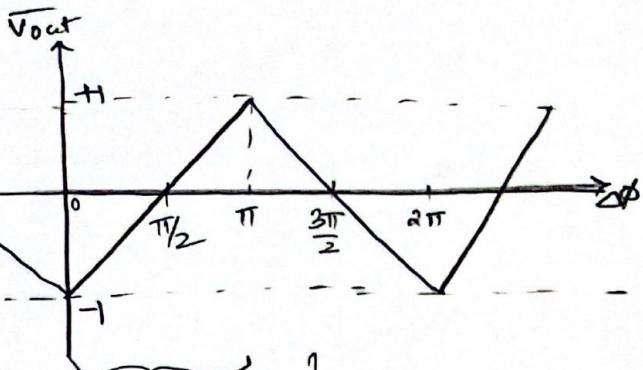
$$\rightarrow \overline{V_{out}} = -1 + \frac{2w}{T/2}$$



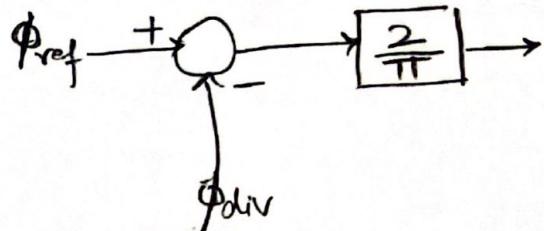
$$\Rightarrow K_D = \frac{2}{\pi} \frac{V}{\text{rad.}}$$

→ Phase detector Gain

$$K_D = \frac{2}{\pi}$$



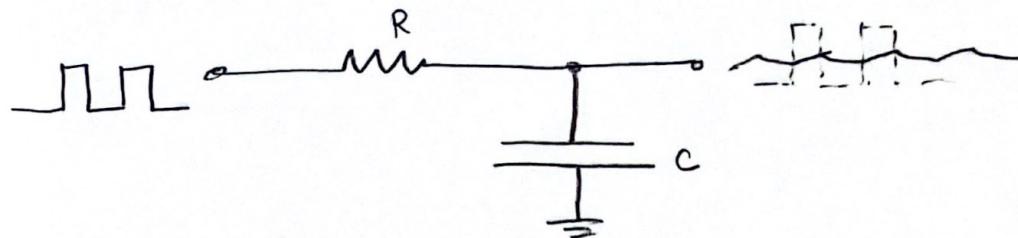
range limited to π



} More sophisticated
PDs have 2π range

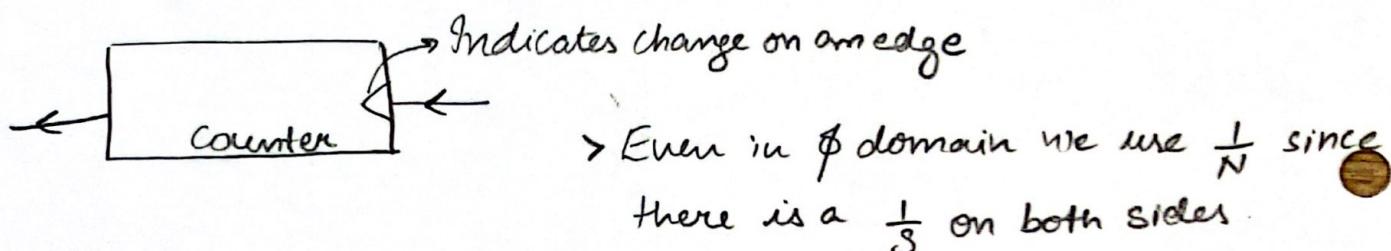
loop Filter Implementation.

RC low pass filter \rightarrow simplest model.



\rightarrow later on we will see more complete implementations.

Divider Implementation.



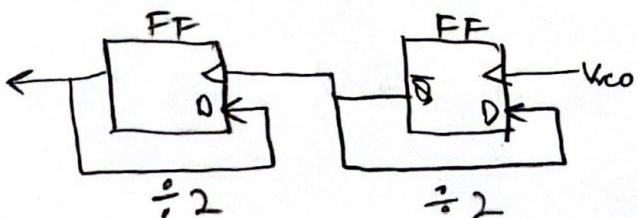
\rightarrow It can be made programmable.

$$\omega_{div} = \frac{1}{N} \omega_{vco}$$

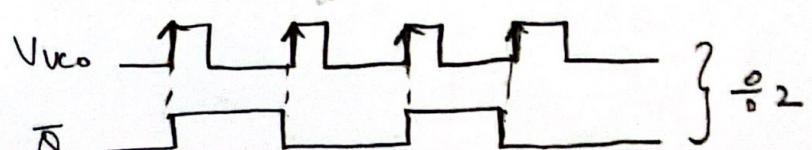
$$\phi_{div} = \int_0^t \frac{1}{N} \omega_{vco}(t) dt$$

$$\boxed{\phi_{div} = \frac{1}{N} \phi_{vco}}$$

\rightarrow Dividing by power of 2 is easier using flip flops.

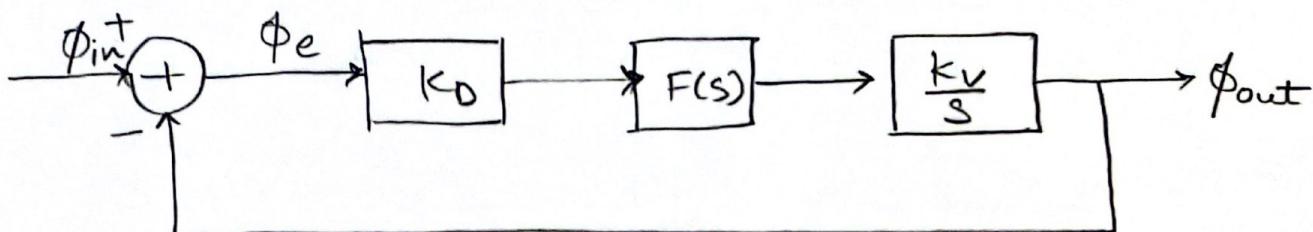


At each edge the state flips



PLL Model - Putting it all together.

(Implementation).



$$\frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{\frac{K_D F(s) K_V}{s}}{1 + \frac{K_D F(s) K_V}{s}} = \frac{K_D F(s) K_V}{s + K_D F(s) K_V}$$

PLL order and type

Order :- Highest power of denominator

Type :- No. of integrators.

$$A_f(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{K_D K_V F(s)}{s + K_D K_V F(s)}$$

At $s=0$ (low freq) $\frac{\phi_{out}}{\phi_{in}} > 1 \rightarrow$ changes in ϕ_{in} are tracked well

→ PLL is locked when $\phi_{out} - \phi_{in}$ is a constant K .

Ideally we want $\phi_{out} - \phi_{in} = 0$ but signals have rise time and there are often offsets in switching circuit.

→ As long as $\left. \begin{array}{l} \phi_{out} - \phi_{in} = K \\ W_{out} = W_{in} \end{array} \right\}$ PHL is locked! 

- If $F(s) = 1 \Rightarrow A(s) = \frac{K_o K_v}{s + K_o K_v}$ ^{single pole} Order 1
 ↗ no filter!
 ↗ So we cannot average → this is not practically used.
- At low frequency gain=1, but it drops at higher frequencies.

→ $\phi_e = \phi_{in} - \phi_{out} \Rightarrow \frac{\phi_e}{\phi_{in}} = 1 - \frac{\phi_{out}}{\phi_{in}} = 1 - \frac{A_s}{1+A_s} = \frac{1}{1+A_s}$ 

⇒ Phase error

$$E(s) = \frac{\phi_e(s)}{\phi_{in}(s)} = \frac{1}{1+A_s} = \frac{s}{s + K_v K_o F(s)}$$

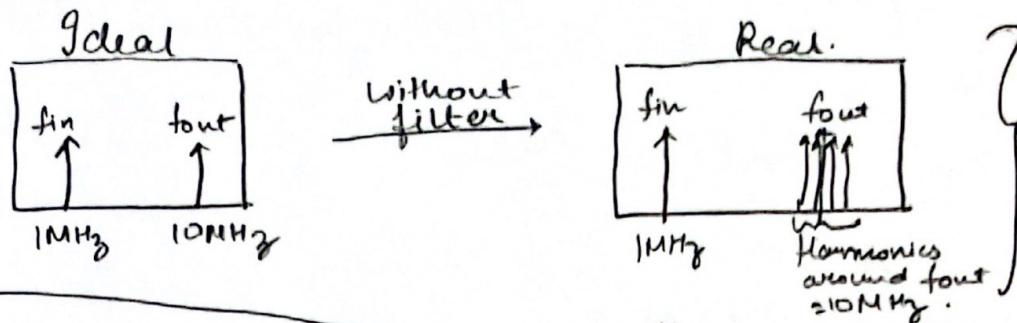
At low freq ($s=0$) $\Rightarrow E(s)=0$

At high freq ($s=\infty$) $\Rightarrow E(s)=1$

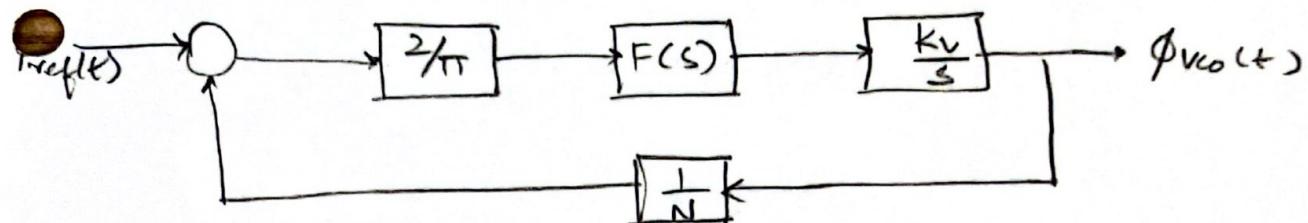
→ A single integrator \Rightarrow gain could be $\infty \Rightarrow$ Error could be 0 if ϕ_{in} and ϕ_{out} are equal.

→ In reality disturbances increase the error so we need more integrators. 

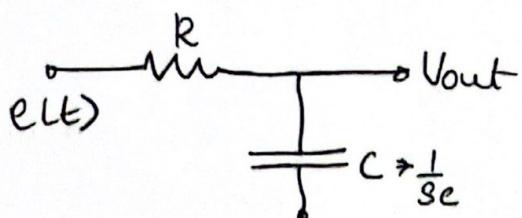
- In type 0, order 0 there is no filter. $\Rightarrow V_{ppout}$ keeps fluctuation and we would see a bunch of harmonics around fout.



→ 2nd order PLL



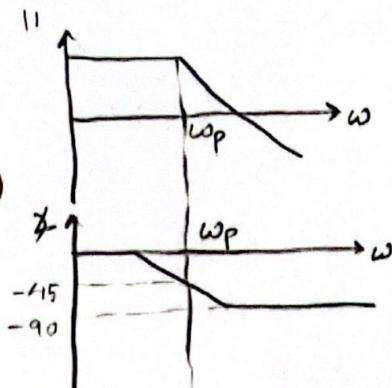
Loop Filter



$$F(s) = \frac{1}{R + \frac{1}{sC}} = \frac{1}{1 + RCs}$$

$$\Rightarrow \omega_{pole} = -\frac{1}{RC}$$

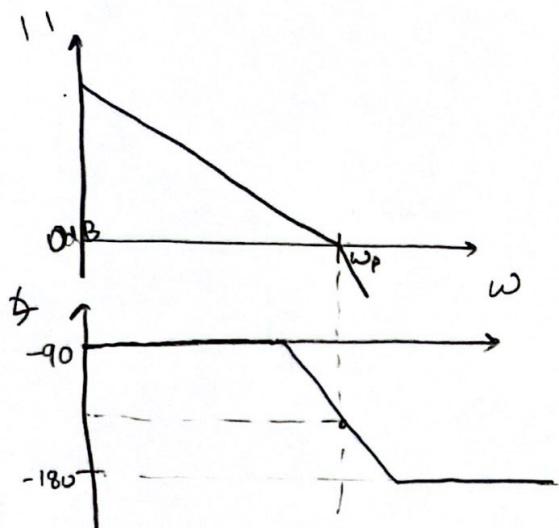
$$F(s) = \frac{1}{1 + \frac{s}{\omega_p}}$$



Filter tradeoff [Filtering vs. Phase Margin/Stability]

- > Low ω_p : Good for filtering, ω_p should be atleast 1 decade lower than ω_u to filter out the bumps.. Bad for phase margin.
- > High ω_p : Good for Phase Margin.

For 45° phase margin.



For 45° phase margin we need $\omega_p = \omega_u \rightarrow$ unity gain frequency.

$$\text{loop gain} = \frac{2}{\pi} \cdot \frac{1}{1 + \frac{s}{\omega_p}} \cdot \frac{Kv}{s} \cdot \frac{1}{N}$$

$$\begin{aligned} \text{loop gain magnitude} &= \frac{2}{\pi} \cdot \left| \frac{1}{1 + \frac{j\omega_p}{\omega_p}} \right| \cdot \left| \frac{Kv}{s} \right| \cdot \frac{1}{N} \\ &\text{at Ph.M}=45^\circ \end{aligned}$$

$$= \frac{2}{\pi} \cdot \frac{1}{\sqrt{2}} \cdot \frac{Kv}{\omega_p} \cdot \frac{1}{N}$$

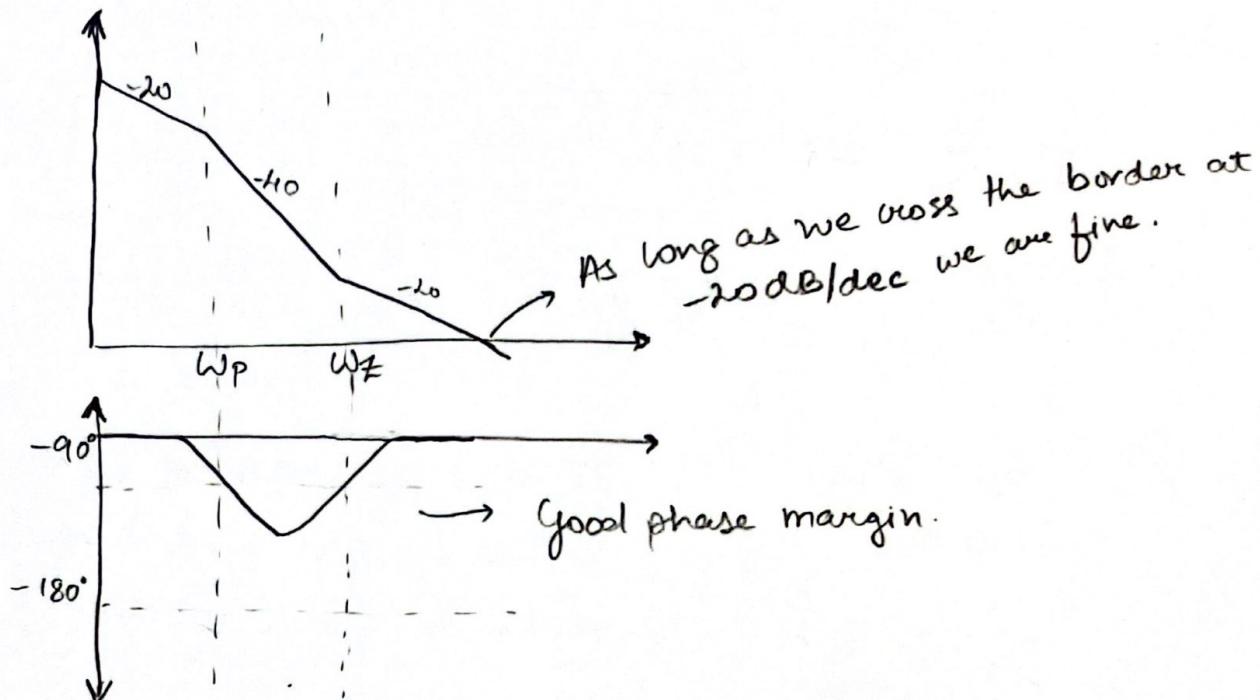
$$\Rightarrow \boxed{\omega_p = \frac{\sqrt{2}}{\pi} \cdot \frac{Kv}{N}} \quad \text{For ph. margin of } 45^\circ.$$

> Ideally we want a higher phase margin $\Rightarrow \omega_p$ should be higher.

> Ph.M $< 60^\circ \Rightarrow$ Peaking in freq. response
Ringing in Step response.

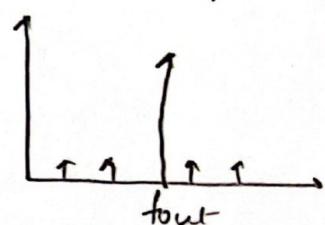
→ If $\omega_p < \omega_u \rightarrow$ Very bad since Ph.M. is $< 45^\circ$.

- In reality ω_p is less than ω_n . How do we solve this problem?
- Add a LHP zero!

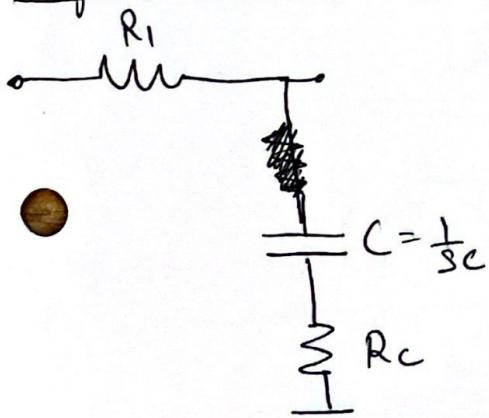


Drawback?

High frequency components are not fully attenuated.
→ End up with sidebands because reference signal is not fully attenuated.



Implementation



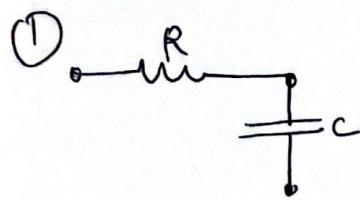
$$F(s) = \frac{R_c + \frac{1}{sC}}{R_1 + R_c + \frac{1}{sC}} = \frac{1 + sR_c C}{1 + sC(R_1 + R_c)}$$

$$\Rightarrow \boxed{\omega_p = \frac{-1}{(R_1 + R_c)C}}$$

$$\boxed{\omega_z = \frac{-1}{R_c C}}$$

$$\Rightarrow \omega_z > \omega_p$$

Damping Factor Viewpoint



$$A_f(s) = \frac{\phi_{out}(s)}{\phi_{in}} = \frac{K_0 K_V \omega_p}{s^2 + s\omega_p + \omega_p K_0 K_V}$$

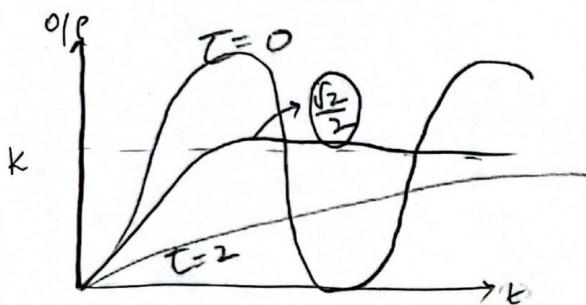
$$= \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Natural frequency

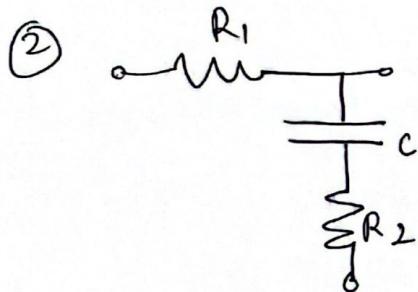
$$\omega_n = \sqrt{\omega_p K_0 K_V}$$

Damping factor

$$\zeta = \frac{1}{2} \sqrt{\frac{\omega_p}{K_0 K_V}} \rightarrow \frac{\sqrt{2}}{2} \text{ is optimal!}$$



⇒ We are constrained in the values of ω_p , K_0 & K_V . This makes it hard to design.



$$A_f(s) = \frac{\phi_{out}(s)}{\phi_{in}} = \frac{K_0 K_V F(s)}{s + K_0 K_V F(s)}.$$

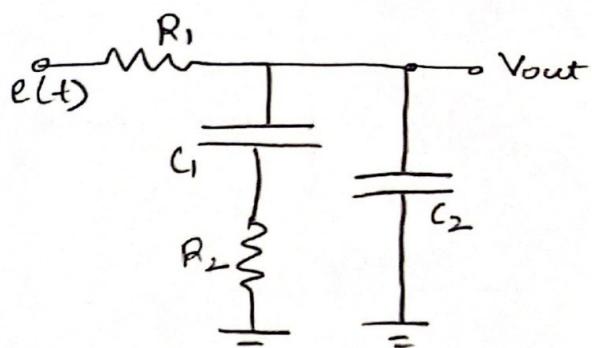
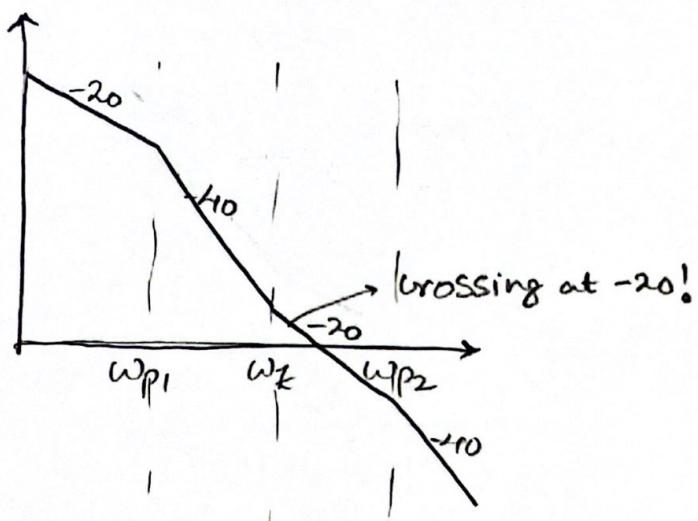
$$F(s) = \frac{1 + sC R_2}{1 + sC (R_1 + R_2)}$$

$$\Rightarrow \omega_p = -\frac{1}{C(R_1 + R_2)}$$

$$\omega_K = -\frac{1}{C R_2}$$

$$\zeta = \frac{1}{2} \sqrt{\frac{\omega_p}{K_0 K_V}} \left(\frac{K_0 K_V}{\omega_K} + 1 \right)$$

- How do we solve the problem of higher frequencies
- not getting attenuated?
- Add another pole!



Type ② Phhs.

> Use a charge pump!

Type ① :- One integrator in VCO and none in filter.

Type ② :- One integrator in VCO and one in filter.

For example

$$A(s) = \frac{k_{\text{loop}} F(s)}{sN} = \frac{1}{N} \cdot \frac{I_d}{2\pi} \cdot \frac{\frac{k_v}{\delta} \cdot \frac{1 + sT_2}{s(C_1 + C_2)(1 + sT_1)}}{\text{2 integrators.}}$$

Filter is 2nd order.

Order: 3

Type: 2

Steady state phase error vs. type requirement.

Frequency 1/p	Phase 1/p	Type required to prevent error E(s).
Ideal/ Impractical No change	Step	Type ①
Step	Ramp	Type ②
Ramp	Quadratic	Type ③ → Not really done.

> Proofs are in subsequent pages.

Steady state phase Error

17

$$E(s) = \frac{\phi_e(s)}{\phi_{in}(s)} = \frac{1}{1+A(s)} = \frac{s}{s + K_v K_o F(s)}$$

Using Laplace Final Value Theorem.

$$\begin{aligned}\phi_e(t \rightarrow \infty) &= \lim_{s \rightarrow 0} s \phi_e(s) \\ &= \lim_{s \rightarrow 0} s \cdot \phi_{in}(s) \cdot E(s) \\ &= \lim_{s \rightarrow 0} \frac{s^2}{s + K_v K_o F(s)} \phi_{in}(s)\end{aligned}$$

For a step input $\phi_{in}(s) \rightarrow \text{Step} \Rightarrow \text{Type 0}$

$$\phi_{in}(t) = \Delta \phi u(t) \Rightarrow \phi_{in}(s) = \frac{\Delta \phi}{s}$$

$$\begin{aligned}\Rightarrow \phi_e(t \rightarrow \infty) &= \lim_{s \rightarrow 0} \frac{s}{s + K_v K_o F(s)} \Delta \phi \\ &= 0\end{aligned}$$

\Rightarrow Even for type 0 PLL, the steady state error is 0 for a step change in input phase!

→ Step input in frequency.

$$\omega_{\text{tot}}(t) = \omega_0 + \Delta\omega u(t)$$

$$\omega_{\text{tot}}(s) = \frac{\Delta\omega}{s} \Rightarrow \phi_{\text{tot}}(t) = \int \omega_{\text{in}}(t) dt = \omega_0 t + \Delta\omega u(t)$$

$$\Rightarrow \phi_{\text{in}}(s) = \frac{\Delta\omega}{s^2}$$

$$\Rightarrow \phi_e(t \rightarrow \infty) = \lim_{s \rightarrow 0} \frac{s^2}{s + k_D k_V F(s)} \cdot \frac{\Delta\omega}{s^2} = \frac{\Delta\omega}{k_D k_V F(0)}$$

→ Steady state error is non-zero for Type I PLL with step change in input frequency. So we need another s term in numerator which comes from adding one integrator!

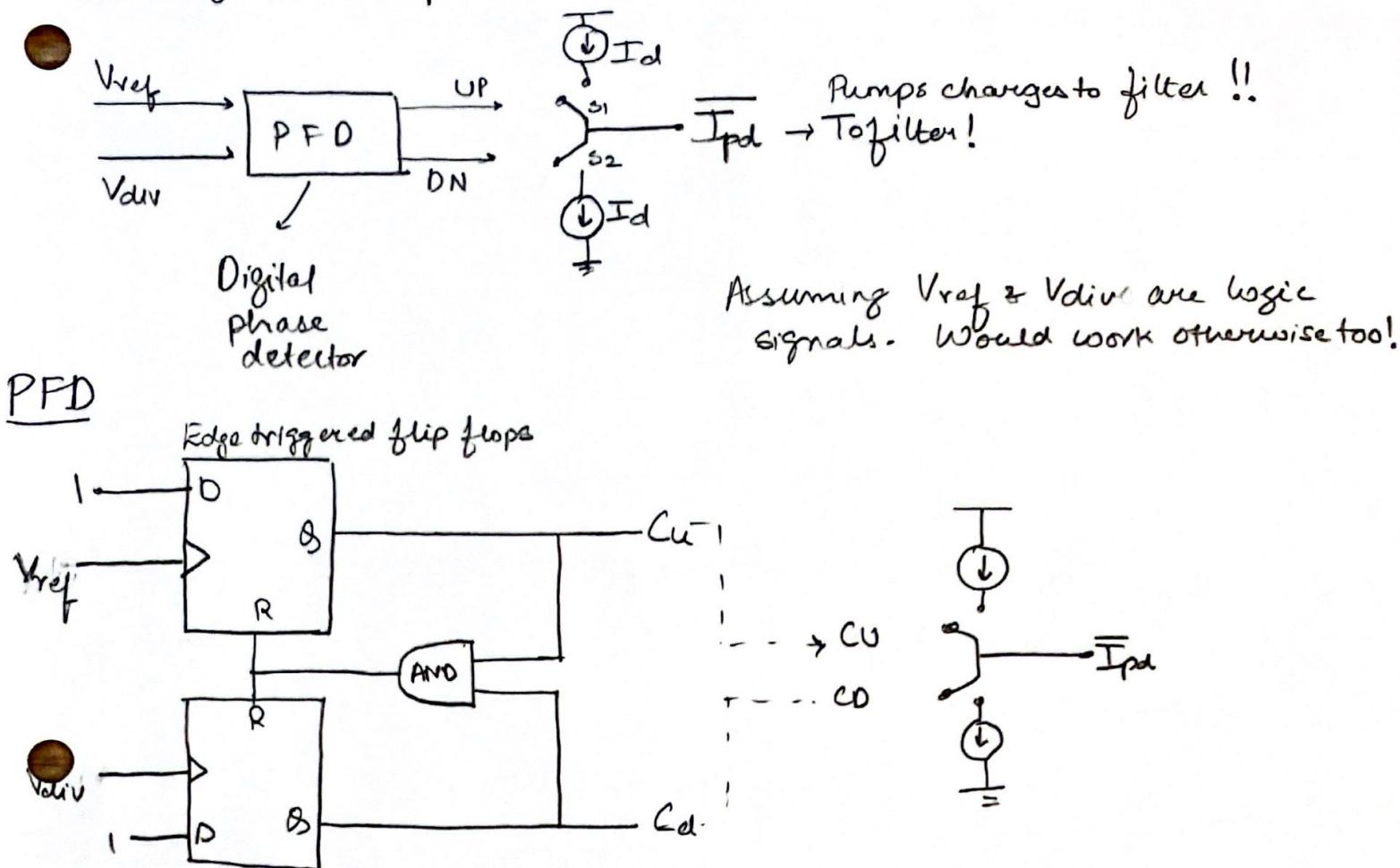
→ The integrator gives us a gain at DC and forces error to 0.

How do we implement this?

Charge pump + Phase Frequency Detector!

Charge Pump based Phase Detector

L17



Three states:- ✓ C_U , C_D low

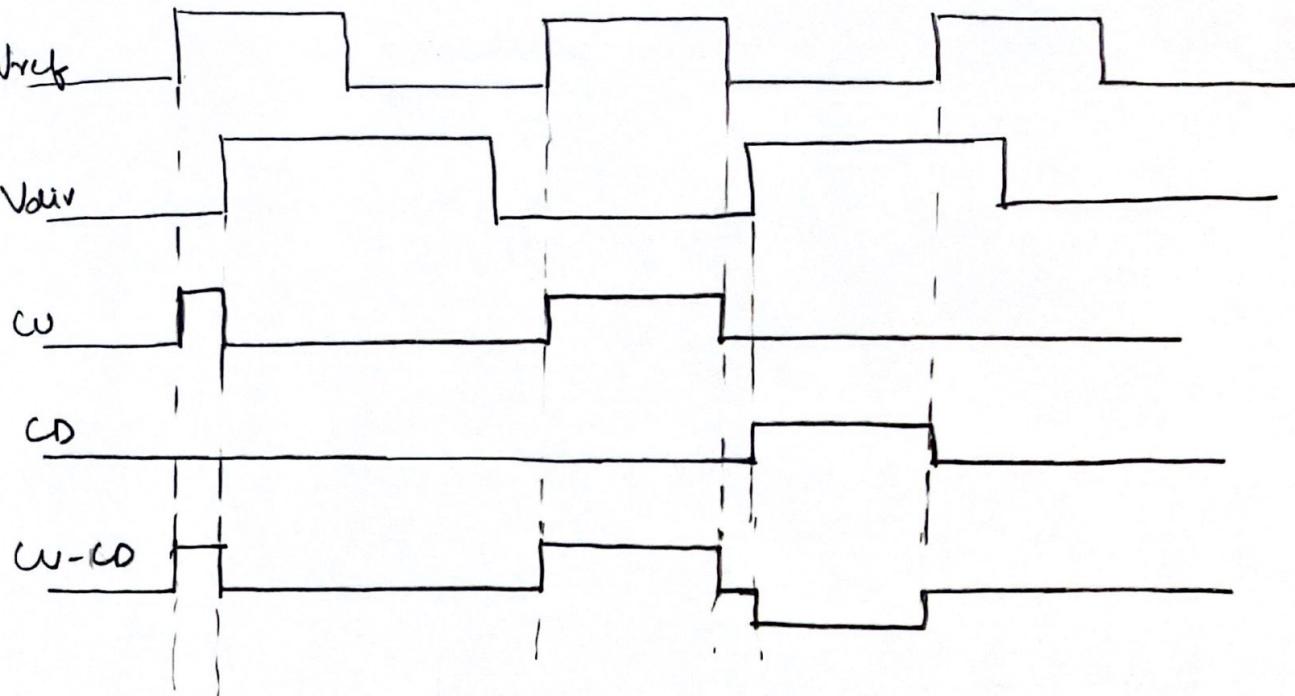
✓ C_U High, C_D low

✓ C_U low, C_D High.

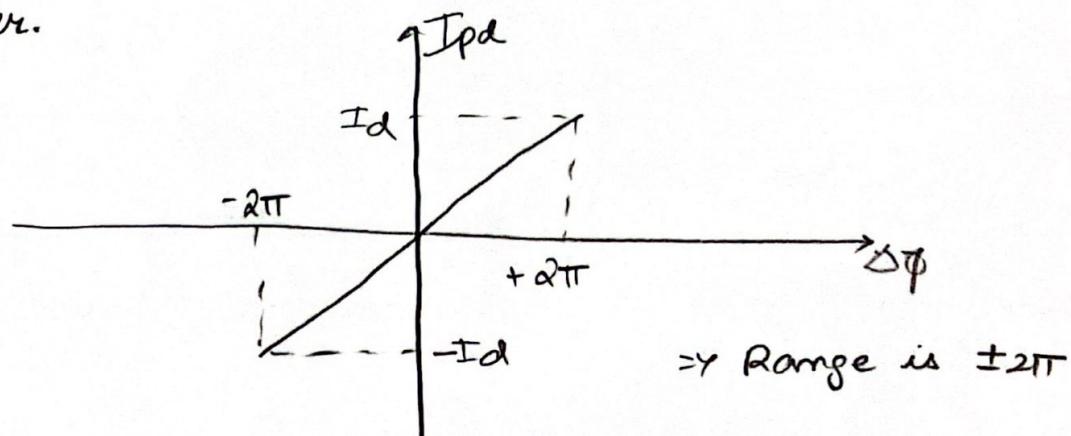
✗ C_U , C_D High \Rightarrow would reset the FFs.

Therefore output is high for all times that there is a phase mismatch between the 2 signals.

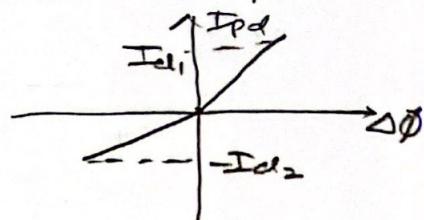
Once there are 3 states it is also known as Tristate PFD.



- Since the output can be above or below 0 value we get more information off of it. We can tell which frequency was higher!
- If the pulse is too thin, the rise time may be insufficient (ω_{CD}) to show the phase mismatch. This results in a Dead band.
- The ω_{CD} signals trigger the switches (S_1, S_2) and current is pumped to the filter when a phase mismatch occurs. The current direction is opposite based on which frequency is higher.



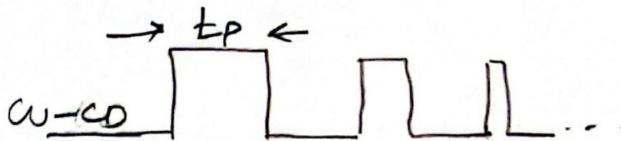
- The two current sources must be exactly equal! Otherwise the I_{pd} vs $\Delta\phi$ graph is ~~non-linear~~ and operation is not optimal.



$$\overline{I}_{pd} = \frac{t_p}{2\pi/\omega} \cdot I_d$$

$$= \frac{\phi_e}{\omega} \cdot \frac{\omega}{2\pi} \cdot I_d$$

$$= \frac{I_d}{2\pi} \phi_e$$

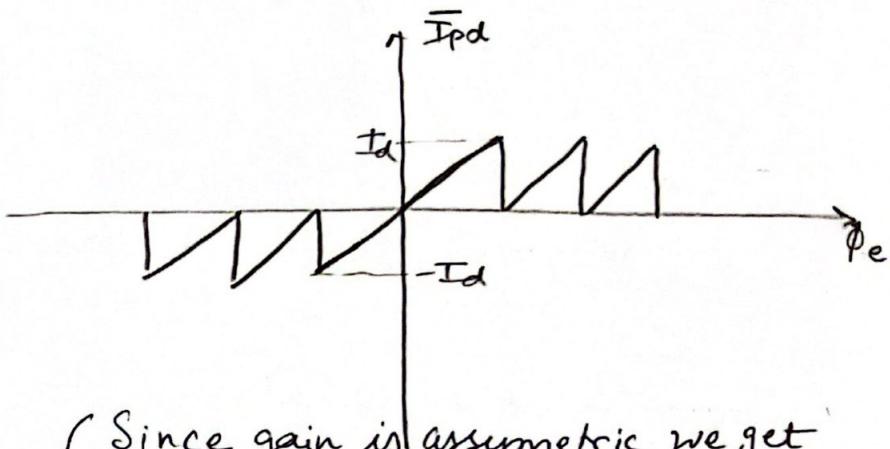


$$\Rightarrow \text{Gain } k_D = \frac{\overline{I}_{pd}}{\phi_e}$$

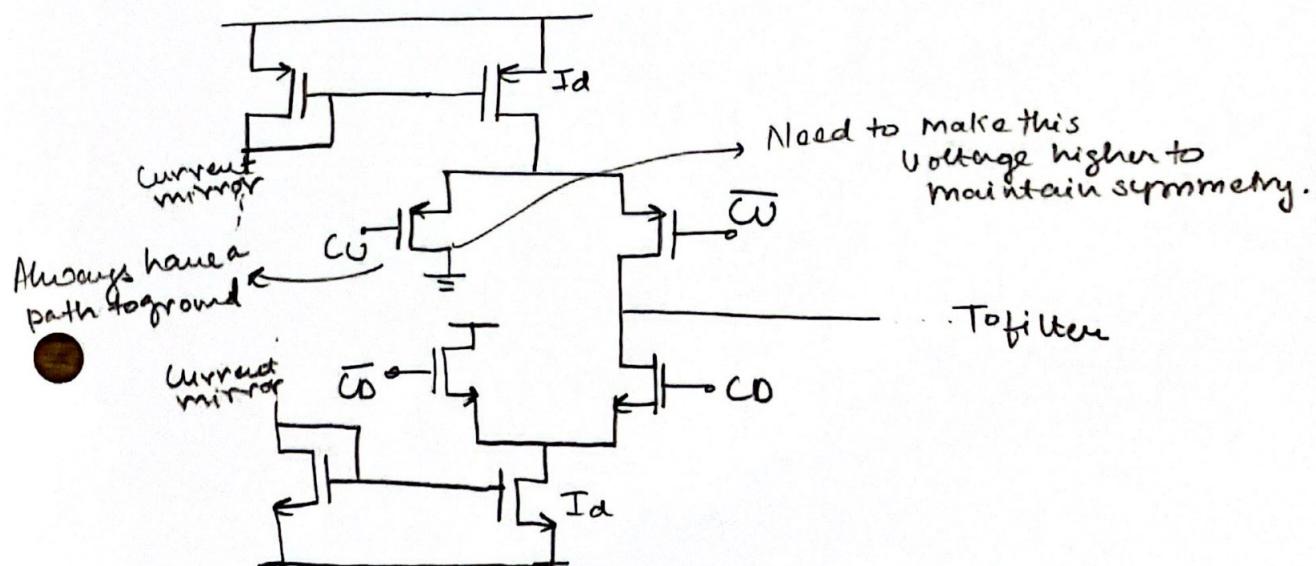
$$k_D = \frac{I_d}{2\pi}$$

Hence it is called phase frequency detector.

Since gain is asymmetric we get more information about which frequency is higher & not just $|f_2 - f_1|$. So PLL locks more easily



Implementation of Charge Pump



XOR vs. PFD

XOR:

- Simple, no need to match currents
- Good linearity
- Limited PD range ($0 - \pi$)
- No dead band.

PFD:

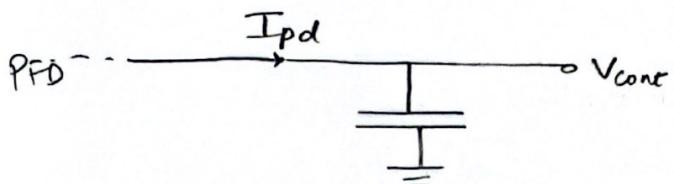
- Wide range ($-2\pi - 2\pi$)
- Frequency info too ➤ helps locking.
- OK linearity.
- Potential dead band.

Charge pump loop filter

(23)

Let's start simple.

$$V = \frac{I_{pd}}{SC}$$



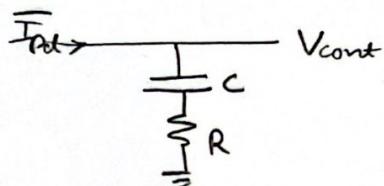
→ Current to Voltage conversion gives us a pole at 0 frequency ⇒ Integrator!

$$A_{loop}(s) = \frac{k_b k_v F(s)}{s} \cdot \frac{1}{N} = \frac{I_d}{2\pi} \cdot \underbrace{\frac{k_v}{s} \cdot \frac{1}{SC}}_{\text{2 poles at } 0} \cdot \frac{1}{N}$$

→ 2 poles at 0 ⇒ Type 2

→ The two poles at 0 give 0 Phase Margin ⇒ Need to fix this!
⇒ Really good oscillator ⇒ Bad PLL.

Add a zero



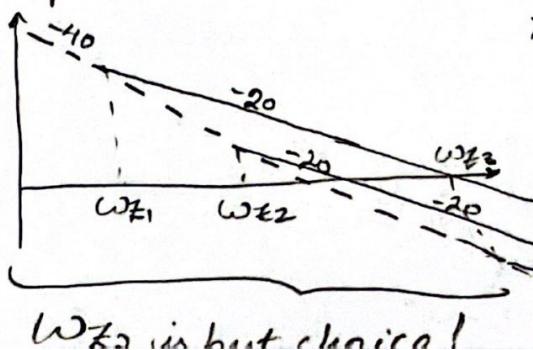
$$F(s) = \frac{1 + sRC}{SC}$$

$$\Rightarrow A_{loop}(s) = \frac{k_b k_v F(s)}{s} \cdot \frac{1}{N} = \frac{I_d}{2\pi} \cdot \frac{k_v}{s} \cdot \frac{1 + sRC}{SC} \cdot \frac{1}{N}$$

$$\omega_{p1} = \omega_{p2} = 0$$

$$\omega_z = -\frac{1}{RC}$$

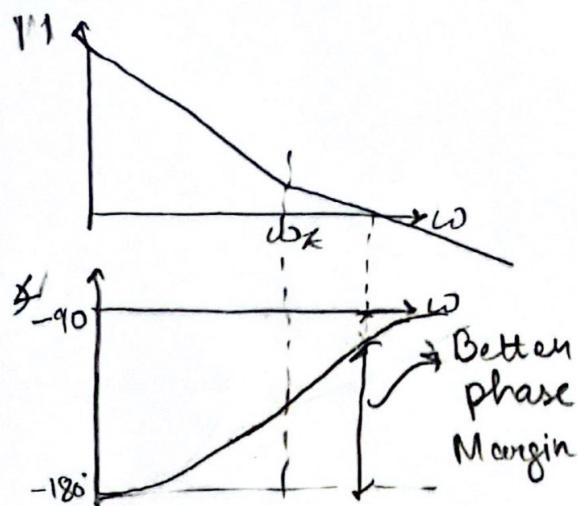
Where do we place this pole?
3 possibilities...



For stability we want zero crossing at -20dB
⇒ $\omega_{z3} \rightarrow$ bad

ω_{z1} is also bad since filtering would be poor at higher frequencies.

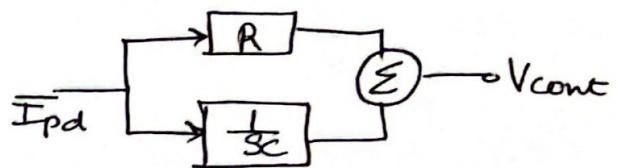
At ω_{Z_2}



$$F(s) = \frac{1 + SRC}{SC} = \frac{1}{SC} + R$$

↓
integral path ↓
proportional path

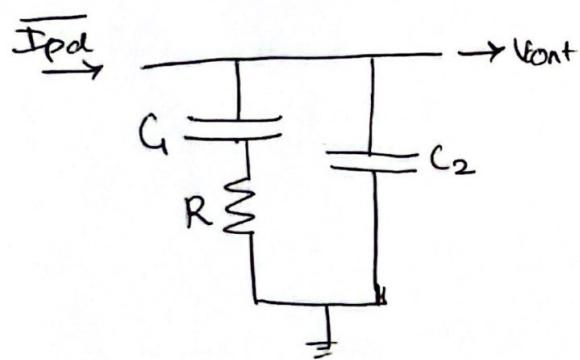
\Rightarrow PI controller!



What is the problem now?

High frequency ripples! \Rightarrow Need another pole.

Adding a high frequency pole \Rightarrow small cap with path to ground

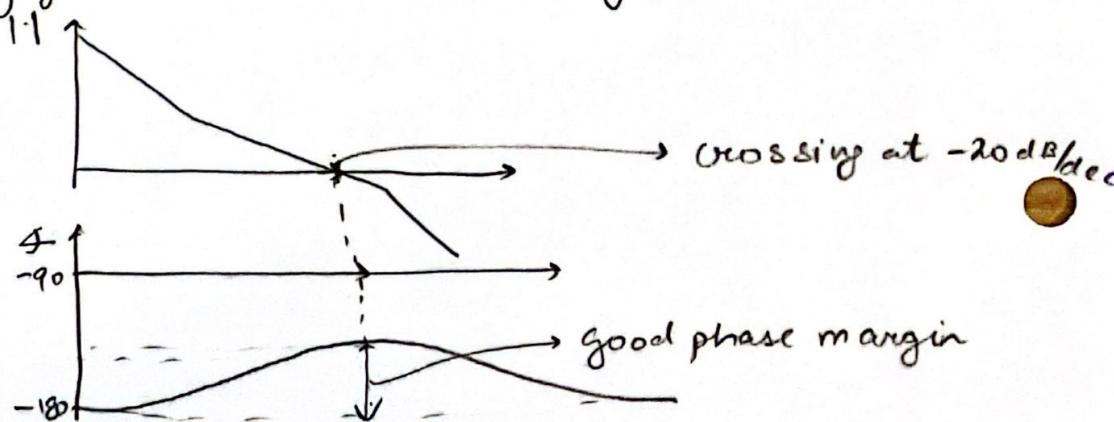


$$\text{Aloop}(s) = \frac{k_D k_V F(s)}{s} \cdot \frac{1}{N}$$

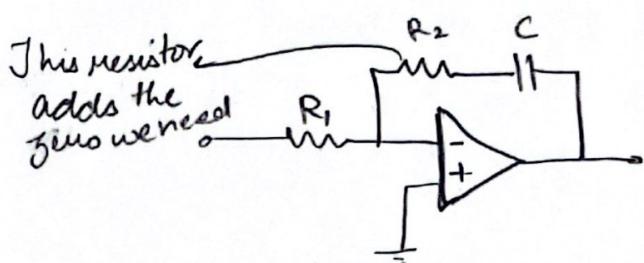
$$= \frac{1}{N} \cdot \frac{I_d}{2\pi} \cdot \frac{k_V}{s} \cdot \frac{1 + sT_2}{s(C_1 + C_2)(1 + sT_1)}$$

$$T_2 = RC_1, \quad T_1 = \frac{RC_1C_2}{C_1 + C_2}$$

\Rightarrow This is a very good PdL and is widely used! Phew!

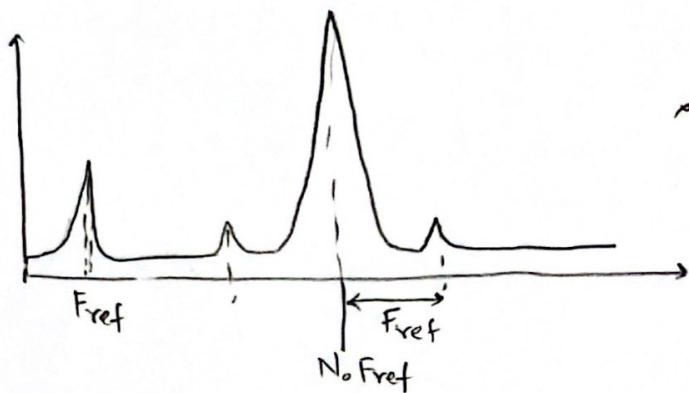


- >To make a Type ② PLL from an XOR PD we can
 - use an integrator at the filter with an opamp.



- higher power consumption
- slower because of opamp.
- More noisy \rightarrow opamp!
- Power supply rejection is better.

Filter Bandwidth Viewpoint



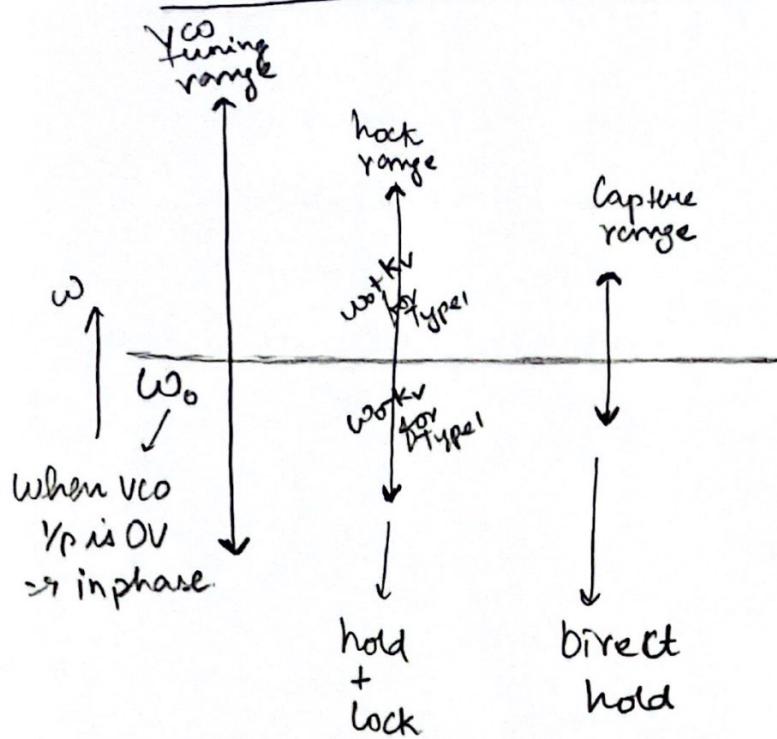
Spurs

- Spurious signals occurring at non harmonic frequencies (at F_{ref} away from $N F_{ref}$).
- Occur in pairs.
- Caused due to charge pump ripples.

Filter Bandwidth Tradeoff

- lower loop BW helps attenuate spurs.
- loop BW is limited to $\frac{1}{10}$ th of F_{ref} .
- Why not lower?
 - Need huge capacitors \Rightarrow no longer monolithic.
 - High settling time.
 - More noise since PLL starts tracking noise signals instead of Reference signal?

Capture/Hold range and lock range.



→ Capture range :-

Frequencies where the PLL can directly lock.

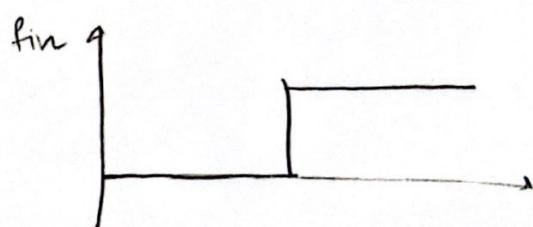
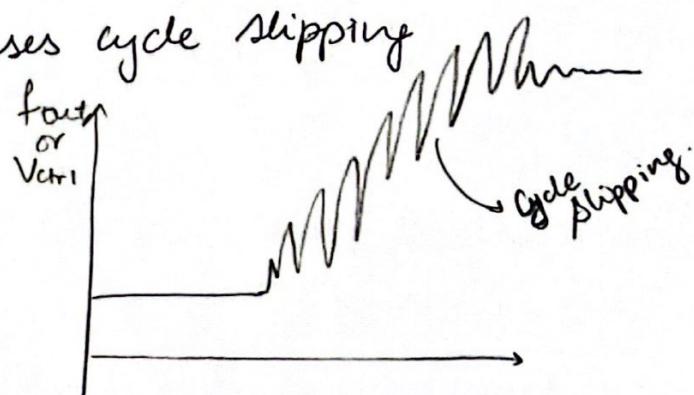
→ lock range :-

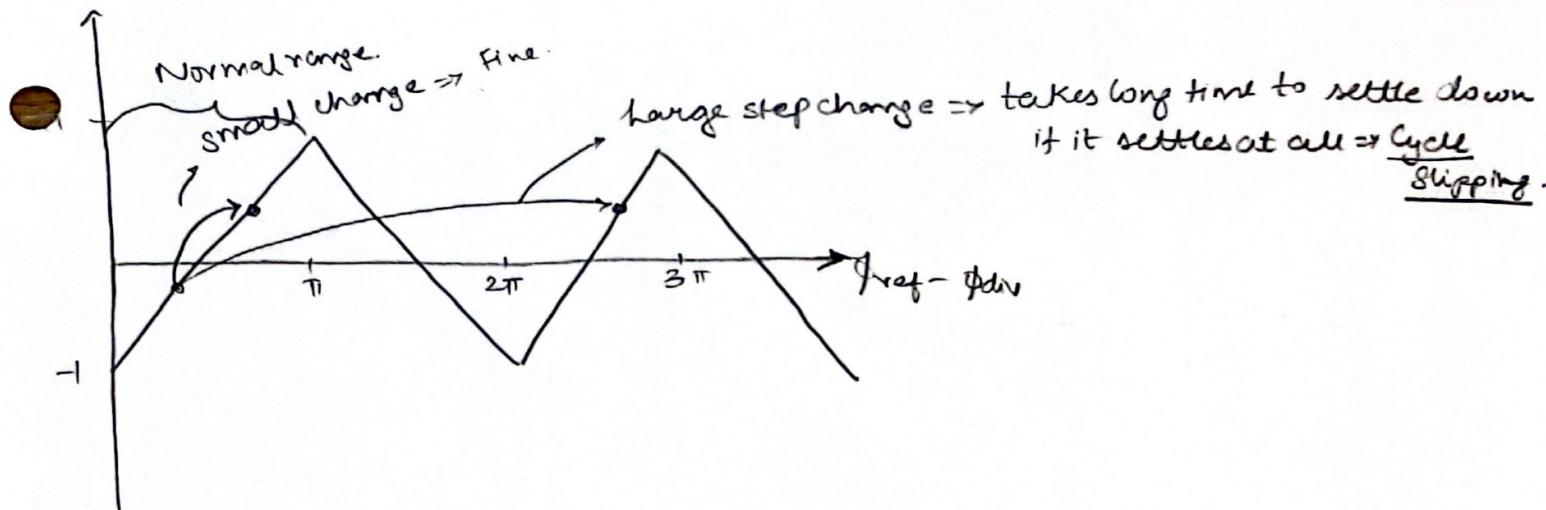
Once Phl is locked in the capture range, we can slowly increase the frequency of reference and Phl remains locked till the lock range.

→ Capture range is very hard to analyze.

→ For a Type I filter, max. possible capture range is $w_0 \pm k_r$

→ A large change in ^{frequency} ~~phase~~ (step) takes a long time to lock, and causes cycle slipping

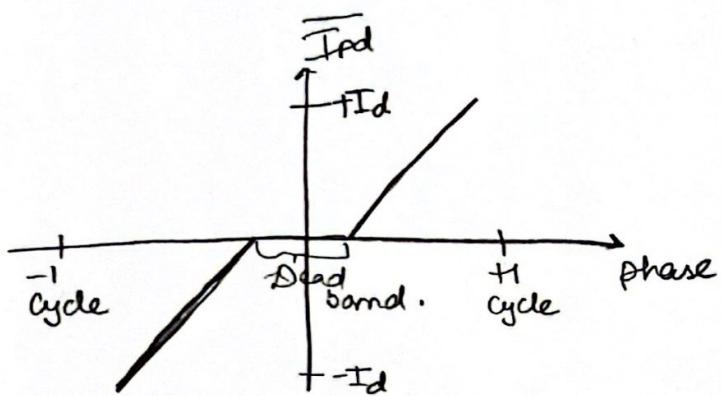




→ Large step input causes large phase error. Too big for XOR PD \Rightarrow cycle slipping. Long capture time (if lucky).

Improvements to PFD

Remember the deadband problem \Rightarrow cannot detect small phase errors.

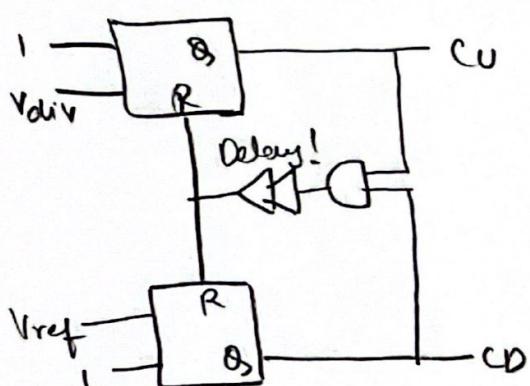


→ A simple solution is to add delay to the reset path!

→ CU & CD both get wider & system has enough time to react!

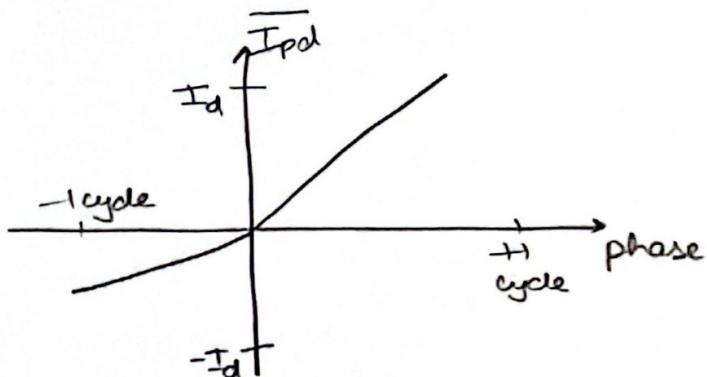
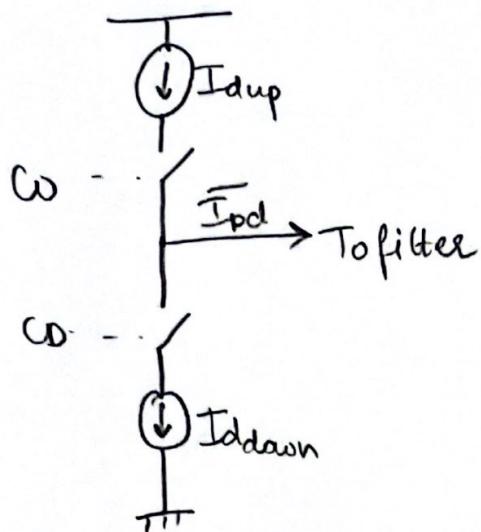
→ Since we subtract CU & CD this delay is removed at output.

→ Delay could be implemented with a few inverters / buffers.



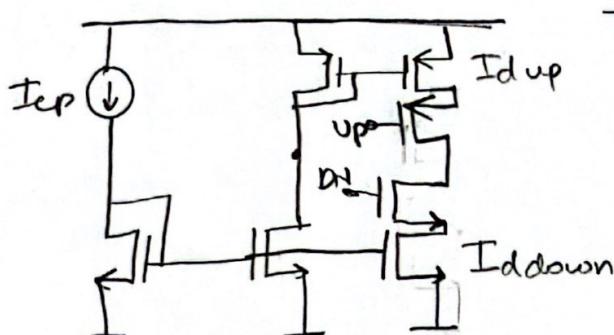
Charge Pump Circuits.

→ $I_{d\text{up}}$ and $I_{d\text{down}}$ should be same! Otherwise we get spur!



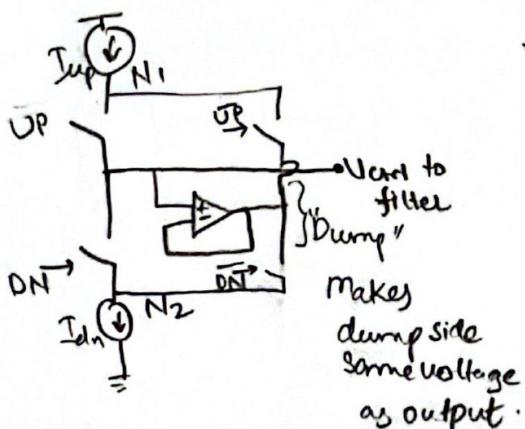
→ K_o is not constant
⇒ Ripples! ⇒ Spurs!

Basic implementation



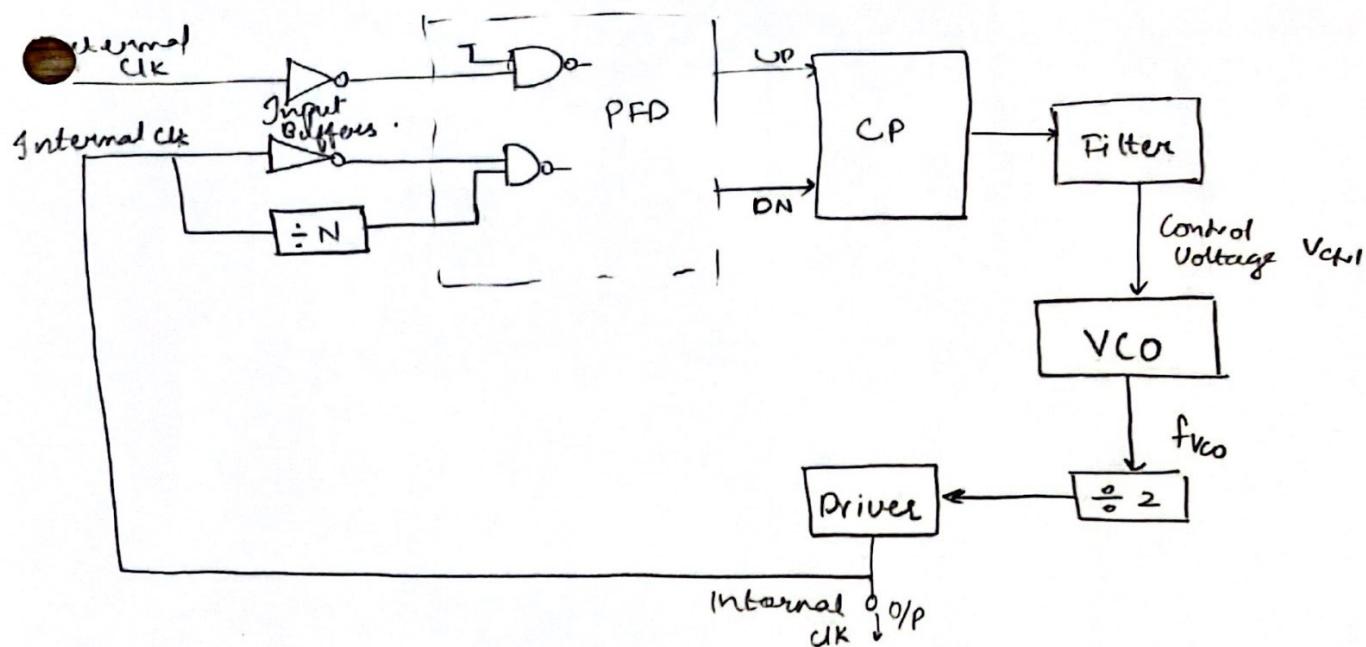
→ Problems?
 → VT mismatch \rightarrow issue
 → CLM mismatch.
 → $\frac{\omega}{L}$ mismatch \rightarrow Not so big

How to ensure both current sources see the same V_p voltage
 Add opamp feedback to match up/down



→ UP & DN are closed \Rightarrow V_{ctrl} is seen by the I_{dn} current source. The buffer is placed so that no current from I_{up} flows into I_{dn} . This way both current sources see same voltage across them at all times \Rightarrow More Stable!

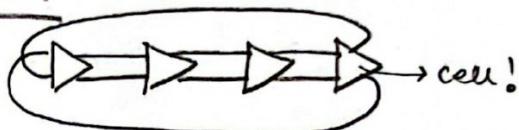
The complete PLL - A sample implementation.



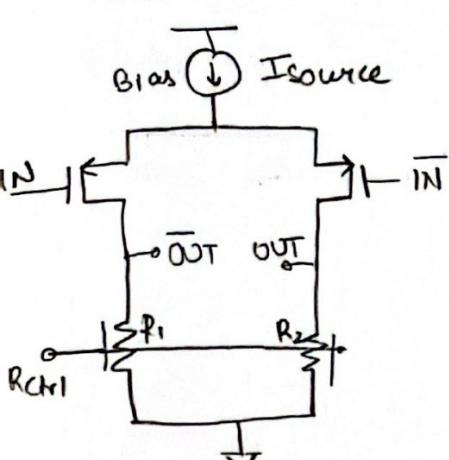
Why use $\frac{1}{2}$? The duty cycle of VCO output may not be 50%, the flipflop used to $\frac{1}{2}$ converts it to a duty cycle of 50% as it only triggers on rising edge!

How is the VCO implemented?

Using a ring oscillator.



Cell architecture



→ The output frequency is a function of cell delay T_d

$$\rightarrow T_d \propto \frac{C * V_{sig}}{I_{source}}$$

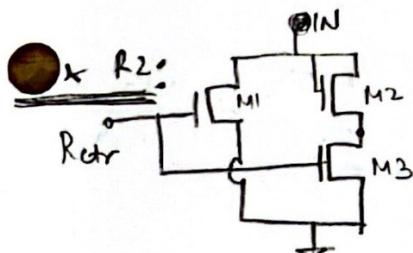
$C \rightarrow$ parasitic cap
 $V_{sig} \rightarrow$ kept constant by adjusting $R_1 \& R_2$

$V_{sig} \rightarrow$ swing.

→ The tail current I_{source} is used to control output frequency.

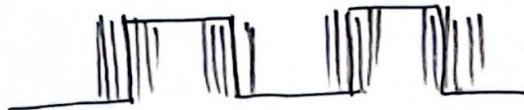
→ $R_1 \& R_2$ are implemented using a diode & a diode connected transistor in parallel

→ Total division is $2N$.



Voltage Controlled Oscillators

What is jitter?



- Random phase errors. Causes timing constraints, especially in clocks.
- Calculated one sigma away from histogram centre.
- Aka phase noise in frequency domain!

Comparison

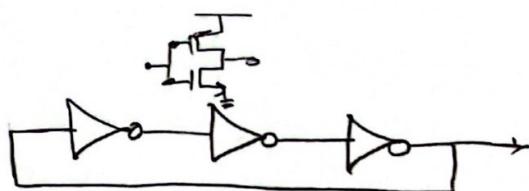
LC

RING

- | | |
|---|--|
| ↔ Tuning range is narrow | ↔ Good tuning range |
| ↔ Large size (coils) | ↔ Small size |
| ↔ Better phase noise for a given power. | ↔ Not so good phase noise
↔ Could make multiple phases based on which section you tap.
↔ Scales with technology. |

Ring oscillators

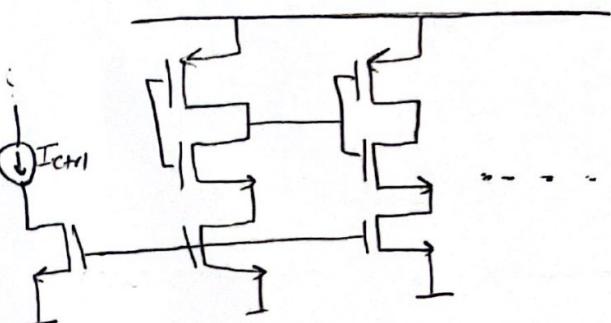
Single ended



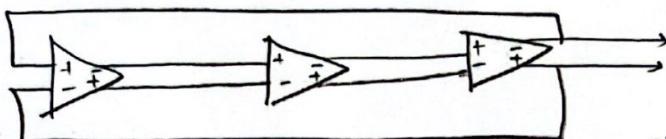
- ↔ Poor power supply rejection ratio (PSRR)
- ↔ Large swing ➔ Better SNR.
- ↔ Flicker noise is a low freq. effect ➔ high in MOSFETs. However it is prominent when it is ON for a long time, here FETs turn off during each cycle ➔ reduced flicker!

Tuning techniques

- > Vary V_{DD}
- > Charge load
- > Current starve $\xrightarrow{\text{charge}} I_{ctrl}$

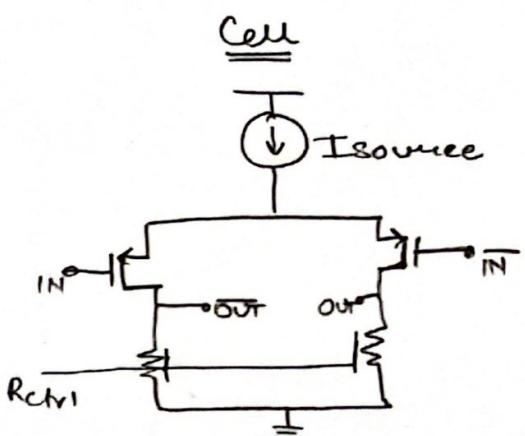


Differential ring oscillators

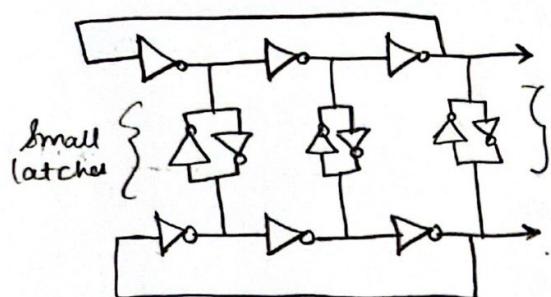


$$T_d \propto \frac{C \cdot V_{DD}}{I_{source}}$$

- ⇒ Small q_p swing due to resistors. $\xrightarrow{\text{phase noise}}$
- ⇒ Always on! \Rightarrow high flicker.
- ⇒ Good PSRR



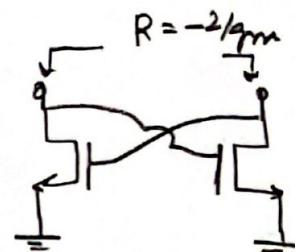
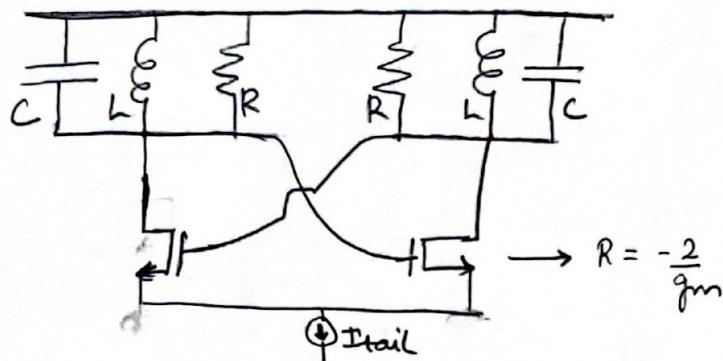
Pseudo differential.



- They couple the two rings to maintain a 180° phase difference at all stages!
- ⇒ Large swing but still differential \Rightarrow Best of both worlds.
- ⇒ Not always on
→ Good PSRR.

LC Oscillators

→ Cross coupled transistor pairs.



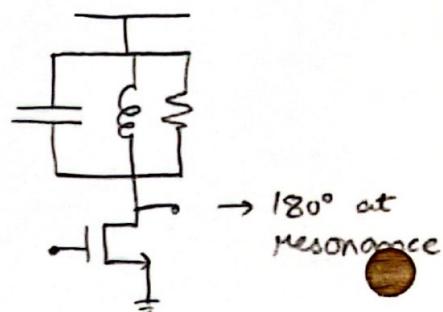
→ Each RLC tank gives 180° phase shift. But we need 2π .
Therefore there are 2 tanks.

→ I_{tail} makes it immune to V_{DD} variation.

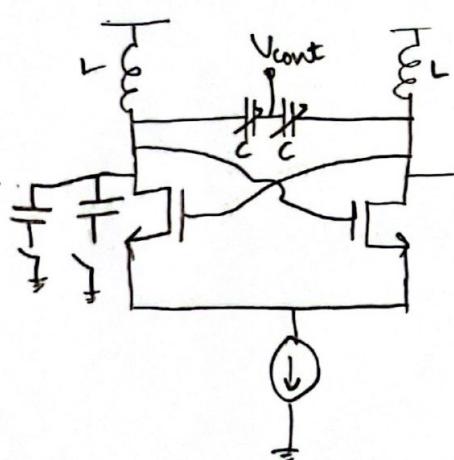
→ Good phase noise rejection!

→ Start up condition $R > \frac{1}{g_m}$

→ How can we improve it? To control oscillation frequency?



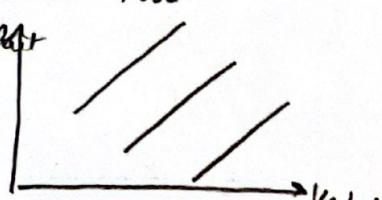
VCO



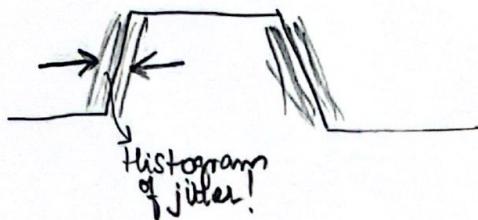
→ Use varactors :- Reverse biased PN junction or MOSFETs in accumulation.

} Switched capacitor banks to extend tuning range! Used for chirp generator in radars!

→ Can be used for coarse and fine tuning of the fosc.

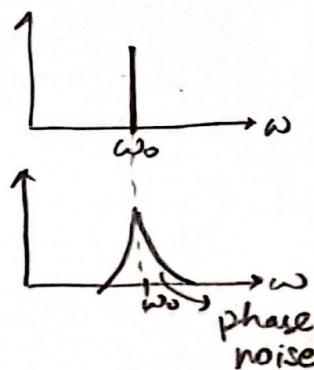


PLL Jitter and Noise



Ideal oscillator

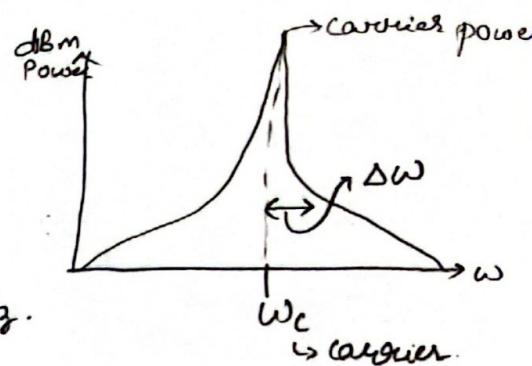
Real oscillator



→ Within the B.W., the VCO need not be great if ref. signal is good because θ/p tracks θ/p(ref) well.

Phase noise

$$L\{\Delta\omega\} = 10 \log_{10} \left\{ \frac{\text{Phase noise}}{P_{\text{carrier}}} \right\} \text{ dBc/Hz.}$$



Take 1Hz $\Delta\omega$ and see how much phase noise power exists w.r.t carrier power. Usually use only one sideband.

Output of PLL $V_{\text{out}}(t) = A \cos(\omega_c t + \phi_n(t))$

↪ Phase noise since ω_c is not perfect.

If noise is small $|\phi_n| \ll 1$

$$A \cos(\omega_c t + \phi_n(t)) \approx \underbrace{A \cos \omega_c t}_{\text{carrier}} - \underbrace{A \phi_n(t) \sin(\omega_c t)}_{\text{Spectrum of } \phi_n \text{ mixed around carrier.}}$$

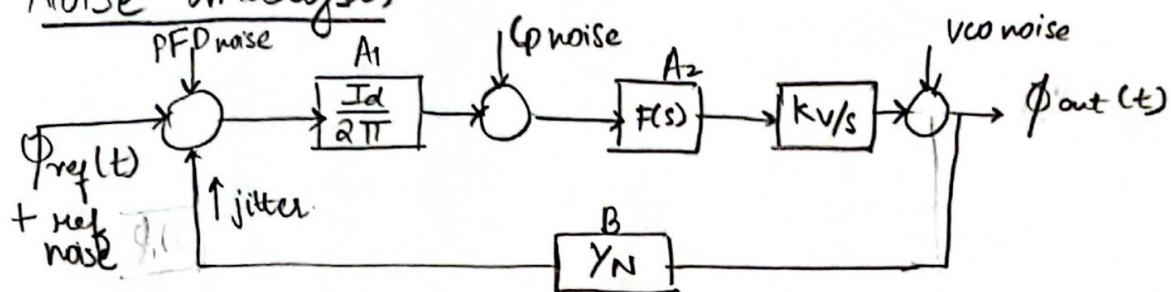
Noise

Sources :- Main :- ① Charge pump noise
② VCO noise

Minor :- ① Reference signal noise
② Divider jitter.

→ Ripple from C.P causes spurs not random noise.

Noise analysis



$$\phi_i(t) = \text{PFD noise} + \text{ref noise} + \text{jitter}.$$

$$\frac{\phi_{out}}{\phi_i} = \frac{(A_1(s) A_2(s))}{1 + A_1(s) A_2(s) B(s)} = \frac{K_D F(s) K_V}{s + \frac{K_D K_V F(s)}{N}}$$

} how pass response
} Gain at low frequency = $\frac{N}{K_D}$
} frequency = N .

$$\frac{\phi_{out}}{\phi_{CP}} = \frac{K_V F(s)}{s + \frac{1}{N} K_D K_V F(s)}$$

} how pass response
} Gain at low frequency = $\frac{N}{K_D}$
} But cannot increase K_D since noise depends on current.

:(Observe that large $N \Rightarrow$ Lots of Noise!!

$$\frac{\phi_{out}}{\phi_{VCO}} = \frac{1}{1 + \frac{1}{N} K_D K_V F(s)}$$

} High pass response (since $F(s)$ is a low pass filter)
} Gets attenuated by VCO if it has a low pass response (L oscillators)

Charge pump noise

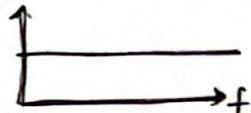
$$\frac{\overline{I_d^2}}{\Delta f} = \frac{4kT}{R} = 4kT\gamma g_{d0}\Delta f$$

$$\gamma \approx 2/3$$

$g_{d0} \sim g_m$ for long channel devices

$$\left. \begin{array}{l} \frac{\overline{I_d^2}}{\Delta f} \propto g_m \\ \Rightarrow \frac{\overline{I_d^2}}{\Delta f} \propto I_d \end{array} \right\} \begin{array}{l} \text{Recall gain at low frequency} = N/k_0 \\ \text{Where } k_0 = \frac{I_{cp}}{2\pi} \end{array}$$

$$\text{Noise out}^2 \propto \left(\frac{N}{k_0} \right)^2 \frac{1}{\frac{I_{cp}}{\Delta f}} \propto \frac{N^2}{I_{cp}^2} \cdot I_{cp} \propto \boxed{\frac{N^2}{I_{cp}}}$$



Charge pump noise is spectrally flat.

Large $N \Rightarrow$ More CP noise goes to opamp

Large $I_{cp} \Rightarrow$ low noise!

VCO noise

$$2\{\Delta\omega\} = \frac{P_{phaser}}{P_{sig}} = \frac{2kT}{P_{sig}} \left[\frac{\omega_0}{2Q\Delta\omega} \right]^2 \rightarrow \begin{array}{l} \text{High } Q \Rightarrow \text{noise is low} \\ \text{offset frequency.} \end{array}$$

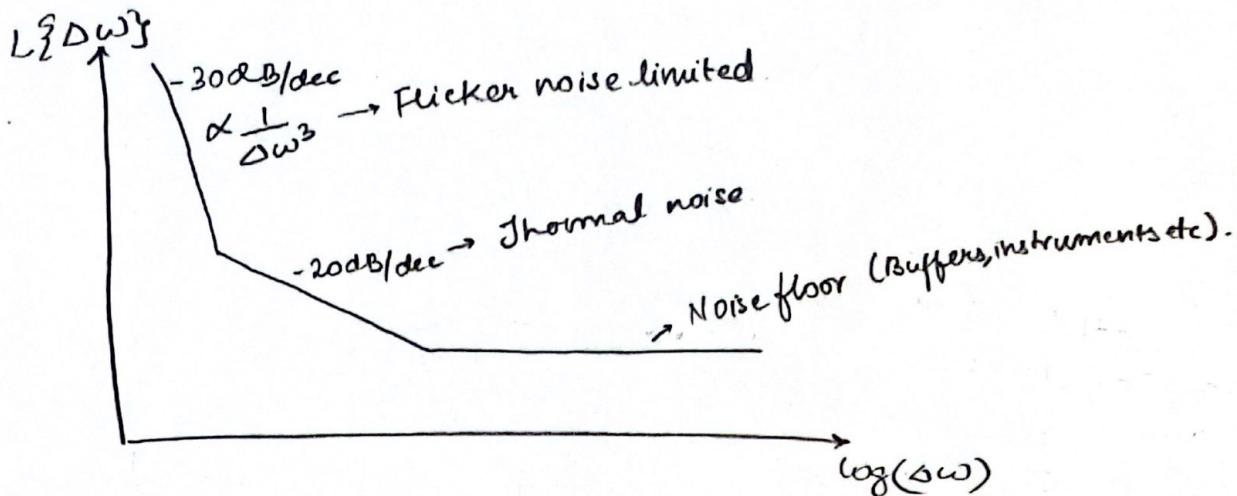
In log

$$2\{\Delta\omega\} = 10 \log_{10} \left\{ \frac{2kT}{P_{sig}} \cdot \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \right\} \rightarrow \text{Slope of } -20 \text{ dBc/dec}$$

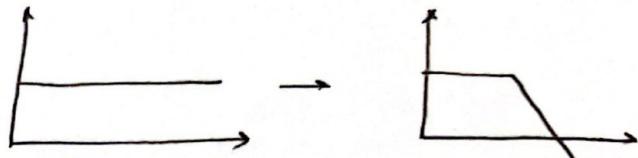
This gives the noise power at a frequency $\Delta\omega$ from the centre/carrier frequency.

→ High ω_0 for some $\Delta\omega$ gives more noise.

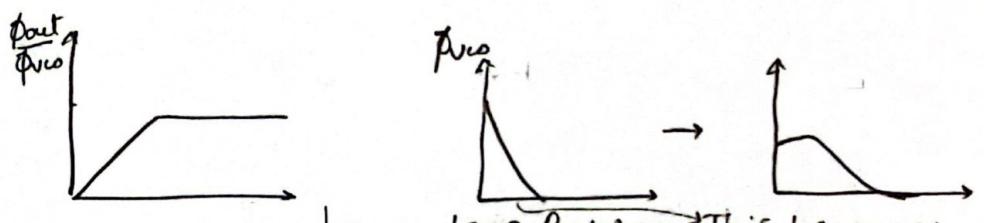
LC oscillator noise plot!



→ Reference noise, divider noise and CP noise are white. They get shaped by LPF.

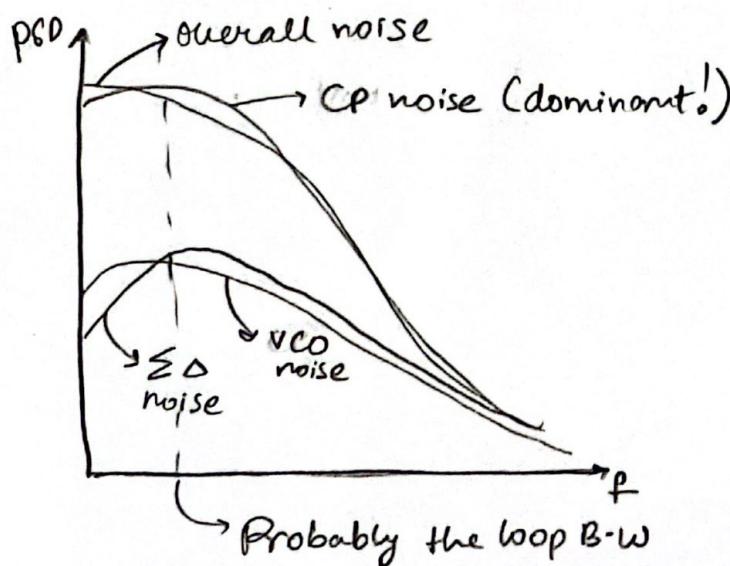


→ VCO noise is high frequency noise and is attenuated by VCO response.



lower loop B-W \Rightarrow This becomes wider & more VCO noise goes to O/P

Overall response



Bandwidth tradeoffs

High loop BW

- + Faster PLL
- + lower VCO noise
- Other noises are higher

lower loop BW

- + Less CP & Ref noise
- More VCO noise
- Slower!

Fractional N PLLs

37

→ When we need small step sizes at large frequency

Example: Local oscillator for GSM:-

① 900 MHz with 200 kHz bands.

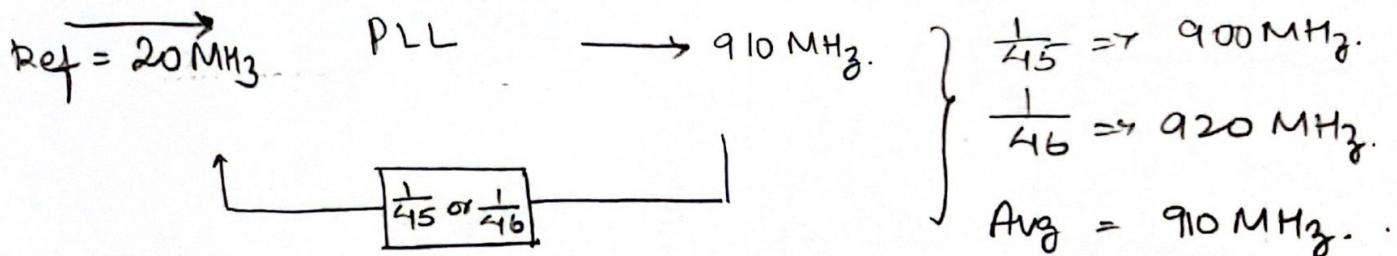
Integer N : ⇒ Reference @ 200 kHz and $N = 4500!$

$$\text{PLL BW} = \frac{1}{10} \text{ th of Ref. freq.}$$

Drawbacks

- ① PLL BW = 20 kHz. → SLOW
- ② $N = 4500$ $\left(\frac{N^2}{I_{cp}} \right)$ → NOISY

Solution:- Large reference frequency & Fractional N.



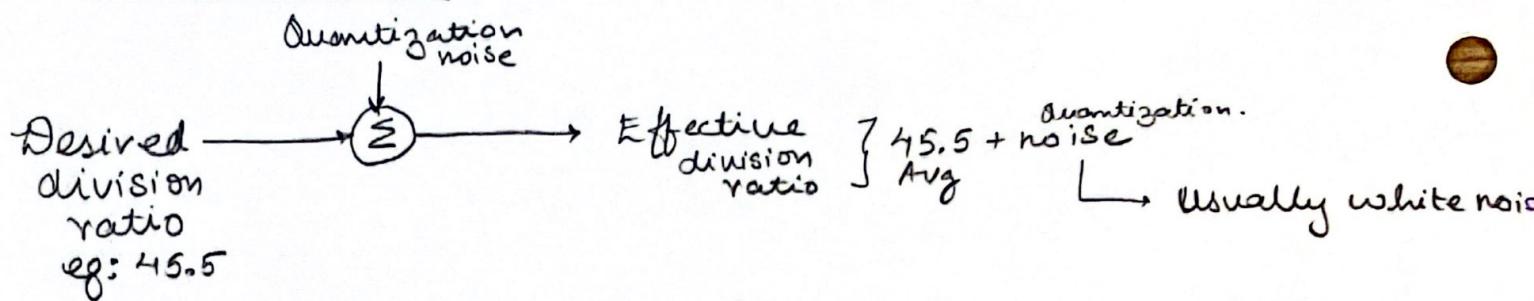
→ On average divide by 45.5 → 910 MHz.

→ If the division ratio is half ⇒ spurs! at the output

→ To avoid this we use a random division ratio. This removes spurs but introduces quantization noise.

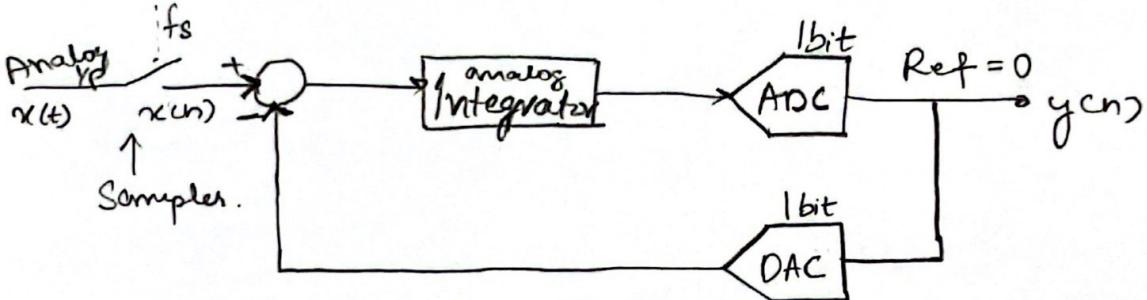
Divider	45	45	46	45	46	46
Error	-0.5	-0.5	+0.5	-0.5	+0.5	+0.5

Divider model



→ How do we attenuate this quantization noise?
 Move it to high frequencies where the loop BW rejects it.
 But how? Use a $\Sigma\Delta$ modulator.
 Called noise shaping!

$\Sigma\Delta$ Modulator



Input x has range -1 to +1

$$x=0 \Rightarrow y = 0, 1, 0, 1, 0, 1, \dots \text{ Avg } y(t) = 0.5$$

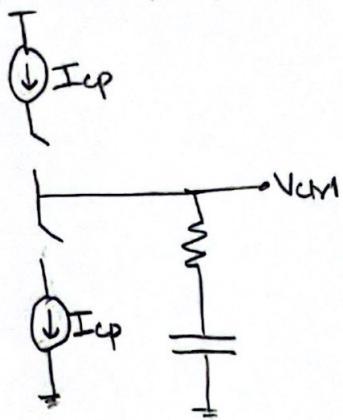
$$x=0.5 \Rightarrow y = 0, 1, 1, 1, 0, 1, 1, 1, \dots \text{ Avg } y(t) = 0.75$$

- Therefore with the proper x value we can get fractional outputs.
- The integrator is only there for noise shaping. More integrators in cascade ⇒ better shaping.
- $u(n)$ is the control word.

Digital PLLs (from IITM lectures)

call Analog PLLs

charge pump



$$\frac{V_{ctrl}}{I_{cp}} = R + \frac{1}{SC}$$

Integrating current over the cap.

Disadvantages
 → Large capacitors!
 → Process variation
 Implement the TF $\frac{V_{ctrl}}{I_{cp}}$ in digital

$$V_{ctrl}(\bar{n+T}) = V_{ctrl}(nT) + \frac{1}{C} \int_{nT}^{\bar{n+T}} i_{cp} dt$$

○ L constant!

$$\Rightarrow V_{ctrl}(\bar{n+T}) = V_{ctrl}(nT) + \frac{i_{cp}}{C} \Delta t(n)$$

↑ phase error at nth reference clock.

$$= V_{ctrl}(nT) + \frac{i_{cp}}{C} \cdot \frac{2\pi \Delta t(n)}{T} \cdot \frac{T}{2\pi}$$

$$= V_{ctrl}(nT) + \frac{i_{cp}}{C} \cdot \frac{T}{2\pi} \cdot \phi_e(nT)$$

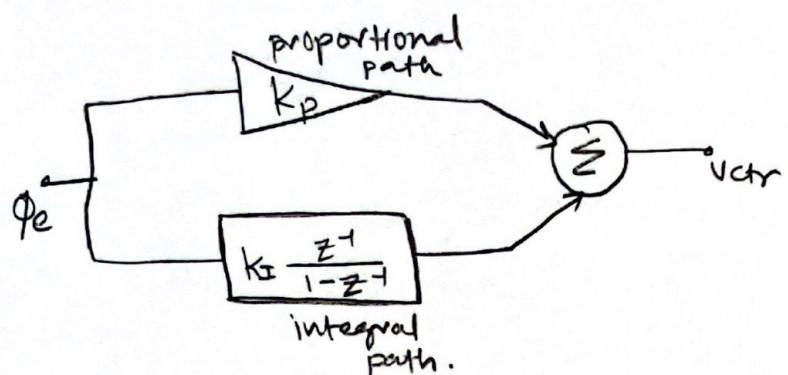
$$\therefore V_{ctrl}(\bar{n+T}) = V_{ctrl}(nT) + \frac{i_{cp}}{C} \cdot \frac{T}{2\pi} \cdot \phi_e(nT) \quad ①$$

Can be implemented digitally.

$$z V_{ctrl}(z) = V_{ctrl}(z) + \frac{i_{cp}}{C} \cdot \frac{T}{2\pi} \cdot \phi_e(z)$$

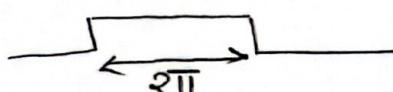
$$\left[\frac{V_{ctrl}(z)}{\phi_e(z)} = \frac{i_{cp} \cdot T}{C \cdot 2\pi} \cdot \frac{1}{z-1} \right] = k_I \cdot \frac{z^{-1}}{1-z^{-1}}$$

→ You could just apply a bilinear transformation to the continuous time transfer function with replacing S by $\frac{2}{T} \cdot \frac{1-z^{-1}}{1+z^{-1}}$ and we would arrive at the discrete time transfer function.



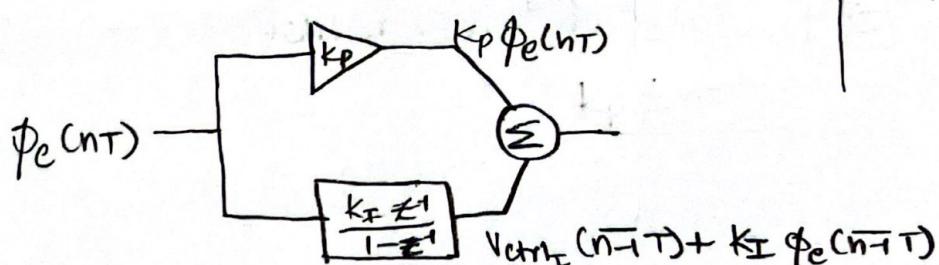
$$\frac{V_{ctrl}(z)}{\phi_e} = K_p + \frac{K_I z^{-1}}{1 - z^{-1}} \quad \text{Choose } K_p, K_I \text{ to replicate the earlier T.F}$$

→ ϕ_e : needs to be a number of bits.



Let's say 4 bits:
 0 rad/s → 0000
 2π rad/s → 1111

→ K_p also needs to be digital.
 Say K_p is 2 bits.
 \Rightarrow gain can be 0 → 3.
 Same goes for K_I .
 \rightarrow If $K_p = 10 \Rightarrow$ gain of 2
 we need to left shift by 1.
 $\Rightarrow 1111 \times 10 = 1110$



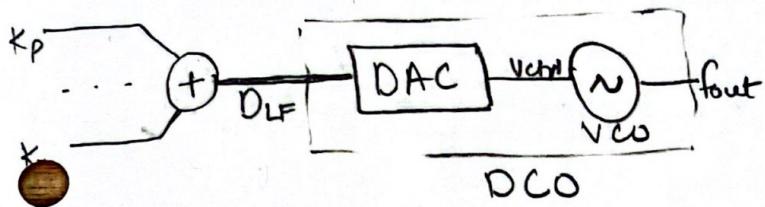
from eq ①

$$\frac{V_{ctrl}}{\phi_e} = k_p + \frac{k_I z^{-1}}{1-z^{-1}} = k_p + \frac{k_I}{z-1} = k_p + \frac{k_I}{e^{sT}-1} = k_p + \frac{k_I}{s} \xrightarrow{\text{Taylor}} T = \frac{1}{fref}$$

$$= \frac{1}{s} \left[s k_p + k_I fref \right] = \frac{k_I fref}{s} \left[1 + \frac{s k_I}{k_I fref} \right]$$

$$\boxed{\omega_z = \frac{k_I \cdot fref}{k_p}}$$

→ How do we use this digital o/p word to control the VCO.
We can use a DAC.



$$K_{VCO} : V_{CM} \rightarrow f_{out}$$

$$K_{DCO} : D_{LF} \rightarrow f_{out}$$

$\phi_e \rightarrow f_{out}$

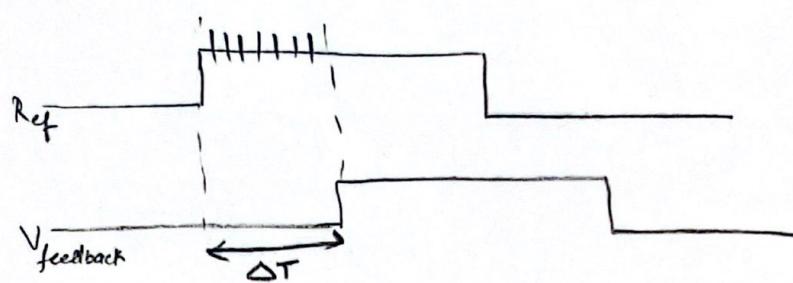
$$\text{Loop gain} = \left[k_p + \frac{k \cdot z^{-1}}{1-z^{-1}} \right] \frac{2 \cdot K_{DCO}}{s} \cdot \frac{1}{N}$$

$\downarrow \text{Divider}$

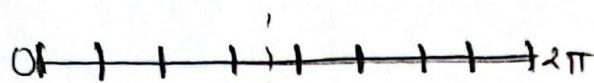
How do we get a digital representation of the phase error?

- PFD gives us $[2\pi, 2\pi]$ $\xrightarrow{\text{Digital}}$ To represent the -ve phase errors use
4 bits $\times \times \times \times$ signed bits or 2's C → $0 \rightarrow 2\pi$
 $0000 \rightarrow 0111$
 $-2\pi \rightarrow 0$
 $1111 \rightarrow 0000$
- Need to consider signed multiplication when using with rest of the circuit.

But how do we do it? Time to digital converters.

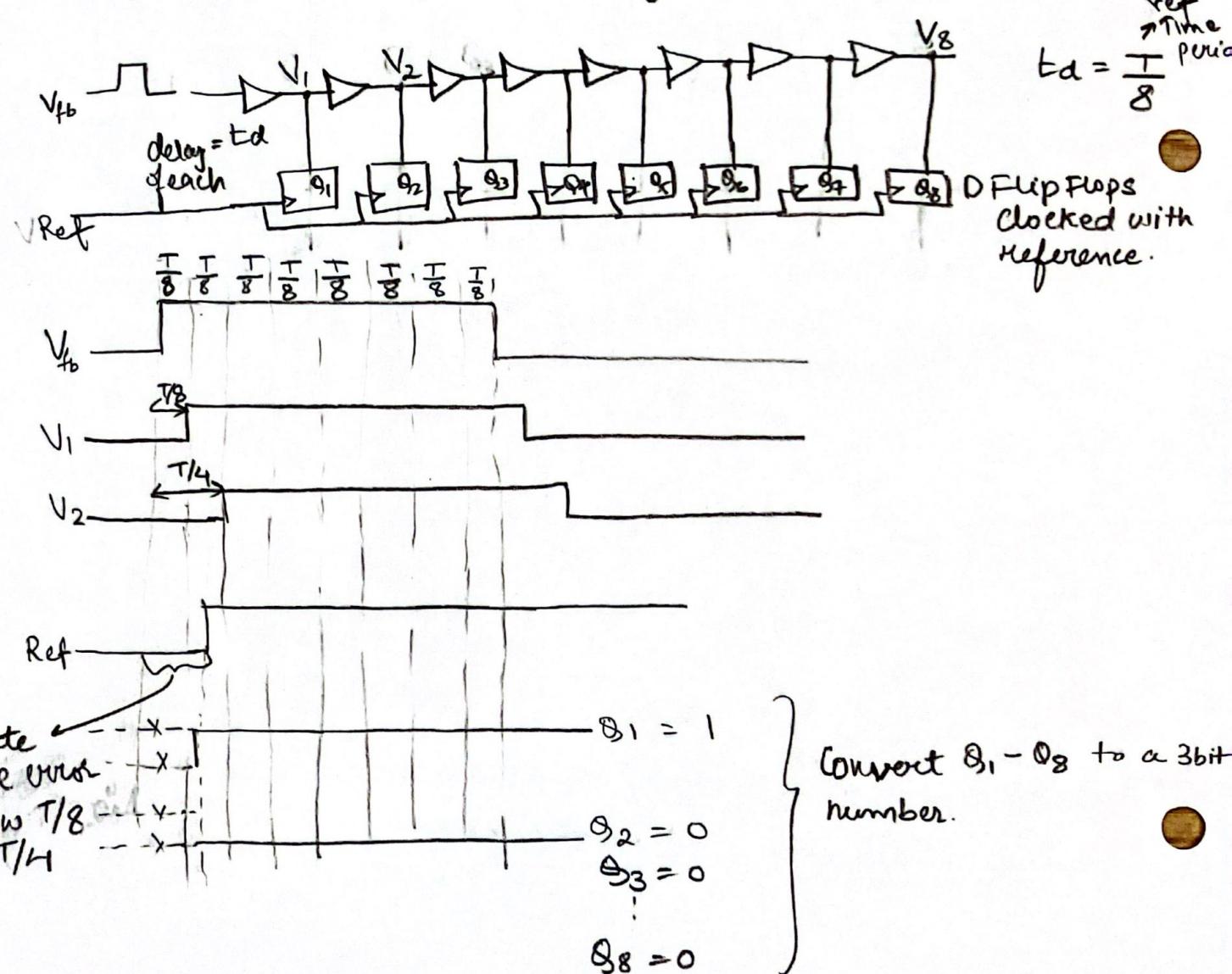


→ only 3 bits to represent phase error.
⇒ 8 levels.



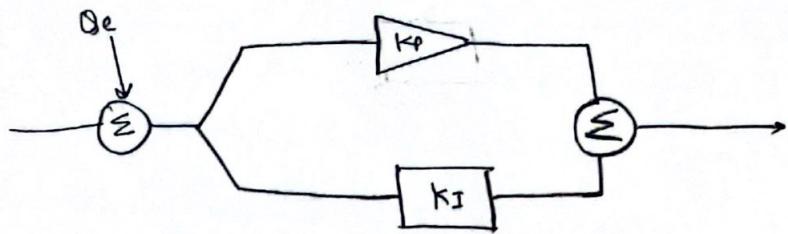
$\Phi_e \rightarrow$ if phase error falls here → Quantization error.

→ For 8 levels we use 8 delay elements (minimum)



- Quantization error is $-\frac{td}{2} < \Delta < \frac{td}{2}$
- $td \downarrow \Rightarrow$ more no. of delay cells. Inverter delay in 180nm process is around 50ps. This is the minimum.
- $td \uparrow \Rightarrow$ high quantization noise at the PLL input.
This noise can be assumed to be white & varying from $-\Delta/2$ to $\Delta/2$
- Spectral density of TDC quantization noise is $S_{TDC,q}$
- $$S_{TDC,q} = \frac{\Delta^2}{12} \quad \text{where } \Delta \text{ is } td \text{ in phase}$$
- $$\Rightarrow \frac{2\pi \cdot td}{T}$$
- $$S_{TDC,q} = \frac{(2\pi \frac{td}{T})^2}{12 \cdot f_{ref}} = \frac{(2\pi td)^2}{12 \cdot T}$$
- Spread over f_{ref}
- Here f_{ref} is usually low frequency (in MHz), $\frac{1}{f_{ref}}$ is usually much larger than td .
- If no. of cells is large, the delay of each cell may vary (mismatch) - Causes errors. Also power consumption is high.
- TDC q. noise demands $\downarrow BW$ } Plays the role of CP noise.
VCO Noise demands $\uparrow BW$

→



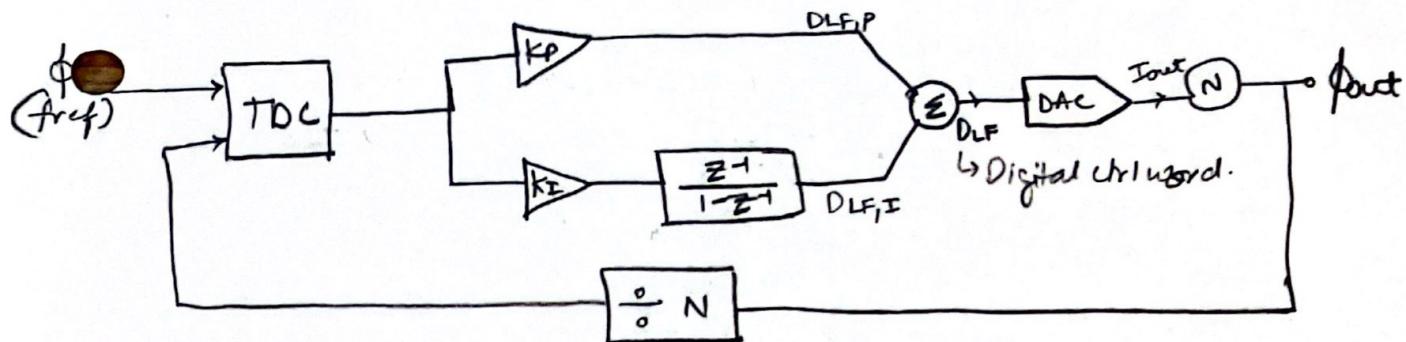
→ θ_e is added before the PI path. Most of it is carried by the K_p path because the K_I path has a low pass response. Solution?

→ Hybrid Digital PLL

Implement proportional path in analog and integral path in digital.

Digital PLL

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In steady state kind of an assumption.

DLF, I is fixed (Avg. value is fixed)

DLF, P varies at fref
 ↳ if this is constant
 ↳ there is no phase error



$$I = P(I_{LSB})$$

↳ some digital value of DAC.

Since kp is not constant and the TDC is never fully locked due to error, the output frequency is not constant

$$V_{out} = \sin(\omega_0 t + K_{vco} \int i_{out} dt) \quad \text{varying!}$$

$$I_{out} = P(I_{LSB})$$

$$\text{Considering only proportional path.} \quad = (\underbrace{\pm TDC_{LSB}}_{\text{quantization error}}) \times k_p \times I_{LSB}$$

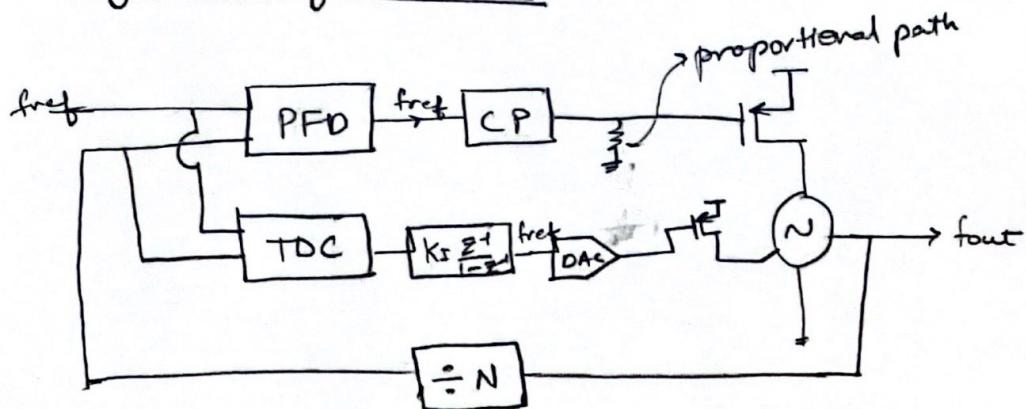
→ How do we reduce this error? → aka reference spur.

Need to reduce I_{LSB} ⇒ Need larger no. of bits in DAC. ⇒ Area ↑ which is the problem which we tried to solve, and building such a DAC is difficult

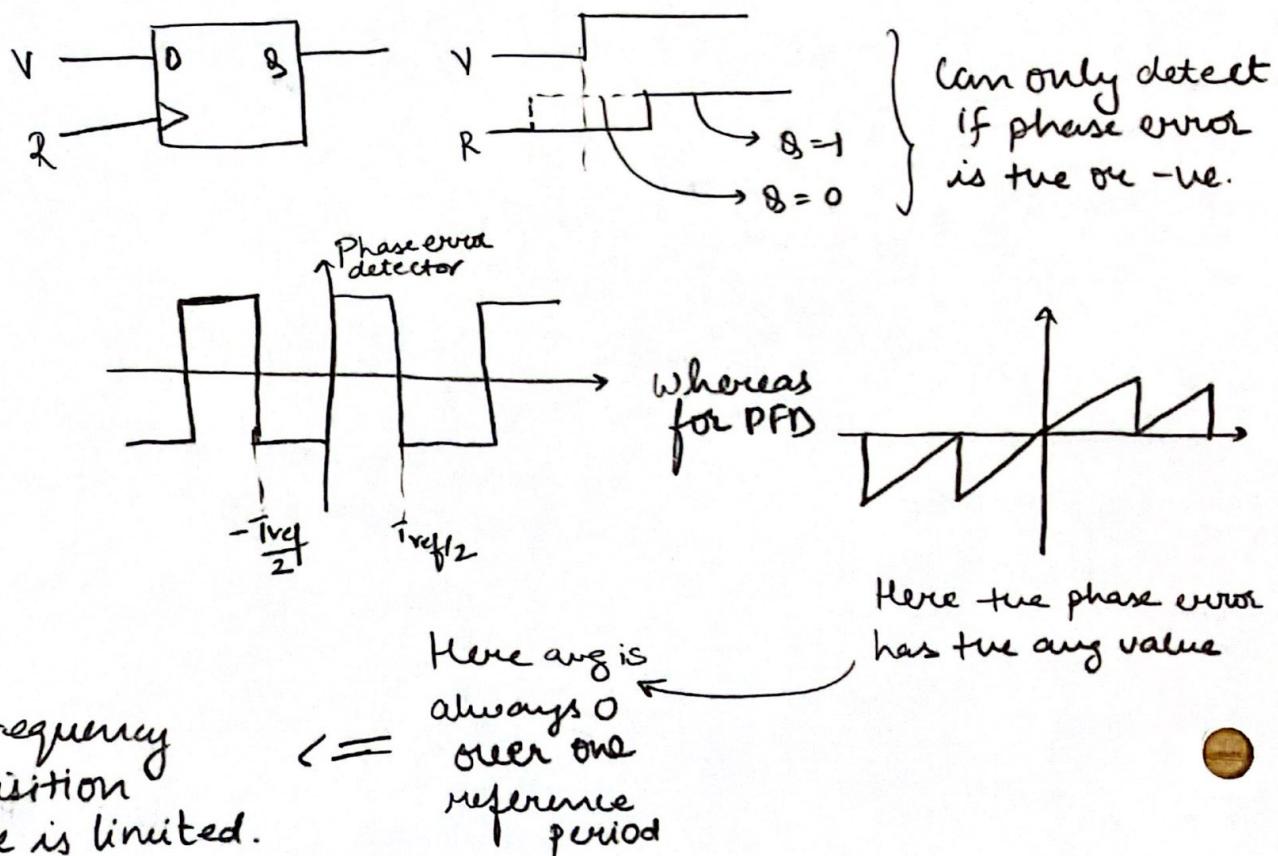
→ Could use a filter to get rid of the ref. spur after DAC. This ↑ area!

→ So really the benefit is scalability, maybe not area.

Hybrid digital PLL

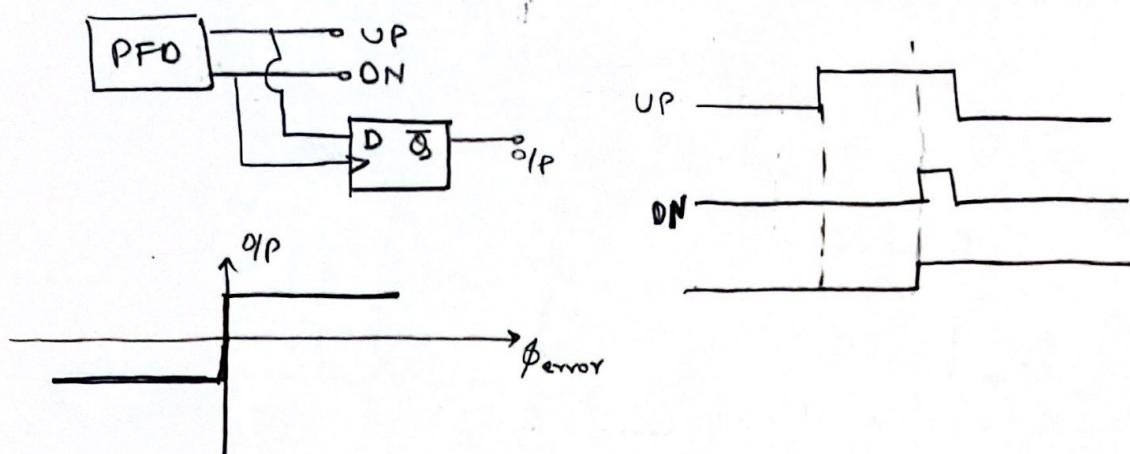


- Need to be synchronized otherwise we get lot of spurs.
- Digital path still has quantization noise.
 - fine resolution → # delay cells ↑
 - coarse resolution → quantization noise ↑
- How coarse can we go? Use just a 1 bit TDC

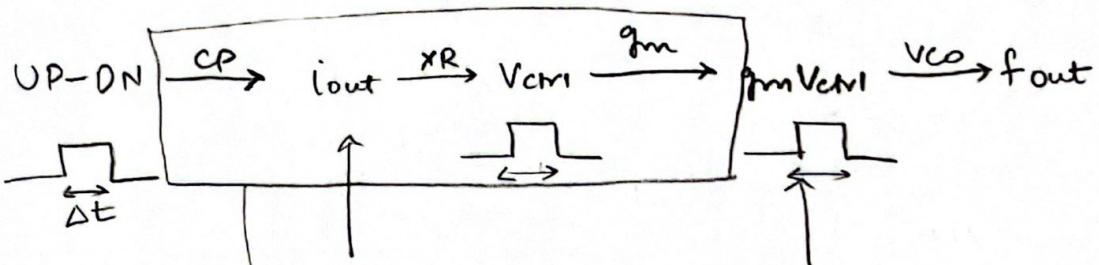
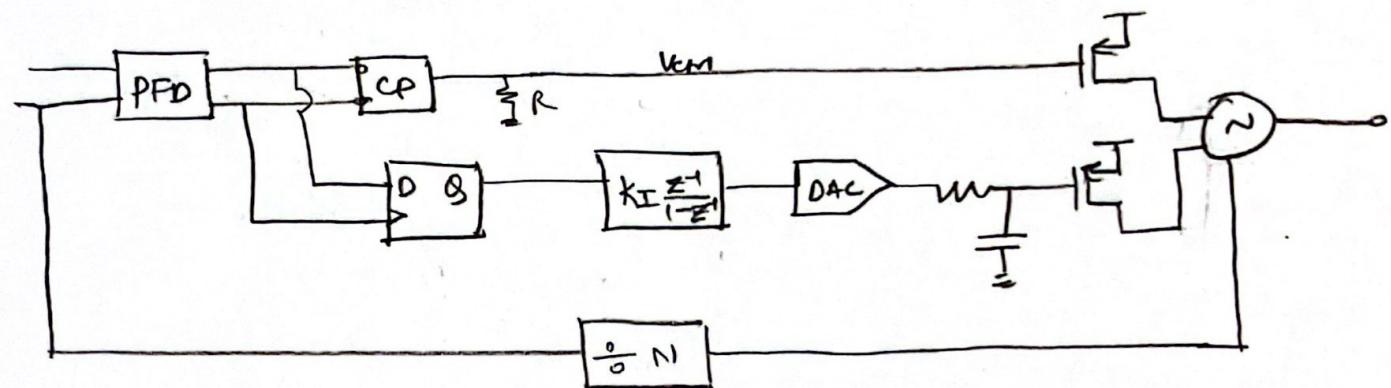


Also quantization noise is higher!

→ If we just want to know the phase error sign (+ve or -ve) we could just use the UP + DOWN signals from the PFD.



How does the PLL look?



These two are currents.

So can we get rid of this? Perhaps

$I_{\text{cp}}^{\text{UP}}$

I_{bias}

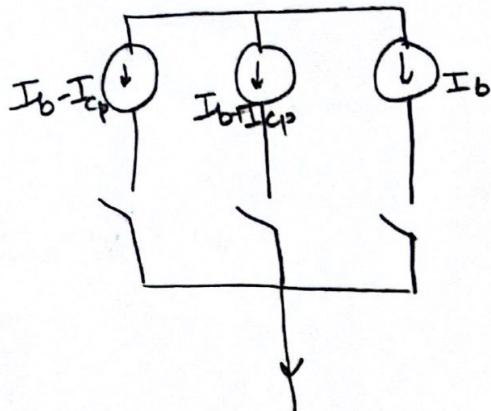
I_{out}

$I_{\text{cp}}^{\text{DN}}$

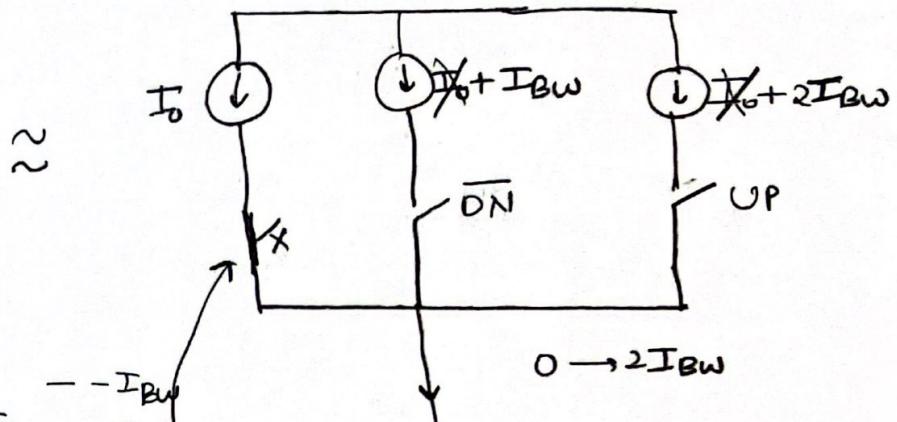
To increase freq. push current in, to reduce freq. pull out current. If both currents are equal Prop-path provides no current. To keep the oscillator at some nominal freq.

I_{out} → I_{bias}
 I_{out} → $I_{bias} + I_{cp}$
 I_{out} → $I_{bias} - I_{cp}$

} 2 are NMOS and 1 is PMOS.
 Mismatch issues !!
 Let's make all 3 as PMOS.



range is $2I_{cp}$
 $-I_{cp} \rightarrow +I_{cp}$

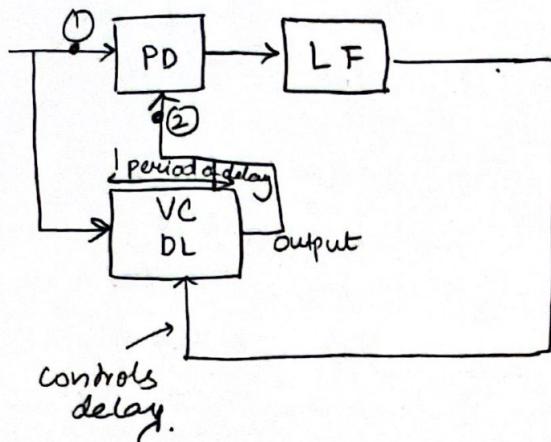
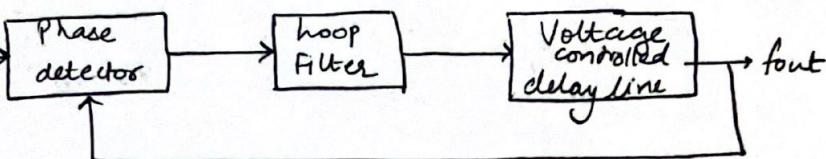


$$\begin{aligned}
 I_0 &= -I_{BW} \\
 I_0 + I_{BW} &= 0 \\
 I_0 + 2I_{BW} &= +I_{BW}
 \end{aligned}$$

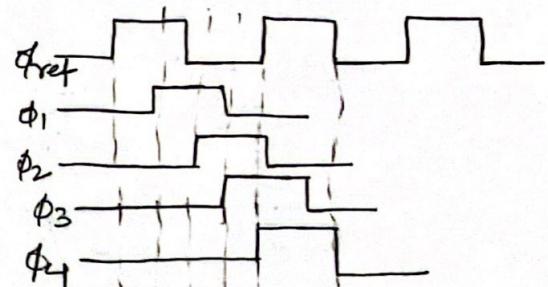
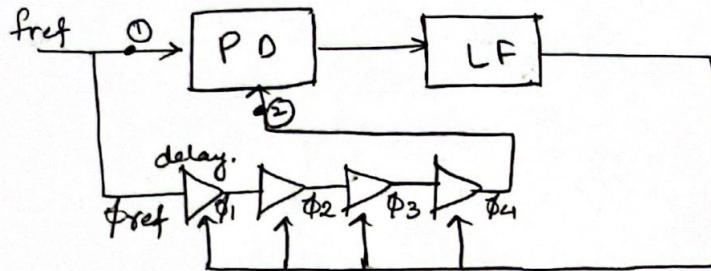
range is $2I_{BW}$. Since I_0 is always there we can remove that switch! & remove I_0 from other sources

→ Could use only PMOS and 2 switches instead of 3.

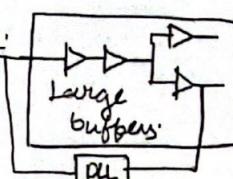
Delay locked loops



- > ① & ② are one period apart. Their edges are locked.
- > Delay through VCDL is locked to one period of ref clock.

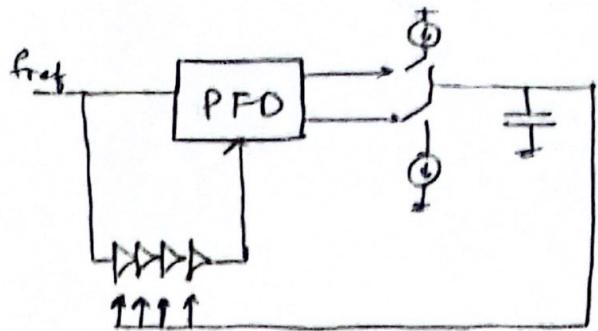


- > ϕ_{ref} & ϕ_4 are locked in phase by the feedback loop.
- Uses ① Clock multiplication (not popular) → Combine multiphase clocks to get a faster clock.
- ② Serial links. → use quarter rate clock.
- ③ Clock distribution. ckt.



Put clk buffer in DLL to ensure phase of buffered clock.

Practical DLL System



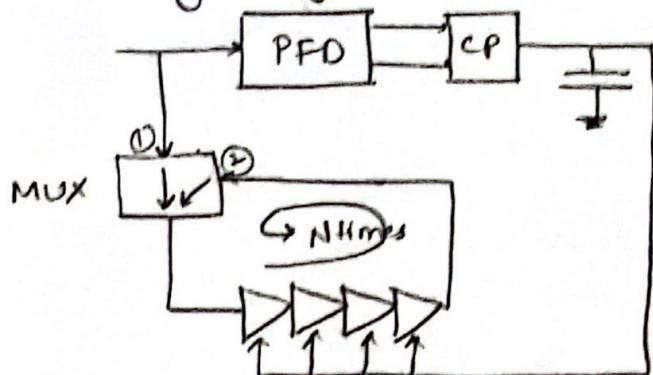
- > Very simple loop filter.
- > No integration in delay line since no VCO.
- + DLL is easy to implement
No VCO \Rightarrow no $\frac{1}{f}$ from VCO
- + DLL does not accumulate jitter.
- No filtering of fref.
- Total delay is controlled but not the individual delays of each buffer: individual delay mismatch
- Harmonic lock problem.



Harmonic lock problem

Solution: Foley & Flynn JSSC 2002 paper.

Recycling DLL (PLL & DLL hybrid)



- > The MUX switches from (1) to (2) and lets the delay build up before comparing & locking
- > Effective delay decreases by N
- > Smaller delay line does the job of a longer delay line.
- > Smaller mismatch due to barrel shifting.
 \Rightarrow mismatch shaping.