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Paper Code: TCS-403

Back Odd End Semester Examination 2024*Name of the Course: B.Tech.**Semester: 4**Name of the Paper: Microprocessors**Paper Code: TCS-403**Time: Three Hours**Maximum Marks: 100***Note:** (i) All the questions are compulsory.

(ii) Attempt any 2 sub-parts from a, b, c option given below.

Q1	(10X2=20 Marks)	CO1/CO2
(a)	With suitable diagram, explain how the Address/Data bus (AD0-AD7) of 8085 microprocessor is de-multiplexed.	
(b)	Differentiate between memory mapped I/O and I/O mapped I/O	
(c)	Draw the architectural diagram of 8085 microprocessor and list out the following (i) General Purpose Registers (ii) Special Purpose registers with their functions (iii) Flags in the flag register with required explanation	
Q2	(10X2=20 Marks)	CO2/CO1
(a)	What are vectored interrupts? How is the address of the Interrupt Service routine calculated in vectored interrupts? Explain with an example.	
(b)	Explain the purpose of the following signals in 8085 (i) READY (ii) AD0-AD7 (iii) HOLD (iv) IO/ M (v) INTR	
(c)	What is an addressing mode? With suitable example, explain any 4 addressing modes in 8085.	
Q3	(10X2=20 Marks)	CO3/CO2
(a)	Draw and explain the architectural diagram of 8086 microprocessor	
(b)	Define logical and effective address. Describe physical address generation process in 8086. Calculate physical address by taking suitable DS, CS and IP.	
(c)	Describe any two Rotate instructions with example. Write an ALP to divide two 8 bit signed numbers.	
Q4	(10X2=20 Marks)	CO3/CO4
(a)	What is the difference between Mode 0, Mode 1 and Mode 2 operations of 8255?	
(b)	Define stack? What are subroutine? Give some ex of input devices to microprocessor-based systems	
(c)	What is DMA? Which hardware pins are used for DMA control? Draw and	

	explain the architecture of DMA controller.	
Q5	(10X2=20 Marks)	
(a)	What is an USART. Draw the functional block diagram of it.	CO3/CO4
(b)	What are the different types of ADC? Differentiate between ADC and DAC.	
(c)	Draw and explain the functional block diagram of 8259 Programmable interrupt controller.	