Graphic Era HILL UNIVERSITY
Established by an Act of the State Legislature of Uttarakhand (Adhiniyam Sankhya 12 of 2011)
University under section 2(f) of UGC Act, 1956

End Term (Even) Semester Examination May-June 2025

Roll no.....

Name of the Program and semester: BCA, 4th Semester
Name of the Course: Computer Organization
Course Code: TBC 403

Time: 3 hour

Maximum Marks: 100

Note:

(i) All the questions are compulsory.
(ii) Answer any two sub questions from a, b and c in each main question.
(iii) Total marks for each question is 20 (twenty).
(iv) Each sub-question carries 10 marks.

Q1.	(2X10=20 Marks)	
a	Define computer organization and explain its importance in the design and operation of a computer system. Illustrate with an example how computer organization influences system performance.	CO1
b	Discuss the evolution of computers, categorizing them into different generations. For each generation, highlight the key technological advancements and their impact on computer performance.	CO1
c	Describe the main components of a computer system (CPU, memory, I/O devices, storage) and explain the role of each component in the overall functioning of the system.	CO1
Q2.	(2X10=20 Marks)	
a	Explain the fetch-decode-execute cycle. Illustrate each stage with an example and discuss how this cycle is critical to the functioning of a CPU.	CO2
b	Describe the various types of registers found in a CPU. Explain the function of each type of register with examples.	CO2
c	Draw and explain the 4-bit arithmetic micro-operation circuit.	CO2
Q3.	(2X10=20 Marks)	
a	Explain the concept of memory hierarchy and discuss its impact on the overall performance of a computer system.	CO3
b	What are the different cache memory organization techniques? Explain how each technique works and the advantages and disadvantages of each.	CO3
c	What is virtual memory? Discuss its significance in modern computing systems. Explain the mechanisms behind virtual memory management, such as paging and segmentation.	CO3
Q4.	(2X10=20 Marks)	
a	Explain the significance/need of I/O interfacing circuit for data communication between CPU and memory/peripherals. Write five differences between Isolated I/O and Memory mapped I/O.	CO4
b	Explain Direct Memory Access (DMA) in detail along with block diagram.	CO4

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c	Write a short note on handshaking and Strobe pulse.	CO4
Q5.	(2X10=20 Marks)	
a	Explain difference between RISC and CISC architecture.	CO5
b	Explain the concept of memory addressing modes. Describe the different addressing modes and give examples of how each mode is used in instruction execution.	CO5
c	Explain the concept of pipelining in processors. Describe the different stages of pipelining and discuss how pipelining increases the throughput of a processor.	CO5