(c) Explain how Tomasulo's algorithm can be used to implement register renaming and operand forwarding. (CO4)

5. (a) Explain in detail the symmetric shared memory architectures with reference to multiprocessor cache coherence problem. (CO5)

(b) Explain in detail the distributed shared memory architecture highlighting the directory-based cache coherence protocol. Substantiate your explanation with suitable examples and state diagrams ? (CO5)

(c) Write the differences between of the following : (CO5)

(i) Message Passing and Shared Memory

(ii) Linear and Non-Linear pipeline

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TCS–704

B. TECH. (CSE) (SEVENTH SEMESTER) END SEMESTER EXAMINATION, Dec., 2023

ADVANCED COMPUTER ARCHITECTURE

Time : Three Hours

Maximum Marks : 100

Note : (i) All questions are compulsory.

(ii) Answer any ***two*** sub-questions among (a), (b) and (c) in each main question.

(iii) Total marks in each main question are **twenty**.

(iv) Each sub-question carries 10 marks.

1. (a) Explain in details the taxonomy of Flynn's Classification. (CO1)

(b) State and explain Amdahl's law for speedup performance. (CO1)

(c) Explain various performance metrices and evaluation measures for the performance of processor. (CO1)

2. (a) What is hit ratio ? Explain the term locality of reference ? How is it used to improve the performance of cache memory. (CO2)

(b) A system is employed with 2-levels of memory. The average access time without level-1 is 150ns and with level-1 is 30ns. The level-1 access time is 20ns. (CO2)

(i) Calculate Hit ratio.

(ii) If hit ratio is made to 100%, what will be the access time of level-1 and level-2 memories ?

(c) Consider a 4-way set associative cache with 16 cache blocks, the main memory blocks requests are in the order (0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92. 155). Calculate Hit ratio and Miss ratio of the cache if LRU replacement policy is used. (CO2)

3. (a) Explain the concept of control dependence with an example. With what problem a pipeline may suffer if a control dependence is there ? (CO3)

(b) What are pipeline stalls and their effect on the utilization of pipeline ? A non-pipelined system takes 50 ns to process a task. The same task can be process in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup and efficiency of the pipeline for the 100 tasks. What is the maximum speed-up that can be achieved ? (CO3)

(c) Discuss various performance issues and Hazards of pipelining. (CO3)

4. (a) Explain RAW and WAW dependencies and also discuss various measures to overcome these dependencies. (CO4)

(b) Discuss in brief the difference between local and global branch prediction strategies, and how two-bit selector may be used per branch to select between the two. (CO4)