Electronics Workshop – II

Audio Amplifier Report

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In loving memory of:

- 3x 2N7000 NMOS
- 2x IFR9540N PMOS
- Unknown number of Resistors and Capacitors.

Objective

We are to design an audio amplifier using the MIC as a source of input and output the signal to drive a 8Ω speaker. The Amplifier must consist of four stages:

- The Pre-Amplifier
- The Gain
- The Filter
- The Power Amplifier

We are to model the amplifier such that the gain from the first two stages (i.e., the pre-amplifier and the gain block) is 500. We model our device assuming our input from the MIC is $20mV_{p-p}$. This means our output voltage should be $10V_{p-p}$.

The input DC supply we have is between 0V and 12V.

Design and Simulation

We look at stages one by one as we build the audio amplifier, with the required specifications. An important assumption made is that we already know the MOSFET parameters, like, transconductance, aspect ratio, threshold voltage, channel length modulation factor. The last factor will not be needed, as it has been ignored in this report. These factors if not available can be approximated from the MOSFET itself

physically, by recording the changes at various levels of V_{GS} and V_{DS}. Note that the accuracy of these values determines all the calculations and the actual circuit implementation.

~~~The Current Source~~~

Our objective here is to create a constant current supplying current source. We will be taking an input from a 12V supply.

Let us first understand the working of a current source by looking at Fig.1.

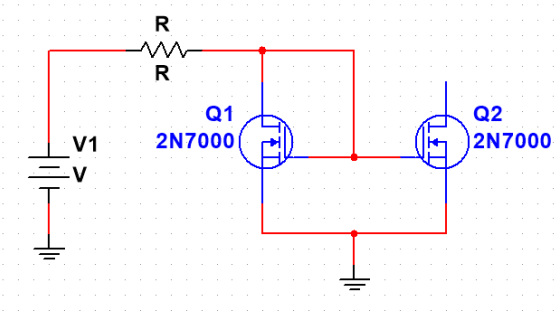

Figure 1

Let us analyse MOSFET Q1. The first observation is that $V_D = V_G$. Hence, $V_{DS} = V_{GS}$.
Therefore, we have $V_{DS} > V_{GS} - V_{th}$.
This tells us that the MOSFET is in the saturation region (we assume V_{DS} is well above V_{th}).

Now, we see that both the MOSFET's have the same gate and source voltages, which imply that both the MOSFET's are being configured in the saturation region, provided Q2 voltage is above V_{th}.

The MOSFET current equation for saturation region is:

$$I_D = \frac{1}{2} K_p (V_{GS} - V_{th})^2$$

As the only factor that I_D depends upon in this equation is V_{GS}, which is matched for both the MOSFET's we can thus conclude that both the drain currents are equal. Whatever current flows through Q1 will also flow through Q2.

Now for the calculation part, let us assume we will use a voltage divider to take a 6V input and we want 1mA of current.

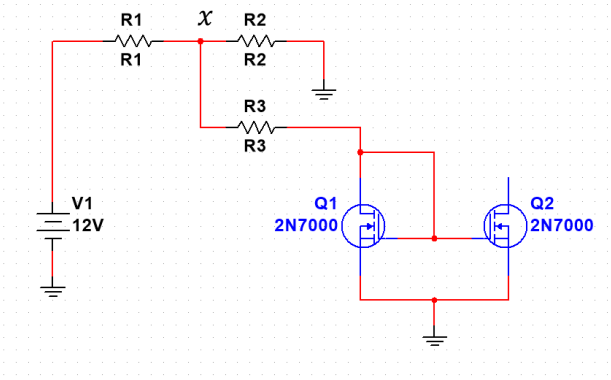

Figure 2

Here R1 and R2 make the voltage divider, and R3 helps to regulate the current passing through Q1.

Now, for current to pass through Q1, the gate voltage should be greater than the threshold voltage. This simply translates to the drain voltage being greater than the threshold voltage. So, if we were to apply nodal analysis at node $'x'$ in Fig.2, we would treat Q1 as a voltage source.

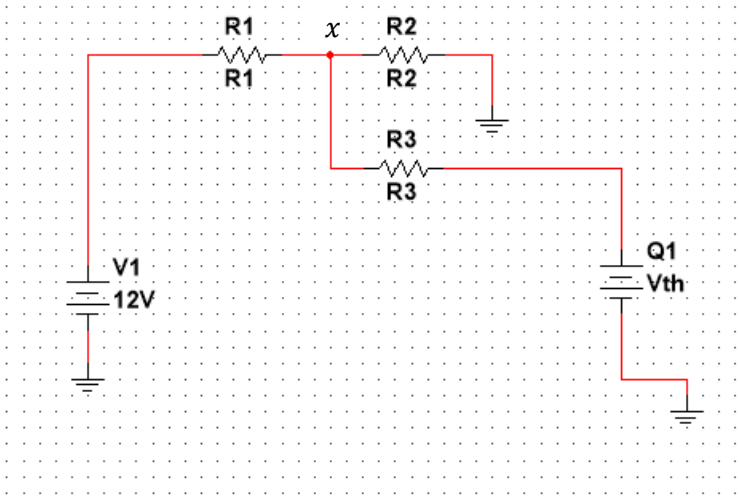

Figure 3

Applying KVL at node 'x', we have,

$$\frac{V-x}{R_1}=\frac{x}{R_2}+\frac{x-2}{R_3}$$

We know that we want $\frac{x-2}{R_3}=1mA \;\&\; x=6V$.

Solving the equation we have,

$$\frac{6}{R_1}=\frac{6}{R_2}+\frac{4}{R_3} \;\&\; \frac{4}{R_3}=1mA$$

Hence, we have $R_3=4k\Omega$, and finding any two values that satisfy the other two resistances, we have $R_1=3k\Omega \,\&\, R_2=6k\Omega$.

Simulating these values in our circuit, makes it work as a charm.

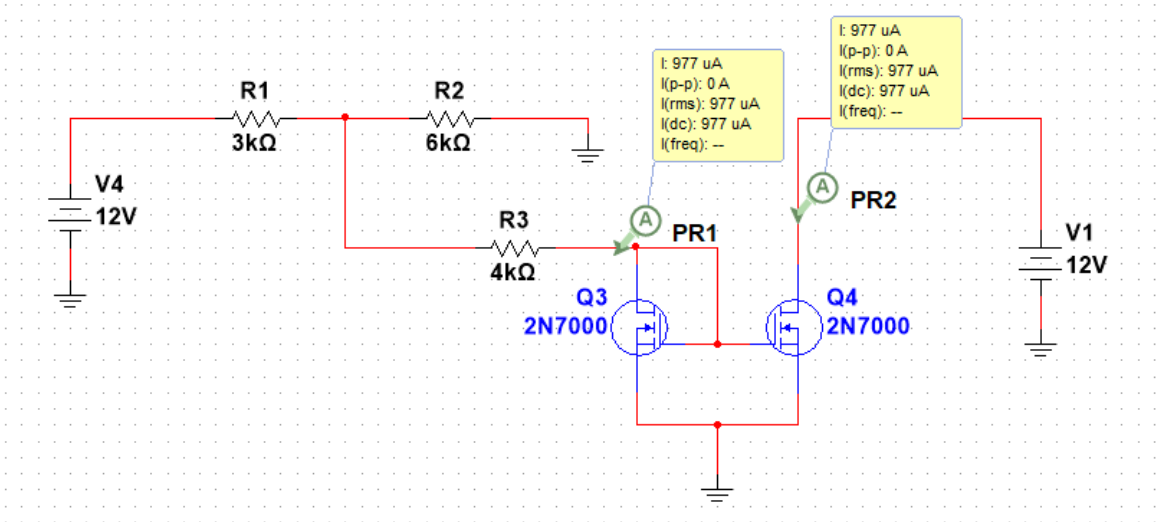

Figure 4

~~~The Differential Amplifier~~~

The work of a differential amplifier is to amplify the difference signal applied between two gates, and to reject any common mode signal between both the gates.

For a differential amplifier, we can either use BJT's or MOSFET's. Each have their own share of advantages and disadvantages. BJT's are better for low power applications such as this one, however here, the MOSFET can work equally well. Hence, we use MOSFET's, just for convenience.

Understanding the working of a differential amplifier is simple. We take the output between both the drains of the MOSFET's. For reference observe Fig.5. The probes correspond to the output voltages.

$$V_{out_1} - V_{out_2} = (V_{DD} - I_{D_1}R_D) - (V_{DD} - I_{D_2}R_D)$$

$$= I_{D_2}R_D - I_{D_1}R_D$$

$$= g_m V_{gs_2} R_D - g_m V_{gs_1} R_D$$

$$\therefore V_{out_1} - V_{out_2} = g_m R_D (V_{gs_2} - V_{gs_1}) \qquad \text{----------①}$$

We have $g_m = 20 \times 10^{-3} A/V = 20\ mS$

$$\therefore V_{out_1} - V_{out_2} = 20 \times 10^{-3} \times 10 \times 10^3 \times [(V_{g_2} - V_{s_2}) - (V_{g_1} - V_{s_1})]$$

Since both the source voltages are the same, they cancel out.

$$\therefore V_{out_1} - V_{out_2} = 20 \times 10^{-3} \times 10 \times 10^3 \times (4 + 10 \times 10^{-3} - V_s - 4 + V_s)$$

$$\therefore V_{out_1} - V_{out_2} = 200 \times 10 \times 10^{-3} = 2V$$

Therefore, to the circuit, by applying 10mV peak voltage, we get an output of 2V peak-peak, which is about a swing of 1V on either side, so 1V peak.

From equation ①, we define our gain as $A = \frac{V_{out_1} - V_{out_2}}{V_{gs_1} - V_{gs_2}} = -g_m R_D = -200$

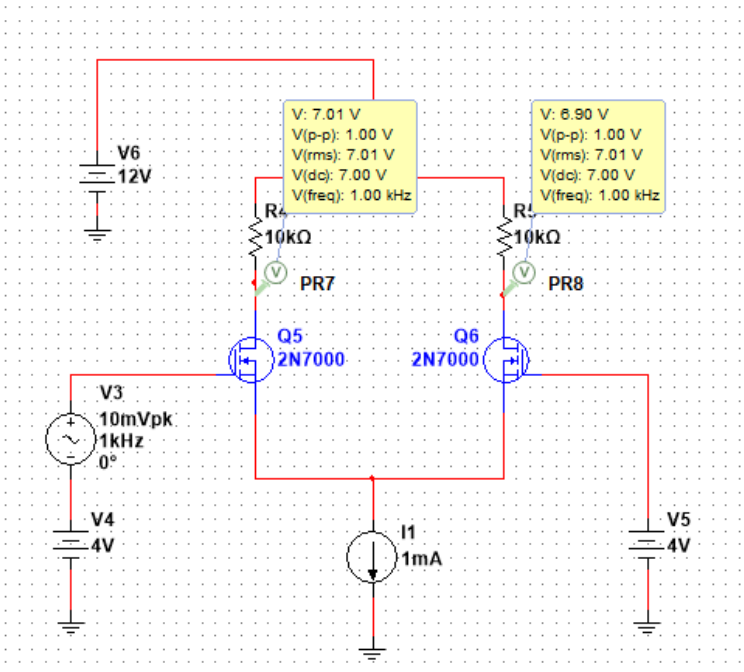

Figure 5

This result is verified by the simulation, where the peak gain is 1V on each side. Both the outputs are $180°$ out of phase. This is shown on an oscilloscope as shown in Fig.6.

The channel A scale is 1V per division, and it covers 2 divisions.

We also see that the MOSFET gates, which have a common voltage of 4V, is completely rejected in the output.

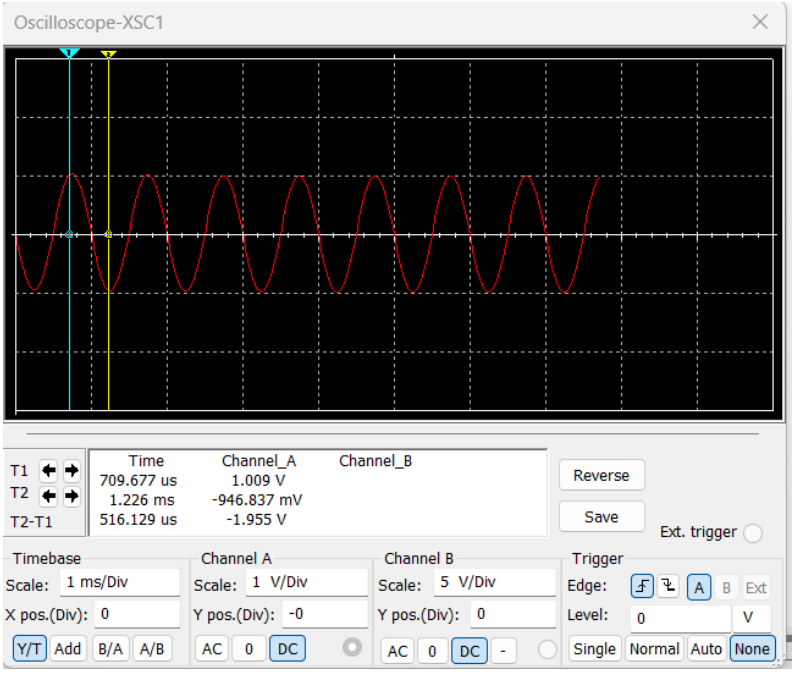

Figure 6

Now, we will not get a current source in real life, as we have used in Fig.5, hence we replace it with the current mirror we built. The output is not much affected.

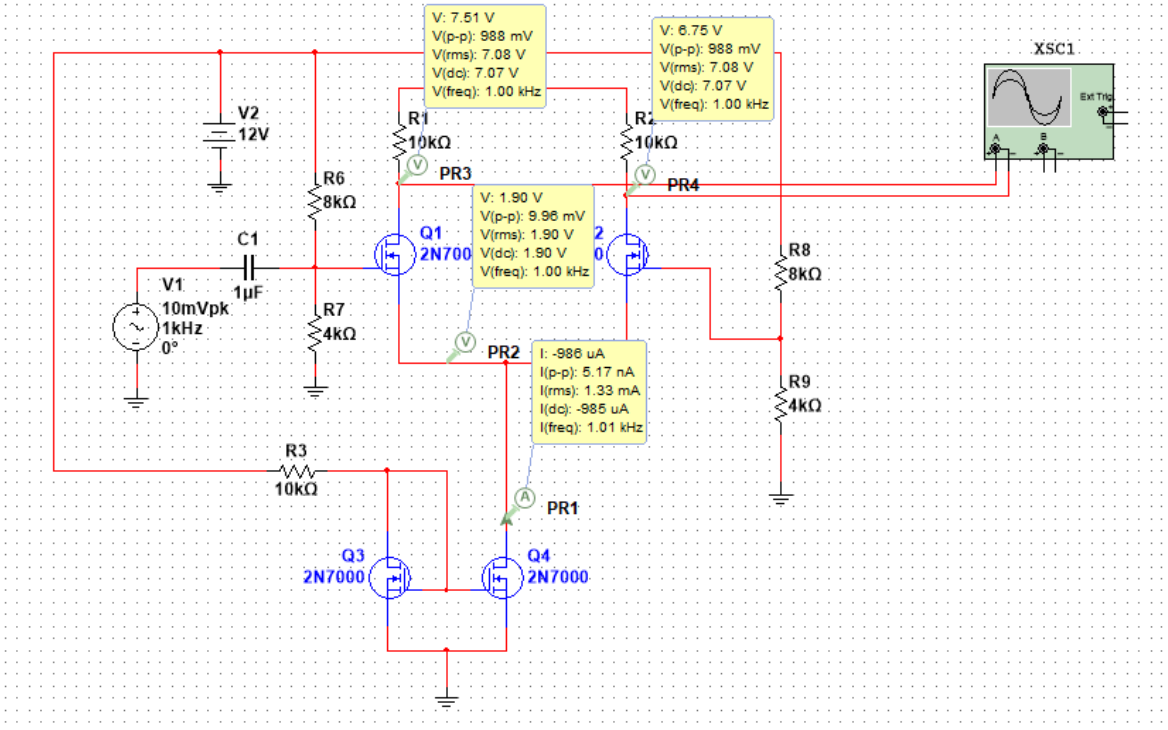

Figure 7

We have biased both the MOSFET's at 4V, but we can choose any other voltage also, such that it still is in saturation along with the swing of the input signal, i.e.,

$$V_{DS} > V_{GS} - V_{th}$$

We assume an equal split of current across the two MOSFET's at equilibrium gate voltage of 4V. Therefore, each branch now has 0.5mA of current through it. We can calculate V_s, form the equation,

$$I_D = \frac{K_p}{2}\frac{W}{L}(V_{GS} - V_{th})^2 \quad where\ V_{GS} = V_G - V_S$$

From the simulation datasheet, we get the value of $K_p = 20.78\mu A/V^2,\ W = 9.7mm,\ \&\ L = 2\mu m$. We know that $I_D = 500\mu A,\ V_{th} = 2V\ \&\ V_G = 4V$. Therefore, by substituting these values, we get $V_s = 1.9V$, which matches with our simulation data, as shown in Fig.7.

We now have three questions,

1) **Since the MOSFET's are already biased, what is the purpose of the constant current source?**
    - If we have a constant current source, then if the current through 1 MOSFET increases, the current through the other MOSFET is forced to decrease. This is a benefit, as if we see Fig.5, if the gate voltage of MOSFET Q5 increases, then the current passing through it increases, which increases the voltage drop across the corresponding resistor. Therefore, the current passing through Q6 decreases, the voltage drops across the Q6 resistor decreases. Thus, we see if one output voltage decreases, the other increases. This gives twice the result that we want.
2) **How do we decide the value of the current source?**
    - The current passing through each MOSFET is 0.5mA, and so through each resistance of the differential amplifier. We can calculate V_D, as $V_{DD} - I_D\ R_D$.
      Hence, we have $V_D = 12 - 0.5 \times 10^{-3} \times 10 \times 10^3 = 7V$, hence,
      $$V_{DS} = V_D - V_S = 7 - 1.9 = 5.1V > V_{GS} - V_{th}.$$
    - As long as the MOSFET is in Saturation region the current can be increased.
    - We can test this in simulation by passing a higher current.
    - For the lower limit, decreasing the current decreases the gain. This is because of the fact of the voltage transfer characteristics. Even though we say that in the saturation the slope is linear, a straight line, it truly isn't. By observing these characteristics, at different current we can draw this conclusion.
    - V_{DS} increases, by channel length modulation the current should increase, but it is constant because of the constant current source, hence the MOSFET is again pushed into the triode region, where gain decreases.
    - Hence, we take 1mA as an ideal value, to start with.
3) **For practical uses, if we want to pass this output to another circuit stage, we can't pass two wires, we can pass only one wire. So, how do we merge the signals, so that we get an output only on one port?**
    - To implement this, we use an active load. An active load is also a current mirror.
    - Also, the problem with the resistor is that, if to increase gain we increase resistance, we risk pushing the MOSFET into the triode region.

~~~The Active Load~~~

Earlier we were using a resistor as a load, and there was a certain voltage drop across this load. A resistor is a passive load. Now we look at active loads. A current source is an example of an active load. If we were to put a current mirror of PMOS (Q5 and Q7) in place of the resistors as shown in Fig.8., the drain voltage for the NMOS (Q1 and Q2) will be constant. The voltage drop across the active load MOSFET's will be just to pull it out of cut-off voltage. The cut-off voltage of this PMOS is 3.43951V. The drain of the NMOS is at $12 - 3.43951 = 8.56049V$, which is close to our simulation value.

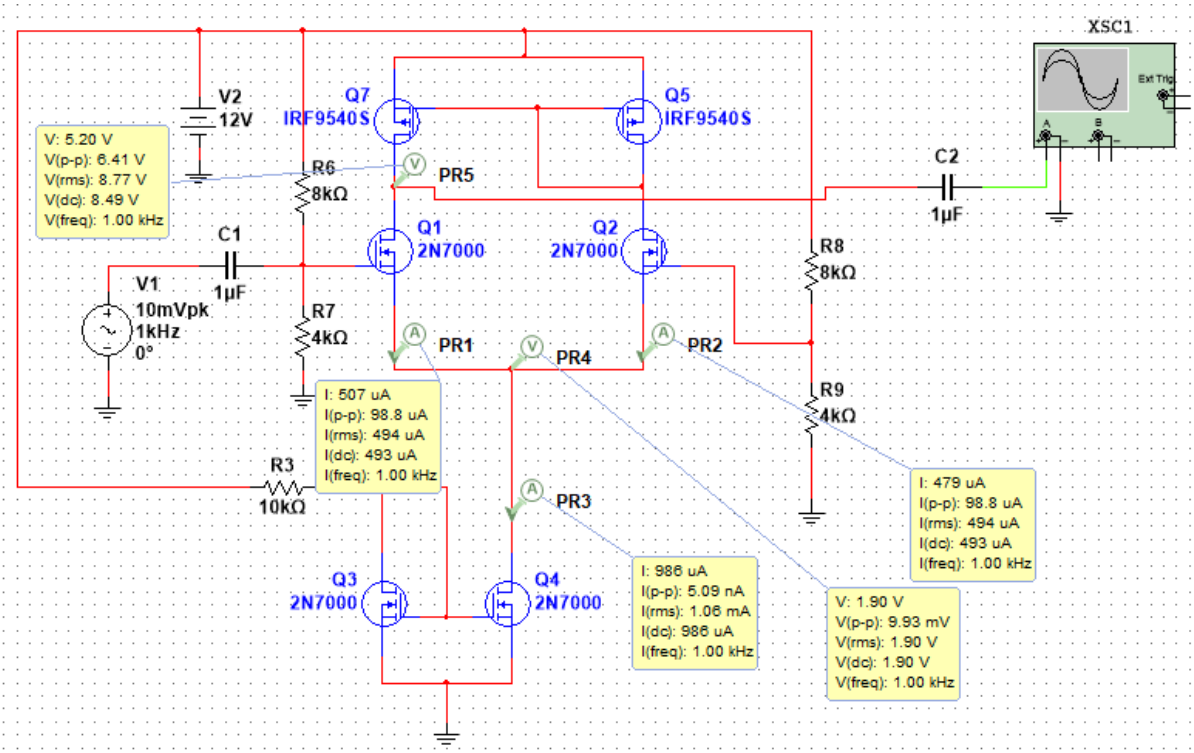

Figure 8

We also must deduce that since a Q5 will replicate whatever current flows through Q7, and the total current is 1mA, current in both the branches will replicate each other in any condition and be equal to 0.5mA.

We must now understand two things:

1) **Why is our gain increasing?**
2) **Why are we able to take output from one port instead of two?**

To answer the first question, we go back to what happens when we increase or decrease resistances. If we increase the resistance to much, the voltage drop across the resistor will be a lot, consequently V_D will decrease, risking pushing our transistor out of saturation into triode, as V_{DS} will keep decreasing compared to V_{GS}. If we decrease our resistances, our gain will decrease as gain $A = -g_m R_D$.

So, now we need to think of a way, to increase the resistance, while keeping the voltage drop across it low. In Fig.8, look at the current mirror (Q5 and Q7). The voltage drop across it is approximately 3.5V, and specified R_{DS} value in the datasheet is $1M\Omega$. It doesn't satisfy the ohm's law because it's an active device.

To answer our next question, we have constant current flowing through both the branches, and that current doesn't change. We have our MOSFET current equation with channel length modulation in saturation as:

$$I_D = \frac{K_p}{2}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$$

Here I_D, is constant, so our equation gives the relation between V_{GS} & V_{DS}, i.e.,

$$\frac{I_D \frac{2}{K_p}\frac{L}{W}\frac{1}{(V_{GS} - V_{th})^2} - 1}{\lambda} = V_{DS}$$

We see that the gain voltage and the drain voltage are inversely proportional. Apart from the differential action, having channel length modulation also boosts up the gain. As the drain voltage is proportional to the square of the gate voltage, a small change in the V_{GS}, leads to a major change in V_{DS}, and both the effects amplify V_{GS} in the same direction.

However, why do we now need the second MOSFET? If the current in both the branches are equal, and we take output from only the drain of one MOSFET, why do we need the other one. The other MOSFET's sole purpose is now to maintain the source voltage at a constant value so that the other MOSFET, always has a constant current flowing through it.

We need an output of 10 V, we got $6.41\ V_{p-p}$ output. We can add the remaining gain in the next stage, however, if we pass this gain directly to the next stage, the MOSFET in the CS amplifier we use may not have such a large saturation region to carry a swing of 6.41V. Therefore, we decrease it to about 1V. Later, if we want to, we can play with this voltage to check it. We decrease it by reducing the current near in the NMOS current mirror (made of Q3 and Q4 in Fig.8), and to do this we increase R3 to about $850k\Omega$.

~~~The CS Amplifier~~~

In this stage we get an input of about $1\ V_{p-p}$. We want an output of $10\ V_{p-p}$. Therefore, we need a gain of 10. Fig.9 shows a traditional CS amplifier design.

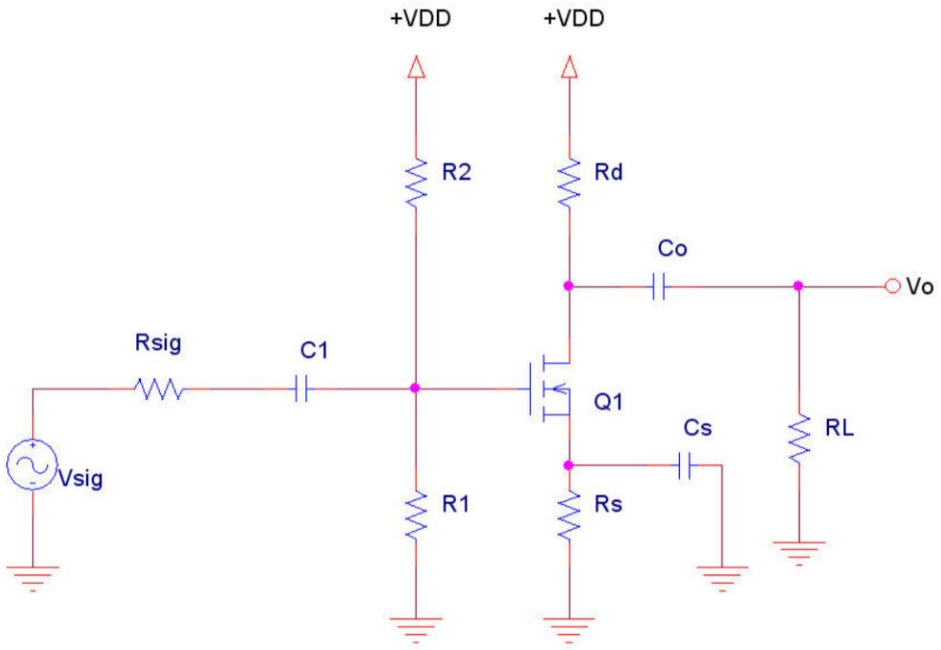

Figure 9

Finding R_D

We know from actual implementation that the output voltage from the pre-amp stage is about 300mV. Therefore, for a $10V_{p-p}$ output, we need to have a further gain of about 35. Therefore $g_m R_D = 35$. Hence, we have $R_D = 17500\Omega$.

R_1 and R_2 are biasing resistors. The MOSFET's threshold voltage is 2V. Hence, $\frac{V_{DD}}{R_1+R_2} R_1 - V_S$, must be greater than 2V, for the transistor to be at least on.

$$\therefore V_G - I_D R_S > 2$$

$$\text{where, } I_D = \frac{V_{DD}}{R_D+R_S} = \frac{12}{17500+R_S}$$

$$\therefore V_G > 2 + \frac{12R_S}{R_D+R_S} \quad \text{-①}$$

Also, $$V_{DS} > V_{GS} - V_{th}$$

i.e., $$V_{DD} - I_D R_D - V_S > V_G - V_S - V_{th}$$

$$\therefore 12 - \frac{12 \times 17500}{17500 + R_S} > V_G - \frac{12R_S}{17500 + R_S} - 2$$

$$\therefore V_G < 14 + \frac{12(R_S-17500)}{17500+R_S} \quad \text{-②}$$

Hence, plotting ① & ② on DESMOS, we get

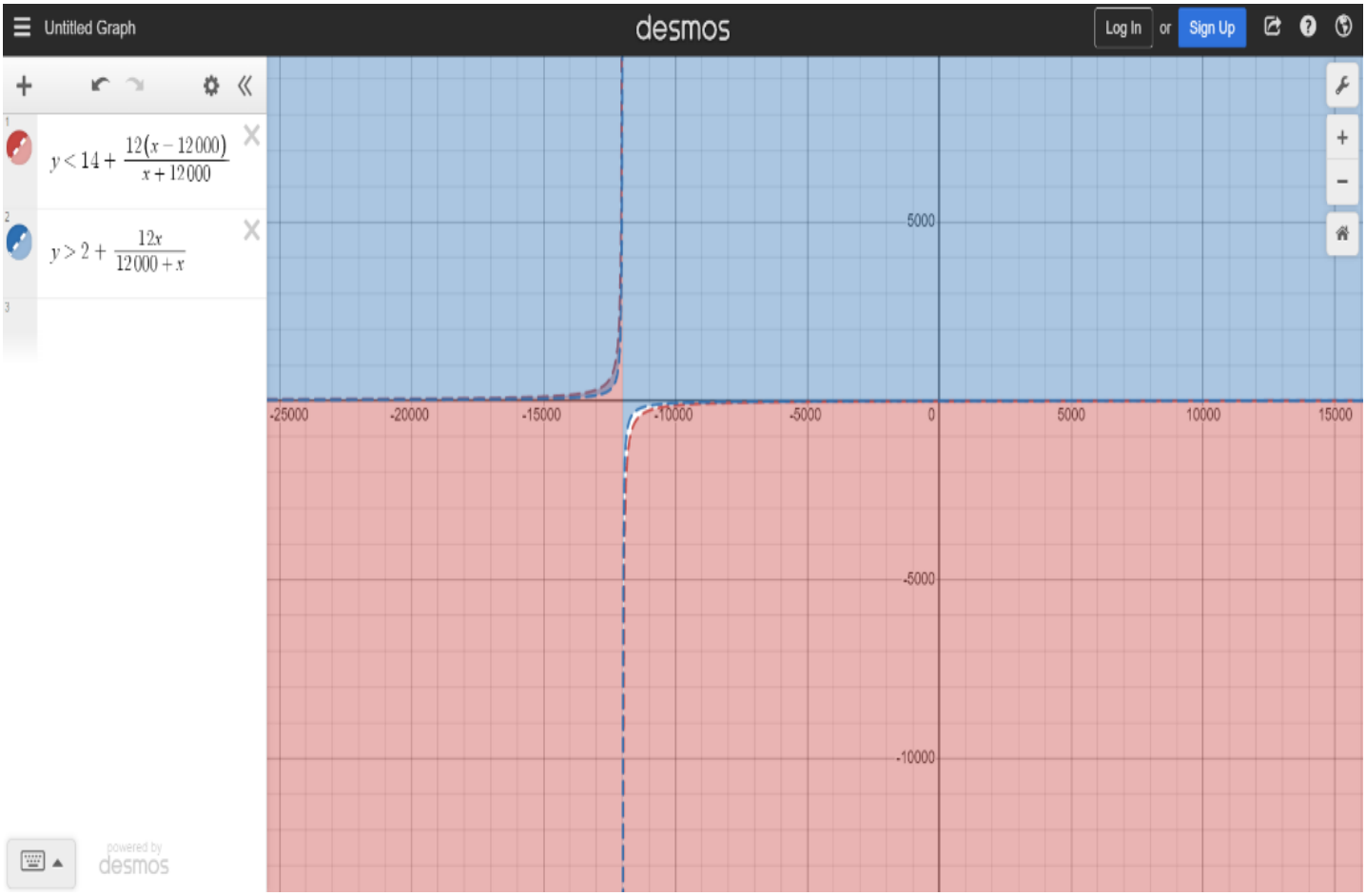

Figure 10

Taking a positive value from Fig.10, zoomed into Fig.11

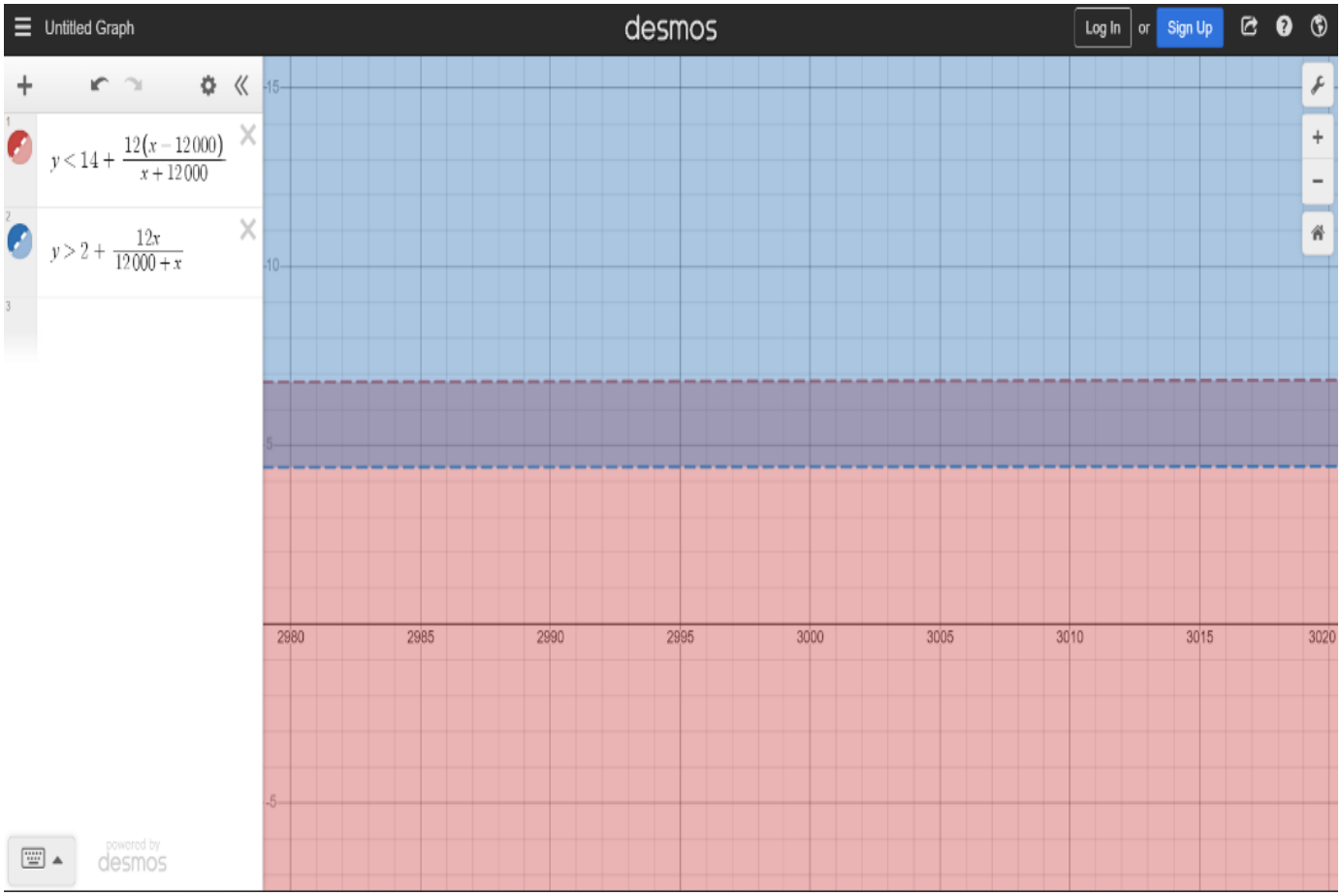

Figure 11

At $R_S = 3000\Omega$ & $V_G \approx 5V$, we can bias our circuit.

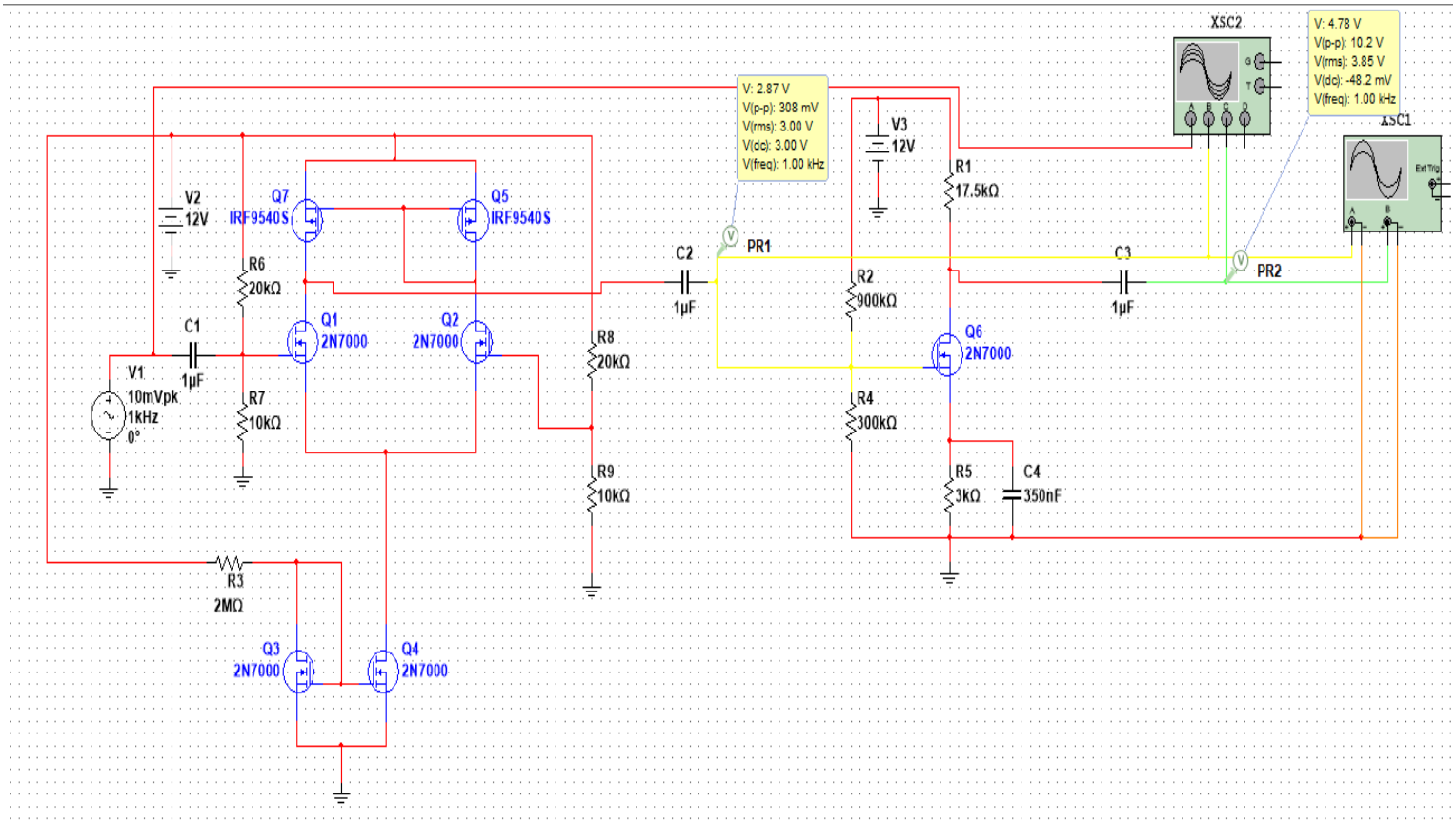

Figure 12

In the following circuit, even though we calculated the bias at 5V, putting it at 3V works for the circuit.

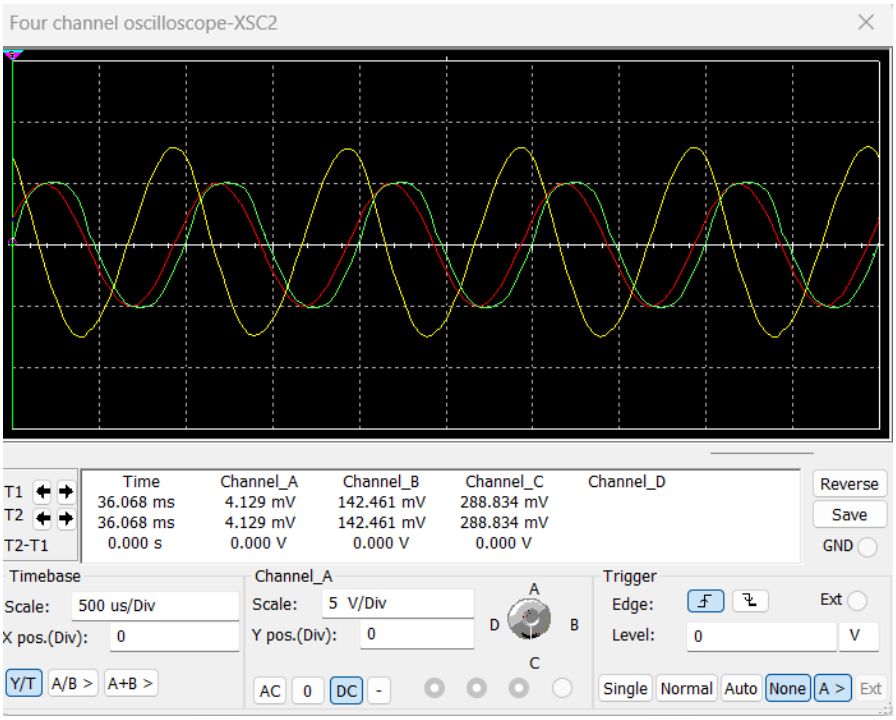

Figure 13

We see in Fig.13, a nice $10V_{p-p}$ output, shown in green.

→**Function of C_S:** C_S acts as a bypass capacitor. After achieving DC stability, this capacitor acts parallel to R_S decreasing the impedance for AC signals at the source of the MOSFET. After achieving DC stability, we can play with this value to increase our AC gain.

~~~The Filter~~~

The filter used here is a simple RC low pass filter, designed for passing frequencies below 8kHz. The gain diminishes by 20KHz. 8kHz was chosen as it is the maximum for human speech. Voices above it can be heard, but if a human's not speaking those frequencies, it can as well be considered as noise.

A passive filter is quite simple to calculate. Since we are making a low pass filter, and we want it to pass all frequencies less than 8kHz,

$$\frac{1}{RC} = 2\pi f_c$$

Here f_c is the cut-off frequency. We want to keep the capacitance as small as possible to voltage and current lag. Hence, we use a ceramic capacitor of 1nF. We can now calculate the resistance as

$$R = \frac{1}{C \times 2\pi f_c} = \frac{1}{10^{-9} \times 2\pi \times 8000} = 19894.35\Omega \approx 20k\Omega$$

The bode plot for the filter can be seen in Fig.14, and the circuit diagram can be seen in Fig.15.

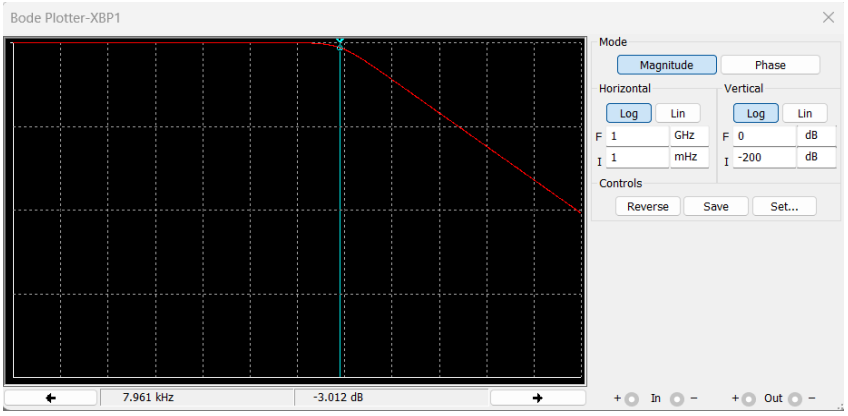

Figure 14

One important question to consider is:

Why is cut-off frequency defined as -3dB? Why not -4dB or -5dB?

→We define the cut-off frequency, not as the point where the filter starts cutting-off, but as the point where the filter has reduced the frequencies gain to half the value it was. So, if the power supposedly at 8kHz was 10W say, after passing the signal through the filter, the power will be 5W.

We express gain as in the logarithmic form, as $10 \log_{10} \frac{P_{output}}{P_{input}} dB$.

Therefore, if the ratio of the output power to input power is 0.5, the gain will be -3dB.

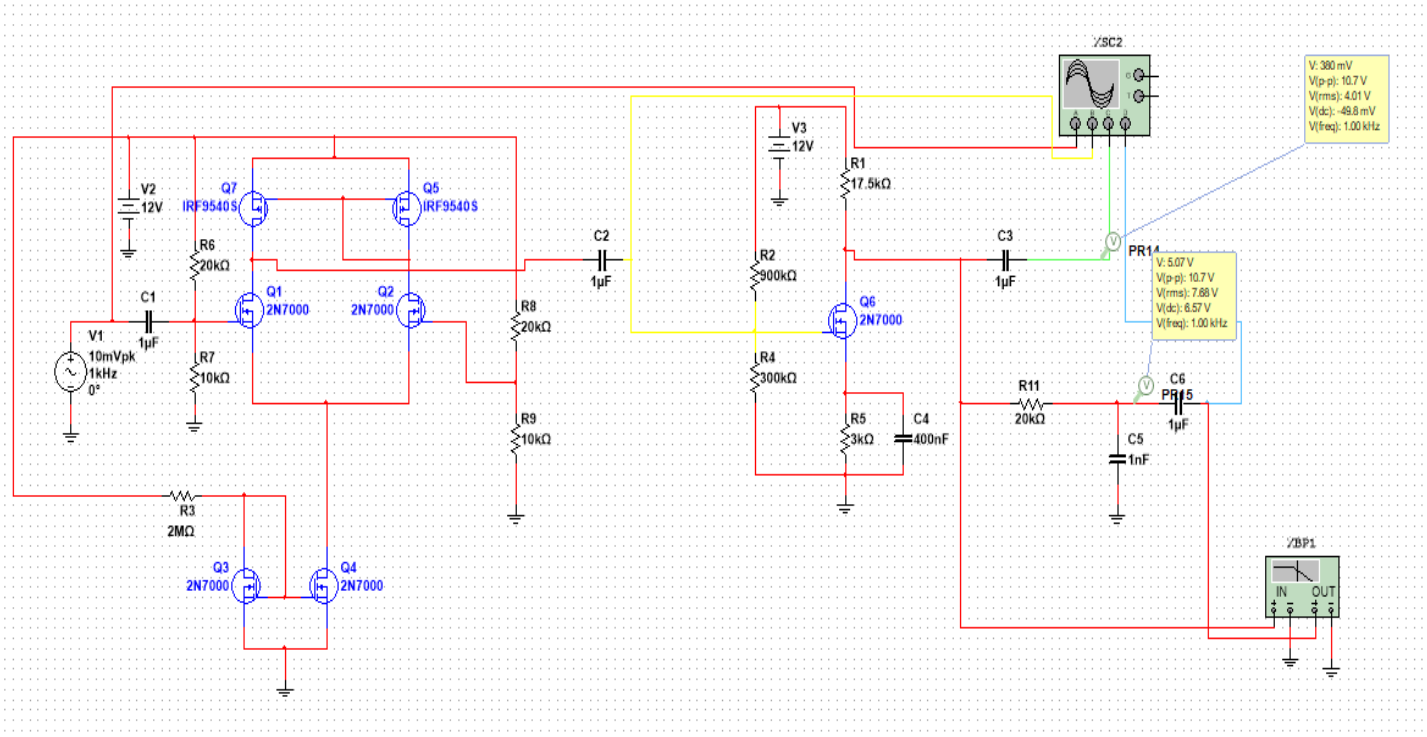

Figure 15

Even though I have used a passive filter for convenience here, I would recommend readers to look into active filters. This gets us to the particularly important question:

Why Active Filters over Passive Filters?

→Active filters like the 741 OP-Amp have easily adjustable gain and frequency. They face loading, i.e., the calculated and placed components themselves change the position of the poles and zeros, or the characteristics of the filter. The OP-Amp on the other hand has high input resistance and low output resistance, hence active filters don't cause loading. In terms of stability, active filters are much better than passive filters.

The last stage is that of the power amplifier. The power amplifier amplifies the current, to increase the power across the output. For the output we use a 8Ω speaker, and we expect a 1W output, so that the speaker can run.

The voltage gain of such an amplifier is '1', therefore for a 1W output, we want the current to be 100mA.

There are various classes of Amplifiers that we can use, however we will be analysing the class 'A' amplifier, class 'B' amplifier and class 'AB' amplifier.

1) Class 'A' Power Amplifier: The class 'A' amplifier is the most common type of power amplifier, and is the most simplest. It uses a single NPN BJT and has a conversion of the entirety of the input wave. However, this configuration is very inefficient. There is a lot of power wastage. There is also inversion of the output signal, compared to the input signal.
2) Class 'B' Power Amplifier: This configuration uses a NPN BJT followed by a PNP BJT. It does not invert the output wave. It is not always switched on; hence the power efficiency is better. However, it only amplifies the power of one half of the wave.
3) Class 'AB' Power Amplifier: The class 'AB' amplifier is the best of both the worlds. It produces an almost full wave amplified signal and is efficient. It has the configuration of a class 'B' power amplifier, except the base voltages of both the BJT's are kept at a potential difference of about 1-2V. Hence, this configuration of the power amplifier is used. I have used diodes to keep the potential difference between both the bases of the BJT's.

The final circuit is shown in Fig. 16.

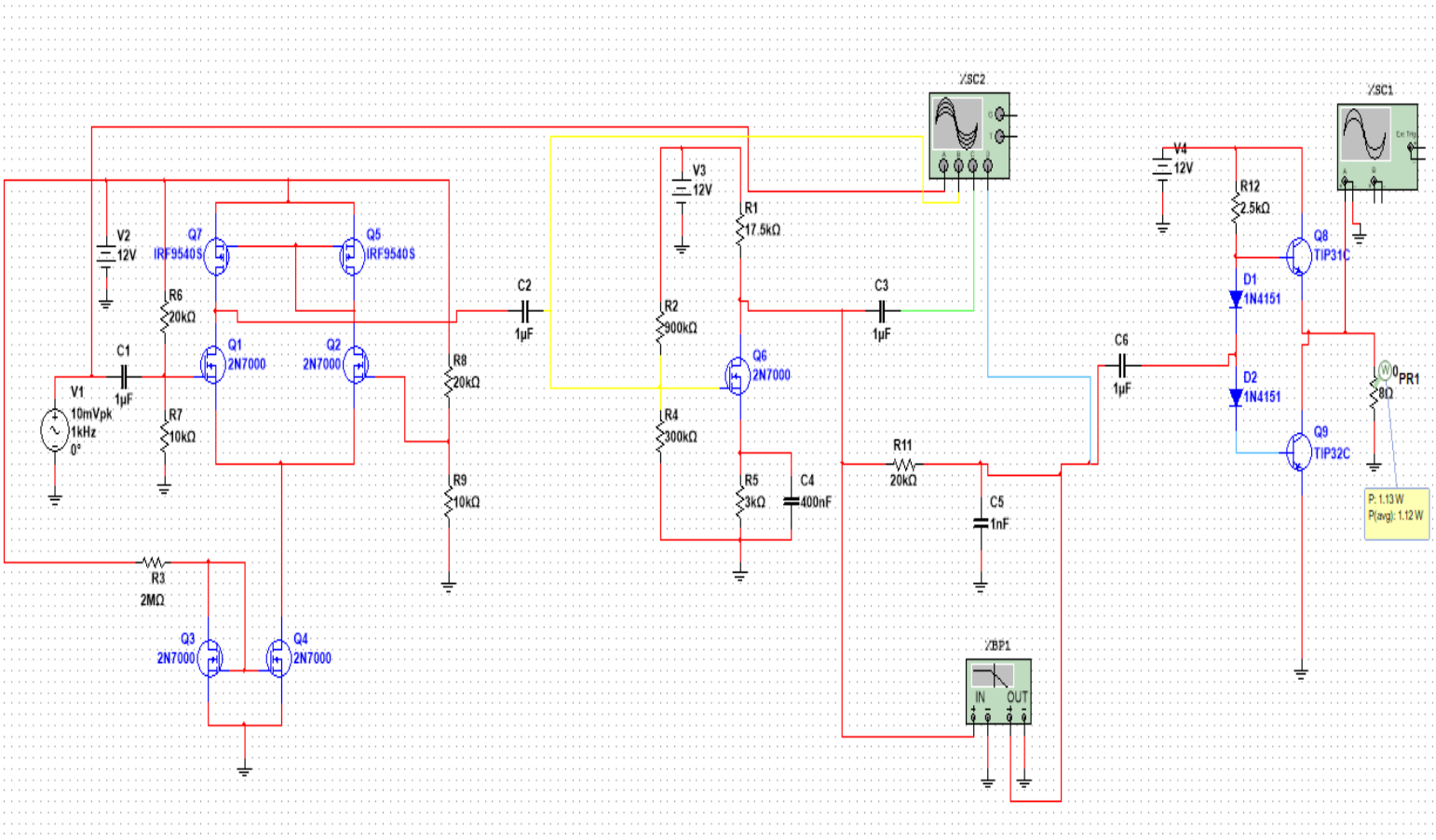

Figure 16

Hardware Implementation

While testing it physically some values were changed, to account for calculation of incorrect parameters. For example, the value of g_m was calculated as 20mS, however there are errors in this calculation also, and changes for different V_{GS}. Hence, parameters were shifted from their calculated value to account for errors, and were only assigned on the basis of the output as seen on an oscilloscope.

Fig.17 shows the resistances and other values used in the actual hardware implementation.

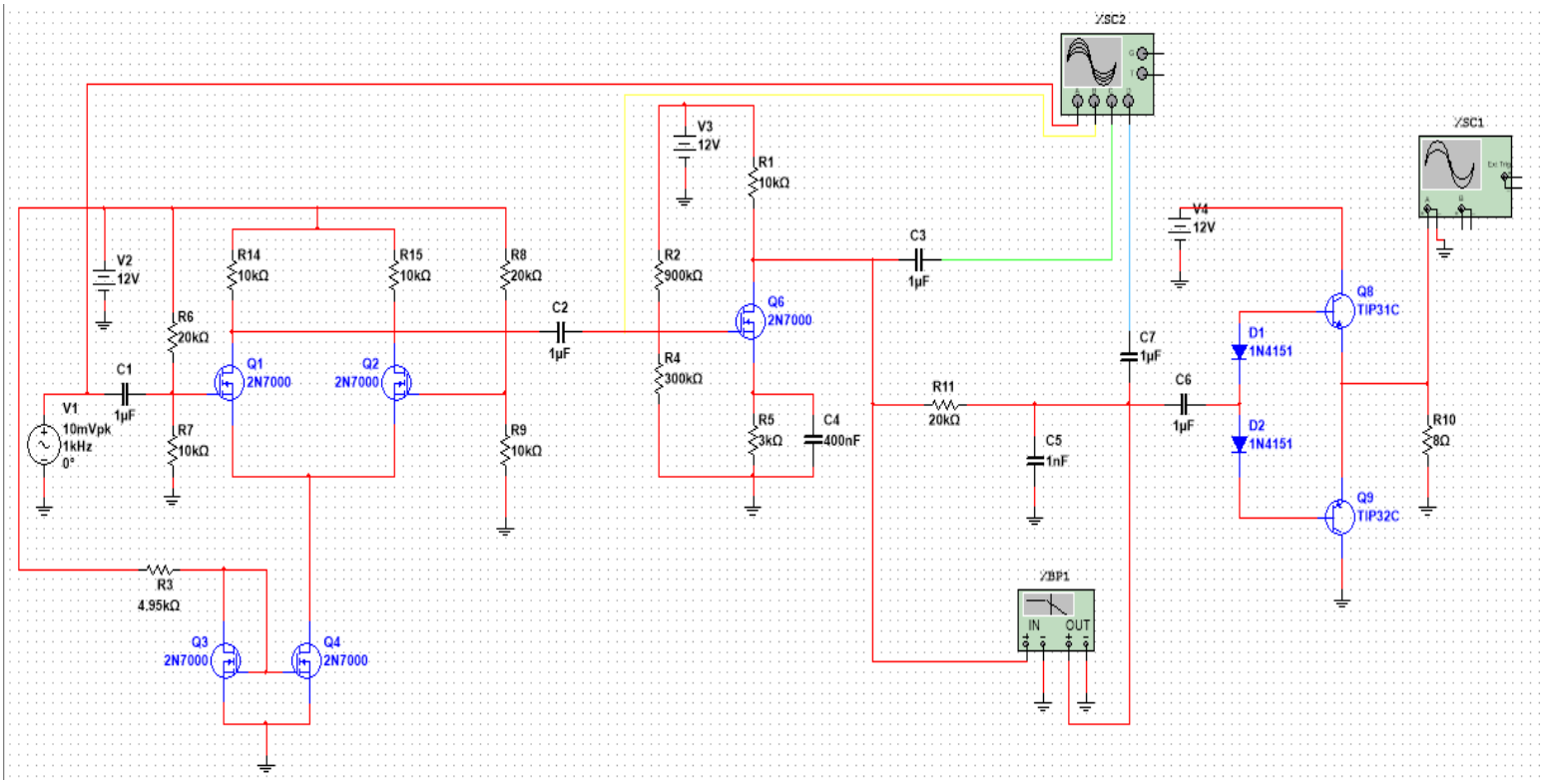

Figure 17

Results for Individual Stages

- Pre-Amplifier: Gain=15: Pre-Amplifier - Version 1 - YouTube
- Gain: Gain=34: Gain Block - Version 1 - YouTube
- Filter: Gain=1: Filter Block - Version 1 - YouTube
- Power Amplifier and Output: Audio-Amplifier - YouTube

Specific Values and Observations to be Included in the Report

- Calculation the Distortion in the Circuit
    - Distortion of the circuit is the amount of variation of the output waveform from the expected waveform. Clipping, phase change, inversion etc, all include in distortion. Reasons of distortion include, incorrect biasing, large input, large capacitances causing phase change, for AC. I would measure the distortion in the circuit by passing an ideal input of $10mV_{p-p}$, and calculating the correlation between the expected output, and the begotten output.

- CMRR
    - Common Mode Rejection Ratio is the percentage by which the pre-amplifier rejects the common signal between both the inputs. It is the ration of the differential gain to the common mode gain.
- How is the circuit output affected by the mismatch? How can it be reduced?
    - Here mismatch indicates resistor mismatch in the pre-amplifier, which here controls the gate voltages of the differential amplifiers. If there is mismatch the common mode signals will no longer be common and will be amplified as noise. It can be reduced by making the resistances higher by maintaining the same ratio.
- Input Range
    - The input range of the circuit can be calculated by calculating the maximum swing that a transistor can handle at every stage and finding the minimum input for that range. Here the maximum swing is about $50mV_{p-p}$.
- Circuit Stability
    - The circuit stability refers to the unnecessary oscillations, overshoot/undershoot, parasitic capacitance, and shift of circuit behaviour in time.

Bibliography

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