# Computer Architecture Assignment-2 Report

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**Code Optimization Techniques for Data :**

**1 . Merging Arrays :**

Allocating arrays so that paired operands show up in the same cache block.

**Without Optimization**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 0.3601 |
| Runtime unhalted [s] | 0.3183 |
| Clock [MHz] | 2582.6619 |
| CPI | 0.4198 |
| L1I request rate | 0.1874 |
| L1I miss rate | 0.0044 |
| L1I miss ratio | 0.0233 |
| L1I stalls | 10053148 |
| L1I stall rate | 0.0051 |

**ICACHE MISS RATE**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 0.3600 |
| Runtime unhalted [s] | 0.3206 |
| Clock [MHz] | 2593.8627 |
| CPI | 0.4226 |
| L1 DTLB load misses | 348903 |
| L1 DTLB load miss rate | 0.0002 |
| L1 DTLB load miss duration [Cyc] | 22.3257 |
| L1 DTLB store misses | 141876 |
| L1 DTLB store miss rate | 0.0001 |
| L1 DTLB store miss duration [Cyc] | 23.3228 |

**TLB_DATA MISS RATE**

**With Optimization**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 1.2536 |
| Runtime unhalted [s] | 1.1537 |
| Clock [MHz] | 2593.9718 |
| CPI | 0.4164 |
| L1I request rate | 0.1563 |
| L1I miss rate | 0.0016 |
| L1I miss ratio | 0.0100 |
| L1I stalls | 15575568 |
| L1I stall rate | 0.0022 |

**ICACHE MISS RATE**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 1.2407 |
| Runtime unhalted [s] | 1.1430 |
| Clock [MHz] | 2593.5578 |
| CPI | 0.4135 |
| L1 DTLB load misses | 1568833 |
| L1 DTLB load miss rate | 0.0002 |
| L1 DTLB load miss duration [Cyc] | 26.7096 |
| L1 DTLB store misses | 350493 |
| L1 DTLB store miss rate | 4.893079e-05 |
| L1 DTLB store miss duration [Cyc] | 26.8994 |

**TLB_DATA MISS RATE**

**Inference:**

The runtime of the optimized code is around **4 times higher** than the non-optimized one. This maybe due to calling of the constructor of the class **Merge** and the allocations to the class since constructors are called and members are initialized during run time. The number of load misses for data in the optimized code is almost **4 times** that of non-optimized code.

On the other hand the optimized code has a relatively lower request and miss rate for instructions.

The store missrate is much lower in the optimized code which is about **40%** of the miss rate of non-optimized code

**2. Loop Fusion:**
Aggregation of loops which access the same data into a single loop.

**Without Optimization**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 1.4069 |
| Runtime unhalted [s] | 2.2914 |
| Clock [MHz] | 4380.1743 |
| CPI | 0.3794 |
| L1I request rate | 0.1786 |
| L1I miss rate | 0.0016 |
| L1I miss ratio | 0.0092 |
| L1I stalls | 8675938 |
| L1I stall rate | 0.0006 |

**ICACHE MISS RATE**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 1.4763 |
| Runtime unhalted [s] | 2.3986 |
| Clock [MHz] | 4451.6754 |
| CPI | 0.3969 |
| L1 DTLB load misses | 270488 |
| L1 DTLB load miss rate | 1.726620e-05 |
| L1 DTLB load miss duration [Cyc] | 21.0404 |
| L1 DTLB store misses | 48720 |
| L1 DTLB store miss rate | 3.109969e-06 |
| L1 DTLB store miss duration [Cyc] | 27.7495 |

**TLB_DATA MISS RATE**

**With Optimization**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 1.5899 |
| Runtime unhalted [s] | 2.2205 |
| Clock [MHz] | 4363.2133 |
| CPI | 0.3836 |
| L1I request rate | 0.1814 |
| L1I miss rate | 0.0016 |
| L1I miss ratio | 0.0090 |
| L1I stalls | 19056079 |
| L1I stall rate | 0.0013 |

**ICACHE MISS RATE**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 1.4090 |
| Runtime unhalted [s] | 2.2251 |
| Clock [MHz] | 4293.0325 |
| CPI | 0.3863 |
| L1 DTLB load misses | 253230 |
| L1 DTLB load miss rate | 1.695980e-05 |
| L1 DTLB load miss duration [Cyc] | 20.9951 |
| L1 DTLB store misses | 45454 |
| L1 DTLB store miss rate | 3.044232e-06 |
| L1 DTLB store miss duration [Cyc] | 28.2600 |

**TLB_DATA MISS RATE**

**Inference:**

Instruction-wise both are very similar with minute differences, whereas on the data we are able to see a significant drop in the load misses and store misses in the optimized code.

**3. Loop Interchange:**
Exchanging inner and outer loop order to improve cache performance.

**Without Optimization**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 0.5210 |
| Runtime unhalted [s] | 0.4993 |
| Clock [MHz] | 2588.3225 |
| CPI | 0.4245 |
| L1I request rate | 0.1936 |
| L1I miss rate | 0.0030 |
| L1I miss ratio | 0.0156 |
| L1I stalls | 13818722 |
| L1I stall rate | 0.0045 |

**ICACHE MISS RATE**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 0.5082 |
| Runtime unhalted [s] | 0.4865 |
| Clock [MHz] | 2586.8048 |
| CPI | 0.4175 |
| L1 DTLB load misses | 319660 |
| L1 DTLB load miss rate | 0.0001 |
| L1 DTLB load miss duration [Cyc] | 21.5924 |
| L1 DTLB store misses | 39235 |
| L1 DTLB store miss rate | 1.299100e-05 |
| L1 DTLB store miss duration [Cyc] | 26.8909 |

**TLB_DATA MISS RATE**

**With Optimization**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 0.5233 |
| Runtime unhalted [s] | 0.5034 |
| Clock [MHz] | 2593.8492 |
| CPI | 0.4445 |
| L1I request rate | 0.1893 |
| L1I miss rate | 0.0030 |
| L1I miss ratio | 0.0157 |
| L1I stalls | 90904312 |
| L1I stall rate | 0.0310 |

**ICACHE MISS RATE**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 0.5008 |
| Runtime unhalted [s] | 0.4673 |
| Clock [MHz] | 2542.0308 |
| CPI | 0.4125 |
| L1 DTLB load misses | 309897 |
| L1 DTLB load miss rate | 0.0001 |
| L1 DTLB load miss duration [Cyc] | 20.7655 |
| L1 DTLB store misses | 39109 |
| L1 DTLB store miss rate | 1.332063e-05 |
| L1 DTLB store miss duration [Cyc] | 26.7094 |

**TLB_DATA MISS RATE**

**Inference:**
The stall rate and stalls of instructions have shown significant increase in the optimized code.

Loop interchanging has shown that there is significant improvement in loading data in the optimized code.The miss penalty for the load miss in L1 data cache is lower by about **1 clock cycle** in the optimized code.

**4.Blocking:**
Maximizing number of instructions executed in a sub-block

**Without Optimization**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 95.7478 |
| Runtime unhalted [s] | 95.5379 |
| Clock [MHz] | 2593.7601 |
| CPI | 0.3554 |
| L1I request rate | 0.1642 |
| L1I miss rate | 0.0001 |
| L1I miss ratio | 0.0005 |
| L1I stalls | 189984140 |
| L1I stall rate | 0.0003 |

**ICACHE MISS RATE**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 95.2939 |
| Runtime unhalted [s] | 95.0881 |
| Clock [MHz] | 2593.7893 |
| CPI | 0.3519 |
| L1 DTLB load misses | 29271786 |
| L1 DTLB load miss rate | 4.179528e-05 |
| L1 DTLB load miss duration [Cyc] | 13.2166 |
| L1 DTLB store misses | 63721 |
| L1 DTLB store miss rate | 9.098306e-08 |
| L1 DTLB store miss duration [Cyc] | 28.9952 |

**TLB_DATA MISS RATE**

**With Optimization**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 194.9057 |
| Runtime unhalted [s] | 194.5210 |
| Clock [MHz] | 2593.8777 |
| CPI | 0.3838 |
| L1I request rate | 0.1647 |
| L1I miss rate | 0.0082 |
| L1I miss ratio | 0.0500 |
| L1I stalls | 33402583911 |
| L1I stall rate | 0.0254 |

**ICACHE MISS RATE**

| Metric | HWThread 1 |
|---|---|
| Runtime (RDTSC) [s] | 194.6033 |
| Runtime unhalted [s] | 194.1958 |
| Clock [MHz] | 2593.9195 |
| CPI | 0.3825 |
| L1 DTLB load misses | 23639393 |
| L1 DTLB load miss rate | 1.796320e-05 |
| L1 DTLB load miss duration [Cyc] | 17.8077 |
| L1 DTLB store misses | 620669 |
| L1 DTLB store miss rate | 4.716367e-07 |
| L1 DTLB store miss duration [Cyc] | 25.2197 |

**TLB_DATA MISS RATE**

**Inference**
With blocking, we see a large increment in the overall runtime of the program.
There is a reduction in the load misses of the optimized code by about **7 million** misses. The miss rate is also **2 times** lesser in the optimized code.