What are the major functions of an 1/0 module? I/o module stands for Input/ Output module, which is a device that acts as the connective bridge between a computer system at one end and an 1/0 or peripheral device of some kind at the other, Such as a printer, web cam or scanner. This enables a computer system to carry out its intended function, which is to communicate with the external world in which ever way it needs to · The key tasks of I/O Module's 1) Processor communication: This involves a number of tasks, primarily the transference of data between the processor and an Ilo module, accepting and decoding commands sent by the processor, reporting of current status, and an ability for the I/O module to recognise its own unique address 2 Device communication: It needs to be able to perform standard device communications, such as reporting of 3 Control and timing: An IIO module needs to be capable of managing data flow between a computer's internal resources and any connected external devices (A) Data buffering: A crucial Function that manages the speed discrepancy that exists between the speed of FOR EDUCATIONAL USE

| transfer of data between the processor and | | | | | |
|--|--|--|--|--|--|
| | | | | | |
| memory and peripherial devices | | | | | |
| Detecting errors, whether mechanical (such as a | | | | | |
| printer experiencing a paper jum) or data based, | | | | | |
| and reporting them to the processor is another | | | | | |
| vital Function of an I/O module. | | | | | |
| - Thus, without an I/O module the ability for | | | | | |
| the exchange of data between a processor | | | | | |
| and a peripheral device is non-existent, also | | | | | |
| making the ability to interplet data into | | | | | |
| information ready for communication and | | | | | |
| consumption impossible. | | | | | |
| | | | | | |
| Compare numbry mapped I/O programmed I/O | | | | | |
| Memory mapped I/O Programmed I/O | | | | | |
| 1 External asynchronous 1 Processor has to check | | | | | |
| input is used to tell the each I/O device in | | | | | |
| processor that Ilo divice sequence and in | | | | | |
| needs its services and effect 'ask' each one | | | | | |
| hence processor does if it needs communic- | | | | | |
| not have to theck ation with the | | | | | |
| whether I/O devices processor. | | | | | |
| needs it services or not | | | | | |
| 2) The processor is 2 During polling processor | | | | | |
| allowed to execute its is busy and therefore | | | | | |
| instruction in sequence have serious and | | | | | |
| and only stop to service decremented effect on | | | | | |
| and unity stop | | | | | |
| | | | | | |

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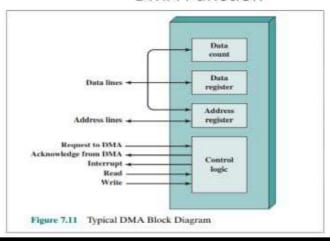
undaram

| | Memory mapped 7/0 | Programmed I/O | | | |
|-----------------|--|----------------------|--|--|--|
| | I/O device when it is | effect on system | | | |
| | told to do so by the | throughput | | | |
| | device itself, this | 0 / | | | |
| | increased system | | | | |
| | throughput | 3 | | | |
| TD | 3 Implemented using | 3) It is implemented | | | |
| | interrupt hardware | without in terrupt | | | |
| | Support + | hard ware support | | | |
| | 1 Must be enabled to | @ Does not depend on | | | |
| | process interrupt driven | interrupt States | | | |
| | 710 | | | | |
| | (5) System throughput | 5) System throughout | | | |
| | does not depend on | decreases as number | | | |
| | | of Ilo devices | | | |
| | connected in the system. | increases | | | |
| | | | | | |
| <u> </u> | lalvite note on interrupt driven Ilo | | | | |
| - Ans | This technique is used to overcome the limitation of programmed I/O. (2) In interrupt driven I/O, instead of making the | | | | |
| | | | | | |
| * | | | | | |
| | processor to verify the status of I/O module. It | | | | |
| | is the responsibility of I/O module to intimate | | | | |
| | 3 CPU responds to interrupt signals and stores | | | | |
| | | | | | |
| | the return address from the program counter | | | | |
| | (PC) into the memory stack and then the control | | | | |
| | brunches to a interrupt service routine (ISR). | | | | |
| | 1 ISR processes the required Ilo Transfer | | | | |
| | | | | | |
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| 5 | After (| pmpletion | of execut | ing interru | of routing |
|-----|---------------------------------------|--------------|----------------------|--|----------------|
| | CPU Yetus | ins to pre | vinus prod | ram and a | ontinue |
| | | was doing | | | |
| | Interrupt | | | | |
| 1.1 | | | xception | ccuses CPU | to transf |
| | the conti | al tempor | arily fro | m its curre | ent progra |
| | to anth | ar procram | i.c. int | errupt hand | 1100. |
| | BLOCK D | icy ram fo | Y TAKEYYUE | ot Driven I | 10 |
| | | · · | | | - |
| | | Interro | of Request | (INTR) | and the second |
| | CPU | | | | T/O |
| | \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ | Taterrupt | Acknowledge | r. onent | sy's tem |
| | | (| ACKNOWLEDGE INTA) | J C · S · · · · · · · · · · · · · · · · · | |
| | Trancfe | r control | From mair | program + | -o |
| | | Handler | | 7-1-0 | |
| | - Mary | / Harris = | | | |
| | | Main Progra | ı <i>r</i> | | |
| | 1 | the property | | 1 | |
| | 2 | • | | | |
| 17 | nterrupt | 9 | | | Interrupt |
| C | ccurs_i | | | 1 | Handler' |
| | rere i+1 | | | 9 | |
| | | | | • | |
| | M | • . | | | |
| - | | • | | | |
| - | | | | | |
| | 1 | | | | |
| - | | | | | |
| - | | | | | E CO |
| 3 | | <u> </u> | FOR EDUCATIONA | AL USE | |
| | | | | | |

| | - | | | | |
|-------------|---|------------------------------|--|--|--|
| | COUL Movin Program | Interrupt Service Routine | | | |
| | execution | Executive Sequence | | | |
| | | | | | |
| | Request device | Strirt TSR | | | |
| | to get recidy | 0.12.61-11-6 | | | |
| | | Save C.P.U Status | | | |
| | | Execute Data | | | |
| | Check next | Transfer Tastruction | | | |
| | Introduction & | | | | |
| | 1 execute data | Bestore | | | |
| | | Processor Status | | | |
| | check for NO | | | | |
| | Interrupt | Enable | | | |
| | | intarupt | | | |
| | Yes | | | | |
| _ | COULTSR ASSOCIAND | Return to | | | |
| | with this interrupt | Main Program | | | |
| | | 1 Dug 2 Francis No. 11 miles | | | |
| <u> </u> | What is the need of DMA? Explain its various techniques of data transfer. | | | | |
| | techniques of data th | ansier | | | |
| Ans | | | | | |
| | | | | | |
| | | | | | |
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DMA Function



DMA Function

- DMA involves an additional module on the system bus. The DMA module (Figure 7.11) is capable of mimicking the processor and, indeed, of taking over control of the system from the processor.
- It needs to do this to transfer data to and from memory over the system bus.
- For this purpose, the DMA module must use the bus only when the processor does not need it, or it must force the processor to suspend operation temporarily.
- The latter technique is more common and is referred to as cycle stealing, because the DMA module in effect steals a bus cycle.

DMA Function

When the processor wishes to read or write a block of data, it issues a command to the DMA module, by sending to the DMA module the following information:

- Whether a read or write is requested, using the read or write control line between the processor and the DMA module
- The address of the I/O device involved, communicated on the data lines
- The starting location in memory to read from or write to, communicated on the data lines and stored by the DMA module in its address register
- The number of words to be read or written, again communicated via the data lines and stored in the data count register

DMA Function

- The processor then continues with other work.
- It has delegated this I/O operation to the DMA module.
- The DMA module transfers the entire block of data, one word at a time, directly to or from memory, without going through the processor.
- When the transfer is complete, the DMA module sends an interrupt signal to the processor.
- Thus, the processor is involved only at the beginning and end of the