Q. P. Code: 39078

(3 Hours) **Total Marks: 80**

N.B.

1. Question No.1 is compulsory
2. Solve any three questions from the remaining questions
3. Assume suitable data if required

1a.	Compare Von Neumann architecture and Harvard Architecture	10
1b.	Explain IEEE 754 floating point representation formats and represent $(34.25)_{10}$ to single precision format.	10
1c	Explain memory hierarchy in the computer system.	
1d	Explain the requirements of the I/O modules.	
2a.	Draw the flowchart of Booth's algorithm. Perform following multiplication using Booth's algorithm M = $(-9)_{10}$ Q= $(6)_{10}$	10
2b.	Explain the restoring method of binary division with algorithm. Divide $(7)_{10}$ by $(4)_{10}$ using restoring method of binary division.	10
3a.	What is the necessity of cache memory? Explain set associative cache mapping	10
3b.	Explain the page address translation in case of virtual memory and explain TLB	10
4a.	Explain interrupt driven I/O method of data transfer.	10
4b.	Explain DMA method of I/O data transfer	10
5a.	Explain the superscalar architecture.	10
5b.	State the functions of control unit. Explain Micro-programmed control unit	10
6	Write short notes on (any two) :-	20
a.	Principle of locality of reference	
b.	Instruction Pipelining and its hazards	
c.	Flynn's Classification	
d.	Bus arbitration	

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(3Hrs) Max Marks: 80

NB: 1. Question No.1 Compulsory.
2. Solve any THREE from Q.2 to Q.6
3. Assume suitable data whenever necessary with justification.

Q1. Answer any four questions

	(A)	Explain Instruction and Instruction Cycle.	(05)
	(B)	Explain Booths algorithm with an example	(05)
	(C)	Give different instruction formats.	(05)
	(D)	Describe the memory hierarchy in the computer system	(05)
	(E)	Explain Superscalar Architecture.	(05)
Q2.	(A)	Explain Branch Predication Logic and delayed branch.	(10)
	(B)	List and explain various data dependencies, data and branch hazards that occur in the computer system.	(10)
Q3.	(A)	A program having 10 instructions (without Branch and Call instructions) is executed on non-pipeline and pipeline processors. All instructions are of same length and having 4 pipeline stages and time required to each stage is 1nsec. i) Calculate time required to execute the program on Non-pipeline and Pipeline processor. ii) Calculate Speedup	(10)
	(B)	What is Microprogram? Write microprogram for following operations. i) ADD R1, M, Register R1 and Memory location M are added and result store at Register R1. ii) MUL R1, R2 Register R1 and Register R2 are multiplied and result store at Register R1.	(10)
Q4.	(A)	Explain Bus Contention and different method to resolve it.	(10)
	(B)	Describe memory segmentation in detail. Explain how address translation is performed in virtual memory.	(10)
Q5.	(A)	State the various types of data transfer techniques. Explain DMA in detail.	(10)
	(B)	Consider a cache memory of 16 words. Each block consists of 4 words. Size of the main memory is 256 bytes. Draw associative mapping and calculate TAG, and WORD size.	(10)
Q6.	(A)	Write short note on Performance measures	(10)
	(B)	Draw and explain floating point addition subtraction algorithm.	(10)

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S.E. SEM IV / COMP / CHOICE BASE / MAY 2019 / 17.05.2019

(3Hrs) Max Marks: 80

NB: 1. Question No.1 Compulsory.
2. Solve any THREE from Q.2 to Q.6
3. Assume suitable data whenever necessary with justification.

Q1. Answer any FOUR questions

(A) Explain Instruction and Instruction Cycle. (05)

(B) Differentiate between Memory Mapped IO and IO Mapped IO. (05)

(C) Give different instruction formats. (05)

(D) Explain Memory Interleaving Techniques. (05)

(E) Explain Superscalar Architecture. (05)

Q2. (A) Explain Branch Predication Logic and delayed branch. (10)

(B) A program having 10 instructions (without Branch and Call instructions) is executed on non-pipeline and pipeline processors. All instructions are of same length and having 4 pipeline stages and time required to each stage is 1nsec. (10)

i) Calculate time required to execute the program on Non-pipeline and Pipeline processor.

ii) Calculate Speedup.

Q3. (A) Explain different technique for design of control unit of computer. (10)

(B) What is Microprogram? Write microprogram for following operations. (10)

i) ADD R1, M, Register R1 and Memory location M are added and result store at Register R1.

ii) MUL R1, R2 Register R1 and Register R2 are multiplied and result store at Register R1.

Q4. (A) Explain Bus Contention and different method to resolve it. (10)

(B) Explain different data transfer technique. (10)

Q5. (A) Explain Booth's Multiplication algorithm and Perform $(17)_{10}$ X $(5)_{10}$. (10)

(B) Consider a cache memory of 16 words. Each block consists of 4 words. Size of the main memory is 256 bytes. Draw associative mapping and calculate TAG, and WORD size. (10)

Q6. (A) Explain different type of pipeline hazards. (10)

(B) Draw and explain floating point addition subtraction algorithm. (10)

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(3 Hours) **[Total Marks: 80]**

NB: 1. Question No.1 Compulsory.

2. Solve any THREE from Q.2 to Q.6

3. Assume suitable data whenever necessary with justification.

Q.1 Answer **any four** questions

(a) Describe the memory hierarchy in the computer system [05]

(b) Give different instruction formats. [05]

(c) Explain principle of locality of reference in detail [05]

(d) Differentiate between Memory Mapped IO and IO Mapped IO. [05]

(e) Explain Superscalar Architecture. [05]

Q.2 (a) A program having 10 instructions (without Branch and Call instructions) is executed on non-pipeline and pipeline processors. All instructions are of same length and having 4 pipeline stages and time required to each stage is 1nsec. [10]

i. Calculate time required to execute the program on Non-pipeline and Pipeline processor.

ii. Calculate Speedup.

(b) With a neat diagram , explain branch prediction in detail. [10]

Q.3. (a) Explain page address translation with respect to virtual memory and further explain TLB in detail. [10]

(b) What is "Microprogram"? Write microprogram for following operations. [10]

i. ADD R1, M, Register R1 and Memory location M are added and result store at Register R1.

ii. MUL R1, R2 Register R1 and Register R2 are multiplied and result store at Register R1.

Q.4 (a) Explain Bus Contention and different method to resolve it. [10]

(b) Define instruction pipelining and its various hazards in detail. [10]

Q.5. (a) Explain multi core processor architecture in detail [10]

(b) Explain Booth's Multiplication algorithm and Perform $(17)_{10}$ X $(-5)_{10}$. [10]

Q.6 Write short notes on any **two** [20]

(a) Data transfer techniques

(b) Set associative cache mapping

(c) Flynn's Classification

(d) Control unit of processor
