

- EE690 -  
Embedded Systems Design  
MidSem Paper  
Assignment

(1)

Q1) a) Yes, as the credit card chip contains an ~~embed~~ embedded computer system for providing additional security during transactions.

Q1) b) Operating System Based: Digital Heads-Up Displays in cars  
Infotainment systems in vehicles

Non-Operating System based: Vehicle ~~to~~ braking system  
ECU for monitoring engine parameters

Q1) c) Yes. If the required functionalities can be achieved using analog ICs, then microcontrollers/microprocessors can be avoided.  
eg) Analog Oscilloscopes, TL494 based PWM generation,  
OpAmp based comparators.

Q2a) Von Neumann

Q2b) 32 bit refers to the data bus width / ALU width

Q2c) a) 4 bit  $\rightarrow$  Intel 4004

b) 8 bit  $\rightarrow$  8085

c) 16 bit  $\rightarrow$  8086, AVR based

d) 32 bit  $\rightarrow$  STM32, ~~ARM~~ Arm Cortex M4 based

Q3a) Flash, EEPROM, ~~ROM~~ ROM, PROM, UV-PROM

Q3b) 32 bit wide data bus; 17 bit wide address bus.

Q4) a) Instruction Set Encoding:

Identical, as all 3 controllers have the same core,  
i.e., Arm Cortex M4F

b) Memory Map:

Non identical, as memory mapping will depend on memory type  
and size of memory paired with CPU.

c) SysTick Registers:

~~Not~~ Identical, as SysTick is a part of the CPU ~~itself~~  
core itself

d) Number of GPIO pins

Non Identical, as number of GPIO pins may vary ~~with~~  
with chip design

e) Clock speed

Non identical, as even though the max clock speed of  
ARM cortex M4 may be 80MHz, it can be lowered by  
chip manufacturers to meet application requirements.

Q5) Benefits of thumb mode:

1) Lesser memory needed to store ~~the~~ thumb instructions (16bit)  
at compared to 32 bit instructions.

2) Ability to fetch higher ~~number~~ number of thumb instructions  
as ~~compared~~ compared to 32 bit instructions for a given bus width.

## Q6) Relative Jump:

- Relative jumps are limited to a smaller address range
- They are to be used for jumping to address locations close to current address location
- They are faster to ~~are~~ execute

## Absolute Jump:

- Absolute jumps are not limited by any address range, and can jump to any ~~location~~ location specified by the program
- They are to be used for ~~jump~~ jumping to address locations present at any location in the code, and not just nearby locations
- They are slower to execute.
- They are to be used if a jump to a ~~to~~ particular location is needed from different locations in the code.

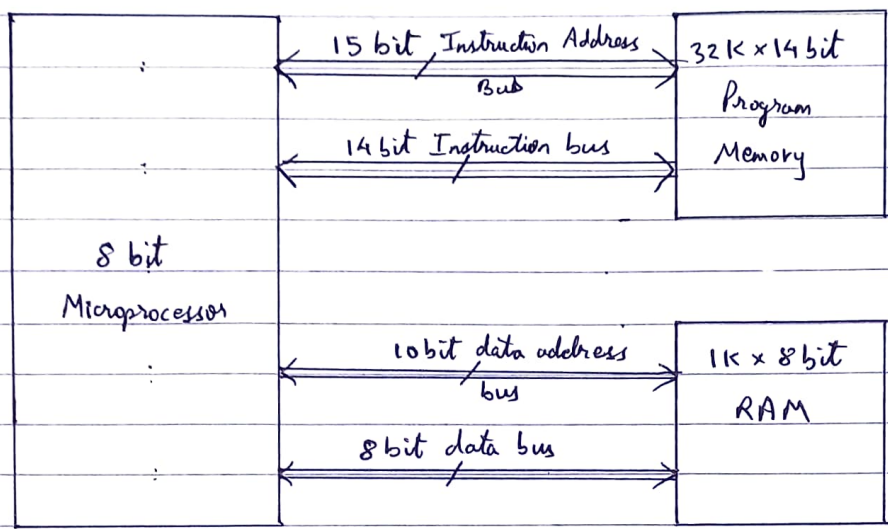
Q7) ~~0x3F~~ → 0x3F → 00  
~~0x303~~ 0x3E → 00  
 0x3D → 04  
 0x3C → F8

## Q8) Embedded toolchain Components :

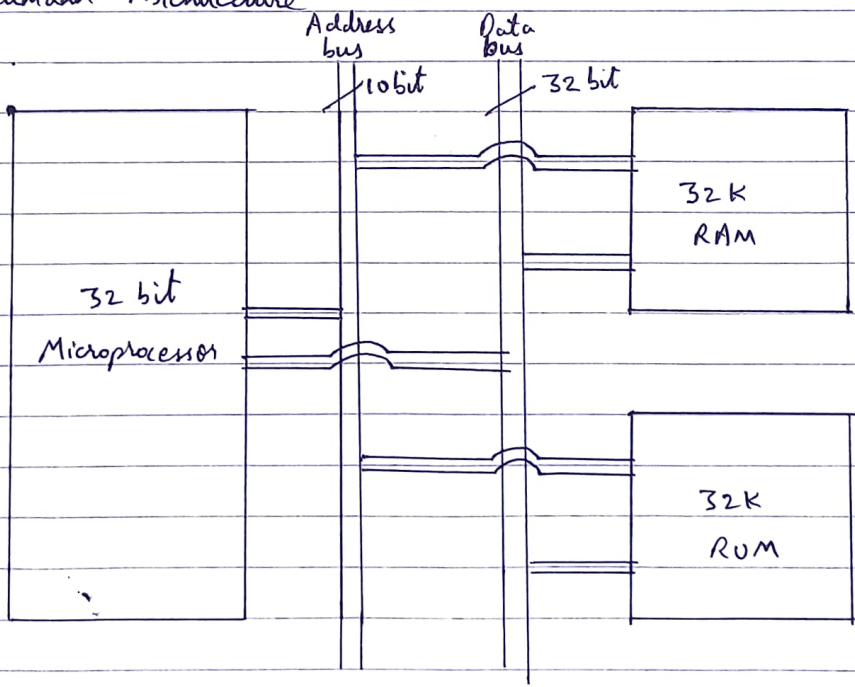
Editor, Compiler, Debugger, Assembler, linker, flasher

## Q9) Hash number, Branch

Q10) Harvard Architecture



Von Neumann Architecture



$32K = 10K \times 32 \text{ bit}$

~~$32K = 10K \times 32 \text{ bit}$~~

(5)

Q11) 16 bit ALU operating on 16 bit instructions with 16 registers ( $R_0$  to  $R_{15}$ )  
 Functions: Add, Subtract, And, Or, Not, XOR

Solution: Use hex instruction coding, encoding, where the encoded instruction has the format  $0x\text{----}$   
 Let  $0x\text{----}$  be  $0xabcd$

$a$ : Range =  $0-F$ , where 'a' is mapped to registers  $R_0$  to  $R_{15}$  and

eg:  $a=0 \rightarrow R_0$

$a=1 \rightarrow R_1$

$a=2 \rightarrow R_2$

$\vdots$

$a=F \rightarrow R_{15}$

$a$  holds operand 1

$b$ : Range =  $0-F$ , where 'b' is mapped to registers  $R_0$  to  $R_{15}$  similar to 'a'

$b$  holds operand 2

$c$ : Range =  $0-F$ , where 'c' is mapped to registers  $R_0$  to  $R_{15}$  similar to 'a'

$c$  holds destination register.

$d$ : Range =  $0-5$ , where  $d=0 \rightarrow \text{ADD}$

$d=1 \rightarrow \text{SUBTRACT}$

$d=2 \rightarrow \text{AND}$

$d=3 \rightarrow \text{OR}$

$d=4 \rightarrow \text{NOT}$

$d=5 \rightarrow \text{XOR}$

Note: for  $d=4$ ; NOT operation, the operation occurs only on operand 1 and operand 2 is ignored. The output is stored in destination register.

eg) Add  $R_0$  and  $R_1$ ; store in  $R_2$

encoded instruction:  ~~$0x1020$~~   
 $0x0120$

eg) XOR  $R_2$ ,  $R_3$ ; store in  $R_{14}$

encoded instruction:  $0x23E5$

Bits:  $[15:12]$   $[11:8]$   $[7:4]$   $[3:0]$

↓  
operand  
1

↓  
operand  
2

↓  
Destination

↓  
operation



Q12 Let Operand 1 be stored in <sup>locations</sup> registers  $w_3, w_2, w_1, w_0$   
 Let Operand 2 be stored in locations  $x_3, x_2, x_1, x_0$   
 Let the sum be stored in locations  $z_3, z_2, z_1, z_0$

$$\begin{array}{r} \text{Addition: } w_3 \quad w_2 \quad w_1 \quad w_0 \\ + \quad x_3 \quad x_2 \quad x_1 \quad x_0 \\ \hline z_3 \quad z_2 \quad z_1 \quad z_0 \end{array}$$

Let registers used for storing operands be  $R_0 - R_{11}$

Let register  $R_{12}$  be used to store address of memory

Assume  $w_0, w_1, w_2, w_3, x_0, x_1, x_2, x_3, z_0, z_1, z_2, z_3$  are stored in a continuous manner.

// $R_{12}$ contains the address of register $w_0$	$R_{11}$	$z_3$
<del>Load <math>R_0</math> <math>E</math></del>	$R_{10}$	$z_2$
LOAD $R_0$ [ $R_{12}$ ] // Load $w_0$	$R_9$	$z_1$
ADD $R_{12}$ #4 // Go to next memory location ( $w_1$ )	$R_8$	$z_0$
LOAD $R_1$ [ $R_{12}$ ] // Load $w_1$	$R_7$	$x_3$
ADD $R_{12}$ #4 // Next Location	$R_6$	$x_2$
LOAD $R_2$ [ $R_{12}$ ] // Load $w_2$	$R_5$	$x_1$
ADD $R_{12}$ #4 // Next Location	$R_4$	$x_0$
LOAD $R_3$ [ $R_{12}$ ] // Load $w_3$	$R_3$	$w_3$
ADD $R_{12}$ #4 // Next Location	$R_2$	$w_2$
LOAD $R_4$ [ $R_{12}$ ] // Load $x_0$	$R_1$	$w_1$
<del>ADD <math>R_5</math> [<math>R_{12}</math>]</del>	$R_0$	$w_0$
ADD $R_{12}$ #4 // Next location		
LOAD $R_5$ [ $R_{12}$ ] // Load $x_1$		
ADD $R_{12}$ #4 // Next location		
LOAD $R_6$ [ $R_{12}$ ] // Load $x_2$		
ADD $R_{12}$ #4 // Next location		
LOAD $R_7$ [ $R_{12}$ ] // Load $x_3$		

ADD R12 #4 // Point to result

ADD R8 R0 R4 //  $R8 = R0 + R4$

ADDC R9 R1 R5 //  $R9 = R1 + R5 + \text{Carry}$

ADDC R10 R2 R6 //  $R10 = R2 + R6 + \text{Carry}$

ADDC R11 R3 R7 //  $R11 = R3 + R7 + \text{Carry}$

// Store final result

STORE R8 [R12] // Stores Z0

ADD R12 #4

STORE R9 [R12] // Stores Z1

ADD R12 #4

STORE R10 [R12] // Stores Z2

ADD R12 #4

STORE R11 [R12] // Stores Z3

Q13) 16 bit memory; 16 bit wide address bus

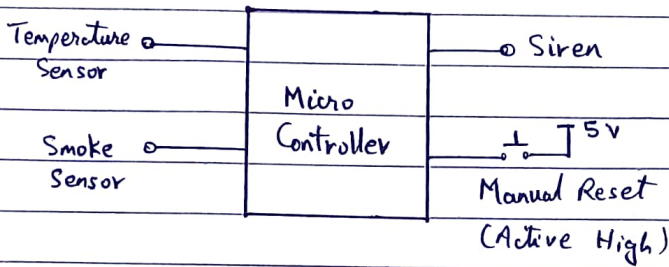
$\hookrightarrow \text{max address} = 2^{16} = 0xFFFF$

Type	Start Address	End Address	Length
IVT	0 (0x0)	63 (0x3F)	64
Unused	64 (0x40)		
SRAM	0x2000	0x3FFF	8192
Unused	0x4000		
IO	0x6000	0x61FF	512
Unused	0x6200		
Flash	0x8000	0xFFFF	32K = 0x8000

IVT	0x00 0x3F
Unused	
SRAM	0x2000 0x3FFF
Unused	
IO	0x6000 0x61FF
Unused	
Flash	0x8000 0xFFFF



Q14 Hardware Requirements: Temperature Sensor  
Smoke Sensor  
Manual Reset  
Siren  
Microcontroller



- High level description:

Smoke detected AND Fire detected  $\rightarrow$  Siren immediately activates

Smoke OR Fire  $\rightarrow$  wait for 5 seconds  $\rightarrow$  Sensor still detects  $\rightarrow$  Siren activated

Siren can be deactivated only through manual reset

On sensor activation, 1ms delay and recheck is done to prevent false positive based siren triggering

State Flow Diagram:

S = smoke  
F = Fire

