Design and analysis of Zaung Full Adder

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***Abstract*—In the realm of digital electronics and computer engineering, a full adder is a pivotal component. It is an essential building block for performing binary addition, a fundamental operation in digital computing. A full adder is a combinational logic circuit designed to add two binary numbers together while accounting for any carry bits from previous addition operations.**

Keywords—component, formatting, style, styling, insert (key words**)**

I. Introduction

At its core, a full adder takes three binary inputs: two single-digit binary numbers (usually denoted as A and B) and a carry-in bit (often designated as Cin). It then produces two outputs: the sum of the inputs (Sum) and a carry-out bit (Cout). The output Sum represents the result of adding A, B, and the carry-in Cin, while Cout represents the carry generated by the addition.

The full adder can be implemented using a variety of logic gates, but the most common implementation uses two XOR gates and an AND gate. The XOR gates are used to calculate the sum and carry bits, while the AND gate is used to generate the carry-out bit.

The truth table for a full adder is as follows:

Table 1. Logic table of a full adder

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

II. Zaung Fulladder

The Zaung full adder is a type of full adder that was invented by Khaing Min Zaung in 2009. It is a two-level full adder that is more efficient than the traditional three-level full adder in terms of power consumption and delay.

The Zaung full adder is implemented using two XOR gates and two AND gates. The first XOR gate calculates the sum bit, and the second XOR gate calculates the carry-out bit. The two AND gates are used to generate the intermediate signals that are needed by the XOR gates..

The Zaung full adder has a number of advantages over the traditional three-level full adder, including:

Lower power consumption: The Zaung full adder consumes less power than the traditional three-level full adder because it has fewer logic gates.

Shorter delay: The Zaung full adder has a shorter delay than the traditional three-level full adder because it has fewer logic levels.

Smaller area: The Zaung full adder occupies a smaller area than the traditional three-level full adder because it has fewer transistors.

The Zaung full adder is a promising new type of full adder that has the potential to be used in a wide variety of digital applications, such as CPUs, calculators, DSPs, and memory.

The diagram of fulladder is given as:

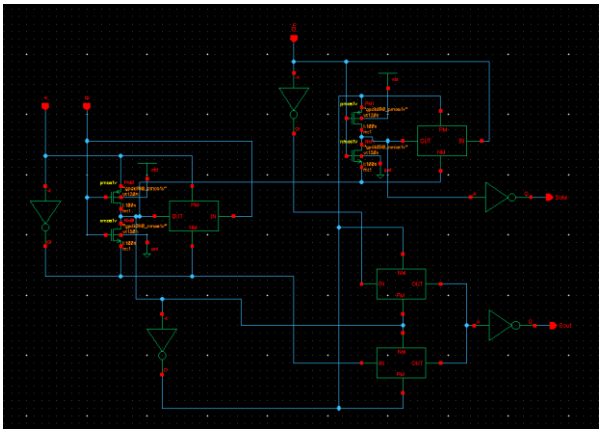

Figure 1. Zaung fulladder schematic

III. Testbench

The ADE-L window in Cadence Virtuoso is a graphical user interface (GUI) for running and analyzing simulations. It provides a variety of features for creating, running, and analyzing simulations, including:

- A schematic editor for creating and editing simulation circuits
- A waveform viewer for viewing the results of simulations
- A parameter editor for setting the parameters of simulations

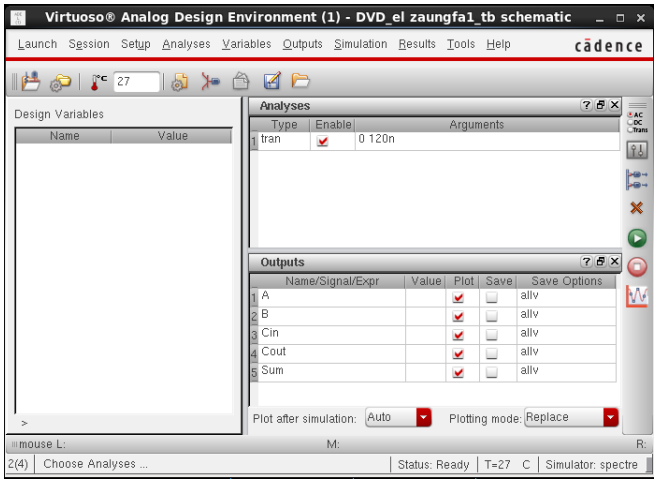

Fig 2.ADEL Window

some of the benefits of using the ADE-L window in Cadence Virtuoso:

- The ADE-L window provides a graphical user interface for running and analyzing simulations, which is easy to use and learn.
- The ADE-L window provides a variety of features for creating, running, and analyzing simulations, which makes it a powerful tool for design engineers.
- The ADE-L window is integrated with Cadence Virtuoso, which makes it easy to use the ADE-L window to simulate circuits that have been designed in Cadence Virtuoso.

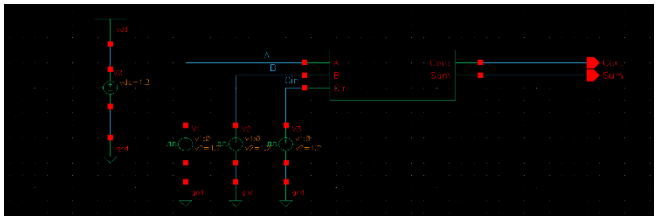

Figure 3. Testbench layout of Zaung Full Adder

A. Design Specifications

The table 2 is used to describe the design of a digital circuit, such as a full adder. The values of the parameters can be used to simulate the circuit and to verify its functionality.

Fig 2. Design Specifications of Zaung Full Adder

Library	Cell name	Parameter 1	Value 1	Parameter 2	Value 2	Parameter 3	Value 3	Delay
gpdk045	nmos1V	W	120nm	L	45nm	-	-	
gpdk045	pmos1V	W	120nm	L	45nm	-	-	
analoglib	vdd	-	-	-	-	-	-	
analoglib	vdc	V	1.2 V	-	-	-	-	
analoglib	gnd	-	-	-	-	-	-	
analoglib	Vpulse(A)	V2	1.2 V	Period	40n s	Pulse width	16n s	8n s
analoglib	Vpulse(B)	V2	1.2 V	Period	40n s	Pulse width	12n s	4n s
analoglib	Vpulse (Cin)	V2	1.2 V	Period	40n s	Pulse width	15n s	10n s

IV. RESULTS

The final simulation of the circuit provides the waveform simulated from cadence virtuoso and helps us to verify the functioning of the fulladder , as shown in the figure 4.

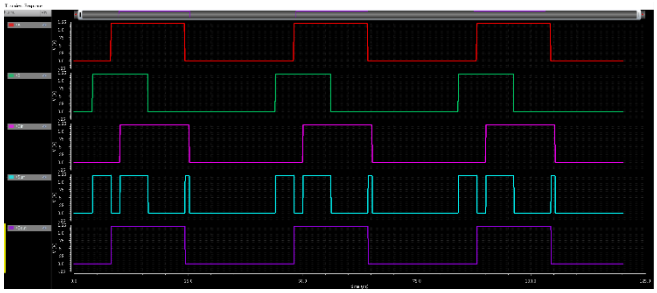

Figure 4. Output wave of the Simulation.