3.5.2 Arithmetic Group

→ This group of instructions perform arithmetic operations such as addition, subtraction, increment and decrement.

→ The arithmetic group of instructions include following instructions:

	No of Byte	Machine Cycle (MC)	T-State	Addressing Mode (AM)
1.) ADD R	1 Byte	1 MC (OF)	4T	Register AM.
2.) ADD M	1 Byte	2 MC (OF + MR)	4T + 3T = 7T	Indirect AM
3.) ADC R	1 Byte	1 MC (OF)	4T	Register AM
4.) ADC M	1 Byte	2 MC (OF + MR)	4T + 3T = 7T	Indirect AM
5.) ADI data	2 Byte	2 MC (OF + MR)	4T + 3T = 7T	Immediate AM
6.) ACI data	2 Byte	2 MC (OF + MR)	4T + 3T = 7T	Immediate AM
7.) DAD Rp	1 Byte	3 MC (OF + BI + BI)	4T + 3T + 3T = 10T	Register AM
8.) SUB R	1 Byte	1 MC (OF)	4T	Register AM
9.) SUB M	1 Byte	2 MC (OF + MR)	4T + 3T = 7T	Indirect AM
10.) SBB R	1 Byte	1 MC (OF)	4T	Register AM
11.) SBB M	1 Byte	2 MC (OF + MR)	4T + 3T = 7T	Indirect AM
12.) SUI data	2 Byte	2 MC (OF + MR)	4T + 3T = 7T	Immediate AM
13.) SBI data	2 Byte	2 MC (OF + MR)	4T + 3T = 7T	Immediate AM.
14.) DAA	1 Byte	1 MC (OF)	4T	Implicit AM
15.) INR R	1 Byte	1 MC (OF)	4T	Register AM.
16.) INR M	1 Byte	3 MC (OF + MR + MW)	4T + 3T + 3T = 10T	Indirect AM.
17.) DCR R	1 Byte	1 MC (OF)	4T	Register AM
18.) DCR M	1 Byte	3 MC (OF + MR + MW)	4T + 3T + 3T = 10T	Indirect AM
19.) INX Rp	1 Byte	1 MC (OF)	6T	Register AM
20.) DCX Rp	1 Byte	1 MC (OF)	6T	Register AM.

1. ADD R

Mnemonic	ADD R
Operation	A = A + R
No. of Bytes	1 byte
Machine Cycles	1 (OF)

Algorithm	A ← A + R
Flags	All the flags are modified.
Addr. Mode	Register addressing mode
T-states	4

Ex: 3.3.2.1

The contents of the accumulator are 93H and the contents of register C are B7H. Add both contents.

Instruction ADD C

		CY	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
(A)	93H =		1	0	0	1	0	0	1	1	
(C)	B7H =		1	0	1	1	0	1	1	1	Carry
		1		1	1		1	1	1		
SUM (A)	= 1 4AH =	1	0	1	0	0	1	0	1	0	
		CY									

Flag Status: S = 0, Z = 0, CY = 1

Arithmetic Operations :-

→ addition } performed in relation to the contents of
→ subtraction } accumulator
→ increment } performed in any reg.
→ Decrement }

INR & DCR :-

1.) affect the contents of the specified reg.
2.) affect all flags except the CY flag

ADD & SUB :-

1.) the accumulator is one of the operands
2.) modify all the flags according to the data conditions of the result
3.) place the result in accumulator
4.) do not affect the contents of the operand reg.

(1) ADD R
→ Add (1 byte inst')
→ Adds the contents of reg R to the contents of the accumulator

(2) ADI 8-bit
→ Add immediate (2-byte)
→ Add second byte to the contents of the accumulator

(3) SUB R
→ Subtract (1-byte)
→ Subtract the contents of reg R from the contents of accumulator

(4) SUI 8-bit
→ Subtract immediate (2-byte)
→ Subtract 2nd byte from contents of accumulator

Q-1 The contents of accumulator are 93H & the contents of reg C are B7H. Add both contents.

Ans ADD C

```
                    1 11
(A) → 93H =  1001 0011
    +
(C) → B7H =  1011 0111
             ---------
(A) → 4AH  [1] 0100 1010
                4    A
```

S	Z		AC		P		CY
0	0		0		1		1
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Q-2 Assume the accumulator holds the data byte FFH Illustrate the differences in the flags set by adding 01H & by incrementing the accumulator contents.

Ans ADI 01H

```
(A) : FFH =  1111 1111
        +
(Data): 01H = 0000 0001
             ---------
(A) :      [1] 0000 0000
           CY   0    0H
```

flag : S=0, Z=1, AC=1, P=0, CY=1

INR A

flag : S=0, Z=1, CY= NA , AC=

(5) INR R → Increment (1-byte)
→ increase the contents of reg R by 1
(All flags except the CY are affected)

DCR R → Decrement (1 byte)
→ decrease the contents of reg R by 1

ex°1 the contents of accumulator are 93H & the contents of reg C are B7H, Add ADD C

ex-2 ADI 01H A → FFH

Problem statement

1. Load the no. BBH in reg D
2. Load the no. 6FH in reg C
3. Inc. reg C by one
4. Add the contents of reg C & D and display the sum at o/p port 01H

```
MVI  D, BBH
MVI  C, 6FH
INR  C          Add 6F + 01 = 70 H
MOV  A, C
ADD  D          70 + BB = FB H
OUT  01H        S=1, Z=0, CY=0
HLT
```

Ex: Register B has 65H and the accumulator has 97H. Subtract the contents of register B from the contents of the accumulator.

B = 65H
A = 97H

sol^n SUB B (A ⇐ A − B)

Step 1 :- Subtrahend B = 65H ⇒ 0110 0101

2's compl of 65H ⇒ 1001 1010

+ 01 ⇒ + 0000 0001

1001 1011

Step 2 :- Add 97 ⇒ + 1001 0111

Step 3 :- CY [1] 0011 0010

[0] 3 2

Step 4 :- Complement carry

Result A = 32H

Flag status S=0, Z=0, CY=0

Note :-

→ Ans is -ve, it will be 2's compl of actual magnitude.

ex: 65 − 97H

→ Ans will be 2's compl of result 32H with the Carry (Borrow) flag set

Result :- CY [1] 1100 1110

Arithmetic Instructions :-

1.) ADD M :- Add Memory

→ 1-byte instruction
→ Adds M to A and stores result in A
→ Memory location - HL reg.

2.) SUB M :-

→ 1-byte inst^n
→ Subtracts M from A & stores result in A

3.) INR M :-

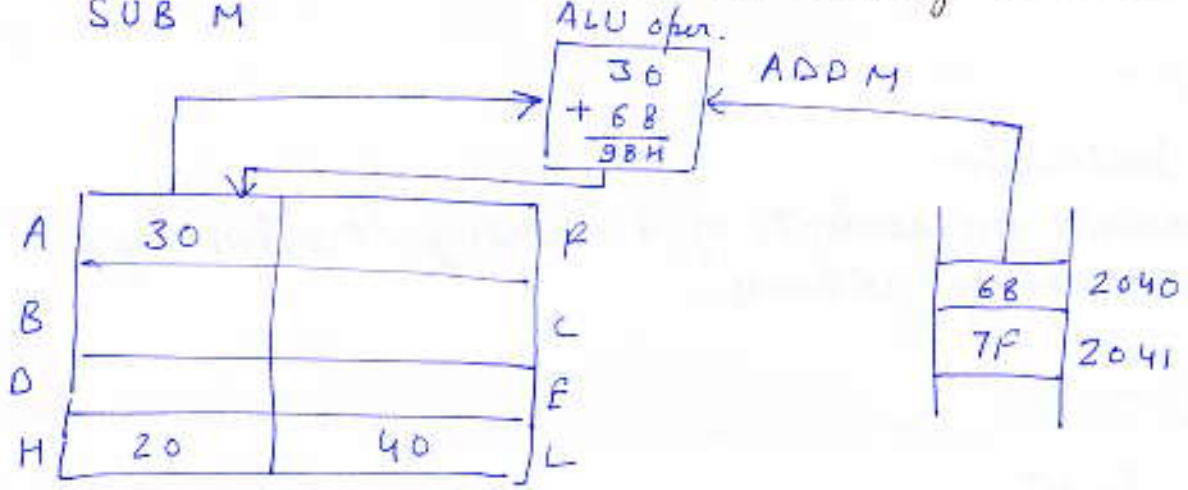
→ 1-byte instruction
→ It increments the contents of a memory location by 1. not the memory address.

4.) DCR M :-

→ 1 byte inst^t
→ Decrement M by 1

Q1 Write inst^n to add the contents of the memory location 2040H to A, & subtract the contents of the memory location 2041H from the 1st sum. Assume A = 30H & memory location 2040H has 68H & the location 2041H has 7FH.

```
LXI H, 2040H  → Load HL reg. pair
ADD M         → add 68H, content of mem 2040H
INX H         → points next memory location
SUB M
```



Q2 1) load 59H in memory location 2040H & inc. the contents of the memory location

2.) load 90H in memory location 2041H & dec. the contents of the memory location.

```
LXI H, 2040H
MVI M, 59H
INR M   → 59H + 1 = 5AH
INX H   → 2040H → 2041
MVI M, 90H
DCR M
```

INX Rp :- Increment Register Pair

→ 1-byte instruction
→ It treats the contents of two registers as one 16-bit no. & increases the contents by 1.

INX B / INX D / INX H / INX SP

DCX Rp :- Decrement Register Pair

→ 1-byte instruction
→ Decreases the 16-bit contents of a register pair by 1.

DCX B / DCX D / DCX H / DCX SP

ADC :- Addition with carry.

ADC R
ADC M
ACI 8-bit

} add the contents of operand, carry & accumulator.

SBB :- Subtraction with carry.

SBB R
SBB M
SBI 8-bit

} sub the contents of operand & borrow from the contents of accumulator.

DAD :- Double reg. add (1 byte)

→ Adds the contents of operand to the contents of HL reg.
→ result is placed in HL reg.

DAD Rp | DAD H
DAD B | DAD SP

Reg. BC contain 2793H & reg. DE contain 3182H. Write instr to add these two 16-bit no, & place the sum in memory location 2050H & 2051H.

B	27	93	C
D	31	82	E

MOV A, C
ADD E
MOV A, A
MOV A, B
ADC D
MOV H, A
SHLD 2050H

A	93		F
A	15	CY=1	F
H		15	L

H	59	15	L

93H
+ 82H
1 15H

27H
+ 31H
59H

CMC :- Complement the carry flag

If carry flag is 1, it is reset
0, " " set

STC :- Set the carry flag

XTHL :- Exchange top of the stack with H & L.

SPHL :- Copy HL into Stack Pointer Reg.

PCHL :- Copy HL into P.C

BCD Addition :-

Add two packed BCD no's : 77 & 48

```
  77 = 0111  0111
+ 48 = 0100  1000
-------------------
 125 = 1011  1111
           + 0110
-------------------
      CY=[1] 0101
         + 0110
-------------------
CY=[1] 0010 0101
```

DAA :- (Decimal Adjust Accumulator)

→ 1-byte
→ adjust an 8-bit no. in accumulator to form two BCD no's by
→ uses AC & CY flags
→ All flags are affected

SOLVED PROBLEMS :-

Ex-3.3.2.10 Specify the register content and flag status of following instructions are executed specify the output at port0.

Ans

Initial Conditions	A	B	S	Z	CY	PORT0
	00	ff	0	1	0	XX
MVI A, F2H	F2	ff	0	1	0	XX
MVI B, 7AH	F2	7A	0	1	0	XX
ADD B	6C	7A	0	0	1	XX
OUT PORT0	6C	7A	0	0	1	6C
HLT						

Ex-3.3.2.11

Ex: What operation can be performed using the instruction ADD A?

Ans The instruction ADD A will add the content of accumulator to itself, this is equivalent to multiplying by 2. (A ← A+A)

Ex-3.3.3.12

What operations can be performed by using the instruction SUB A? Specify the status of Z and CY

Ans The instruction SUBA will clear the accumulator. The status will be

CY = 0

Z = 1

Ex-3.3.2.13

Specify the register contents and the flag status as the following instructions are

		A	C	S	Z	CY
MVI A, 5EH	I.C -	XX	XX	0	0	0
ADI A2H		5EH	XX	0	0	0
MOV CA		00H	XX	0	1	1
HLT		00H	00H	0	1	1

Ex-3.3.2.14

Write a program using ADI instruction to add the two hexadecimal numbers 3AH and 48H and to display the answer at an output port

Ans

	A	PORT1
IC:-	XX	XX
MVI A, 3AH ;	3AH	XX
ADI 48H	82H	XX
OUT PORT1	82H	82H
HLT		

Output

A = 0011 1010 (3A)
+ 0100 1000 (48)
1000 0010
(82H)

Ex-3.3.2.15

Write instruction to

a) to load 00H in the accumulator
b) decrement the accumulator
c) display the answer

Ans

	A	PORT0
IC:-	XX	XX
MVI A, 00H	00H	XX
DCR A	FFH	XX
OUT PORT0	FFH	FFH
HLT		

Output

A = 0000 0000
2's comp of 01H 1111 1111
(FFH)

The instruction DCR does not set CY flag

Ans = FFH