BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

CSE210 (Computer Architecture Sessional), July 2025 Term
All Lab Sections

Specification for Floating Point Adder Simulation

In this assignment, you are required to design a floating point adder circuit which takes two floating points as inputs and provides their sum, another floating point as output. Each floating point will be 16 bits long with the following representation:

Sign	Exponent	Fraction
1 bit	4 bits	11 bits

You have to implement your design in any simulator software of your choice. Please note that, you can directly use adder and subtractor (instead of an ALU) from the simulator wherever needed.

Submission Guideline

- Soft copy Submission: Submit your assignment on Moodle. You have submit two files. 1) Block diagram of your design in pdf format, 2) simulation project files. Make a zip folder named *Subsection No - Group No.* and submit this folder. Please ensure a single submission from each group.
  Submission Deadline: For all lab groups: February 07, 2026 (Saturday) at 10.00 pm.
- Report Submission: Hard copy will be submitted on the respective lab time. The report should include the Block diagram and an example of step by step simulation of adding any two input numbers according to your design. During the evaluation, you have to demonstrate the process by showing intermediate results.
- For any query, please reach to rimpi@cse.buet.ac.bd.