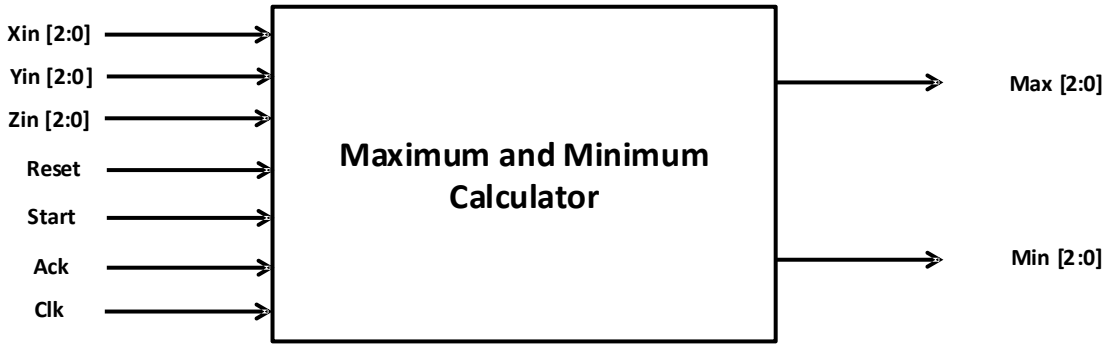
Maximum Minimum Calculator (10%)

In this assignment you are requested to design a HLSM for a digital system that receives ***three 3-bit unsigned numbers*** (i.e. Xin, Yin, and Zin) and produces ***two 3-bit outputs*** that represent the maximum and the minimum of the three inputs.

The following block diagram shows the inputs and outputs of the system:



- At "Reset", the system should ***asynchronously*** proceed to an INITIAL state and wait for the "Start" signal to become active.

- In the INITIAL state, the input numbers ***must*** be stored in local registers.

- Once the "Start" signal is active, the system proceeds to calculate the values of the two outputs.

- After the calculation is complete, the system proceeds to the DONE state and remains until the "Ack" signal becomes active, at which time the system returns back to the INITIAL state.

You should design two versions of this system: ***Moore*** design and ***Mealy*** design.

Here is what you need to submit:

1. ***Max_Min_3_Moore.v***: This Verilog file should include your RTL design of the calculator system implemented as a *Moore* HLSM. Your control unit (CU) and data path unit (DPU) must be implemented using a *single* always procedural block. The name of your module should be Max_Min_3_Moore. *Assume that there are only two comparators allocated to the datapath of the system. Hence, in any state a maximum of two comparisons can be performed.*

2. ***Max_Min_3_Mealy.v***: This Verilog file should include your RTL design of the calculator system implemented as a *Mealy* HLSM. Your control unit (CU) and data path unit (DPU) must be implemented using a *single* always procedural block. The name of your module should be Max_Min_3_Mealy. *Assume that there are only three comparators allocated to the datapath*

of the system. Hence, in any state a maximum of three comparisons can be performed. Your design should contain at most 5 states including INITIAL and DONE states.

3. ***Max_Min_3_TB.v***: This Verilog file should serve as a testbench that instantiates the two versions of the calculator system and generates appropriate stimulus to test them. *The testbench should print the total number of clock cycles (ignore the cycles spent in the INITIAL and DONE states) and the output values for the two versions on the command window of ModelSim.*

4. A file which that shows the HLSM for the Moore and the Mealy designs. You can submit a clear image of your handwritten drawings.

Submission details and deadline:

- Tuesday, June 8th @ 11:59 PM.
- A maximum of two students can work together **and submit one set of files**.
- You must submit your files on Teams as a single zipped file which must be named as ***Max_Min_3_ID1_ID2.zip***. For example, if the students with the following IDs: 0150334 and 0183947 are working together, then their submitted file should be named: ***Max_Min_3_0150334_0183947.zip***.