

1	D0	VCC	24
2	D1	$\overline{\text{CS}}$	23
3	D2	$\overline{\text{WR}}$	22
4	D3	A15	21
5	D4	A14	20
6	AA13	A13	19
7	AA14	RA14	18
8	$\overline{\text{RAM_CS}}$	RA15	17
9	RAM_CS	RA16	16
10	$\overline{\text{RESET}}$	RA17	15
11	$\overline{\text{RD}}$	RA18	14
12	GND	$\overline{\text{ROM_CS}}$	13