Tarea #991 - Circuitos digitales

ALUMNO: Adolfo Tun Dzul

Compuerta NOT

Diagrama

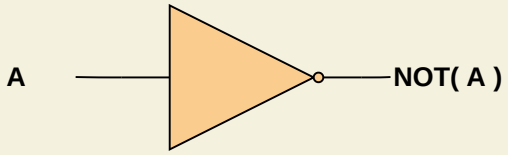
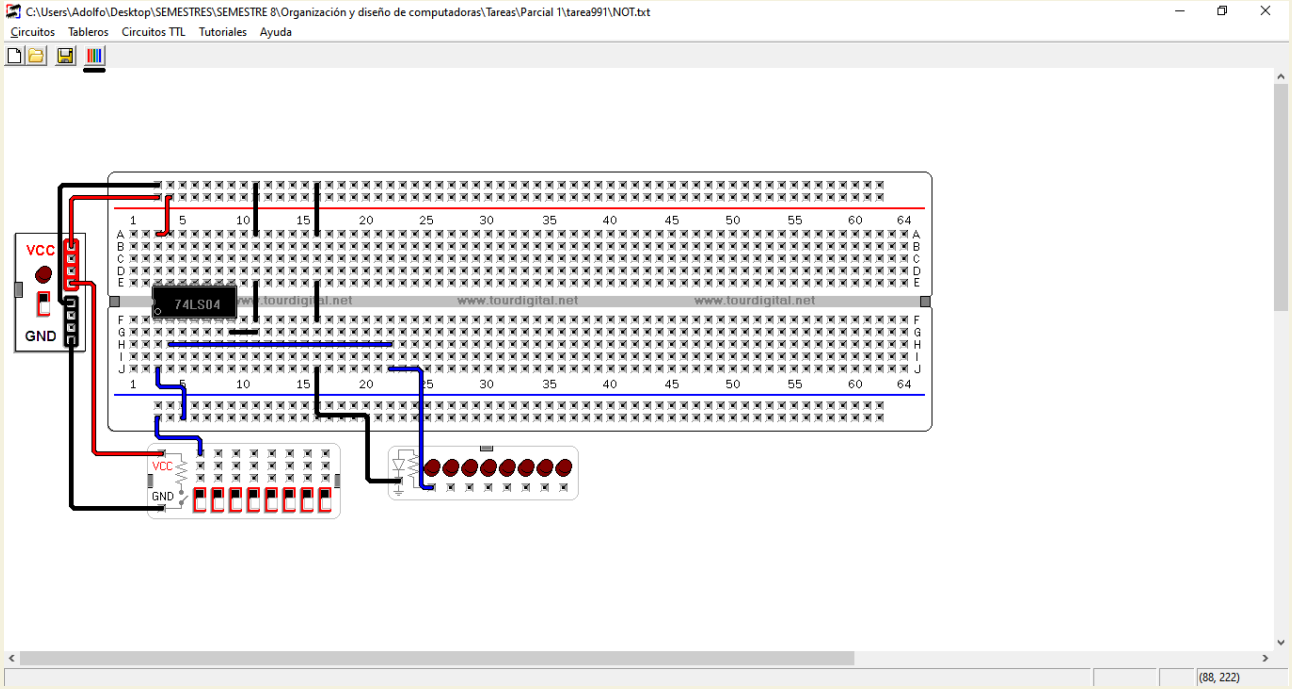


Tabla de Verdad

a	Output
0	1
1	0

Captura de pantalla del Circuito NOT



Compuerta AND - 2 entradas

Diagrama

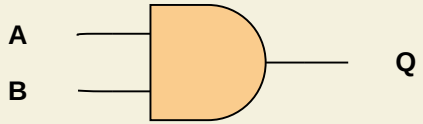
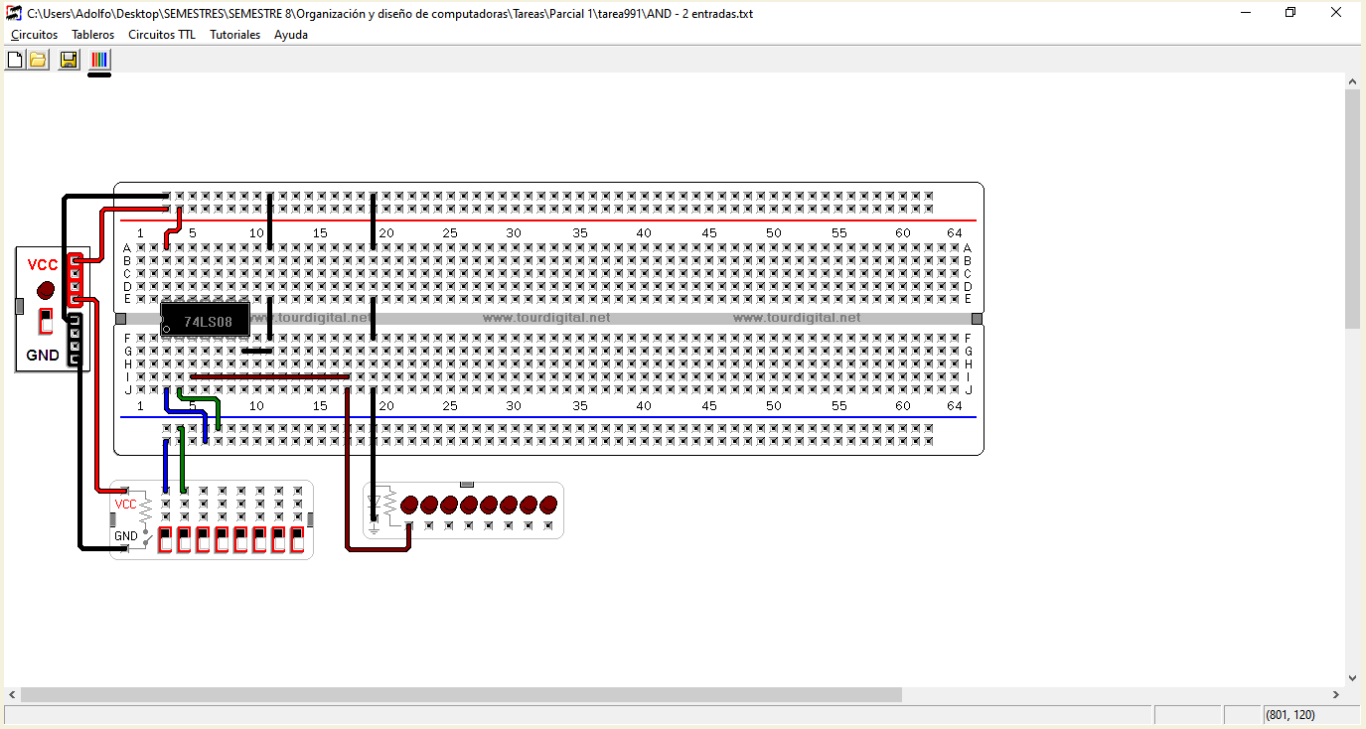


Tabla de Verdad

a	b	Output
0	0	0
0	1	0
1	0	0
1	1	1

Captura de pantalla del Circuito AND - 2 entradas



Compuerta AND - 3 entradas

Diagrama

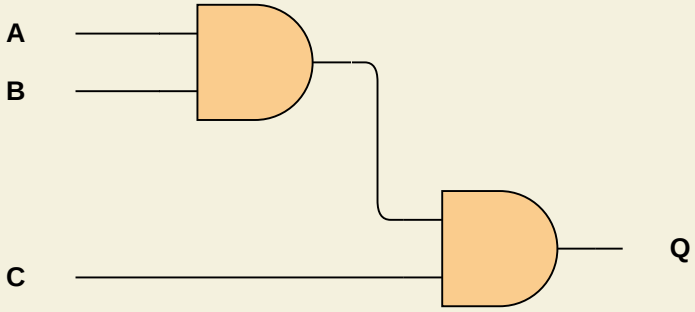
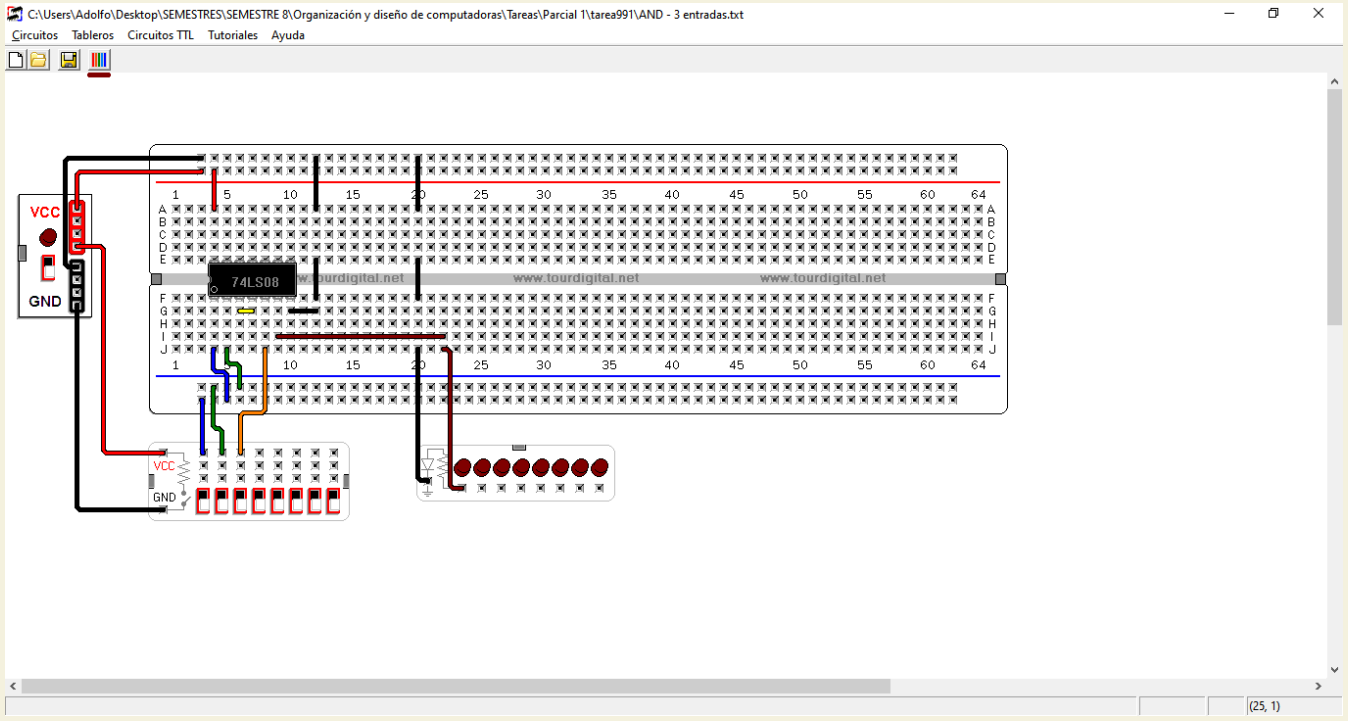


Tabla de Verdad

a	b	c	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Captura de pantalla del Circuito AND - 3 entradas



Compuerta AND - 4 entradas

Diagrama

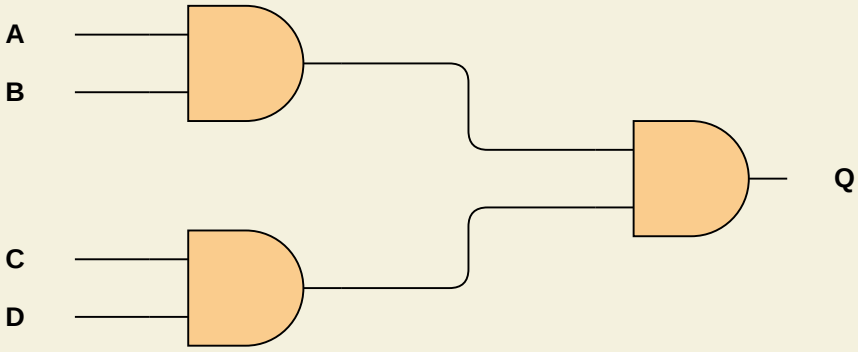
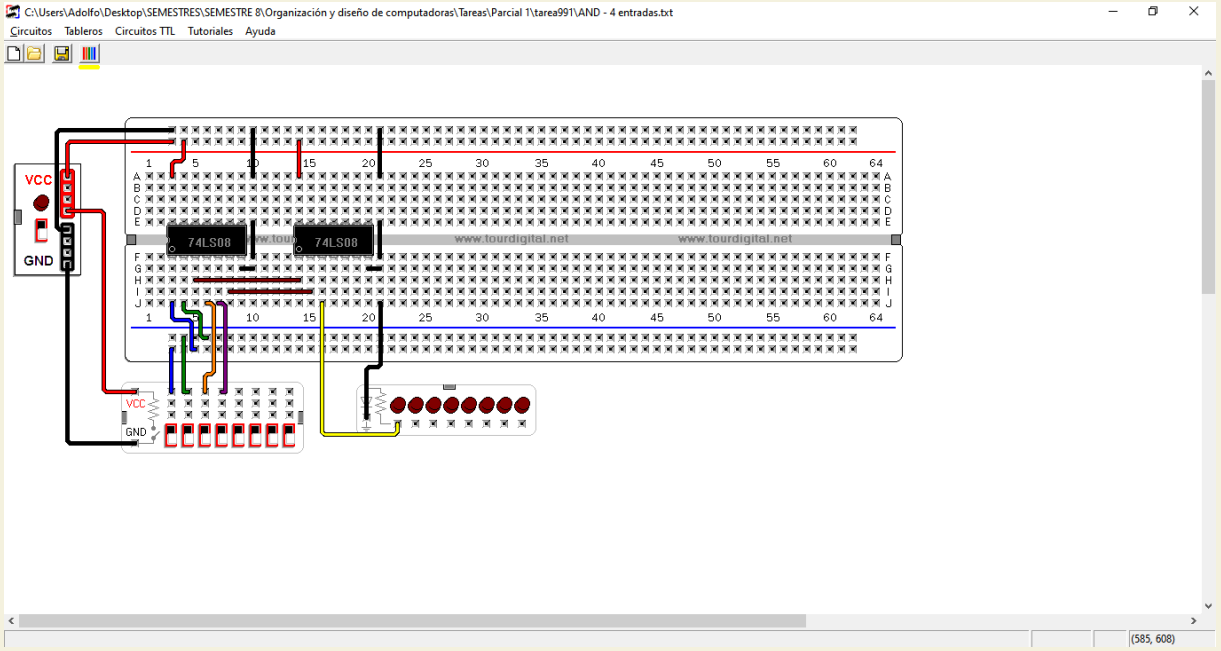


Tabla de Verdad

a	b	c	d	Output
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Captura de pantalla del Circuito AND - 4 entradas



Compuerta OR - 2 entradas

Diagrama

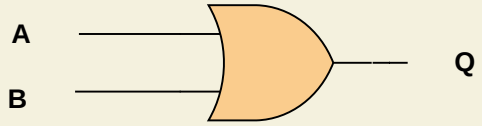
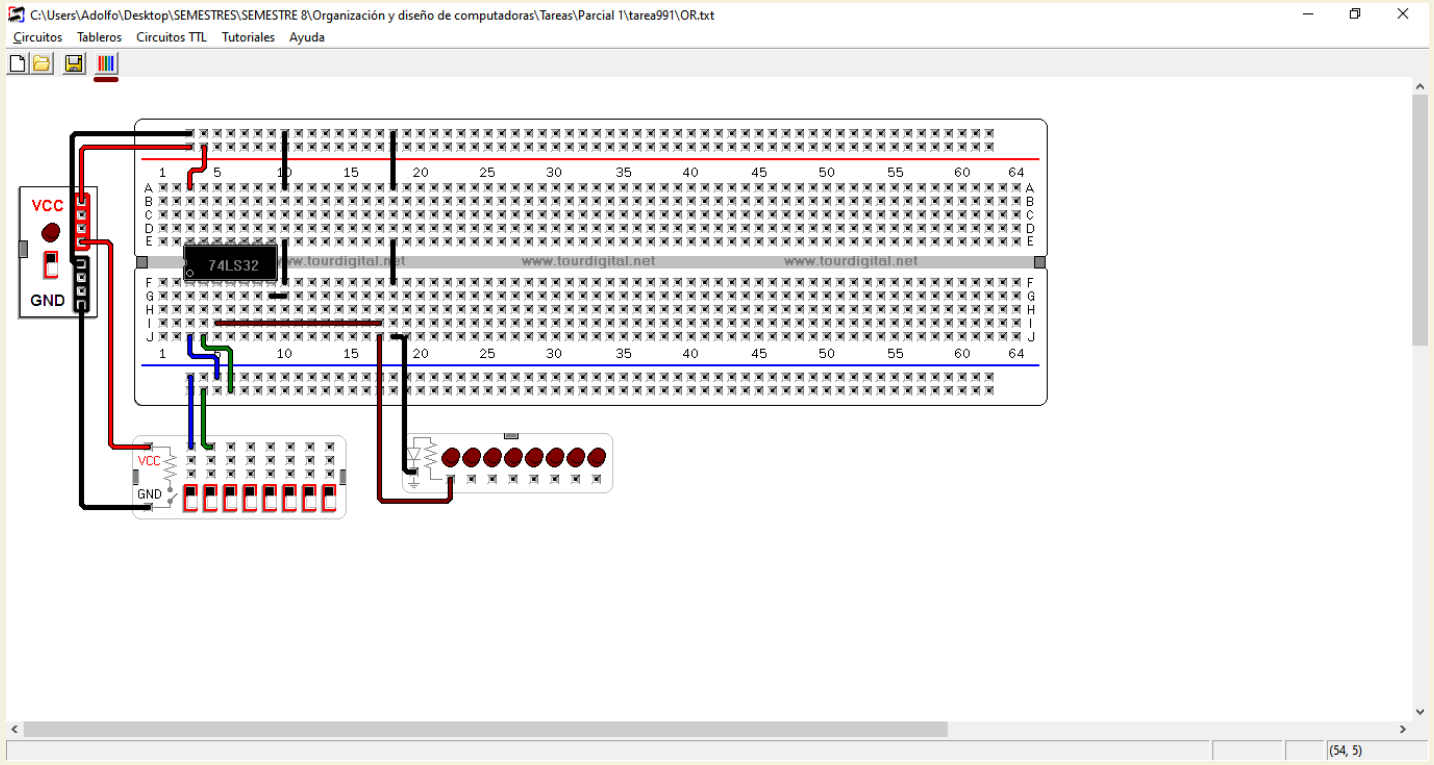


Tabla de Verdad

a	b	Output
0	0	0
0	1	1
1	0	1
1	1	1

Captura de pantalla del Circuito OR - 2 entradas



Compuerta NAND - 2 entradas

Diagrama

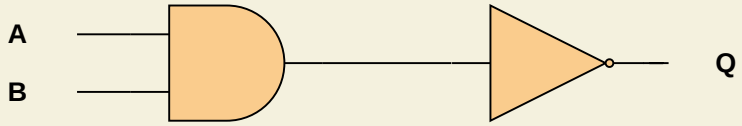
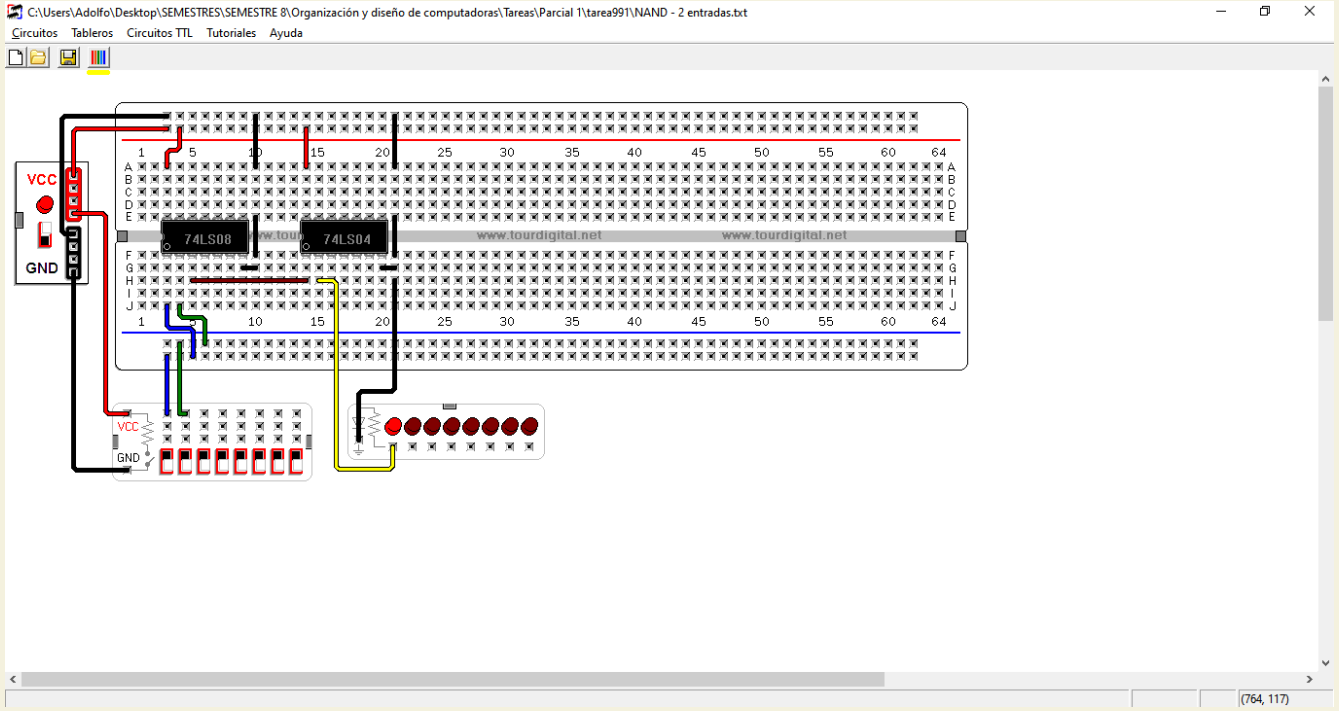


Tabla de Verdad

a	b	Output
0	0	1
0	1	1
1	0	1
1	1	0

Captura de pantalla del Circuito NAND - 2 entradas



Compuerta NAND - 3 entradas

Diagrama

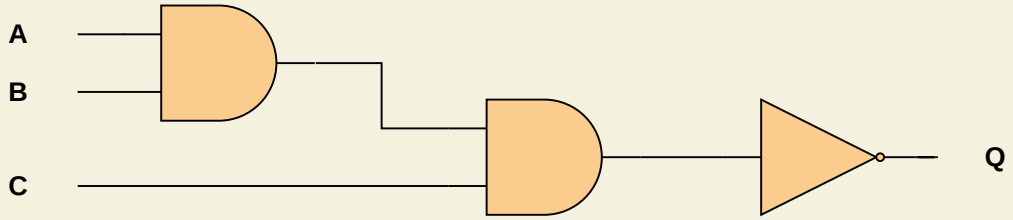
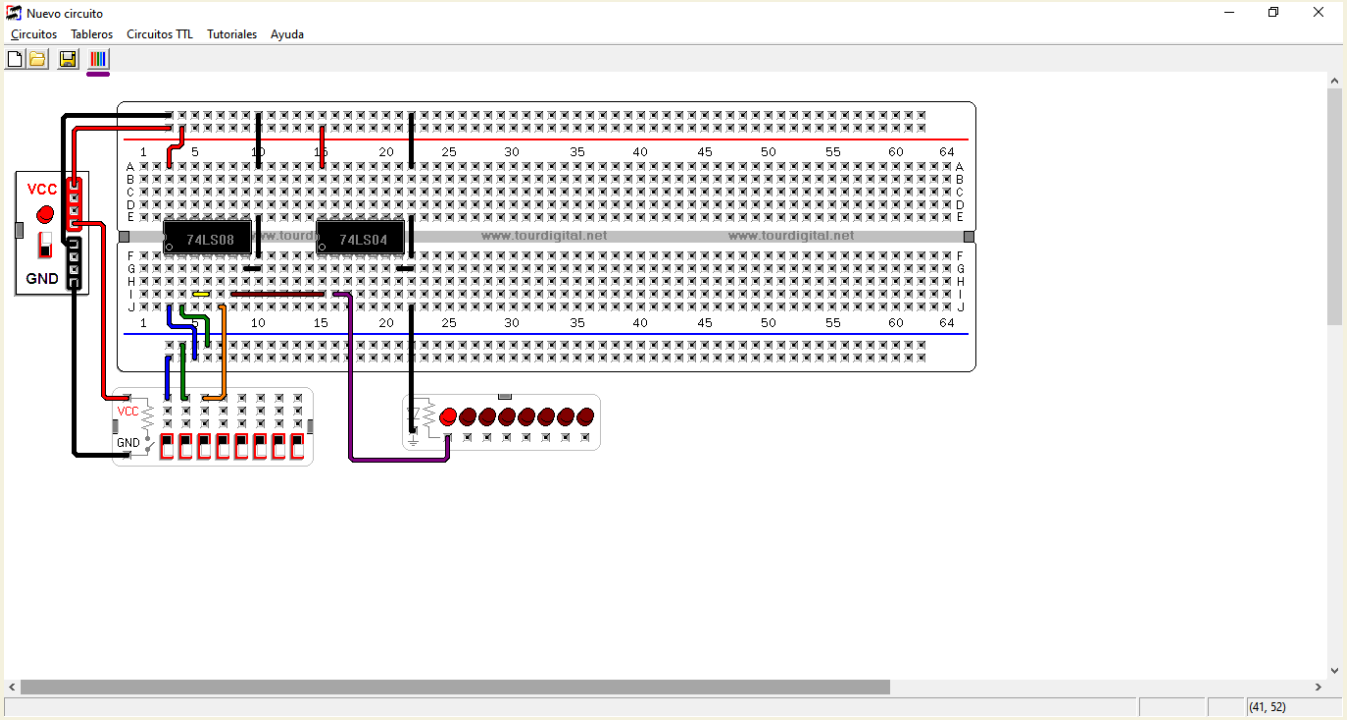


Tabla de Verdad

a	b	c	Output
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Captura de pantalla del Circuito NAND - 3 entradas



Compuerta NAND - 4 entradas

Diagrama

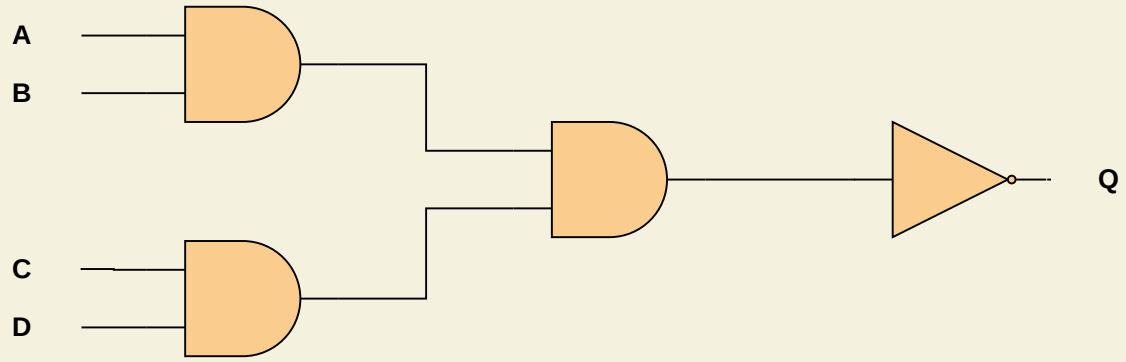
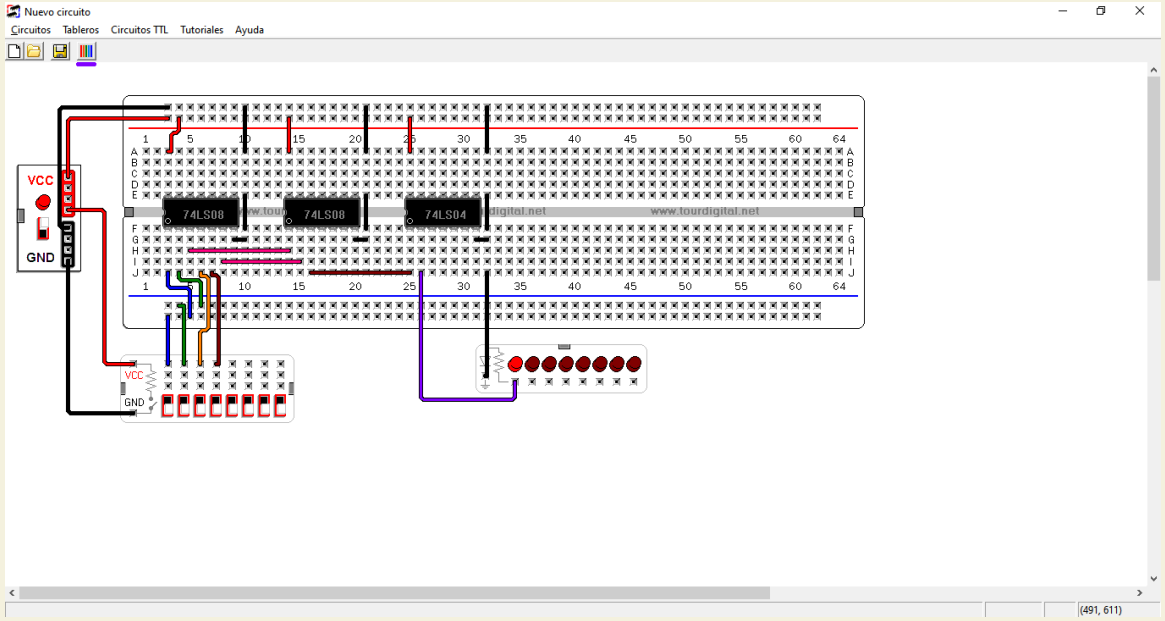


Tabla de Verdad

a	b	c	d	Output
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Captura de pantalla del Circuito NAND - 4 entradas



Compuerta NAND - 8 entradas

Diagrama

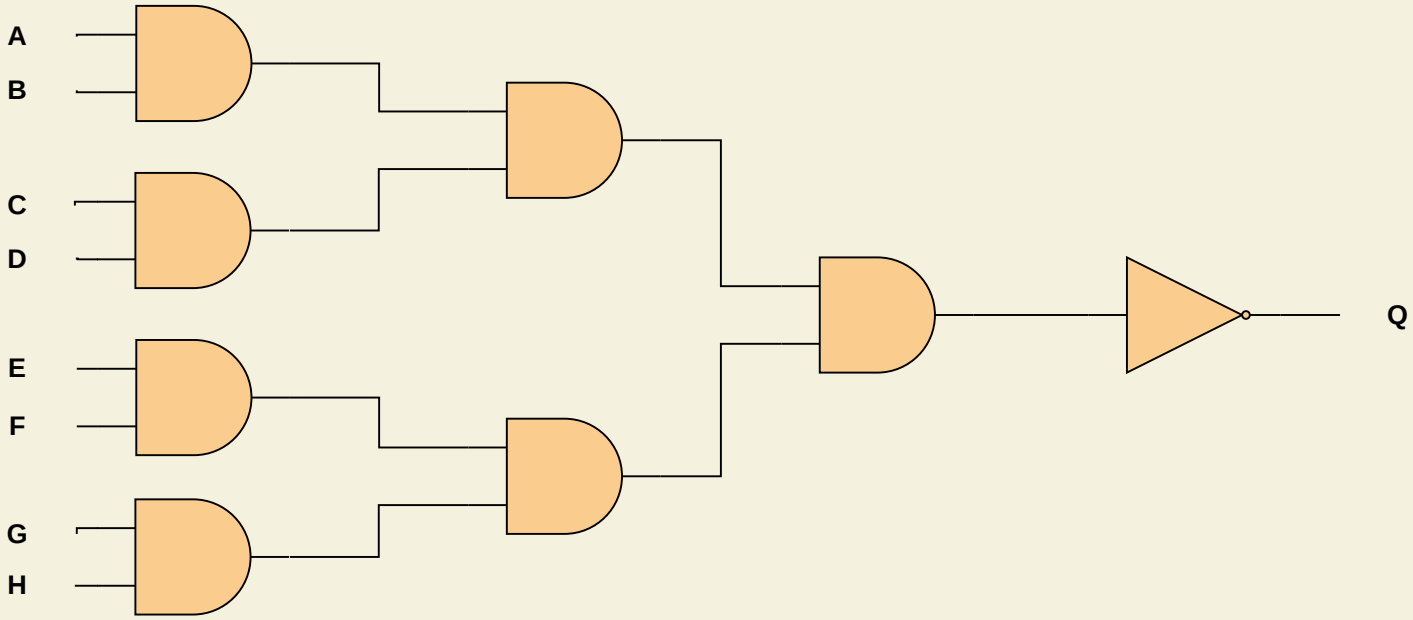


Tabla de Verdad

a	b	c	d	e	f	g	h	output
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	1	1
0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	0	1	1
0	0	0	0	0	1	1	0	1
0	0	0	0	0	1	1	1	1
0	0	0	0	1	0	0	0	1
0	0	0	0	1	0	0	1	1
0	0	0	0	1	0	1	0	1
0	0	0	0	1	0	1	1	1
0	0	0	0	1	1	0	0	1
0	0	0	0	1	1	0	1	1
0	0	0	0	1	1	1	0	1
0	0	0	0	1	1	1	1	1
0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	1	1
0	0	0	1	0	0	1	0	1
0	0	0	1	0	0	1	1	1
0	0	0	1	0	1	0	0	1
0	0	0	1	0	1	0	1	1
0	0	0	1	0	1	1	0	1
0	0	0	1	0	1	1	1	1
0	0	0	1	1	0	0	0	1
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0	0	0	1	1	0	1	1	1
0	0	0	1	1	1	0	0	1

0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	0	1
0	0	0	1	1	1	1	1	1
0	0	1	0	0	0	0	0	1
0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	0	1
0	0	1	0	0	0	1	1	1
0	0	1	0	0	1	0	0	1
0	0	1	0	0	1	0	1	1
0	0	1	0	0	1	1	0	1
0	0	1	0	0	1	1	1	1
0	0	1	0	1	0	0	0	1
0	0	1	0	1	0	0	1	1
0	0	1	0	1	0	1	0	1
0	0	1	0	1	0	1	1	1
0	0	1	0	1	1	0	0	1
0	0	1	0	1	1	0	1	1

NOTA IMPORTANTE: La tabla de verdad se encuentra completa en un pdf dentro de la carpeta *tarea991* bajo el nombre de ***"tabla de verdad NAND - 8 entradas***"

1	1	1	0	1	0	1	0	1
1	1	1	0	1	0	1	1	1
1	1	1	0	1	1	0	0	1
1	1	1	0	1	1	0	1	1
1	1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	1	1
1	1	1	1	0	0	0	0	1
1	1	1	1	0	0	0	1	1
1	1	1	1	0	0	1	0	1
1	1	1	1	0	0	1	1	1
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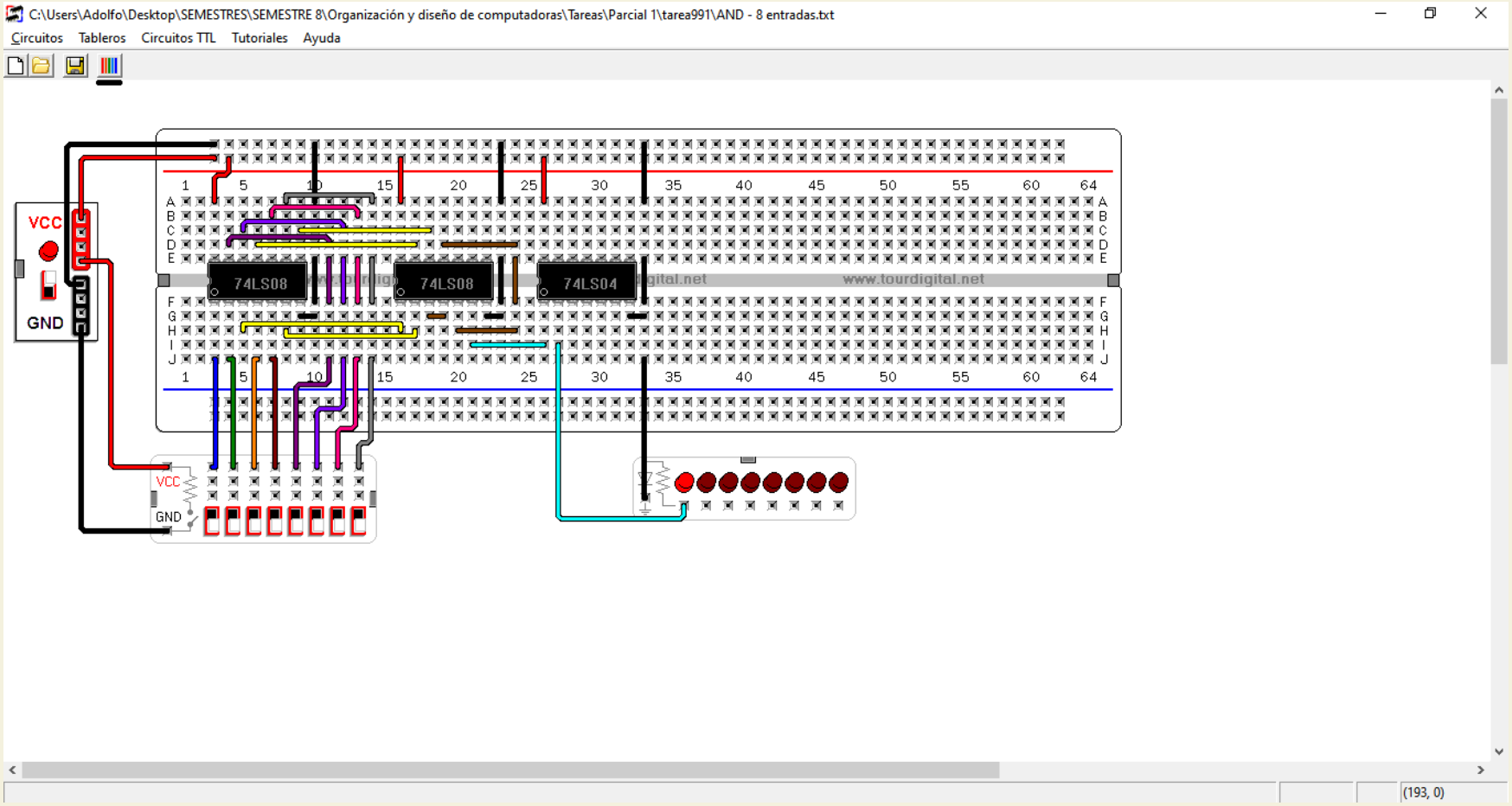
1	1	1	1	0	1	1	0	1
1	1	1	1	0	1	1	1	1
1	1	1	1	1	0	0	0	1
1	1	1	1	1	0	0	1	1
1	1	1	1	1	0	1	0	1
1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	0	0	1
1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	0

Captura de pantalla del Circuito NAND - 8 entradas



Compuerta NAND - 13 entradas

Diagrama

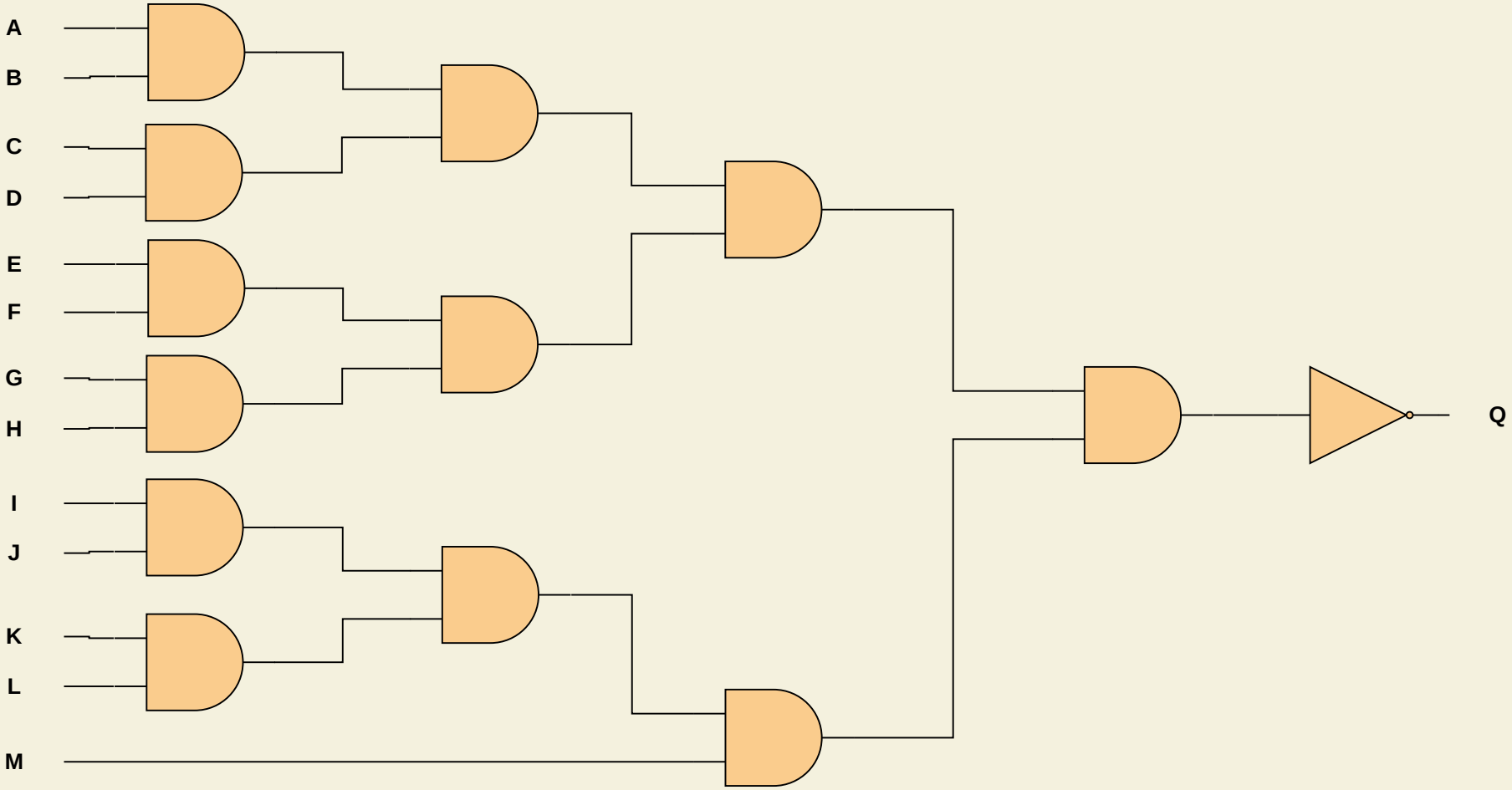


Tabla de Verdad

a	b	c	d	e	f	g	h	i	j	k	l	m	output
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0	0	1	0	1	1
0	0	0	0	0	0	0	0	0	0	1	1	0	1
0	0	0	0	0	0	0	0	0	0	1	1	1	1
0	0	0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	1	0	0	1	1
0	0	0	0	0	0	0	0	0	1	0	1	0	1
0	0	0	0	0	0	0	0	0	1	0	1	1	1
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0	0	0	0	0	0	0	0	0	1	1	0	1	1
0	0	0	0	0	0	0	0	0	1	1	1	0	1
0	0	0	0	0	0	0	0	0	1	1	1	1	1
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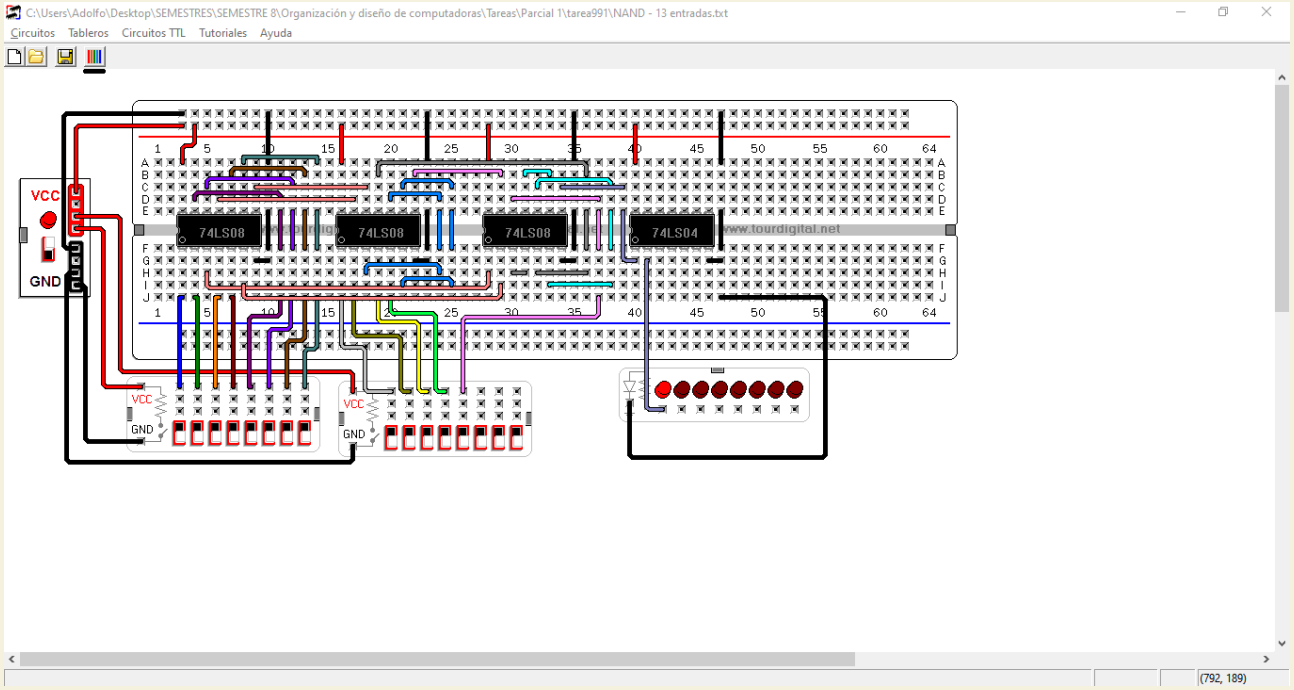
0	0	0	0	0	0	0	0	1	0	0	0	1	1
0	0	0	0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	0	0	1	0	0	1	1	1
0	0	0	0	0	0	0	0	1	0	1	0	0	1
0	0	0	0	0	0	0	0	1	0	1	0	1	1
0	0	0	0	0	0	0	0	1	0	1	1	0	1
0	0	0	0	0	0	0	0	1	0	1	1	1	1
0	0	0	0	0	0	0	0	1	1	0	0	0	1
1	1	1	1	1	1	1	1	1	0	0	0	1	1
1	1	1	1	1	1	1	1	1	0	0	1	0	1
1	1	1	1	1	1	1	1	1	0	0	1	1	1
1	1	1	1	1	1	1	1	1	0	1	0	0	1
1	1	1	1	1	1	1	1	1	0	1	0	1	1
1	1	1	1	1	1	1	1	1	0	1	1	0	1
1	1	1	1	1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	1	1	0	0	0	1
1	1	1	1	1	1	1	1	1	1	0	0	1	1
1	1	1	1	1	1	1	1	1	1	0	1	0	1
1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	1	1	1	1	0	0	1
1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	0

Captura de pantalla del Circuito NAND - 13 entradas



NOTA IMPORTANTE: La tabla de verdad se encuentra completa en un pdf dentro de la carpeta *tarea991* bajo el nombre de ***"tabla de verdad NAND - 13 entradas***"

Compuerta NOR - 2 entradas

Diagrama

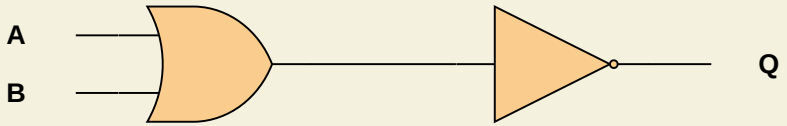
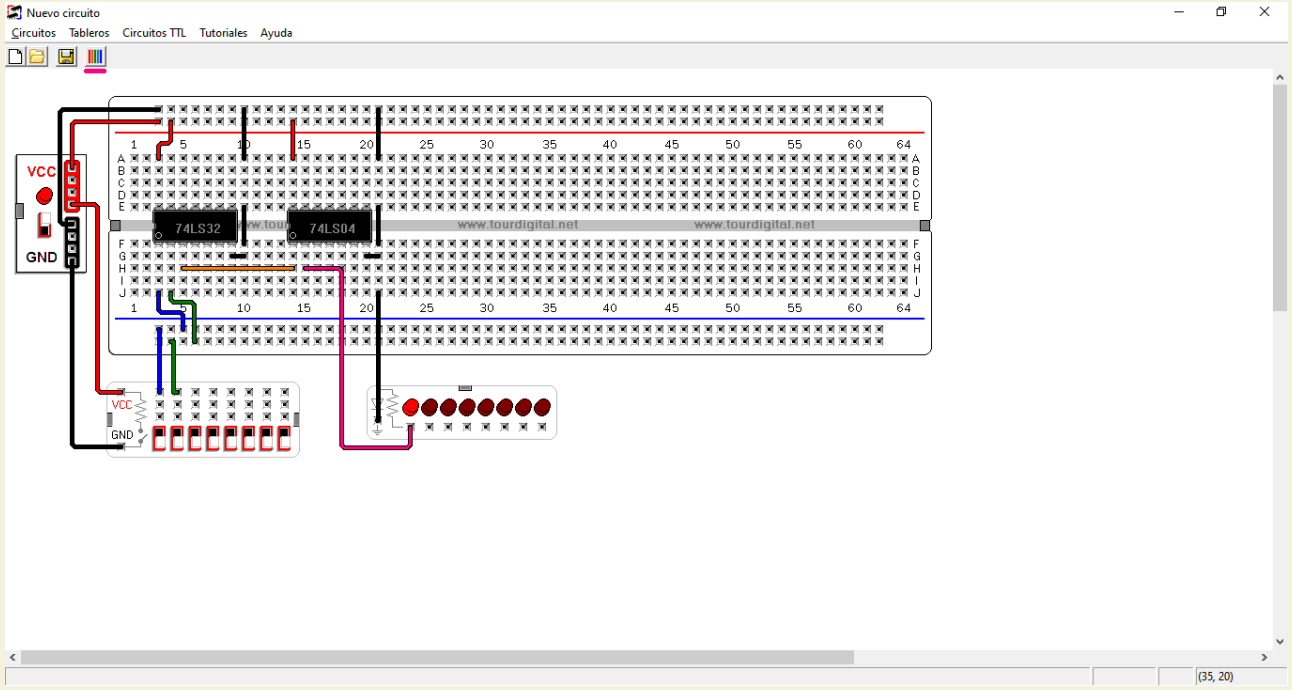


Tabla de Verdad

a	b	Output
0	0	1
0	1	0
1	0	0
1	1	0

Captura de pantalla del Circuito NOR - 2 entradas



Compuerta NOR - 3 entradas

Diagrama

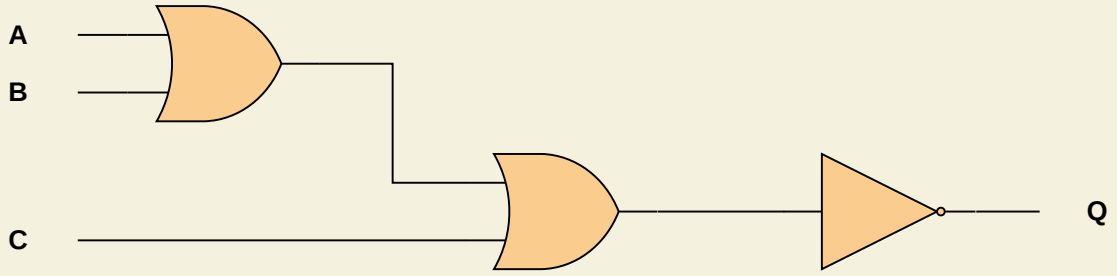
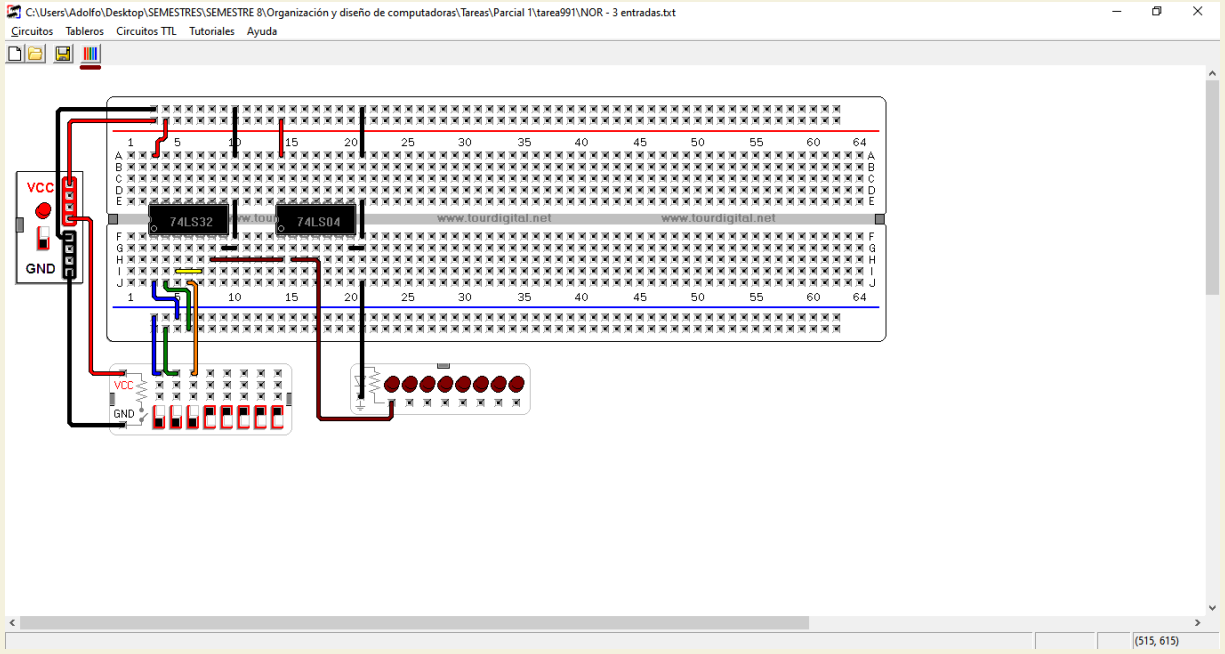


Tabla de Verdad

a	b	c	Output
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Captura de pantalla del Circuito NOR - 3 entradas



Compuerta NOR - 5 entradas

Diagrama

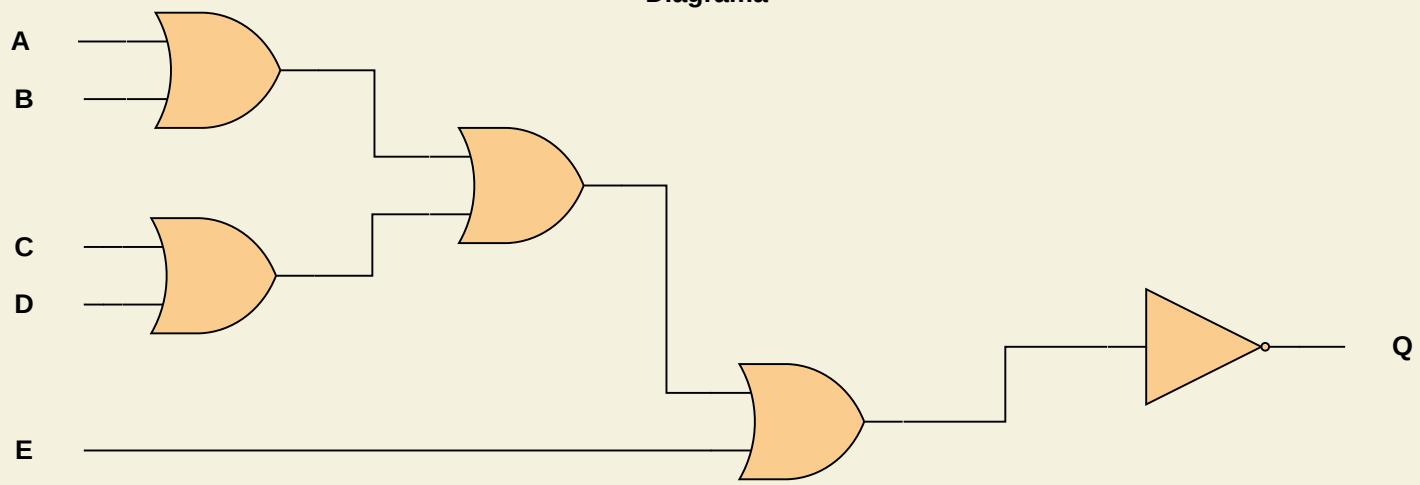


Tabla de Verdad

a	b	c	d	e	Output
0	0	0	0	0	1
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	0	1	0
1	0	1	1	0	0
1	0	1	1	1	0
1	1	0	0	0	0
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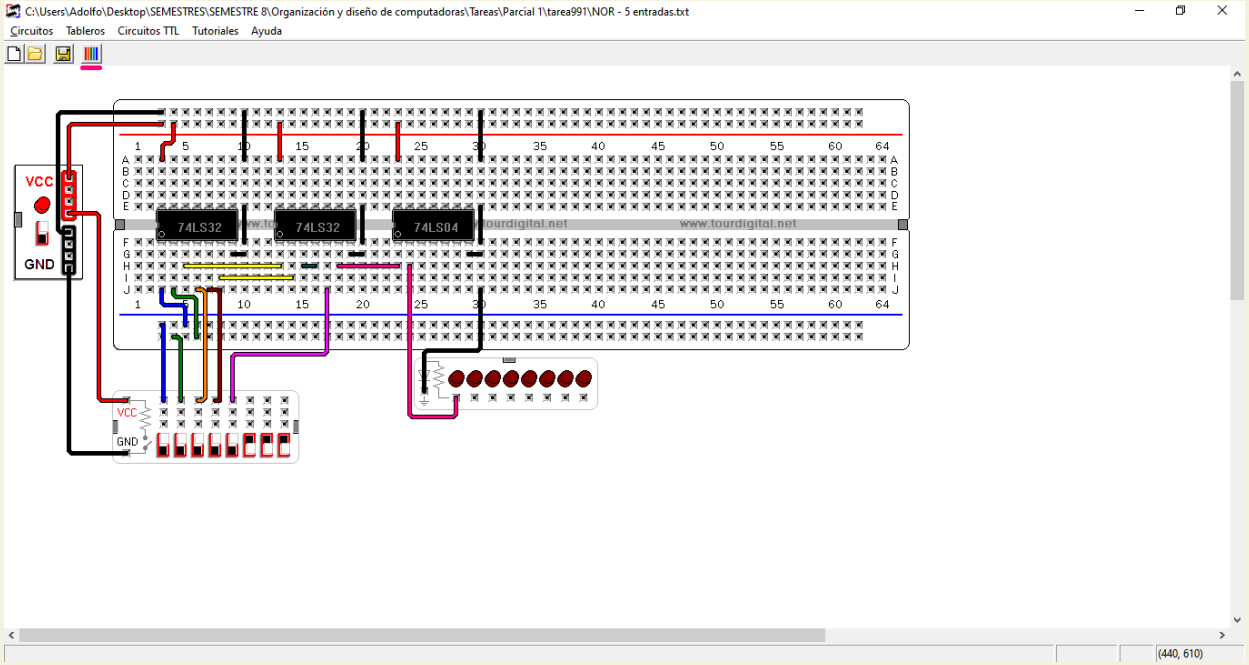
1	1	0	1	0	0
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	0

Captura de pantalla del Circuito NOR - 5 entradas



Compuerta XOR - 2 entradas

Diagrama

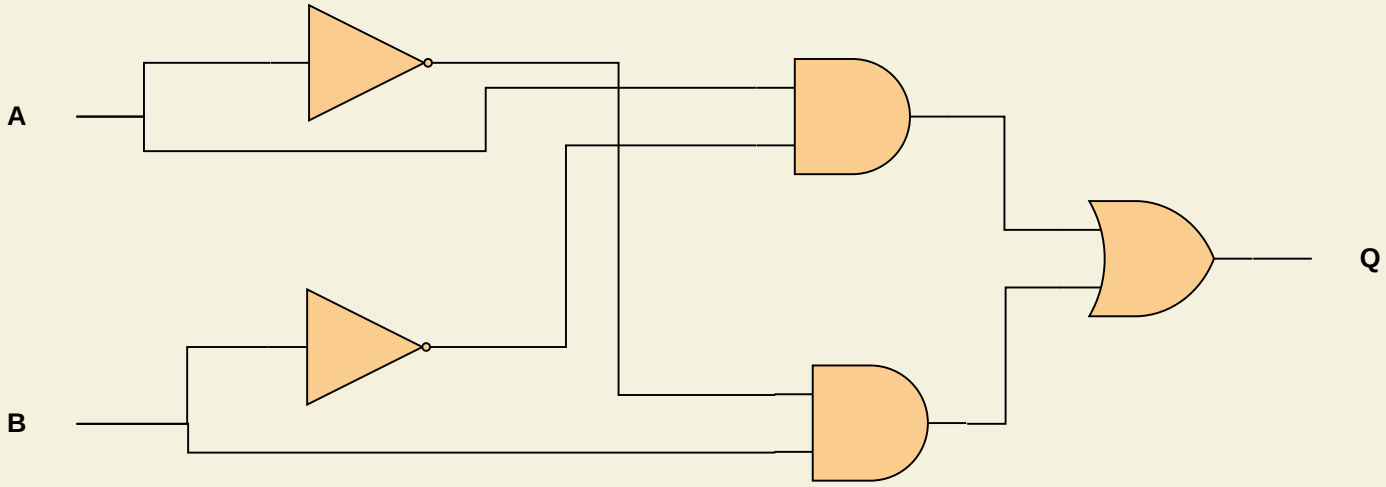


Tabla de Verdad

a	b	Output
0	0	0
0	1	1
1	0	1
1	1	0

Captura de pantalla del Circuito XOR - 2 entradas