COURSERA COURSE
INTRODUCTION TO FPGA EMBEDDED SYSTEM

Assignment #01. Week #01.

1. Using only logic gates, design a 2-bit full adder with carry. Here is a partial truth table for the circuit.

INPUTS					OUTPUTS		
A0	A1	B0	B1	Ci	S0	S1	Co
0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0
0	1	0	0	0	0	1	0
1	0	1	0	0	0	1	0
0	1	0	1	0	0	0	1
0	1	0	0	1	1	1	0
1	0	1	0	1	1	1	0
1	1	1	1	1	1	1	1

Figure 1

Where A and B are inputs, Ci is carry in, Si is output and Co is carry out.

Draw a schematic showing the gate interconnections. Include either a Boolean equation or an explanation of your design that matches the schematic you submit.

Boolean Equation:

For S0:

$$F_{S0} = A0A1'B0'B1'Ci' + A0'A1B0'B1'Ci + A0A1'B0B1'Ci + A0A1B0B1CI$$

$$F_{S0} = (A0 \oplus B0) \oplus Cin$$

For S1:

$$F_{S1} = A0'A1B0'B1'Ci' + A0A1'B0B1'Ci' + A0'a1B0'B1'Ci + A0A1'B0B1'Ci + A0A1B0B1Ci$$

$$F_{S1} = (A1 \oplus B1) \oplus Cin$$

For C0:

$$F_{C0} = A0'A1B0'B1Ci' + A0A1B0B1Ci$$

$$F_{C0} = A1.B1 + Cin(A1 \oplus B1)$$

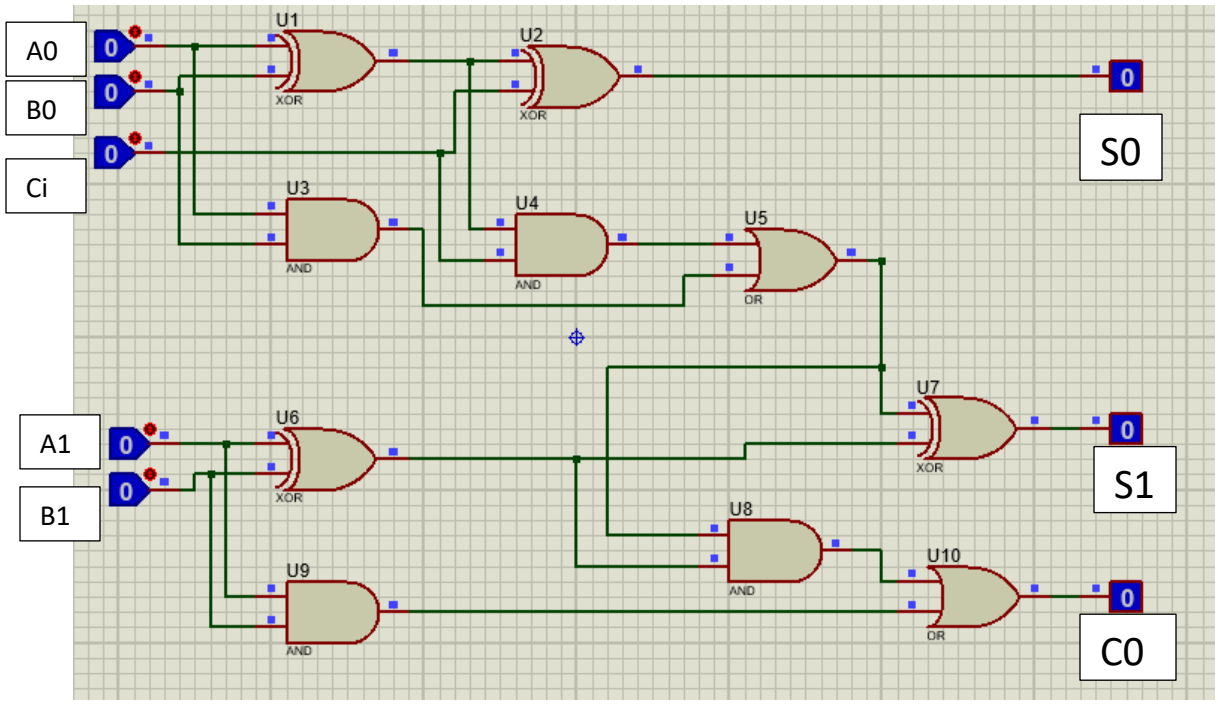

Figure 1.1.

The following circuit is a 2-bit adder circuit. We have five inputs A0,A1,B0,B1 and Cin. First, using the truth table we get the following equation for F_{S0} , F_{S1} and F_{C0}. Then, using these equations we come up with the following circuit.

It works according to the truth table. The Carry bit of the first adder circuit is fed into the XOR Gate of the second adder circuit. It works as the Ci for the second adder circuit. Due to this we don't need a separate Carry bit and it works as the carry bit. So, it is connected into series as shown in the block diagram below.

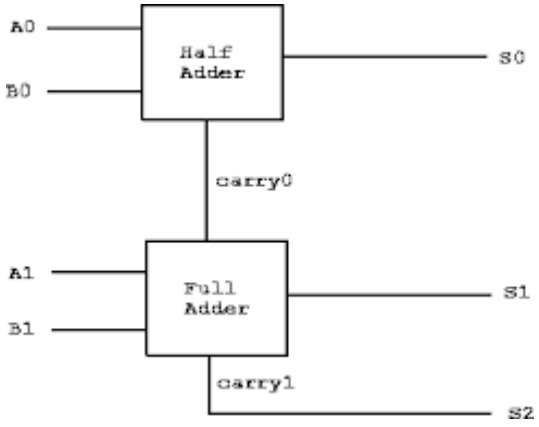

Figure 1.2.

2. Show how the logic equation (A AND NOT(B)) OR (C AND NOT(D)) can be implemented using the following:

A. The PLA shown here:

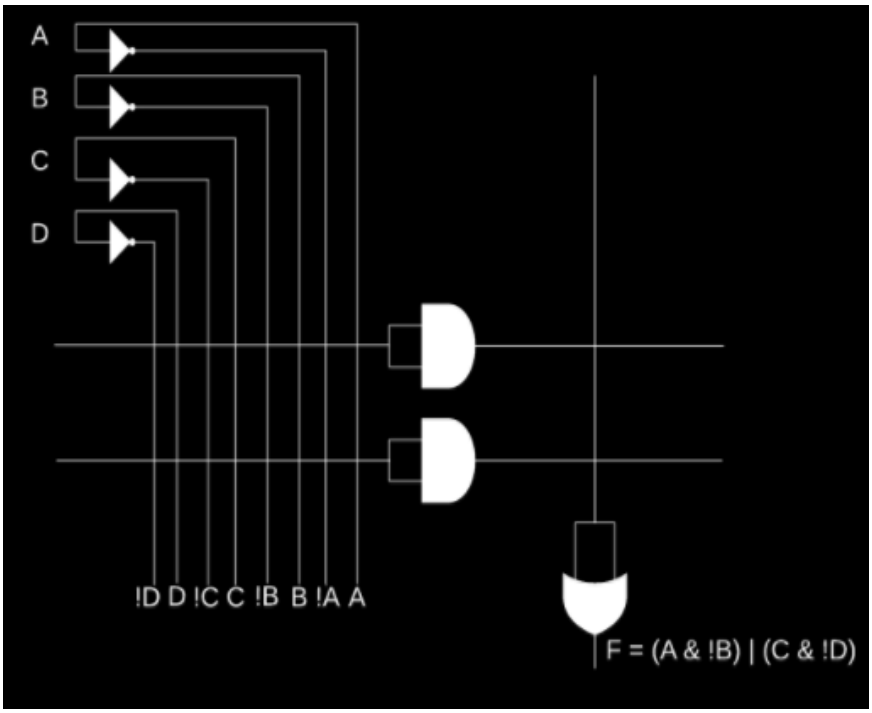

Figure 2. (a)

The PLA circuit shown above can be implemented as shown in the figure below:

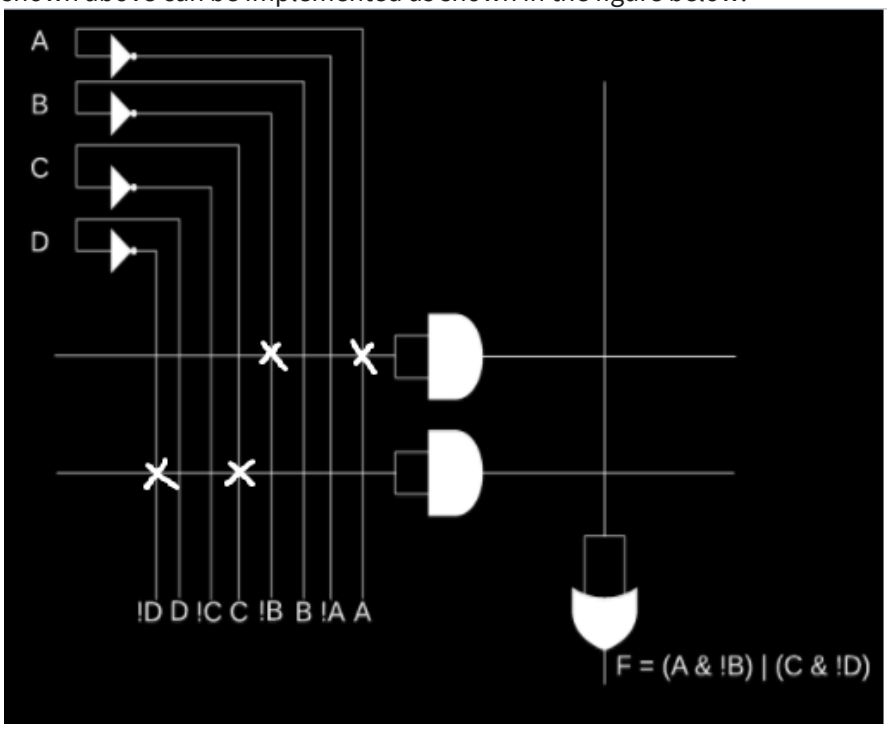

Figure 2.1.

As shown in the circuit above. The equation is as follows **F = (A.B') + (C.D').** Which can be implemented if the circuit is connected the way it is shown in the Figure 1.2.
The inverted outputs are shown with the sign "!" while normal inputs are shown with proper English.

B. The LUT shown here:

RAM CONTENTS				
Address				Output Data
A	B	C	D	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Figure 2. (b)

Answer:
In the following equation **F = (A.B') + (C.D')**. We were given the following table for 4-bit. The answer for this LUT table is as follows. It has 4-bit or 16 inputs.

RAM CONTENTS				
Address				Output Data
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

Figure 2.2.