EEE 491 Lab Assignment
Lab-WINDOW: Windowing

1. Technical Specifications

Lab-WINDOW shall read 512 samples of 12-bit (two's complement) data from the Lab-ADC's dual-port RAM. Starting address of the RAM shall be 14-bit input as starting address parameter. 512 samples of data constitute a frame. HANNING windowing function shall be executed over the frame. That is, 512 samples shall be multiplied by 512 coefficients of HANNING windowing function. Coefficients shall be stored in a single port read-only memory (ROM). Each coefficient data shall be 8-bit. The multiplication output (hence 20-bit) shall be stored in a simple dual-port RAM. The size of the RAM shall be 512 words (one frame length). The multiplier shall be used from the "Multipliers" in Vivado "IP Catalog". The ROM shall be selected from the "Block Memory Generator" in Vivado "IP Catalog".

Lab-WINDOW in FPGA shall have the following input/output (IO) signals.

- "reset_in" input control signal, which resets all the registers in the design.
- "clock_in" input clock signal of the 100MHz clock oscillator on the Basys-3 board.
- "frame_addr_in" input signal that specifies the start address of a frame in dual-port RAM in Lab_ADC.
- "adc_addr_out" output signal that addresses the read-only port of the dual-port RAM in Lab-ADC.
- "adc_data_in" input signal from the read-only port of the dual-port RAM in Lab-ADC.
- "mem_addr_in" input signal that addresses the read-only port of the dual-port RAM in Lab-WINDOW.
- "mem_data_out" output signal of the read-only port of the dual-port RAM in Lab-WINDOW.
- "start_in" input control signal, which starts the windowing function for 512 samples. This signal is active high asserted on a single clock pulse (refer to waveform in Lab-ADC assignment).
- "ready_out" output status signal that indicates if windowing function is completed over the 512 samples and output is written to dual-port RAM of Lab-WINDOW and the function is ready for the next execution. This signal is active high and asserted low just after the start signal is asserted (refer to waveform in Lab-ADC assignment).

Write a test-bench in VHDL for the simulation of your design. Verify by using your test-bench simulation results that your design satisfies the technical specifications.

2. Demonstration

- Show that your design is implemented on FPGA.
- Present your test bench simulation results: inputs, outputs (waveforms). Multiplication result at the dual-port RAM output and framing addressing must be shown clearly on the waveforms. Observe the input, output waveforms, and verify the technical specifications listed above.

3. Guidance

- You can generate the HANNING windowing function 512 coefficients on MATLAB. Quantize data to unsigned 8-bit.
- An example for a multiplier configuration from Vivado Library is shown below. Use signed data for the signal, and unsigned for window coefficients. Let multiplier construction use built-in multipliers in DSP blocks of the FPGA. Check also "Output and Control" tab. Set pipelining to zero for no latency, hence no need to use clock signal also.
- Test-bench simulation example: The test-bench generates a constant 12-bit signed data, a frame starting address and then Lab-WINDOW generates addresses, executes the windowing function, and writes the data

to its dual-port RAM. Then, the test bench reads 20-bit data from the dual-port RAM. You can show the analog behavior plots from your simulation data.

- Keep versions of your design during development.