How to Connect PL to PS using Zynq 7020

Creating Vivado Project:

Select Device as following

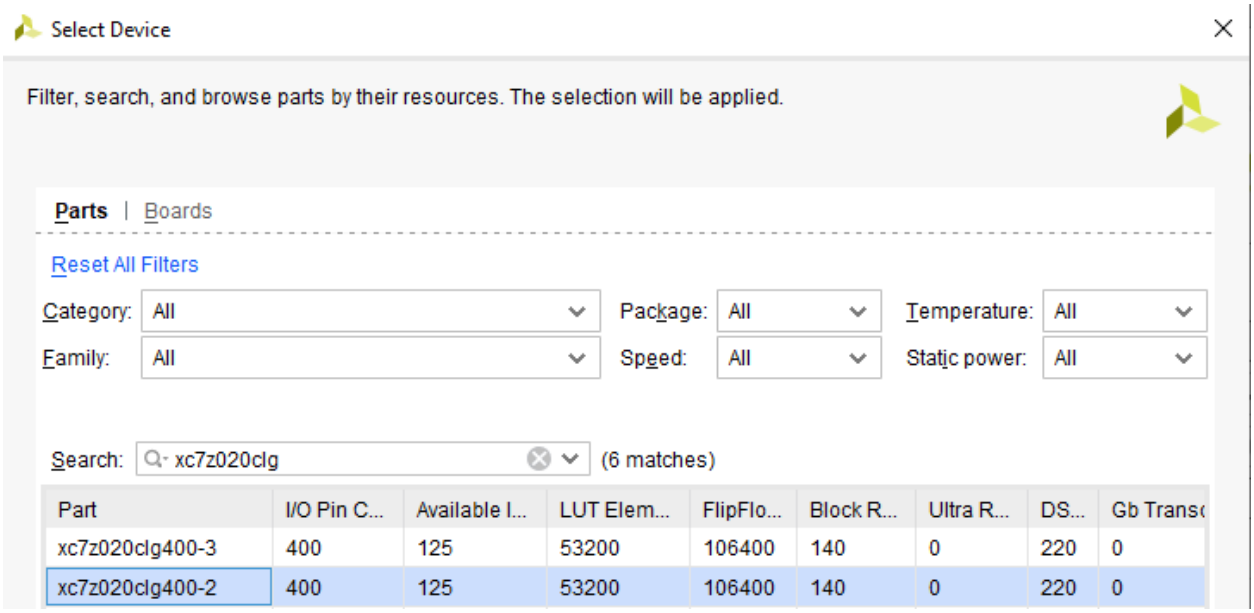

Figure 1: Selecting Target Device

Create Block Design:

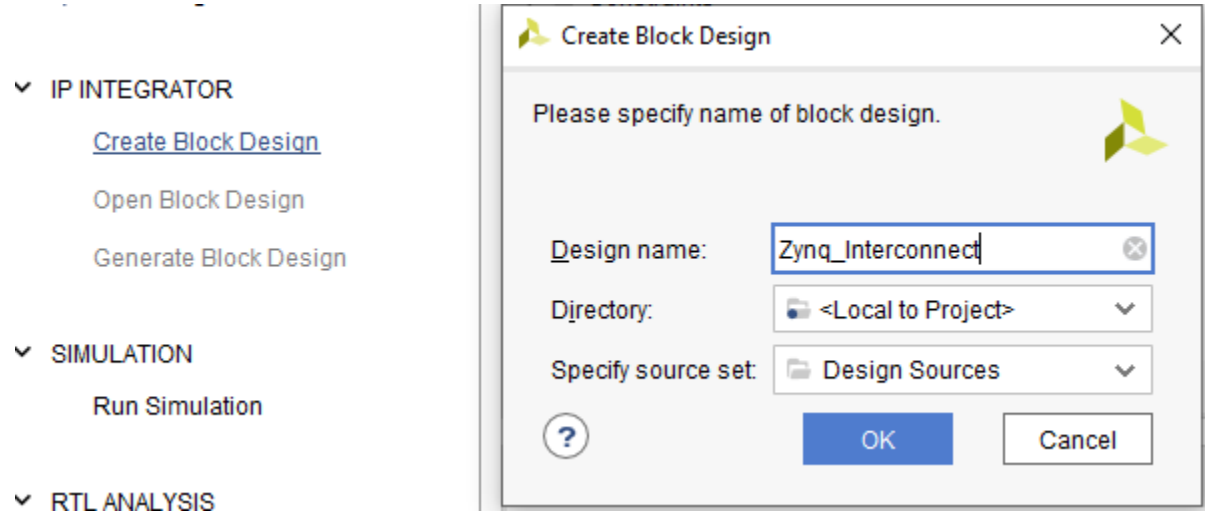

Figure 2: Creating Block Design for the Project

Click OK and continue.

Once you are in Block Design. It should look like this.

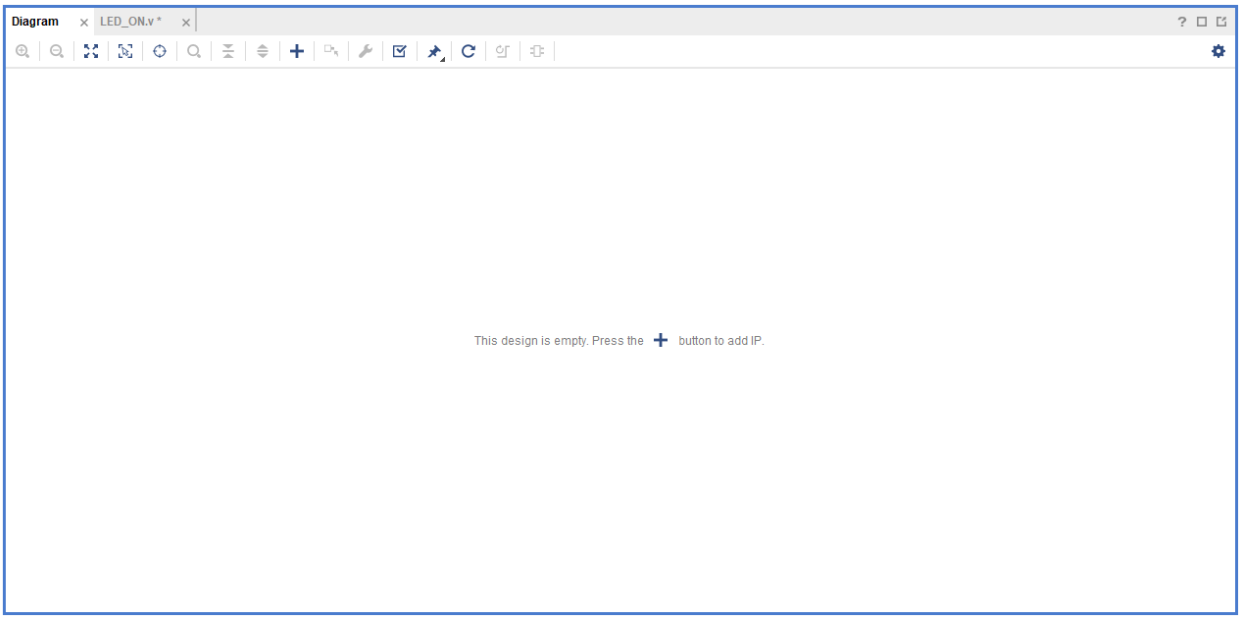

Figure 3: Default Block Design Screen

Adding IP

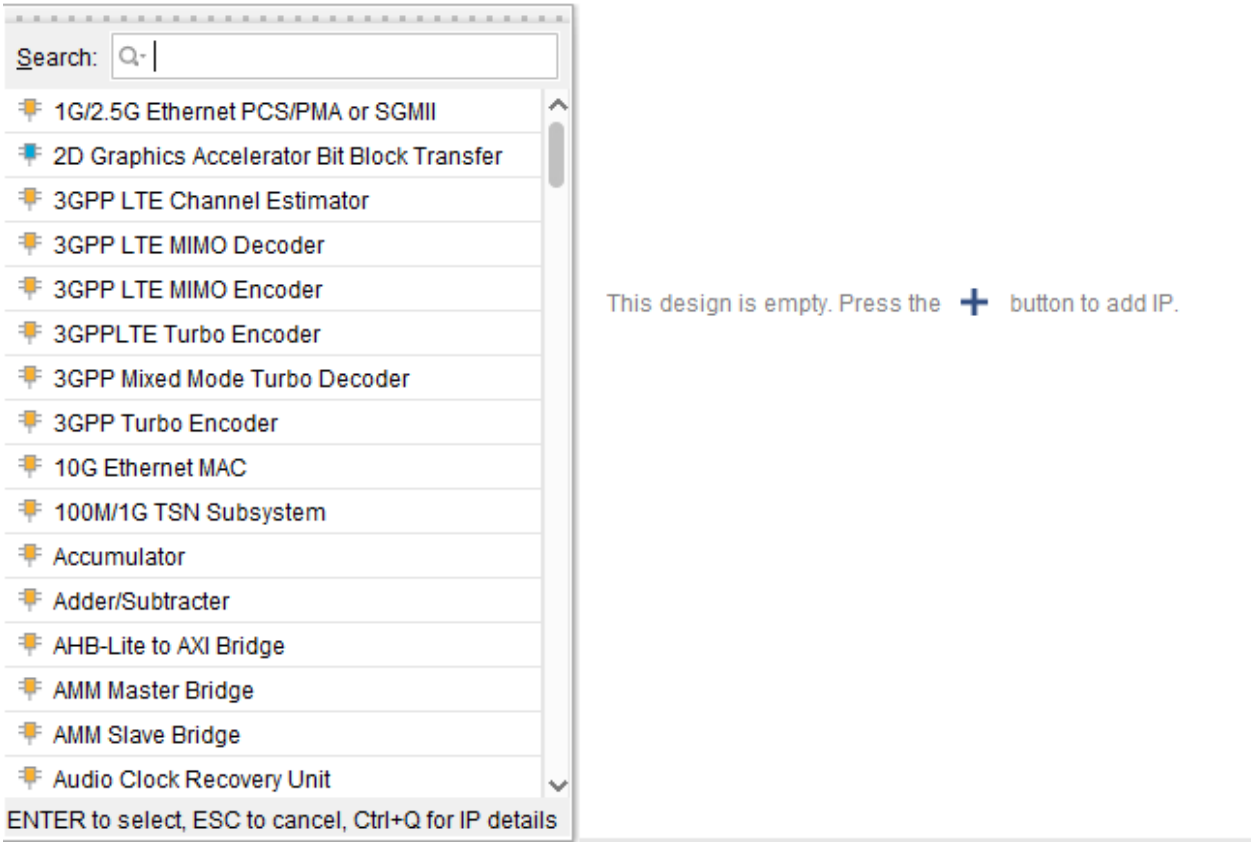

Figure 4: Adding IP to the block Design

Search and add the following Ips:

- ZYNQ7 Processing System
- AXI GPIO x2
- Utility vector Logic

It should look like this

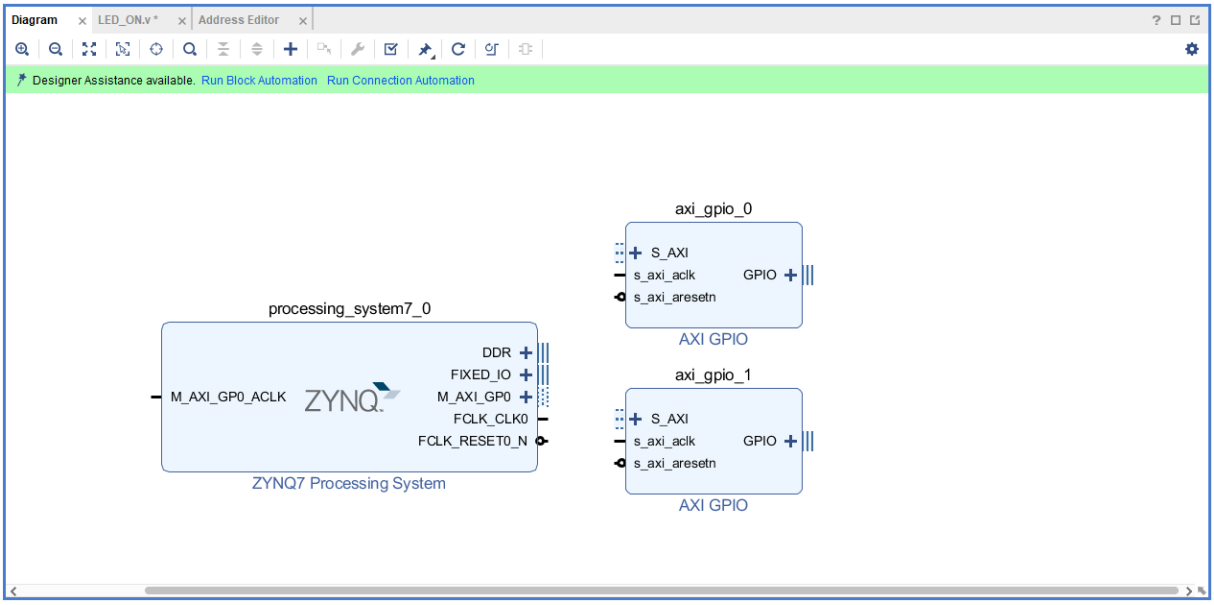

Figure 5: Zynq PS and AXI GPIO IP in block Design

Now, the designer assistance available option should be good. But we need to configure DDR First.

Enable this in PS IP.

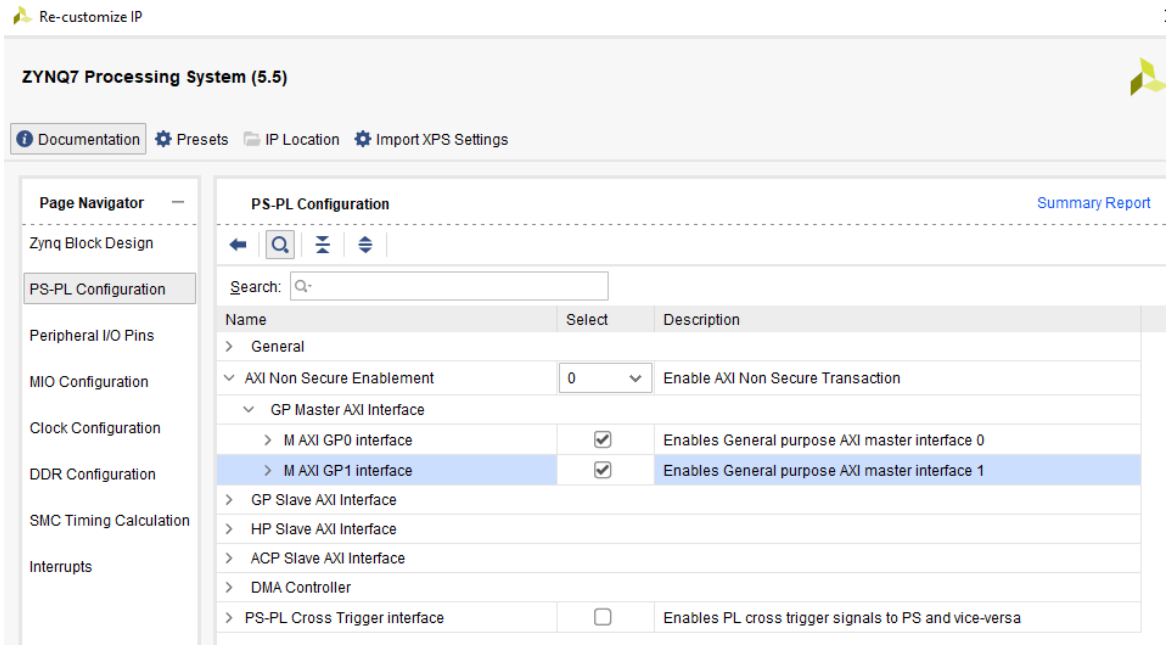

Figure 6: Enable AXI GPIO in PS

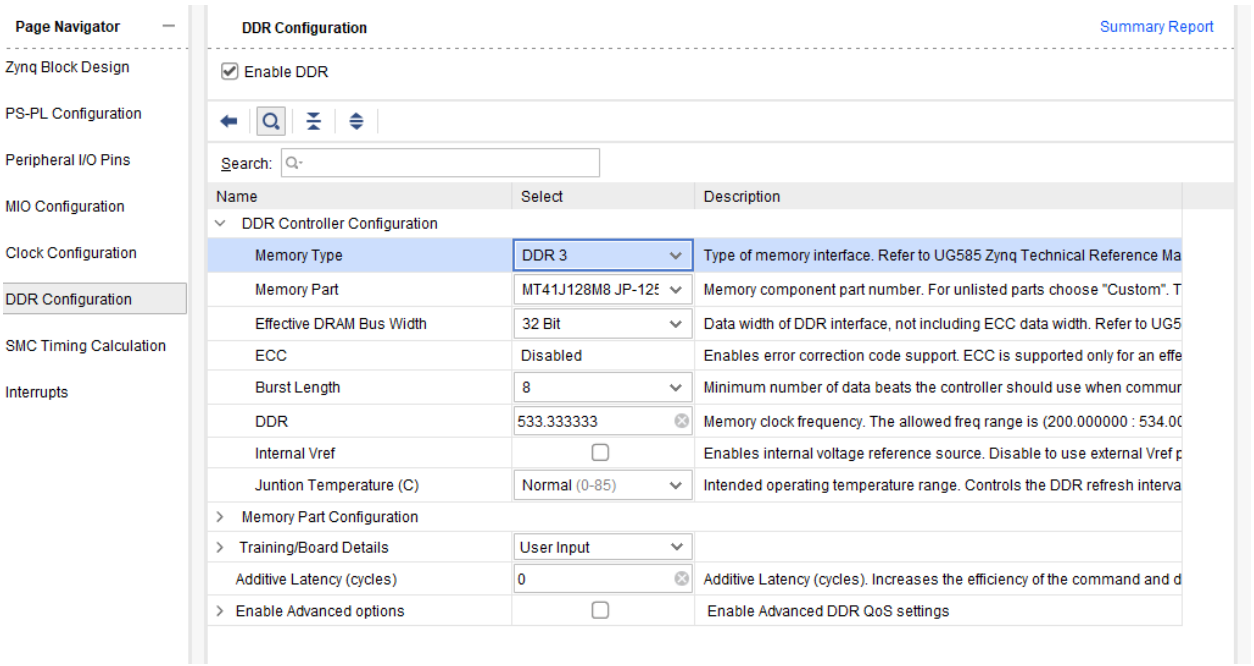

Figure 7: Configuring DDR in PS

Now, we need to run block automation and select the following options

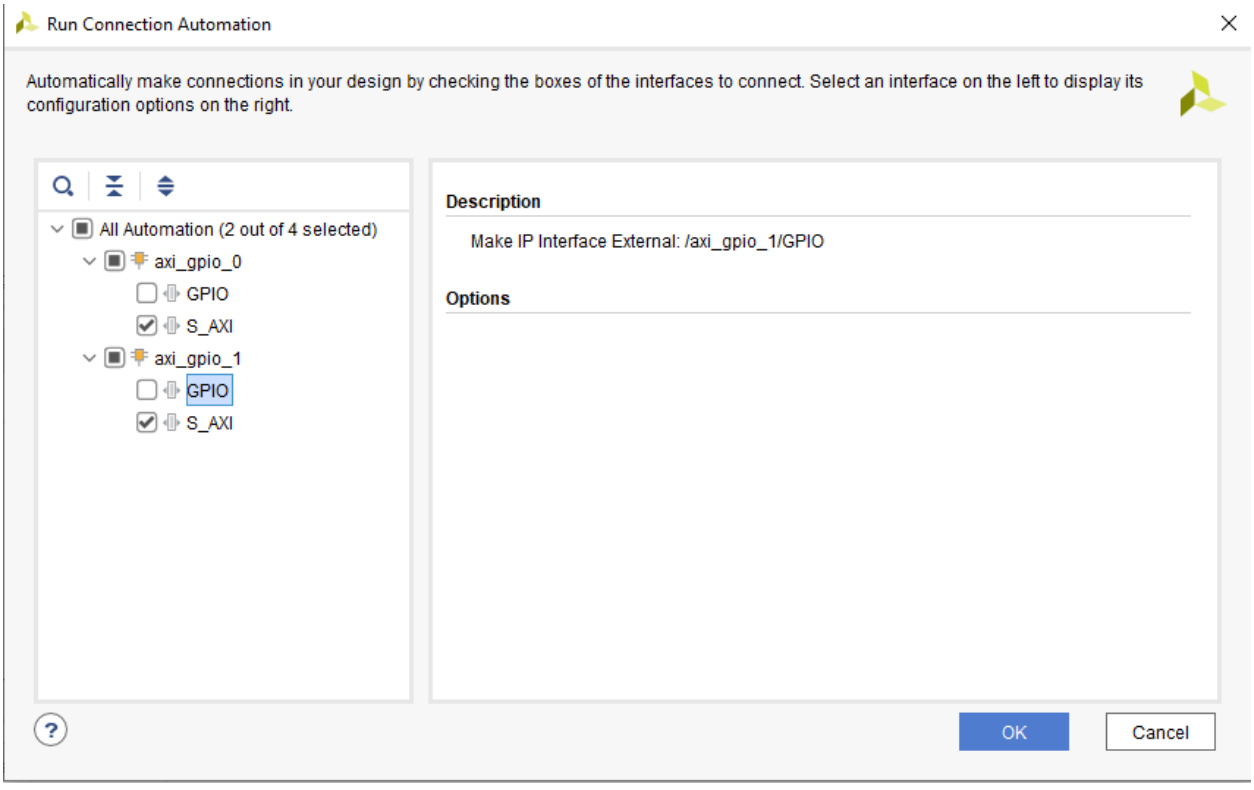

Figure 8: Selecting Run connection Automation Connections in Block Design

After selecting these options, the diagram should be as follows:

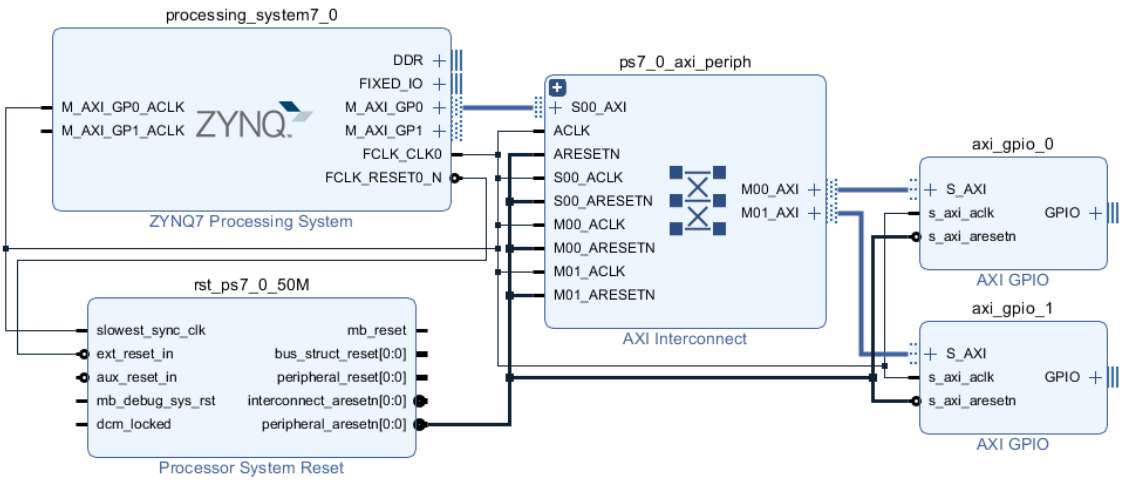

Figure 9: PS GPIO Configuration

Add utility vector logic Ip and set it as not gate you should have something like this.

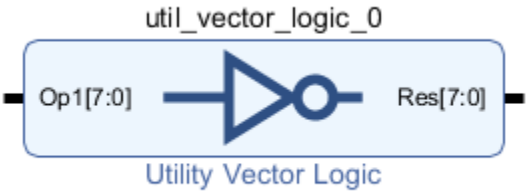

Figure 10: Utility Vector Logic IP

Connect its input to switch and output to AXI GPIO.

Use the second GPIO to connect it to LED.

Select GPIO 0 as following settings.

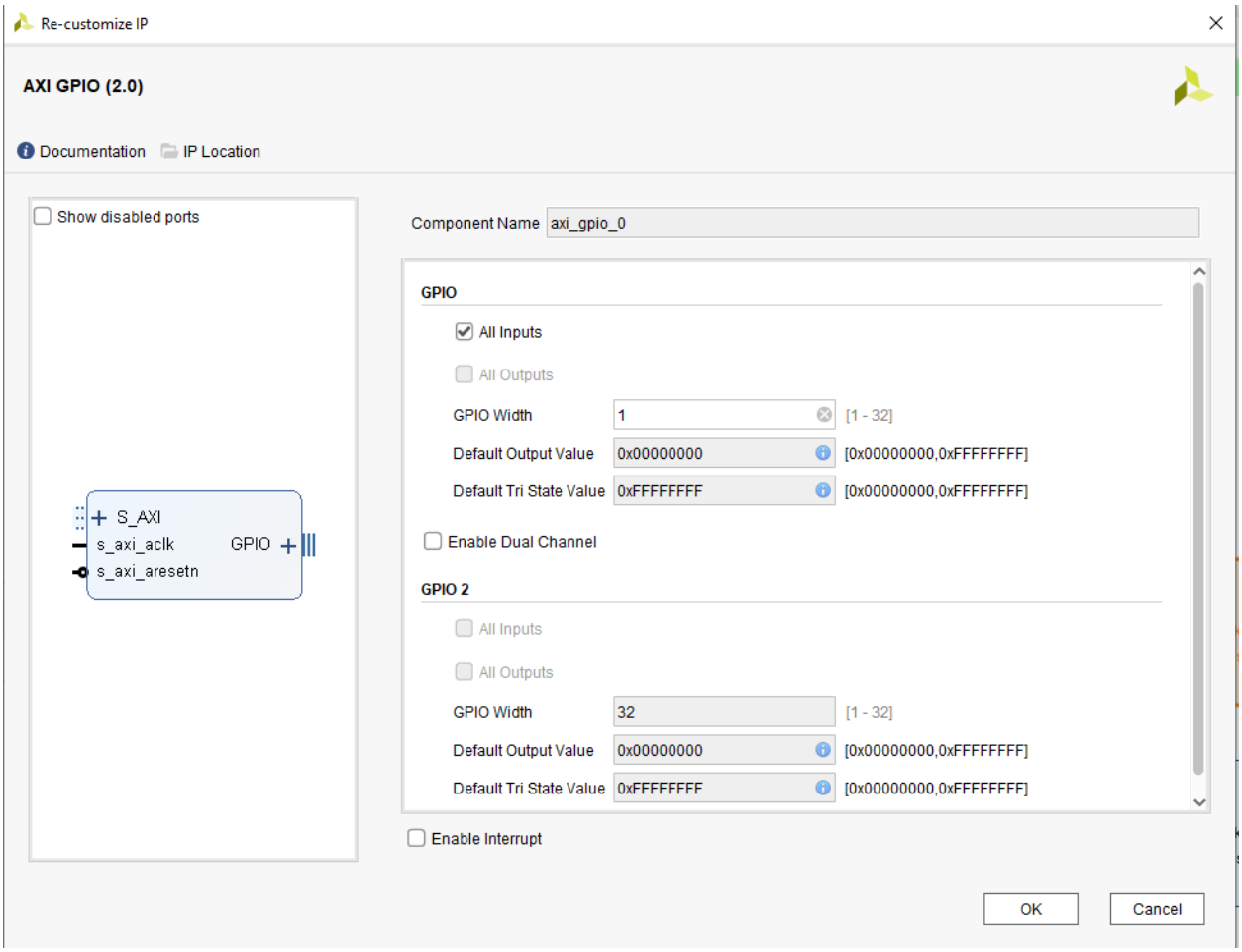

Figure 11: GPIO 0 settings as an Input to PS

And GPIO 1 as following settings:

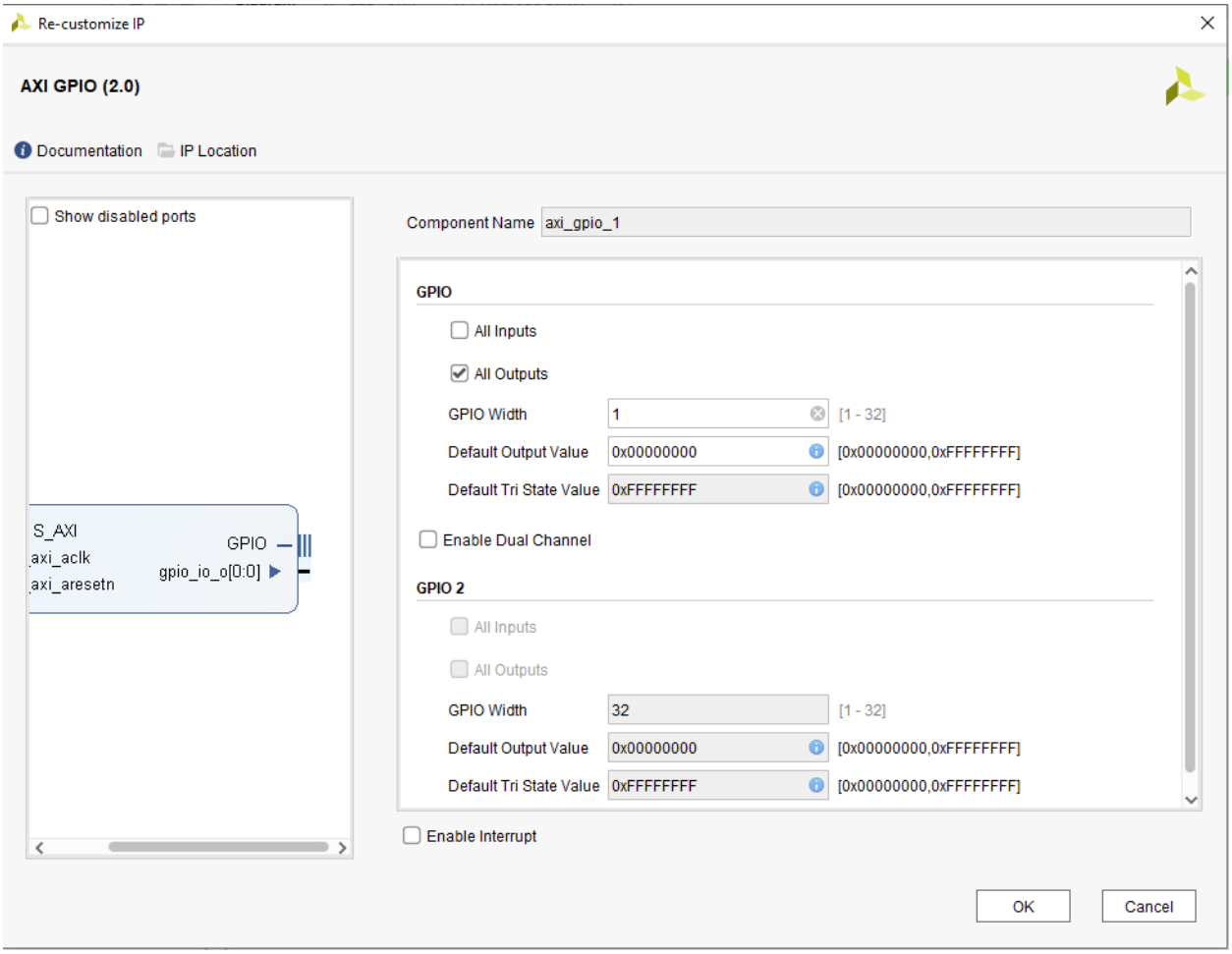

Figure 12: GPIO 1 configuration as on output

All in together the block design should come out to this.

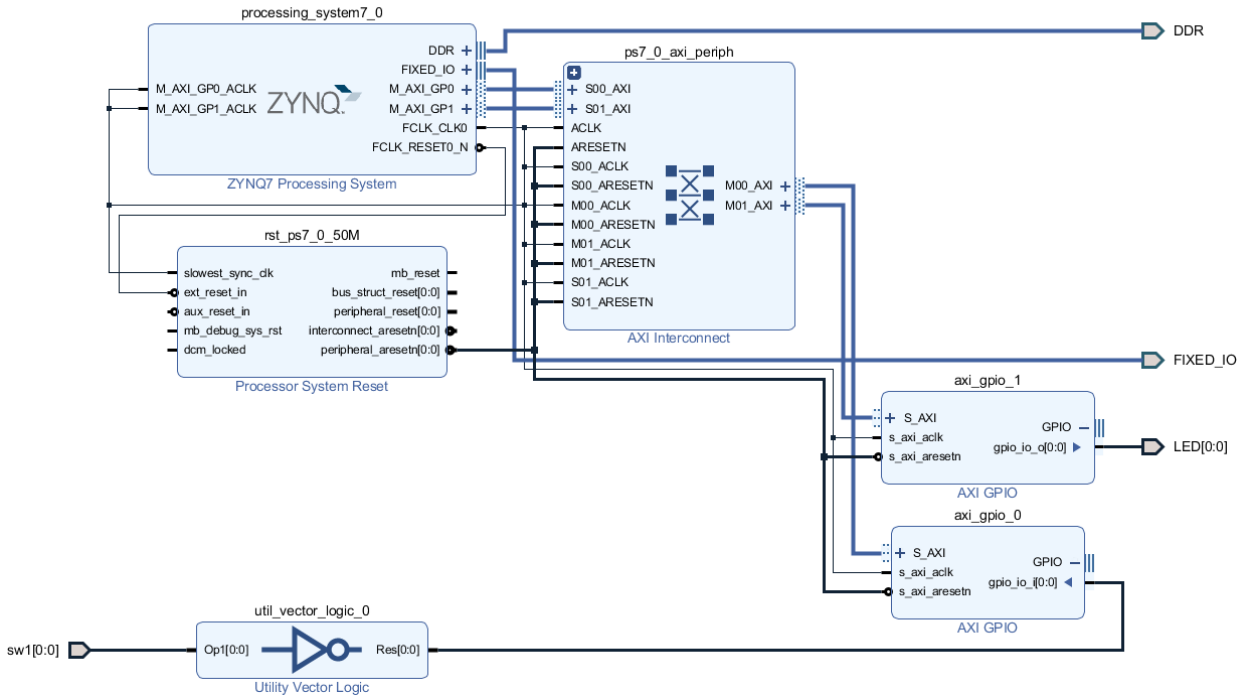

Figure 13: Completed Design

Now, write its constraint file and it should be ready for bitstream.