The mathematical expression must be implemented in the form of:

- RTL Project (operational part and control part)

For each implementation, the following information must be obtained:

- Total execution time of the expression (for certain input values to be chosen, perform simulation and synthesis for different input values. Results must be obtained for the same input values for both types of projects);
- Area used.

It is necessary to present the design of the operational and control parts (state diagram).

Mathematical expression to implement in VHDL:

if (a = b) then perform ($4a^3 + 3b^2 + b^3 + c$); else perform ($(a^3 + b^2) - (b^3 + c)$)