

# How to Connect PL to PS using Zynq 7020

Creating Vivado Project:

Select Device as following

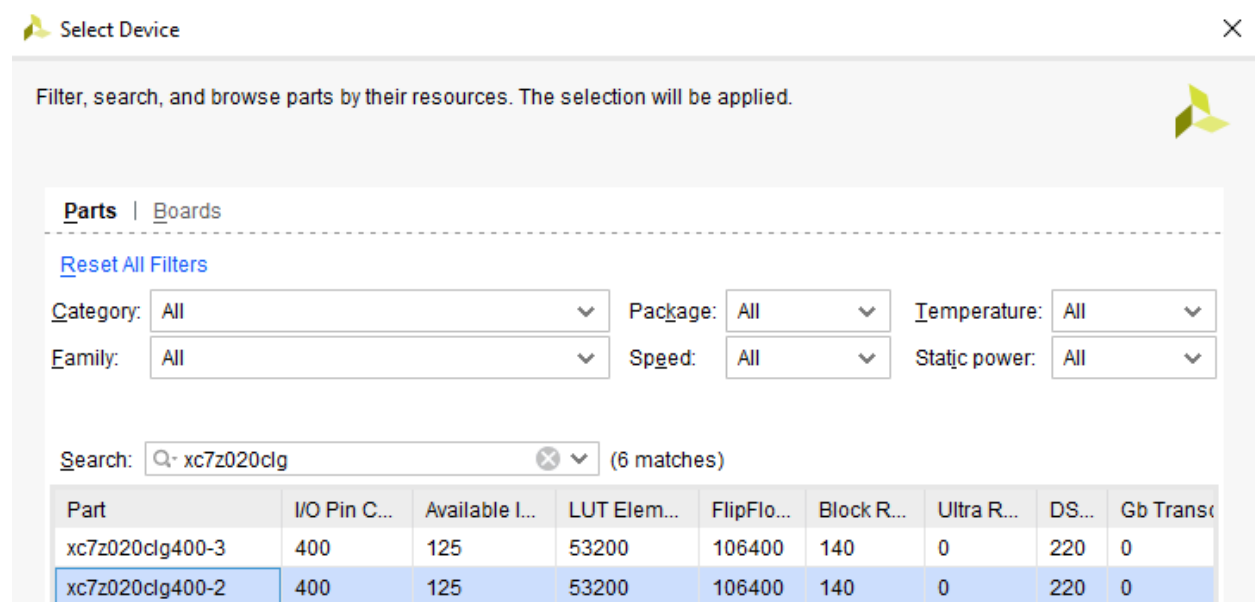


Figure 1: Selecting Target Device

Create Block Design:

IP INTEGRATOR

[Create Block Design](#)

[Open Block Design](#)

[Generate Block Design](#)

SIMULATION

[Run Simulation](#)

RTL ANALYSIS

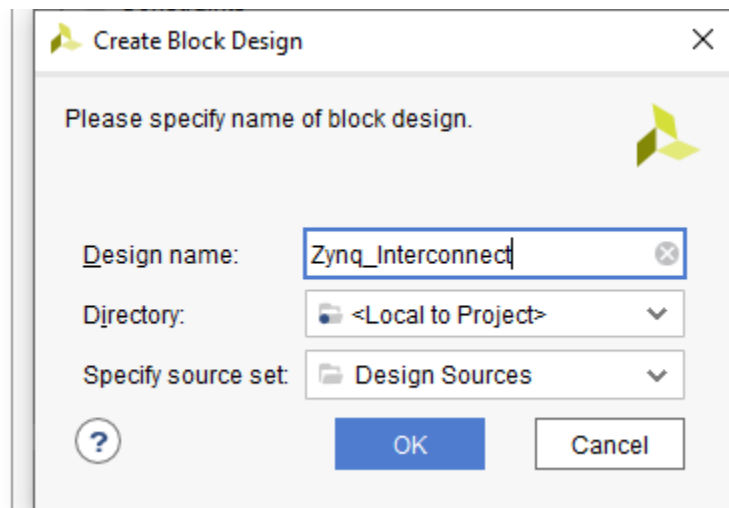


Figure 2: Creating Block Design for the Project

Click OK and continue.

Once you are in Block Design. It should look like this.

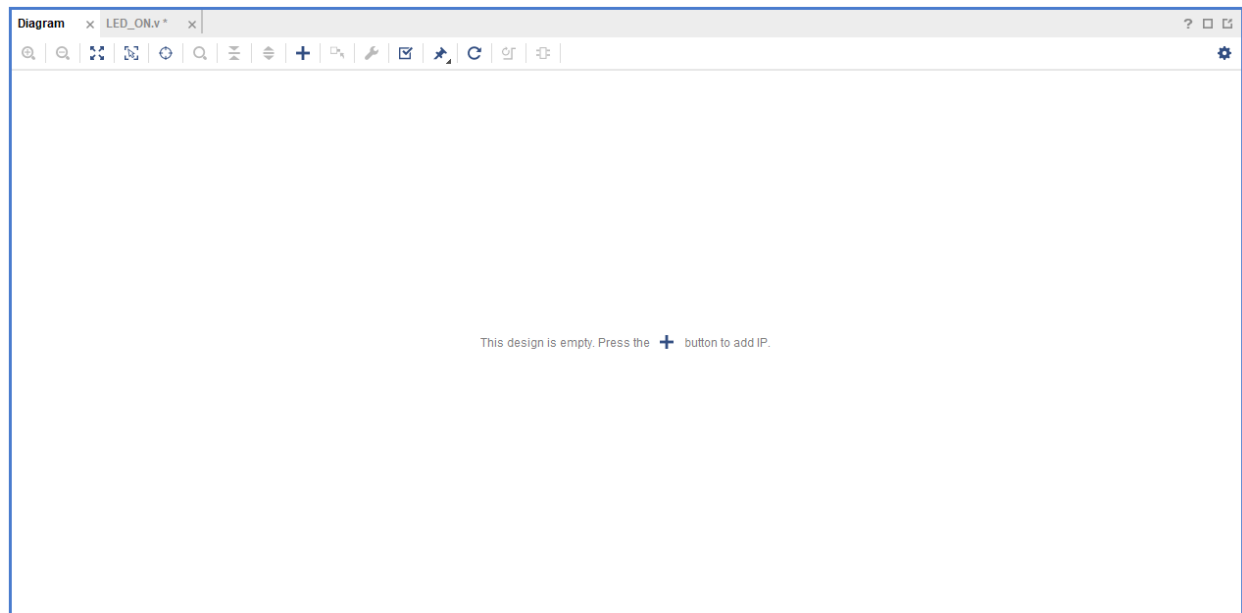


Figure 3: Default Block Design Screen

## Adding IP

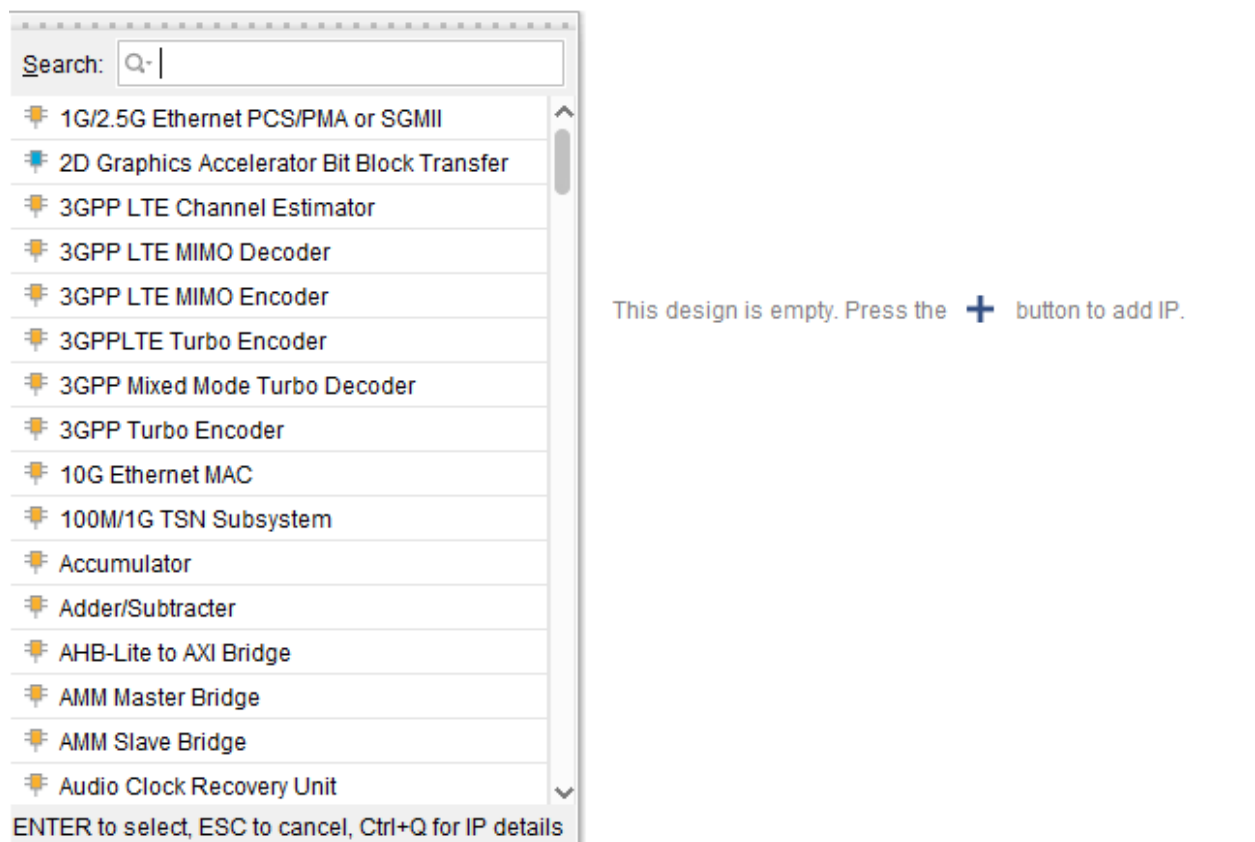


Figure 4: Adding IP to the block Design

Search and add the following Ips:

- ZYNQ7 Processing System
- AXI GPIO x2
- Utility vector Logic

It should look like this

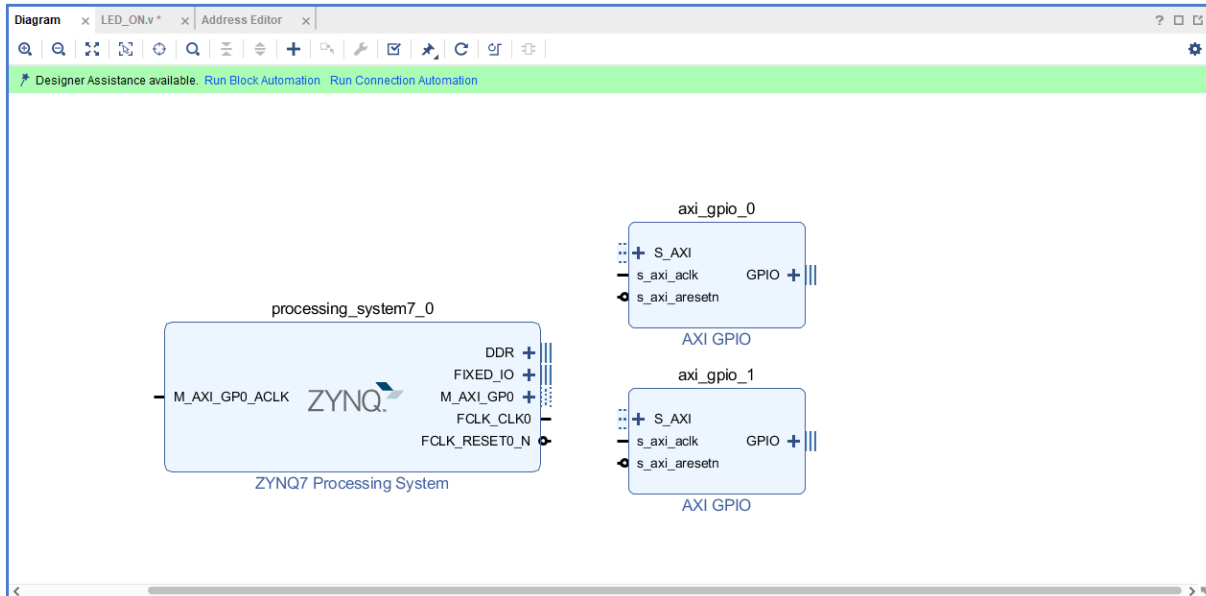


Figure 5: Zynq PS and AXI GPIO IP in block Design

Now, the designer assistance available option should be good. But we need to configure DDR First.

Enable this in PS IP.

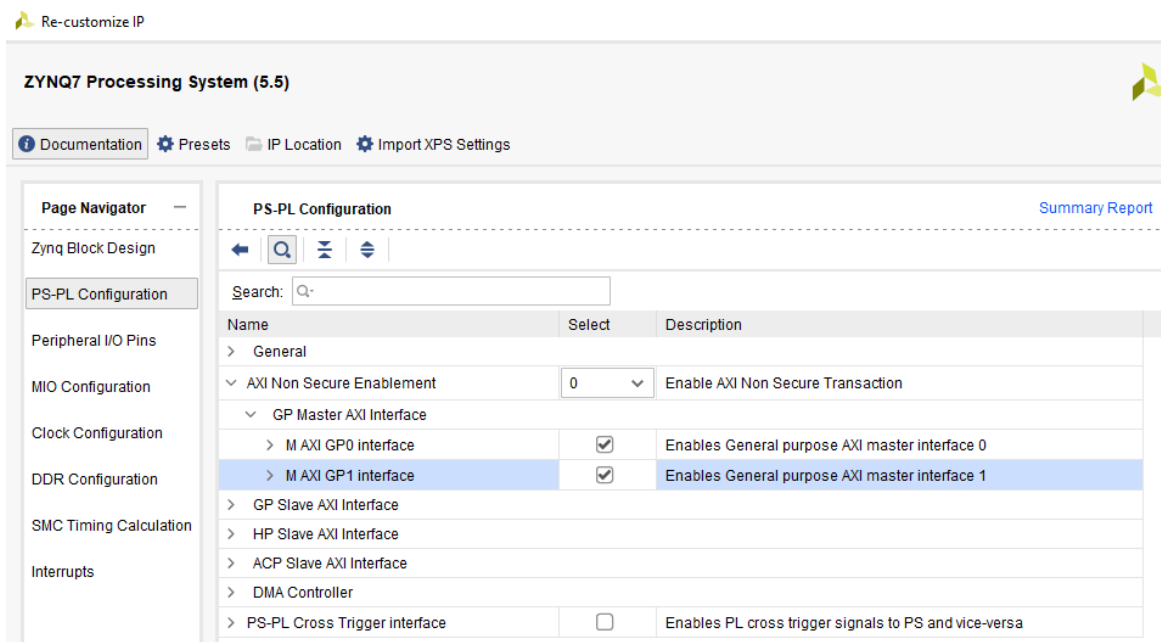


Figure 6: Enable AXI GPIO in PS

Page Navigator

Zynq Block Design
PS-PL Configuration
Peripheral I/O Pins
MIO Configuration
Clock Configuration
DDR Configuration
SMC Timing Calculation
Interrupts

DDR Configuration

Summary Report

☒ Enable DDR

←

Q

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Search:

Name	Select	Description
▼ DDR Controller Configuration		
Memory Type	DDR 3	Type of memory interface. Refer to UG585 Zynq Technical Reference Ma
Memory Part	MT41J128M8 JP-125	Memory component part number. For unlisted parts choose "Custom". T
Effective DRAM Bus Width	32 Bit	Data width of DDR interface, not including ECC data width. Refer to UG5
ECC	Disabled	Enables error correction code support. ECC is supported only for an effe
Burst Length	8	Minimum number of data beats the controller should use when commur
DDR	533.333333	Memory clock frequency. The allowed freq range is (200.000000 : 534.00
Internal Vref	<input type="checkbox"/>	Enables internal voltage reference source. Disable to use external Vref p
Junction Temperature (C)	Normal (0-85)	Intended operating temperature range. Controls the DDR refresh interva
> Memory Part Configuration		
> Training/Board Details	User Input	
Additive Latency (cycles)	0	Additive Latency (cycles). Increases the efficiency of the command and d
> Enable Advanced options	<input type="checkbox"/>	Enable Advanced DDR QoS settings

Figure 7: Configuring DDR in PS

Now, we need to run block automation and select the following options

Run Connection Automation

×

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

Q

≡

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All Automation (2 out of 4 selected)

axi\_gpio\_0

☐ GPIO
☒ S\_AXI

axi\_gpio\_1

☐ GPIO
☒ S\_AXI

Description

Make IP Interface External: /axi\_gpio\_1/GPIO

Options

?

OK

Cancel

Figure 8: Selecting Run connection Automation Connections in Block Design

After selecting these options, the diagram should be as follows:

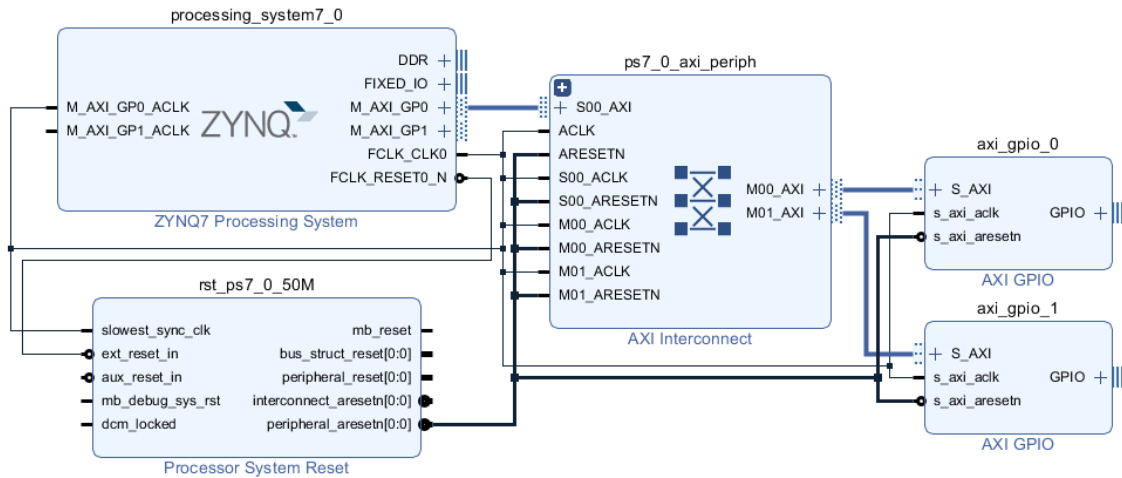


Figure 9: PS GPIO Configuration

Add utility vector logic Ip and set it as not gate you should have something like this.

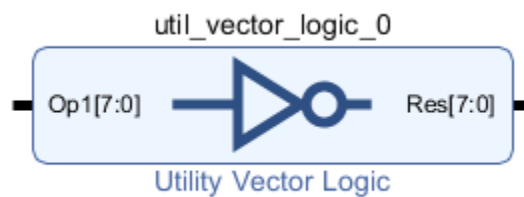


Figure 10: Utility Vector Logic IP

Connect its input to switch and output to AXI GPIO.

Use the second GPIO to connect it to LED.

Select GPIO 0 as following settings.

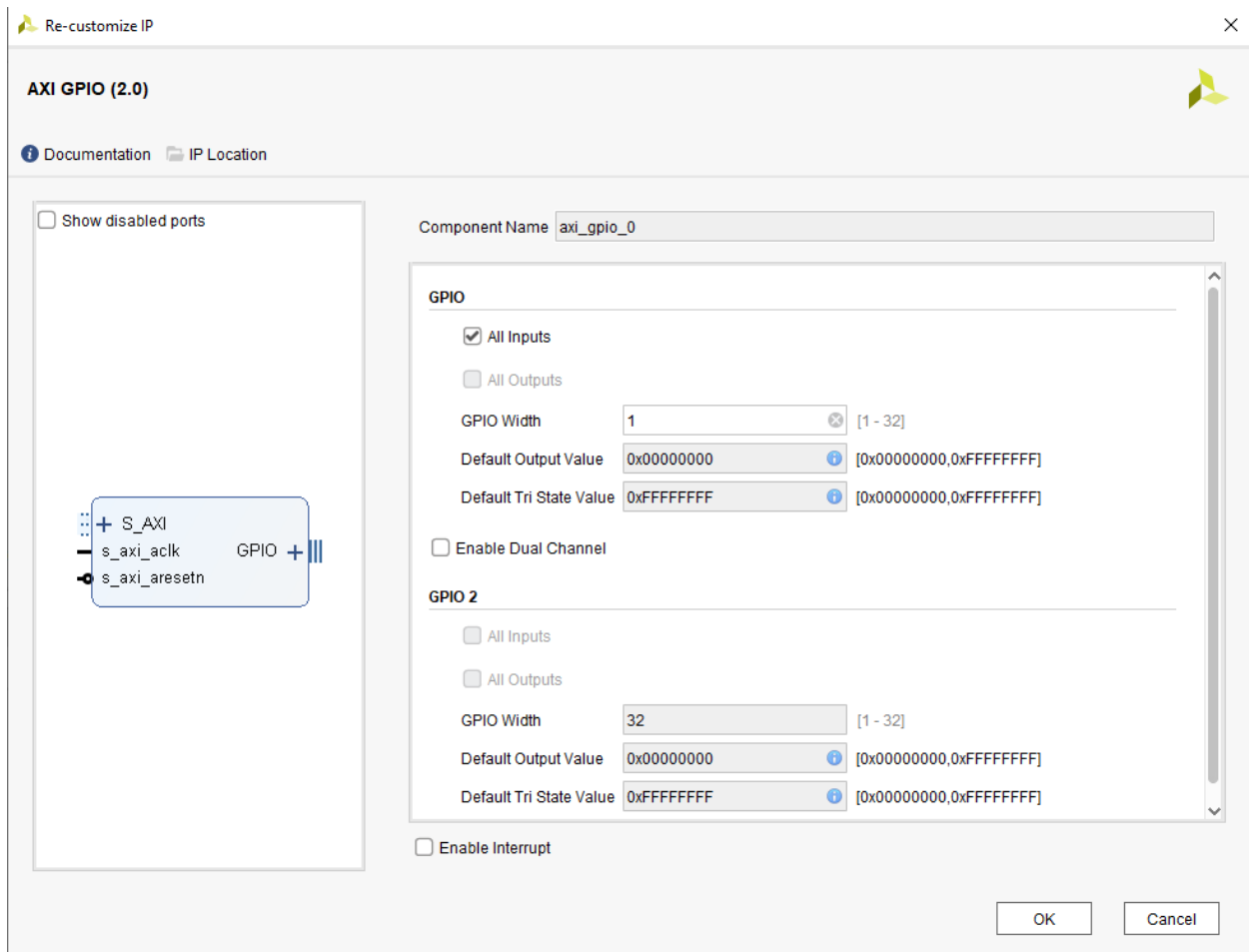


Figure 11: GPIO 0 settings as an Input to PS

And GPIO 1 as following settings:

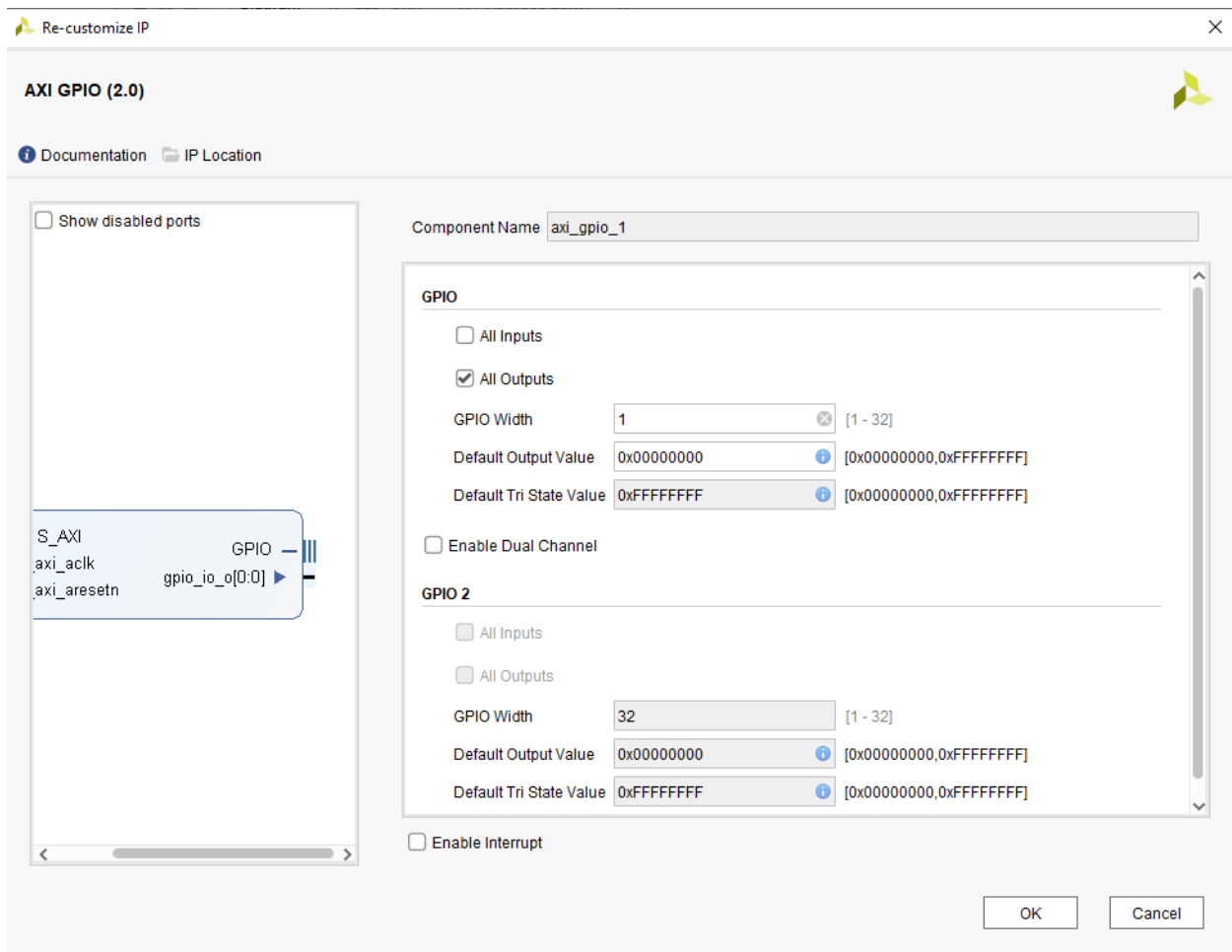


Figure 12: GPIO 1 configuration as on output

All in together the block design should come out to this.

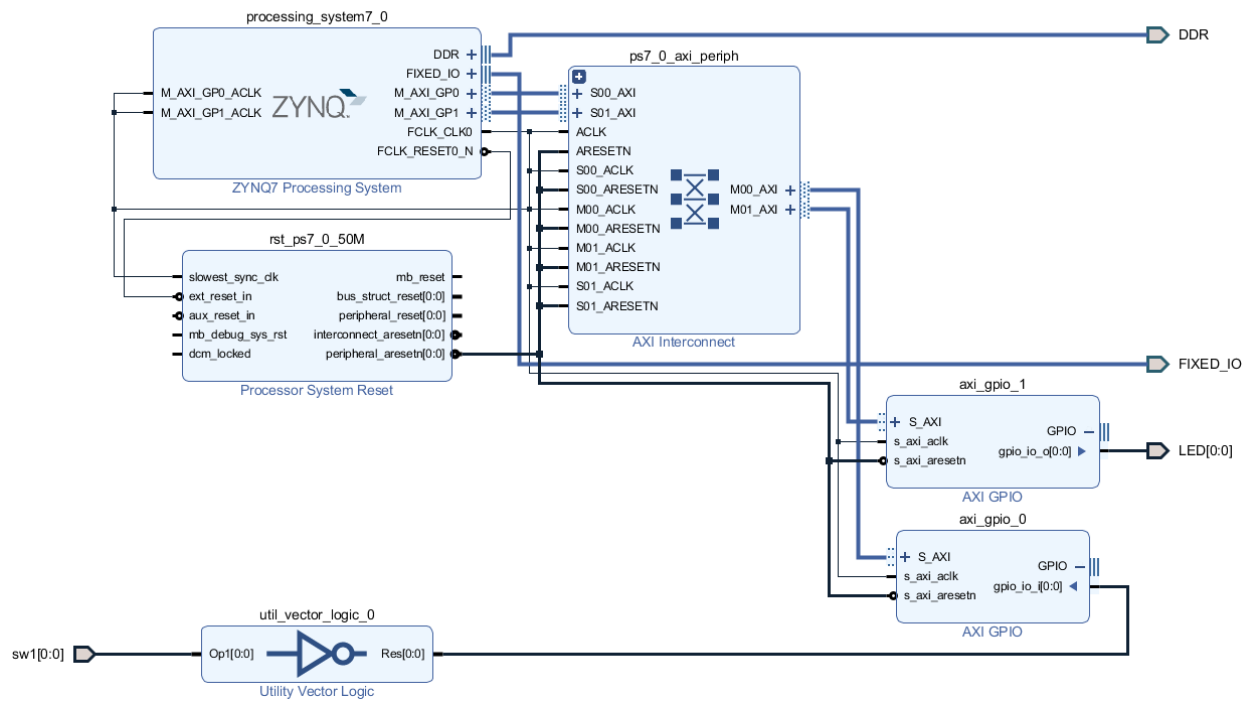


Figure 13: Completed Design

Now, write its constraint file and it should be ready for bitstream.