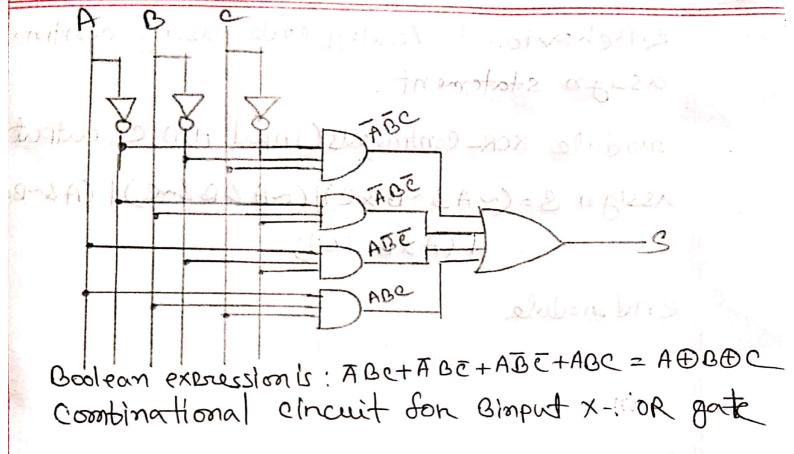
## Pre-lab Report-3

Name: Adri Saha ID: 2019-1-60-024



1. Behavirol Code using procedural model.
module xor-Procedural (input A,B,C, output regs):
always @(A,B,C)

begin S=0; if (~A&~B&C)S=1; if (~A&B&~C) S=1; if (A&B&~C) S=1; if (A&B&C) S=1;

endmodule

2. Behavional Verilog code using continuous assign statement.

module xor-continuous (mput A, B, C, outputs); assign S=(~A&~B&C)|(~A&B&~C)|(A&~B&~C) 1 (A&B&C);

endmodule

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