



East West University
Department of Computer Science and Engineering

Course: CSE345 Digital Logic Design

Expt No.: 6

Title: Multiplexer and Its Use in Combinational Logic Implementation

Objectives:

1. To implement and test a 4-to-1-line multiplexer with active-LOW enable input using discrete gates.
2. To implement and test combinational logic function using IC 74151 (8-to-1-line multiplexer with active-LOW enable input).

Theory:

Design of multiplexers using discrete gates is discussed in Section 8.7 of textbook. The IC 74151 (8-to-1-line multiplexer with active-LOW enable input) is introduced in Section 8.7 of textbook. Combinational logic implementation using multiplexers is also discussed in Section 8.7 of textbook.

Pre-Lab Report Questions:

Implementing and testing a 4-to-1-line multiplexer with active-LOW enable input using discrete gates:

1. Write the truth table of a 4-to-1-line multiplexer with active-LOW enable input.
2. Draw the logic diagram of a 4-to-1-line multiplexer with active-LOW enable input using discrete gates.

Implementing and testing combinational logic function using IC 74151 (8-to-1-line multiplexer with active-LOW enable input):

3. Prepare the implementation table for implementing the combinational logic function $F(A, B, C, D) = \sum(0, 3, 4, 6, 8, 11, 13, 15)$ using an 8-to-1-line multiplexer.
4. Draw the logic diagram for implementing the above logic function using IC 74151 (8-to-1-line multiplexer with active-LOW enable input).

ICs Required:

7404 Hex Inverters (NOT gates)

7421 Double 4-input AND gates

7432 Quadruple 2-input OR gates

74151 8-to-1-line multiplexer with active-LOW enable input

Pin Diagram of the Required ICs:

1	1A	V_{CC}	14	1	1A	V_{CC}	14	1	1A	V_{CC}	14
2	1Y	6A	13	2	1B	2D	13	2	1B	4B	13
3	2A	6Y	12	3	NC	2C	12	3	1Y	4A	12
4	2Y	5A	11	4	IC	NC	11	4	2A	4Y	11
5	3A	5Y	10	5	ID	2B	10	5	2B	3B	10
6	3Y	4A	9	6	1Y	2A	9	6	2Y	3A	9
7	GND	4Y	8	7	GND	2Y	8	7	GND	3Y	8

7404 (6 NOT)

7421 (2 4-In AND)

7432 (4 2-In OR)

16	15	14	13	12	11	10	9
V_{CC}	I_4	I_5	I_6	I_7	A_0	A_1	A_2
74151							
I_3	I_2	I_1	I_0	O	O	$EGND$	
1	2	3	4	5	6	7	8

Lab Procedure:

Implementing and testing a 4-to-1-line multiplexer with active-LOW enable input using discrete gates:

1. Construct the logic diagram for a 4-to-1-line multiplexer with active-LOW enable input from your pre-lab report using discrete gates. Connect the four data inputs I_0 through I_3 to an arbitrary 4-bit binary number. Connect A_1 , A_0 , and E to three switches and the output O to an LED indicator.
2. Apply binary 00 to 11 to address lines A_1A_0 and observe the outputs by changing E input. Check that, when the circuit is enabled, the output is equal to the selected data input.
3. Show the outputs of the circuit to your instructor.

Implementing and testing combinational logic function using IC 74151 (8-to-1-line multiplexer with active-LOW enable input):

4. Construct the logic diagram for implementing the logic function $F(A, B, C, D) = \sum(0, 3, 4, 6, 8, 11, 13, 15)$ from your pre-lab report using IC 74151 (8-to-1-line multiplexer with active-LOW enable input).
5. Show the outputs of the circuit to your instructor.

Pre-lab report submission:

6. Submit the pre-lab report to your instructor.

Post-Lab Report Questions:

1. Write structural Verilog code for the logic diagram for a 4-to-1-line multiplexer with active-LOW enable input from your pre-lab report and simulate it using Quartus II software.
2. Write behavioral Verilog code for a 4-to-1-line multiplexer with active-LOW enable input and simulate it using Quartus II software.