East West University
Department of Computer Science and Engineering

Course: CSE345 Digital Logic Design
Expt No.: 4
Title: Binary Adder and Subtractor

Objectives:
1. To implement and test a full adder using discrete gates.
1. To implement and test a 4-bit 2's complement adder/subtractor using IC 7483 (4-bit binary parallel adder).

Theory:
Design of full-adder using discrete gates is discussed in Section 7.2 of textbook. The IC 7483 (4-bit binary parallel adder) is introduced in Section 7.8 of textbook. Design of a 4-bit 2's complement adder/subtractor using a 4-bit binary parallel adder is discussed in Section 7.6 of textbook.

Pre-Lab Report Questions:
Implementing and testing a full adder using discrete gates:
1. Draw the logic diagram of a full-adder using EXOR gates.
2. Write the truth table of a full-adder.

Implementing and testing a 4-bit 2's complement adder/subtractor using IC 7483 (4-bit binary parallel adder):

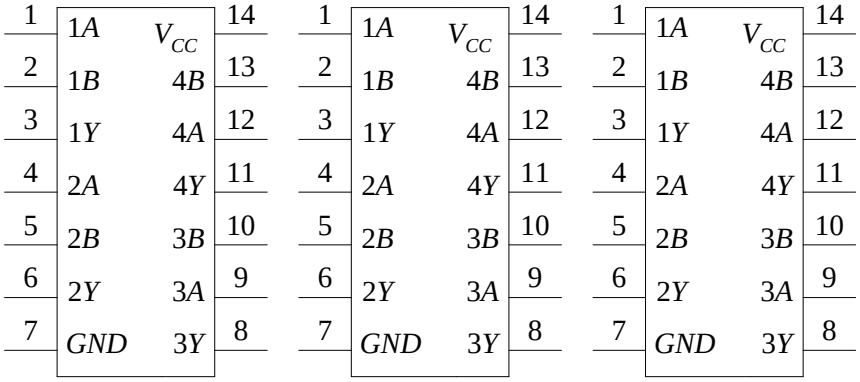
3. Draw the schematic diagram for implementing a 4-bit 2's complement adder/subtractor using IC 7483 (4-bit binary parallel adder). Write the operation of the circuit explaining how the mode selector input *M* determines the mode of operations as adder or subtractor.

2's complement addition and subtraction:
4. Perform the following 2's complement additions and subtractions using 4-bit data:

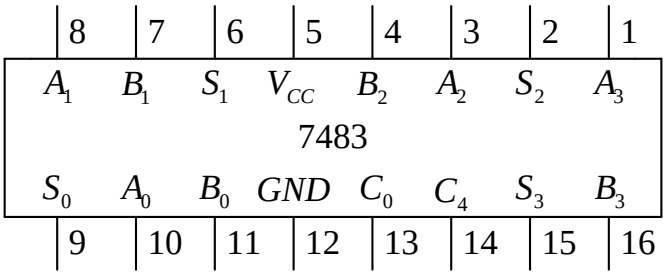
3 + 3	3 – 2
3 + 4	3 – 3
3 + 5 (overflow)	3 – 4

ICs Required:
7408 Quadruple 2-input AND gates
7432 Quadruple 2-input OR gates
7486 Quadruple 2-input EXOR gates
7483 4-bit binary parallel adder

Pin Diagram of the Required ICs:



7408 (4 2-In AND) **7432** (4 2-In OR) **7486** (4 2-In EXOR)



Lab Procedure:

Implementing and testing a full adder using random gates:

1. Construct the logic diagram for a full-adder from your pre-lab report on the breadboard. Connect the three inputs of the circuit to three data switches and two outputs to two LED indicators.
2. Show the outputs of the circuit to your instructor.

Implementing and testing a 4-bit 2's complement adder/subtractor using IC 7483 (4-bit binary parallel adder):

3. Construct the schematic diagram for a 4-bit 2's complement adder/subtractor using IC 7483 from your pre-lab report. Connect the four *A* inputs to a fixed binary number 0011 (decimal 3) to two data switches and the four *B* inputs to four data switches. Connect the mode select input *M* to a data switch. Connect the four sum outputs *S* and carry output C_4 to five LED indicators.
4. Perform the following addition/subtraction operations.

3 + 3	3 – 2
3 + 4	3 – 3
3 + 5 (overflow)	3 – 4

5. Show the outputs of the circuit to your instructor.

Post-Lab Report Questions:

1. Write structural Verilog code for full-adder circuit form your pre-lab report and simulate it using Quartus II software.
2. Write behavioral Verilog code for a 4-bit parallel adder and simulate it using Quartus II software.