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ID : 2019-1-60-024
Sub :

Sat ☐ Sun ☐ Mon ☐ Tue ☐ Wed ☐ Thu ☐ Fri ☐

Time : Date : 18 / 04 / 21

1. Draw the logic diagram of a full-adder using EXOR gates.

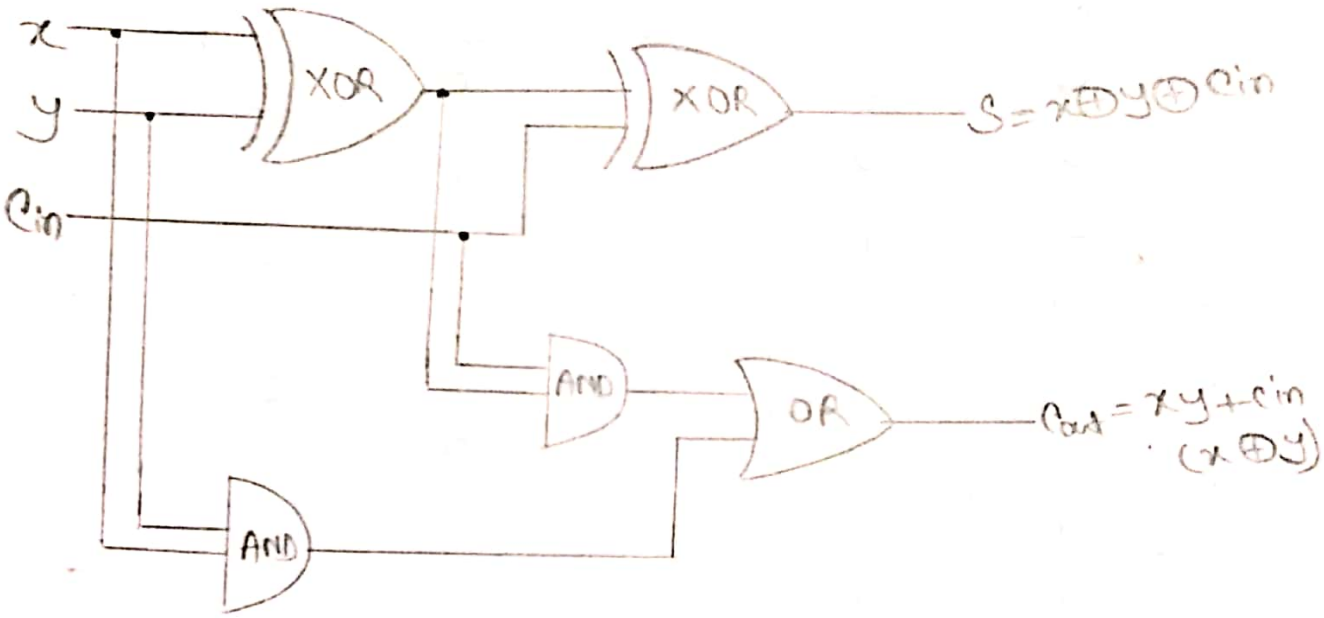
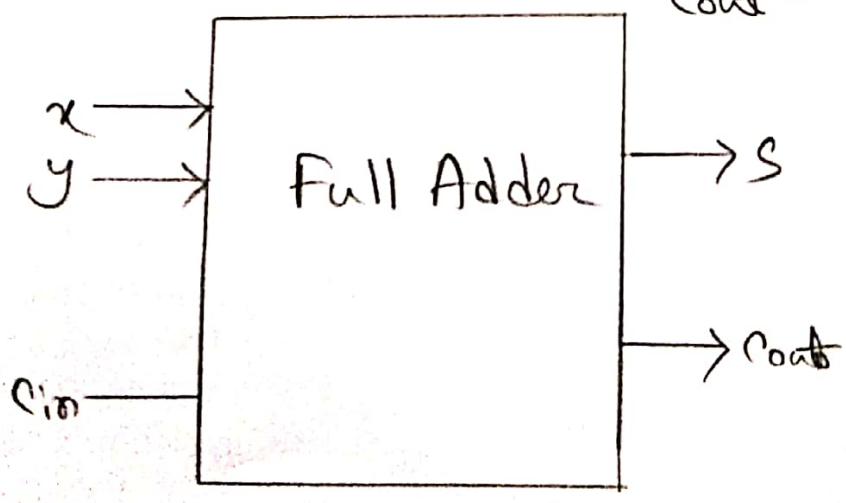


Figure: 1 bit full adder logic circuit using XOR gates. (using 2 half adder)

Boolean expressions are, $S = x \oplus y \oplus c_{in}$

$C_{out} = xy + c_{in}(x \oplus y)$



2. Truth table of a full adder:

Input			Output	
x	y	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth table of full adder