East West University
Department of Computer Science and Engineering

Course: CSE345 Digital Logic Design
Expt No.: 1
Title: Schematic and Structural Verilog Simulation of Combinational Logic Circuits

Objectives:
1. To learn schematic simulation of combinational logic circuits using Quartus II software.
2. To learn structural Verilog simulation of combinational logic circuits using Quartus II software.

Introduction to Structural Verilog Code:

Verilog Hardware Description Language (HDL) is discussed in Chapter 14 of Textbook of this course (Md. Mozammel Huq Azad Khan, *Digital Logic Design*, University Grants Commission of Bangladesh, Dhaka, Bangladesh, 2006). Structural Verilog coding of a combinational logic circuit is discussed in Section 14.2.1. Please go through this section before proceeding with this experiment. If needed, take help from the TA of this course. The structural Verilog code of the combinational logic circuit of Figure 1 is shown below:

```
module expt1_2(input A, B,
               output S);
    wire w1, w2;
    and g1(w1,~A,B),
        g2(w2,A,~B);
    or g3(S,w1,w2);
endmodule
```

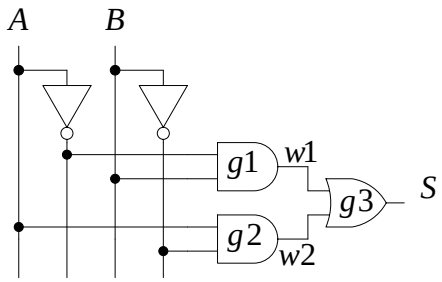


Figure 1: Example of combination logic circuit.

The Boolean expression of the output of the combinational circuit of Figure 1 is $S = A'B + AB'$. The truth table of the circuit is shown in Table 1. The corresponding waveform is shown in Figure 2.

Table 1: Truth table of the combinational circuit of Figure 1.

AB	*S*
00	0
01	1
10	1
11	0

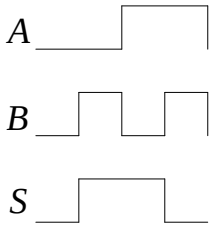


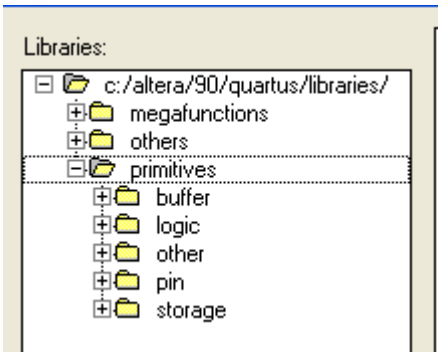
Figure 2: Input/output waveform of the combinational circuit of Figure 1.

Steps to Follow for Schematic Simulation of Combinational Logic Circuit Using Quartus II Software:

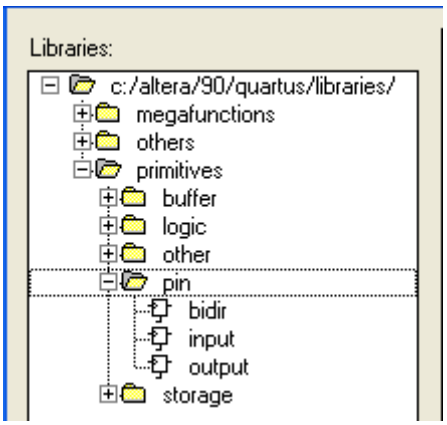
1. Open the Quartus II software.
2. Create Project:
   Click Flie→New Project Wizard→Next. Change working directory to your own directory. Write name of the Project. Name of the Top level design entity will be automatically seen same as the name of the Project. Click Finish

3. Create Design:
   Click File→New→Block Diagram/Schematic File→OK. Design window will appear.

   Click Symbol Tool icon  for inserting gate symbols. For inserting logic gates of Figure 1, expand Libraries, then primitive, then logic; and then select not, and2, and or2 as needed. Click OK. The cursor symbol will show the gate symbol. By moving the cursor position, place the gate symbol in a suitable location of the design window and insert the symbol by clicking the mouse. Press ESC key to disappear the gate symbol from the cursor.



   For insert input pins (input) and output pin (output), expand Libraries, then primitives, then pin; and then insert the pins as needed. Double click on the names of the input and output pins and change there names according to Figure 1.



Connect the wires using Orthogonal Node Tool icon  . Click on Orthogonal Node Tool icon. Place the cursor at the start location of the wire and then drag the cursor to the end location of the wire while pressing the left button of the mouse. Release the mouse button.

The drawn schematic circuit corresponding to the circuit of Figure 1 will look like Figure 3.

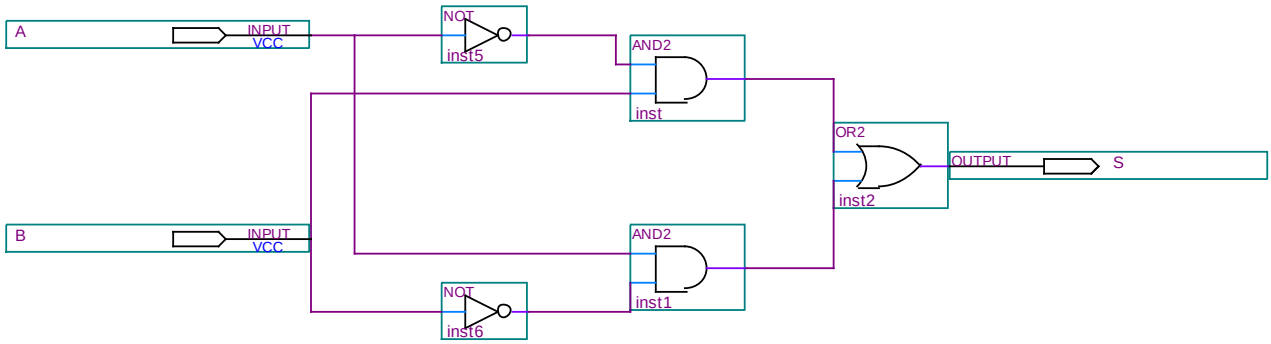


Figure 3: Schematic circuit corresponding to Figure 1.

4. Simulate the Design:
Determine simulation mode. Click Assignment→Settings. Choose simulation mode to Functional. Click OK

Compile the design. Click Processing→Start Compilation→Yes. File name will automatically be your top level entity name. Click Save. Compilation message will appear. Click OK.

Create input vector waveform. Click File→New→Vector Waveform File→OK. Vector input window will appear. Right click on the left side of the window. Click Insert→Insert Node or Bus→Node Finder→List→>>→OK→OK. Input and output signal lines will appear in the window.

Configure grid. Click Edit→End Time→40 ns (number of possible input combinations, 4 × 10 ns) →OK.

Fit the waveform in the window. Right click on the window. Click Zoom→Fit in window.

Determine input waveform by selecting appropriate location of the input signal and then pressing 1.

The input vector file will look like Figure 4.

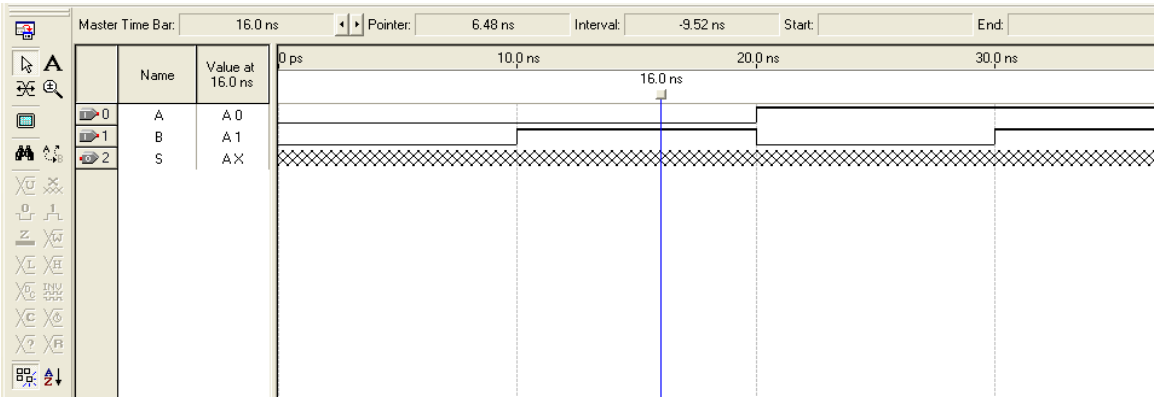


Figure 4: Input waveform.

Generate Netlist. Click Processing→Generate Functional Simulation Netlist→Yes→Save. Netlist generation message will appear. Click OK.

Simulate design. Click Processing→Start Simulation→OK.

The simulation output will look like Figure 5. Verify the simulation result with expected output of the circuit of Figure 1 as shown in Figure 2.

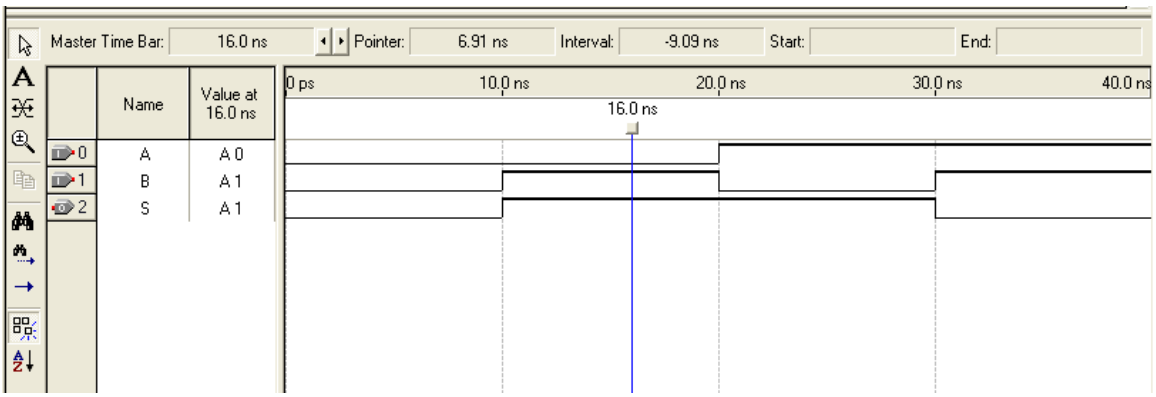


Figure 5: Simulation output.

Steps to Follow for Simulation of Verilog Code for Combinational Logic Circuit Using Quartus II Software:

For simulating Verilog code using Quartus II software, all steps are as above except step 3, which is as follows:

3. Write the Verilog Code:
   Click File→New→Verilog HDL File→OK. Editor window will appear. Write your Verilog code.

   The editor window will look like Figure 6.

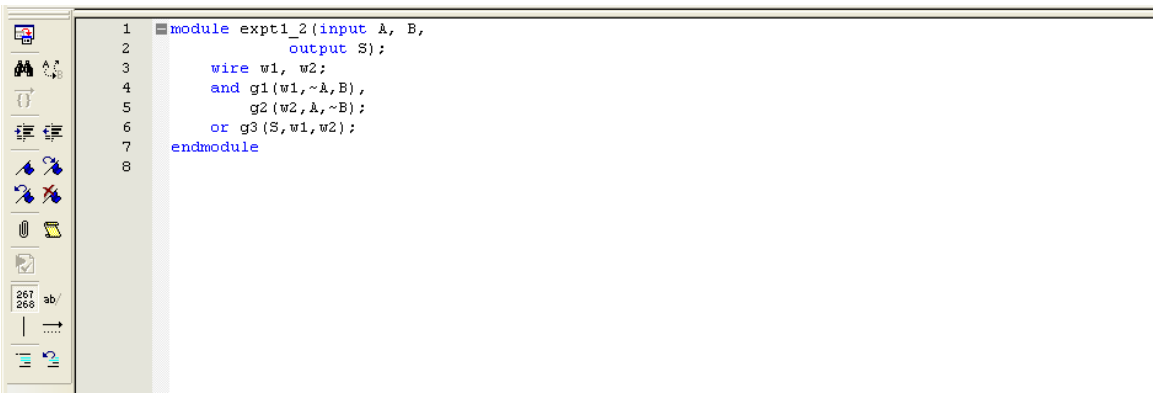


Figure 6: Editor window.

Pre-Lab Report Questions:

1. Determine the Boolean expression and the truth table of the output *S* of the combinational circuit of Figure 7.
2. Write down the structural Verilog code for describing the combinational circuit of Figure 7.

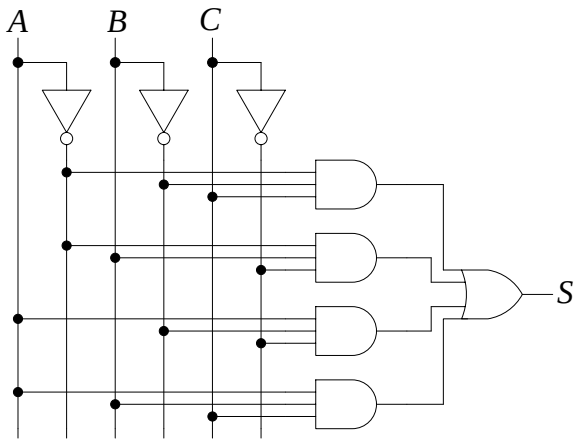


Figure 7: Combinational circuit for lab practice.

Lab Procedure:

1. Perform the schematic simulation of the combinational circuit of Figure 7. Copy the schematic circuit and the simulation waveform in a Word file.
2. Perform the structural Verilog simulation of the combinational circuit of Figure 7. Copy the simulation waveform in the same Word file.
3. Write down Date, Course Number, Experiment Number, and Student ID at the top of the Word file. Get a printout of the Word file and have it signed by your instructor.
4. Submit the pre-lab report and the data sheet together to your instructor.