ID: 2019-1-60-024

Sub: Pre-lab

Sat ☐ Sun ☐ Mon ☐ Tue ☐ Wed ☐ Thu ☐ Fri ☐

Time: Date: 11 / 03 / 2021

1.

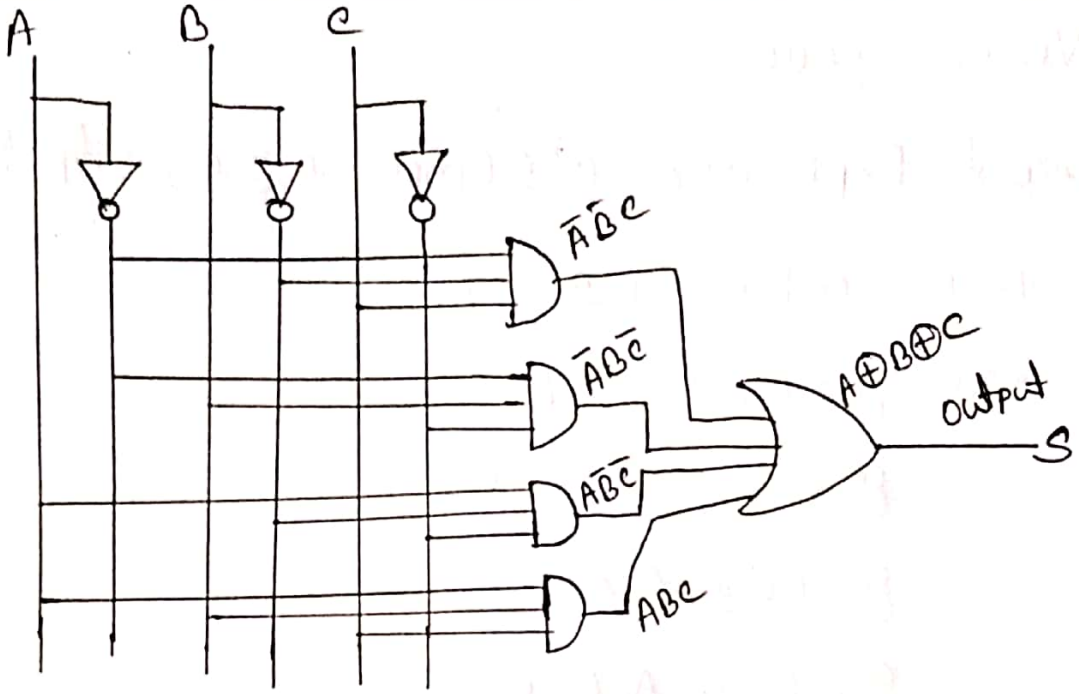

Figure-7

Boolean expression, $S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= A \oplus B \oplus C$ [3 input Ex-or gate]

A	B	C	$\bar{A}\bar{B}C$	$\bar{A}B\bar{C}$	$A\bar{B}\bar{C}$	ABC	S
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1
0	1	0	0	1	0	0	1
0	1	1	0	0	0	0	0
1	0	0	0	0	1	0	1
1	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0
1	1	1	0	0	0	1	1

JPS

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2. Verilog Code:

```
module Experiment-2-2(input A,B,C, output S);
  wire w1,w2,w3,w4;
  and g1(w1,(~A,~B,C),
         g2(w2,~A,B,~C),
         g3(w3,A,~B,~C),
         g4(w4,A,B,C);
  or g5(S,w1,w2,w3,w4);
endmodule
```