Post Lab Report-01

Date: 15 March 2021	Course: CSE345
Experiment 1	Id: 2019-1-60-024
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Experiment Name: Schematic and Structural Verilog Simulation of Combinational Logic Circuits

Abstract: Logic Circuit design is one of the introductory courses for Electrical Engineering and Electrical Engineering Technology students. Ideally, it introduces students to hands-on circuit building, problem solving, testing and function verification. The lab teaches them to use correct lab equipment from digital meters and oscilloscopes to digital logic analyzers. The logic design lab is a learning experience that most students enjoy, as it is their first hands-on experience with designing and building miniature systems.

Introduction:

Combinational Logic Circuits: Combinational Logic Circuits are memoryless digital logic circuits whose output at any instant in time depends only on the combination of its inputs. Each type of gate has one or more (most often two) inputs and one output. The principle of operation is that the circuit operates on just two voltage levels, called logic 0 and logic 1.

Uses:

- Use in computer circuits to perform Boolean algebra on input signals and on stored data.
- Practical computer circuits normally contain a mixture of combinational and sequential logic.

Objective: Our main goal is to verify Schematic and Structural Verilog Simulation of Combinational Logic Circuits.

• Creating a project using Quartus II software.

• Design entry using Verilog code.

• Assigning the circuit inputs and finding specific outputs.

• Simulating the designed circuit.

Theory and experiments results:

A. **2 Input XOR Gate:** The logic function implemented by a 2-input Ex-OR is given as either: “A OR B but NOT both” will give an output at Q. In general, an Ex-OR gate will

give an output value of logic “1” ONLY when there are an ODD number of 1’s on the inputs to the gate, if the two numbers are equal, the output is “0”.

Uses:

- It is used in simple digital addition circuits which calculate the sum and carry of two (half-adder) or three (full adder) bit numbers.
- XOR gates are also used to determine the parity of a binary number, i.e., if the total number of 1's in the number is odd or even.
- The XOR gate is achieved by combining standard logic gates together to form more complex gate functions that are used extensively in building arithmetic logic circuits, computational logic comparators and error detection circuits.
- The two-input “Exclusive-OR” gate is basically a modulo two adder, since it gives the sum of two binary numbers and as a result are more complex in design than other basic types of logic gate.

Boolean expression is:

$$S = (A \oplus B) = A.B' + A'.B$$

Schematic Circuit:

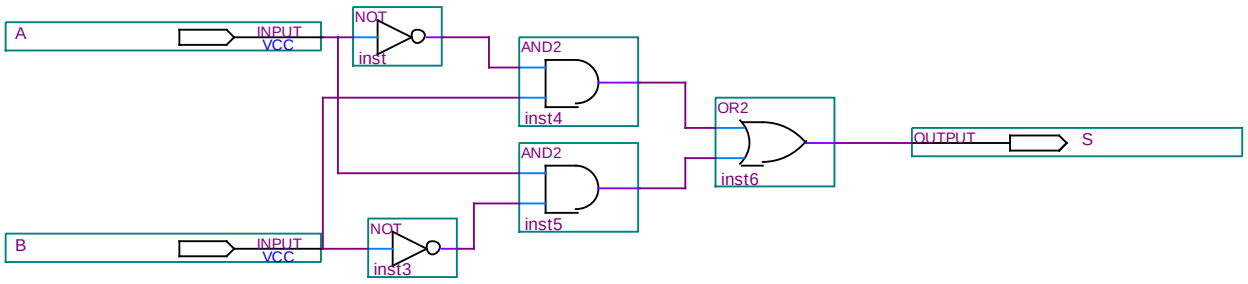

Figure 1 : 2 input XOR Gate Circuit

Schematic drawing: This is a schematic of the design using primitive components such as logic gates, flipflops, decoders, encoders and wires for interconnections. There is a list of components in the software library that users can pick from.

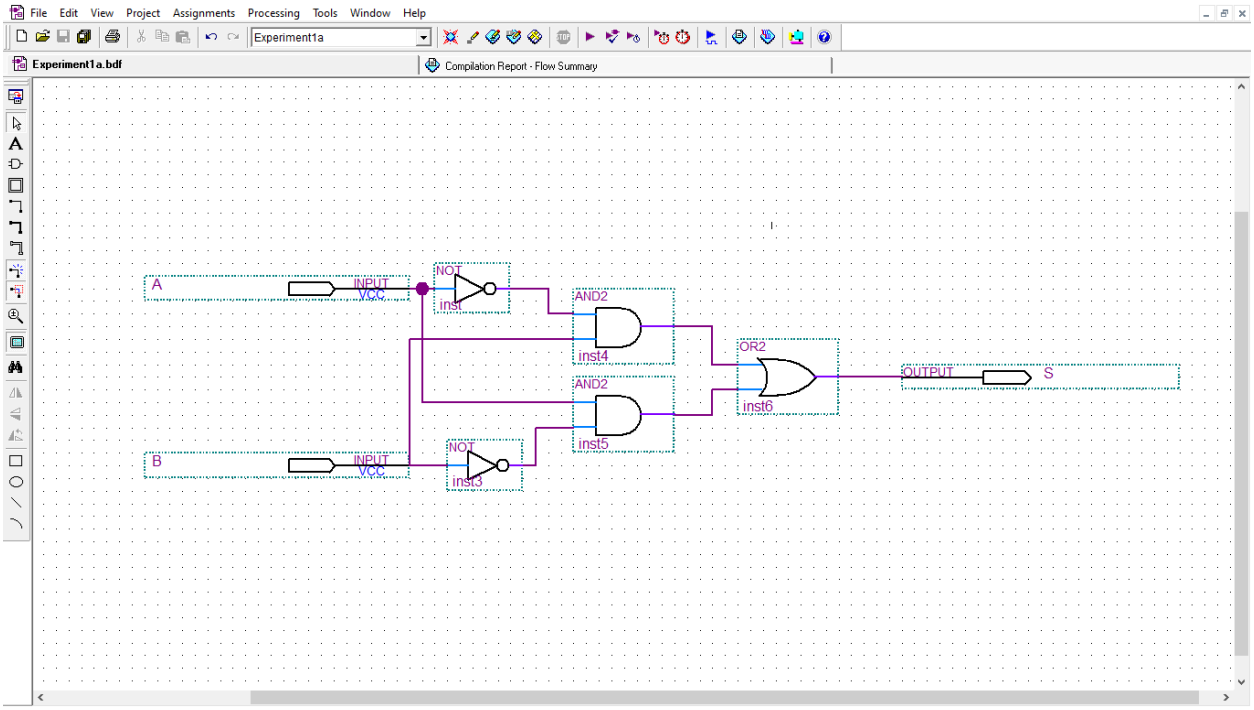

Figure 2 : 2 input XOR Gate Circuit Screenshot

The truth table of 2 input XOR gate is:

Here, A & B is input & output S.

Input		Output
A	B	S
0	0	0
0	1	1
1	0	1
1	1	0

Figure 3: Truth table of 2 input XOR Gate

Schematic Waveform Simulation:

In this simulation, we have taken end time 40 nano seconds. So, time period of A & B is 40 & 20 nano seconds in sequent. As there are 2 inputs.

We see, in exclusive or gates output is “high” or 1 if the input logic levels are different.

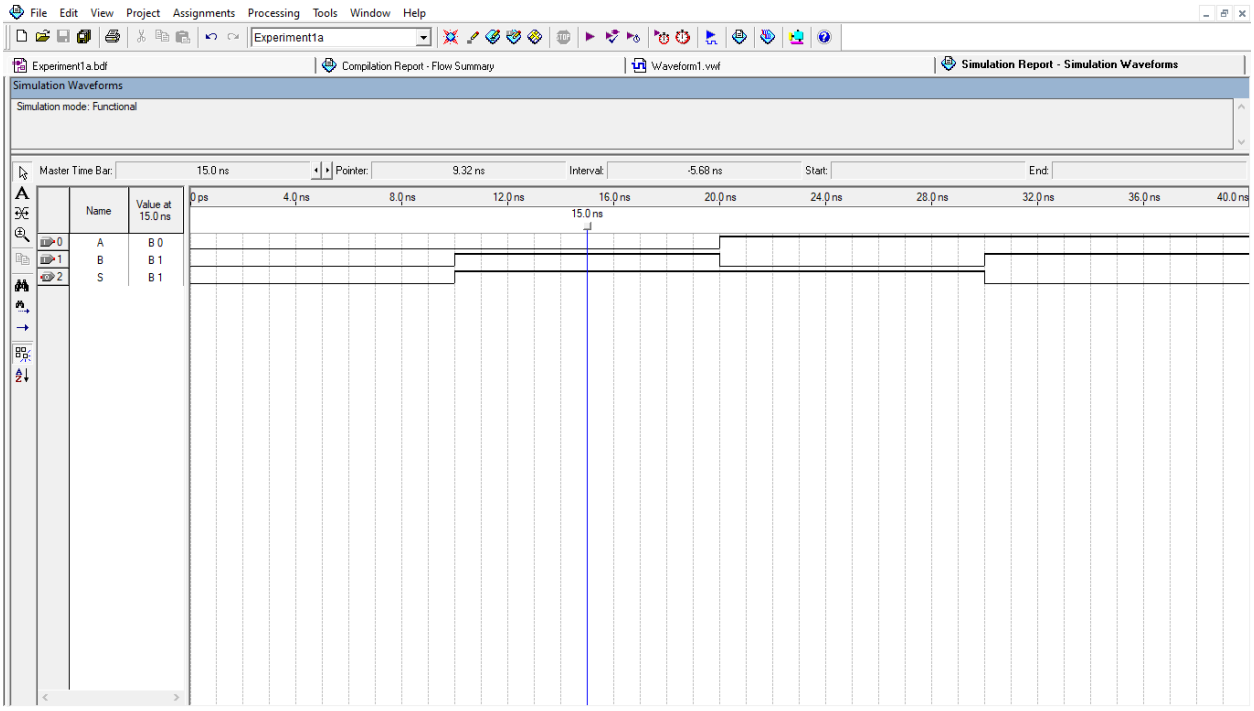

Figure 4: 2 input XOR Gate Simulated Waveform by Circuit

Verilog Codes: Verilog is a Hardware Description Language; a textual format for describing electronic circuits and systems.

Uses:

- Applied to electronic design.
- Verilog is intended to be used for verification through simulation, for timing analysis, for test analysis (testability analysis and fault grading) and for logic synthesis.

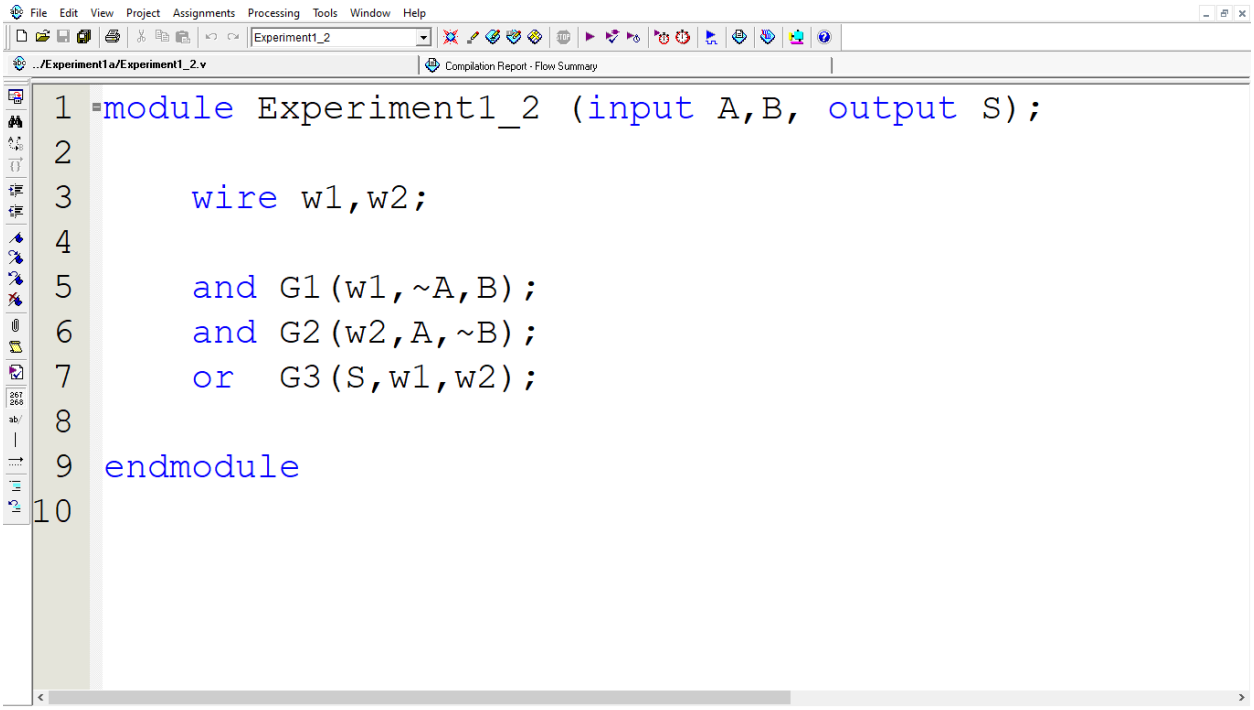

Figure 5: 2 input XOR Gate Verilog Codes

Verilog simulation:

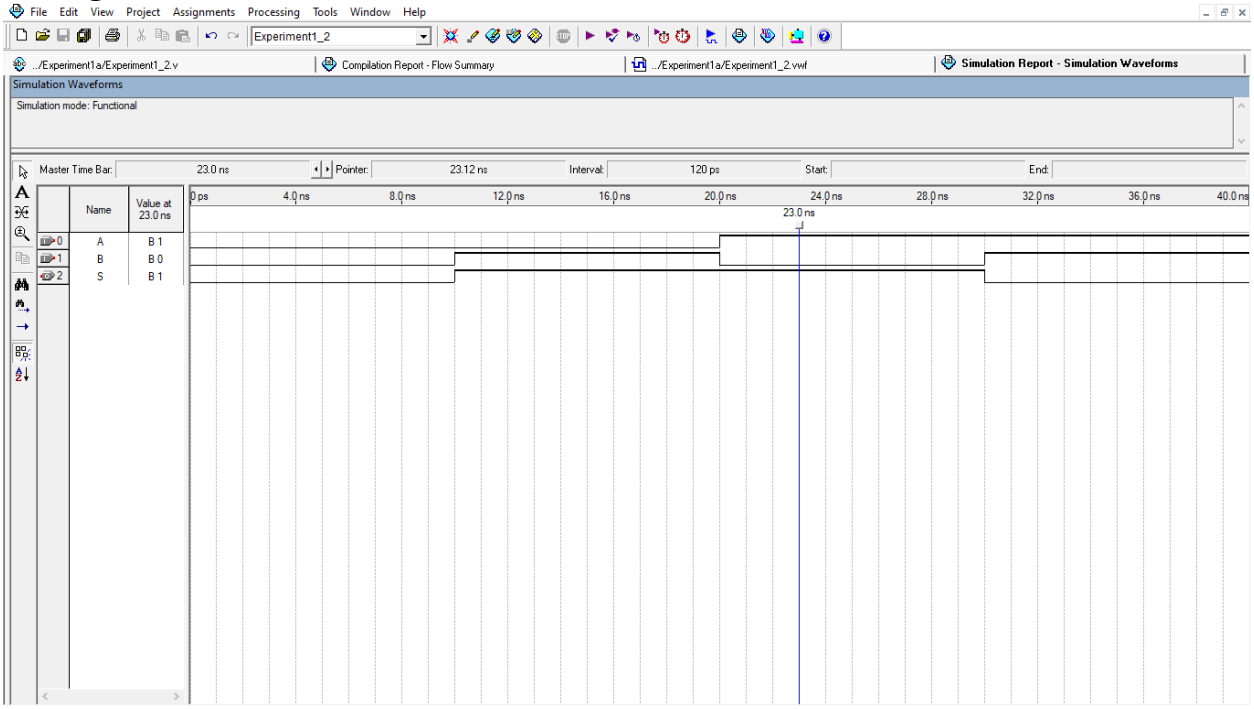

Figure 6: 2 input XOR Gate Simulated Waveform by Verilog Codes

B. 2 Input XNOR Gate

The **Exclusive-NOR Gate**, also written as: “Ex-NOR” or “XNOR”, function is achieved by combining standard gates together to form more complex gate functions.

Uses:

- The XNOR logic gates are used in error detecting circuits which are to detect
- Odd parity or even parity bits in digital data transmission circuits.
- XNOR gate is mainly used in arithmetic and encryption circuits.

Here, A & B is input & output S.

Boolean expression of 2 input exclusive nor gate:

$$Q = (A \oplus B) = A'.B' + A.B$$

Schematic Circuit:

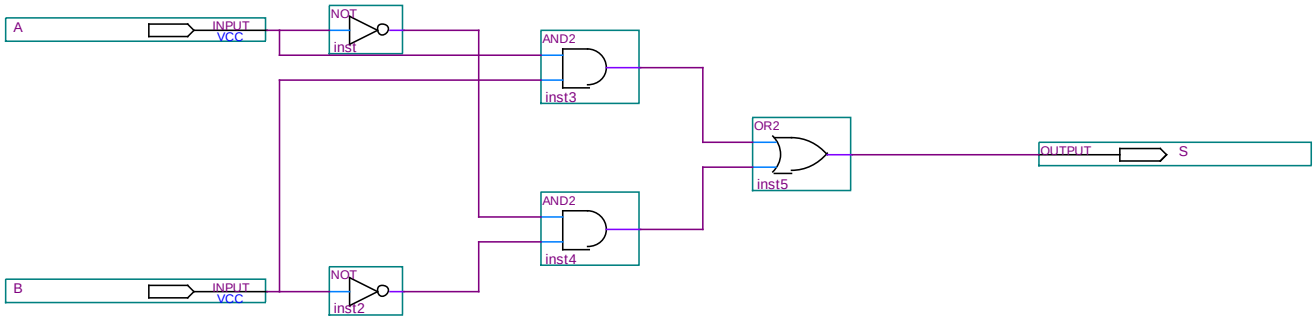

Figure 7: 2 input XNOR Gate Circuit

The truth table of 2 input XNOR gate is:

Here, A & B is input & output S.

Input		Output
A	B	S
0	0	1
0	1	0
1	0	0
1	1	1

Figure 8: Truth Table of 2 input XNOR Gate

The expression of XNOR operation can be realized by using two NOT gates, two AND gates, and one OR gate as followers,

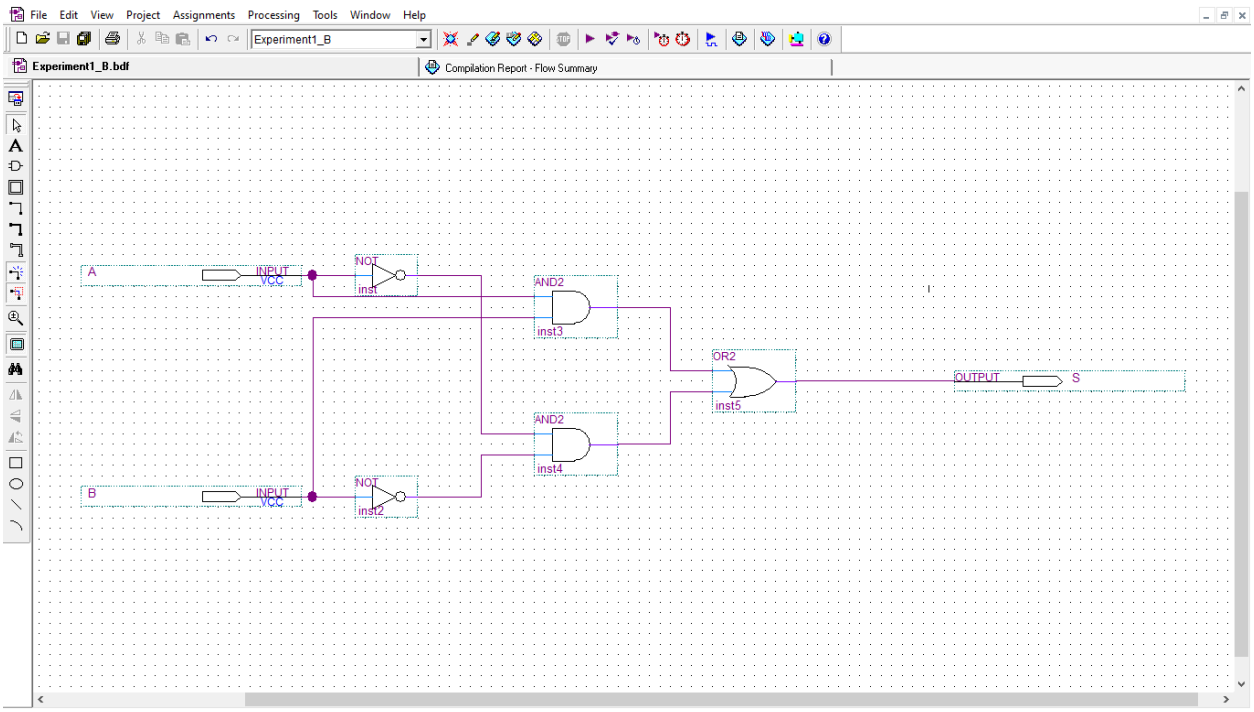

Figure 9: 2 input XNOR Gate Circuit Screenshot

We see, in exclusive or gates output is “high” or 1 if the input logic levels are the same.

Simulation: In this simulation, we have taken end time 40 nano second. So, time period of A & B is 40 & 20 nano seconds in sequent. As there are 2 inputs.

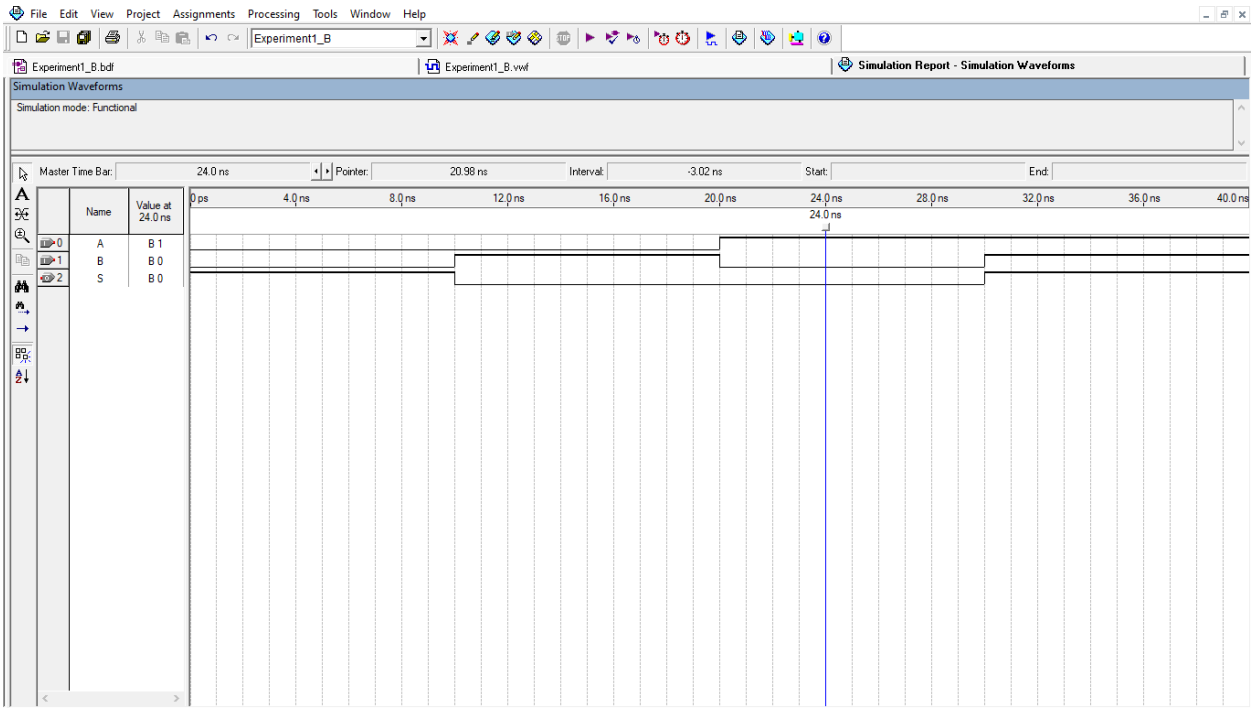

Figure 10: 2 input XOR Gate Simulation by Circuit

Verilog Code:

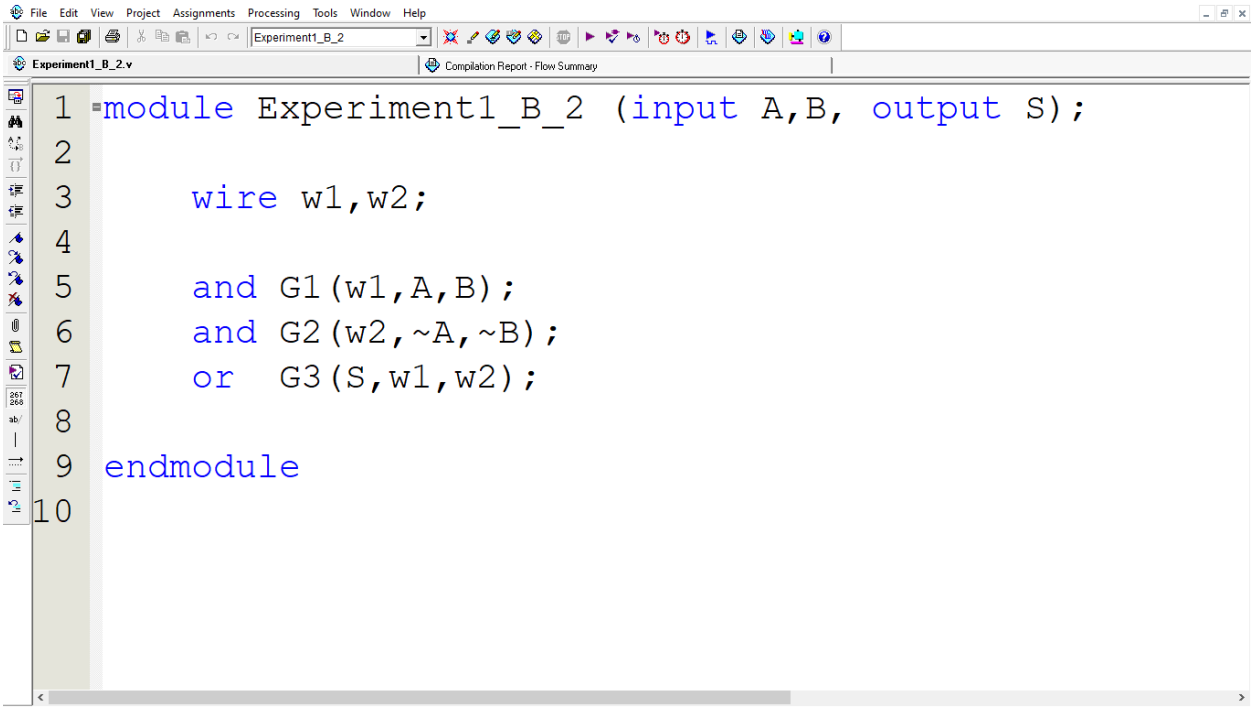

Figure 11: 2 input XNOR Gate Verilog Codes

Verilog Simulation:

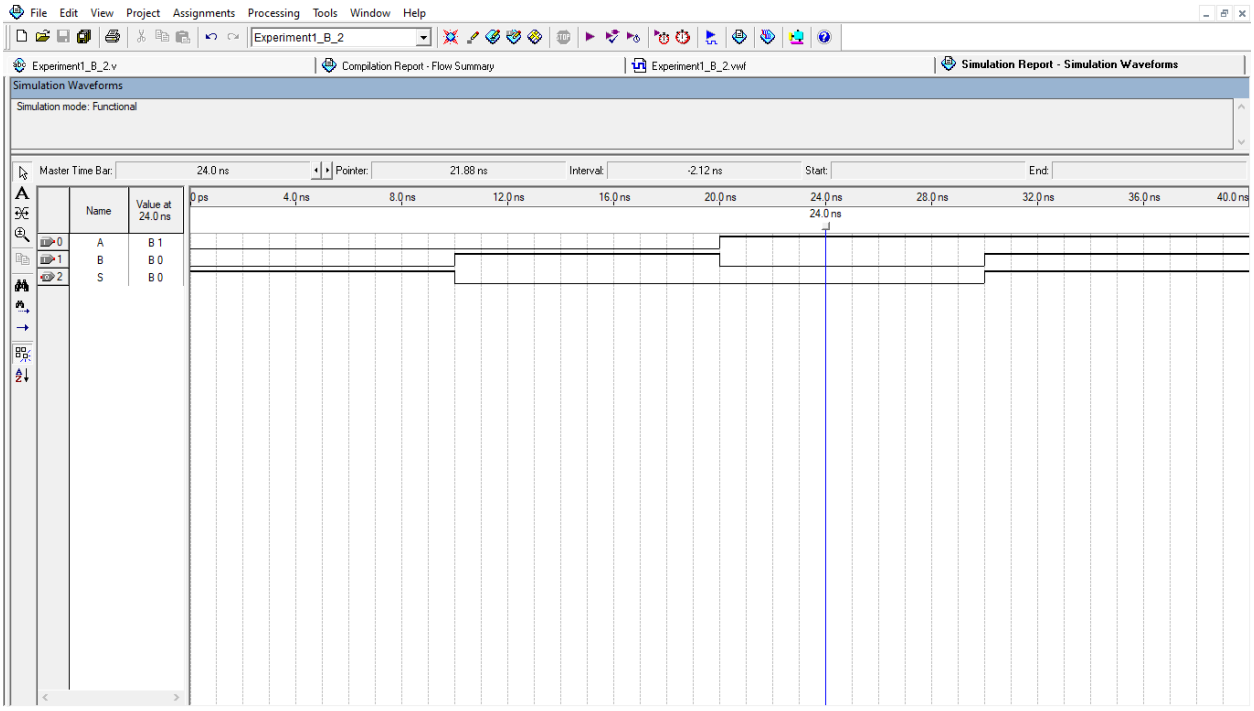

Figure 12: 2 input XNOR Gate Waveform simulation by Verilog Codes

C. 3 Input XOR Gate

Here, A, B, C is input & output S.

Boolean expression: **S = A′B′C + A′BC′ + AB′C′ + ABC**

Schematic Circuit:

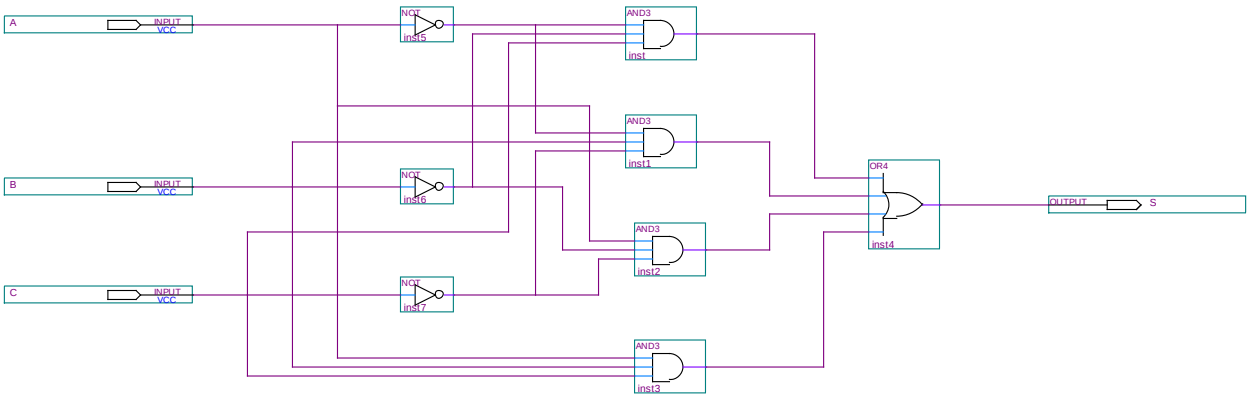

Figure 13: 3 input XOR Gate Circuit

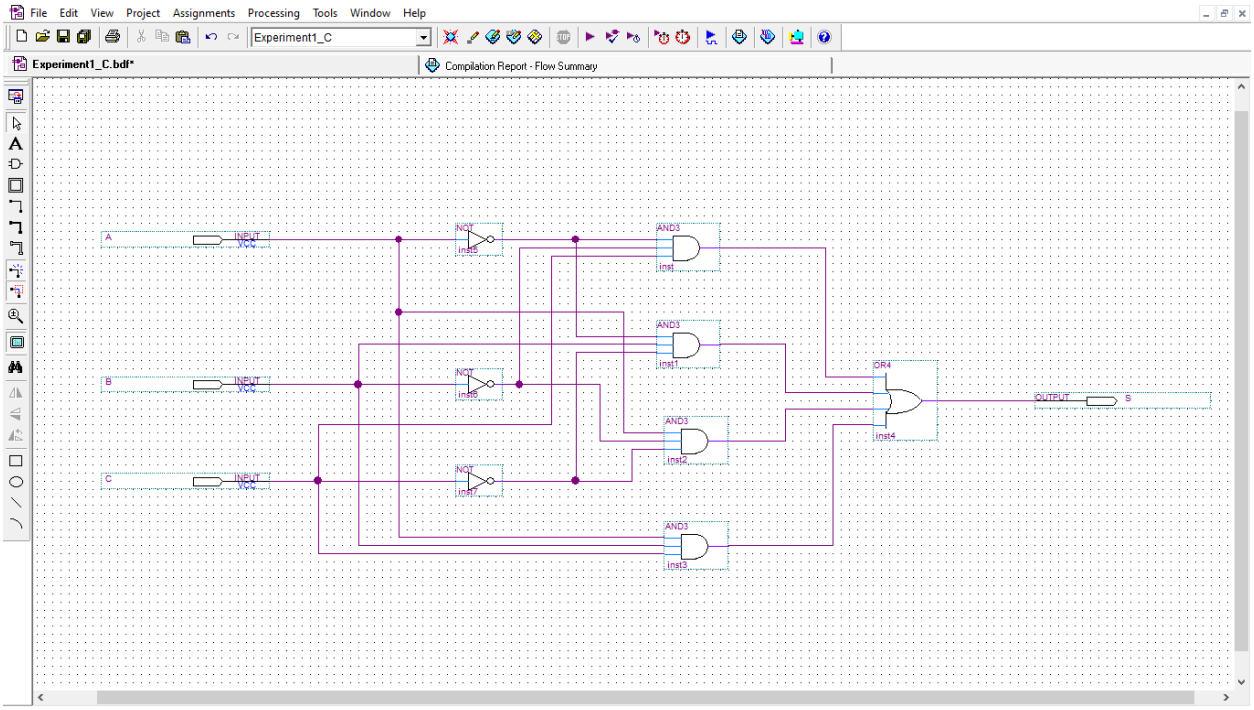

Figure 14: 3 input XOR Gate Circuit Screenshot

The truth table of 3 input XOR gate is:

Here, A, B, C is input & output S.

Input			Output
A	B	C	S
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Figure 15: Truth table of 3 input XOR Gate

Simulation:

In this simulation, we have taken end time 80 nano seconds. So, time period of A, B & C is 80, 40 & 20 nano seconds in sequent. As there are 3 inputs.

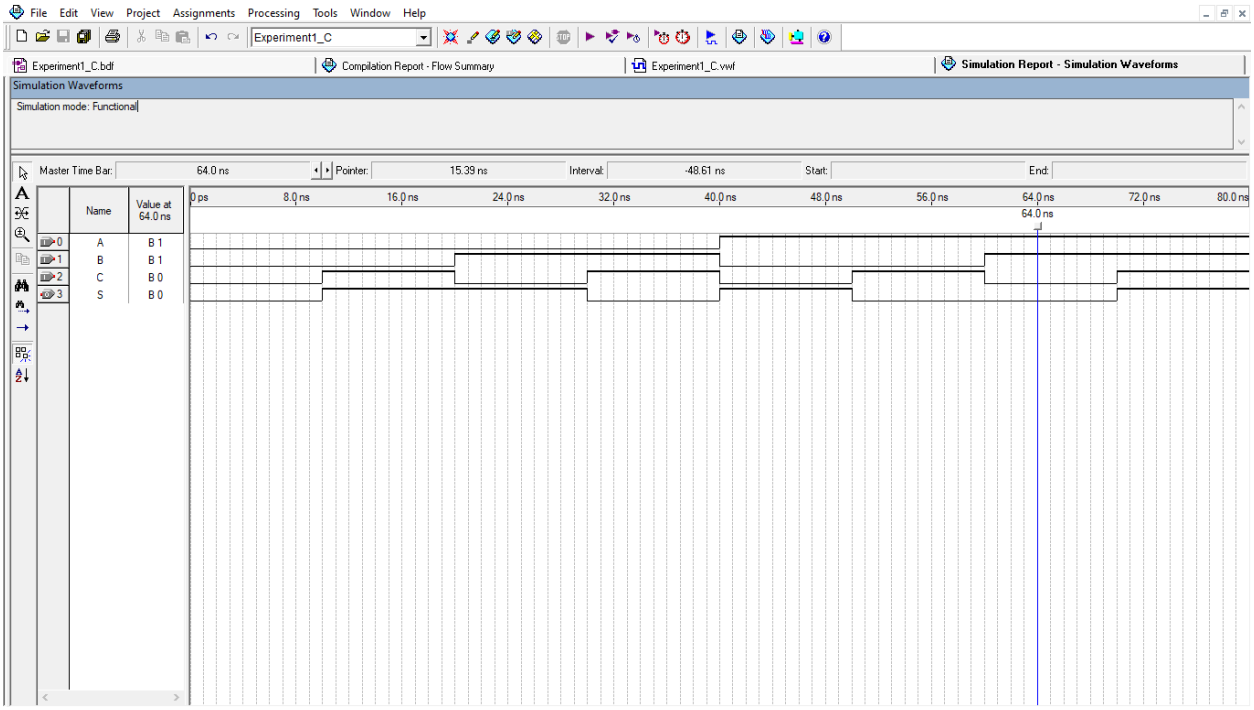

Figure 16: 3 input XOR Gate Waveform Simulation by Circuit

Verilog Code:

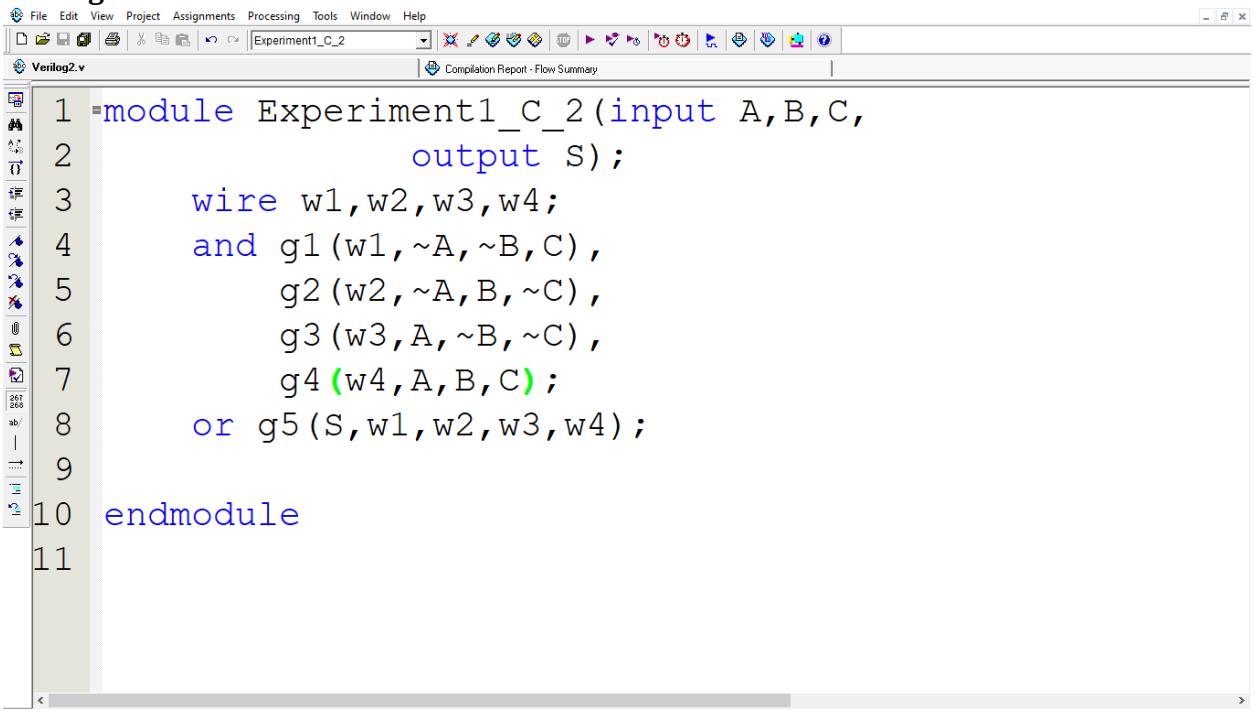

Figure 17: 3 input XOR Gate Verilog Codes

Verilog simulation:

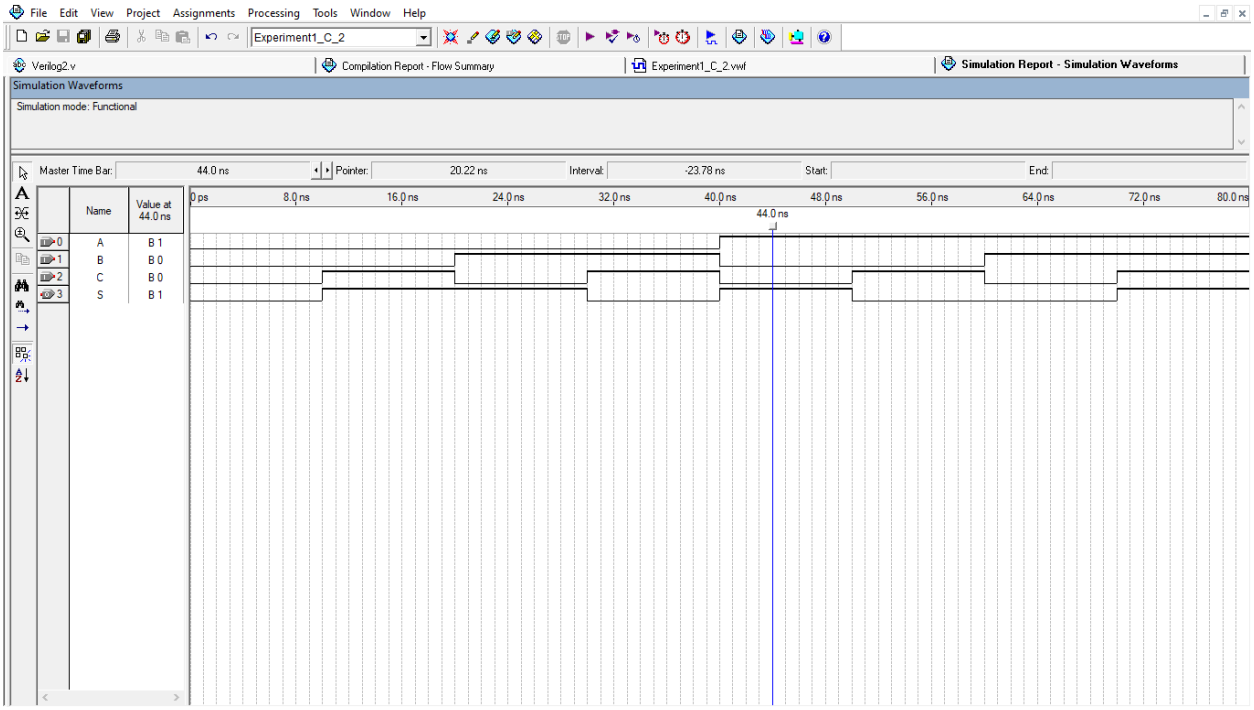

Figure 18: 3 input XOR Gate Circuit Waveform Simulation by Verilog Codes

3 Input XNOR Gate:

Here, A, B & Cis input & output S.

Boolean expression of: S = AB′C + ABC′ + A′BC + A′B′C′

Schematic Circuit:

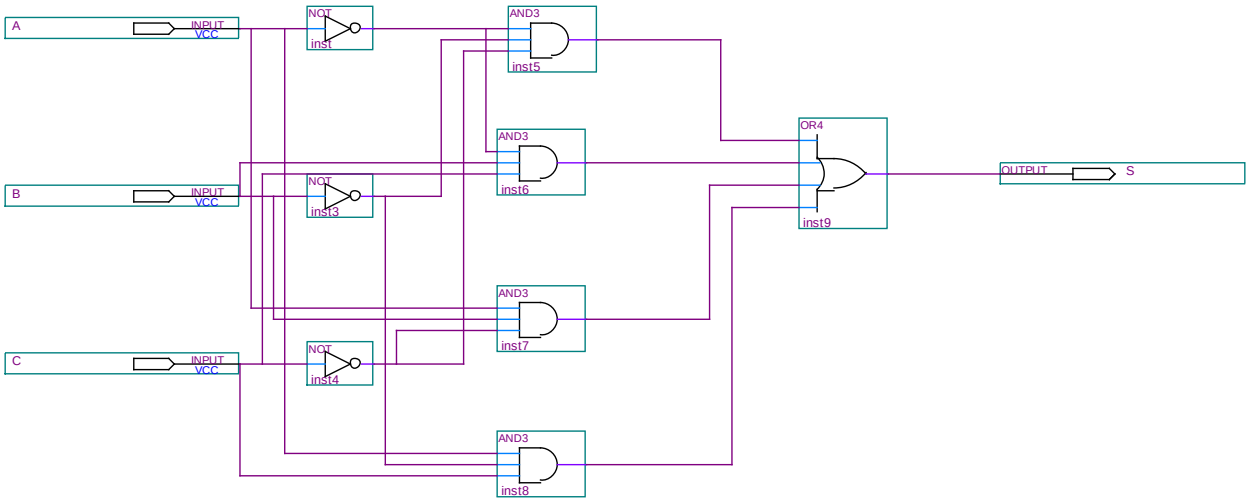

Figure 19: 3 input XNOR Gate Circuit

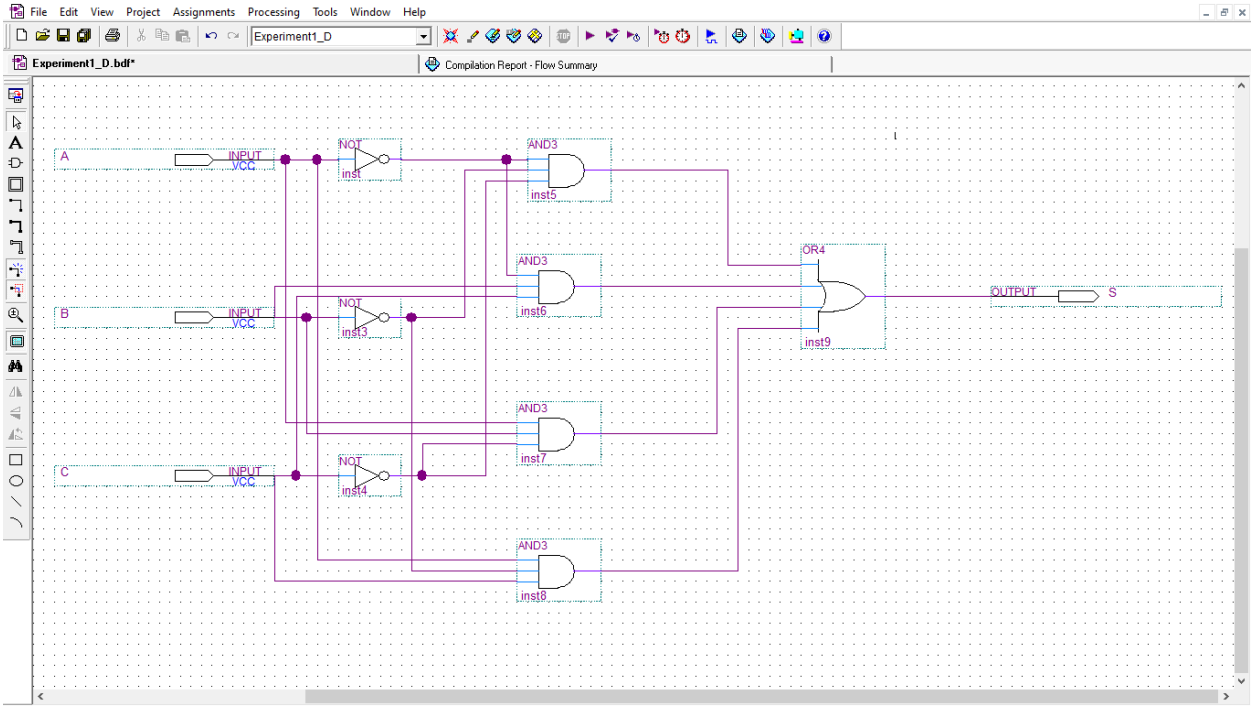

Figure 10: 3 input XNOR Gate Circuit Screenshot

The truth table of 3 input XNOR gate is:

Here, A, B, C is input & output S.

Input			Output
A	B	C	S
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Figure 21: Truth table of 3 input XNOR Gate

Schematic Simulation:

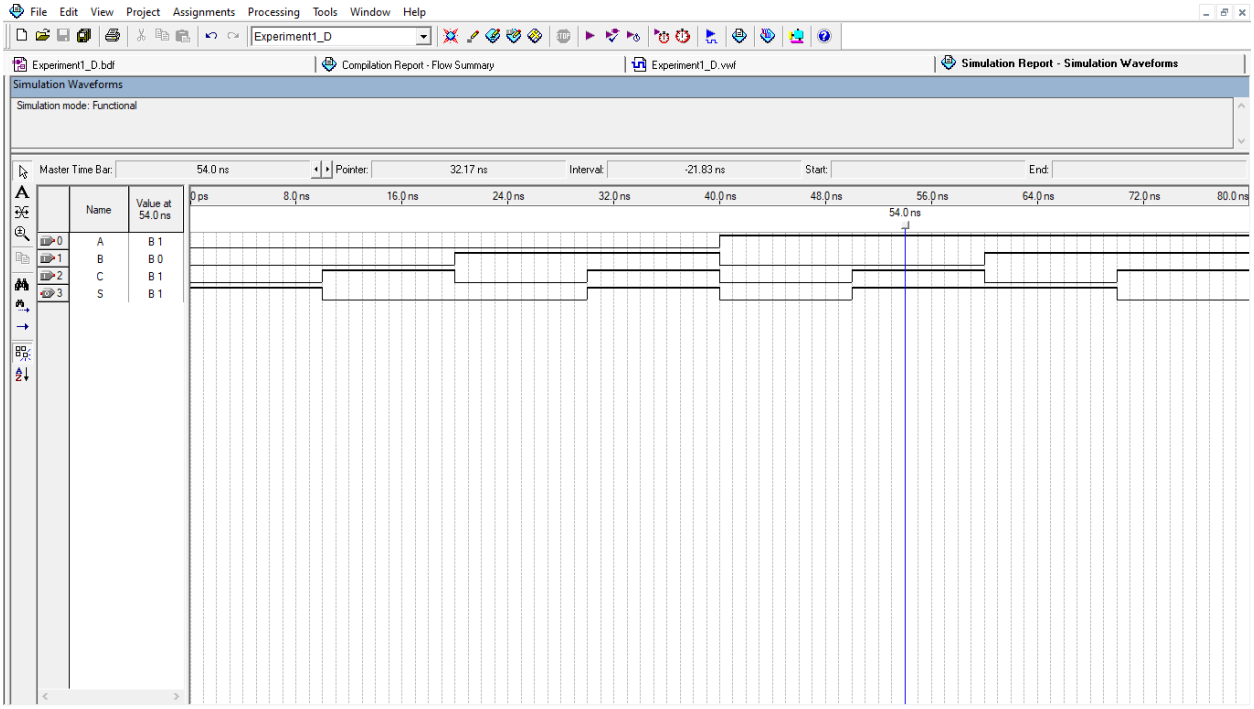

Figure 22: 3 input XNOR Gate Waveform Simulation by circuit

Verilog Code:

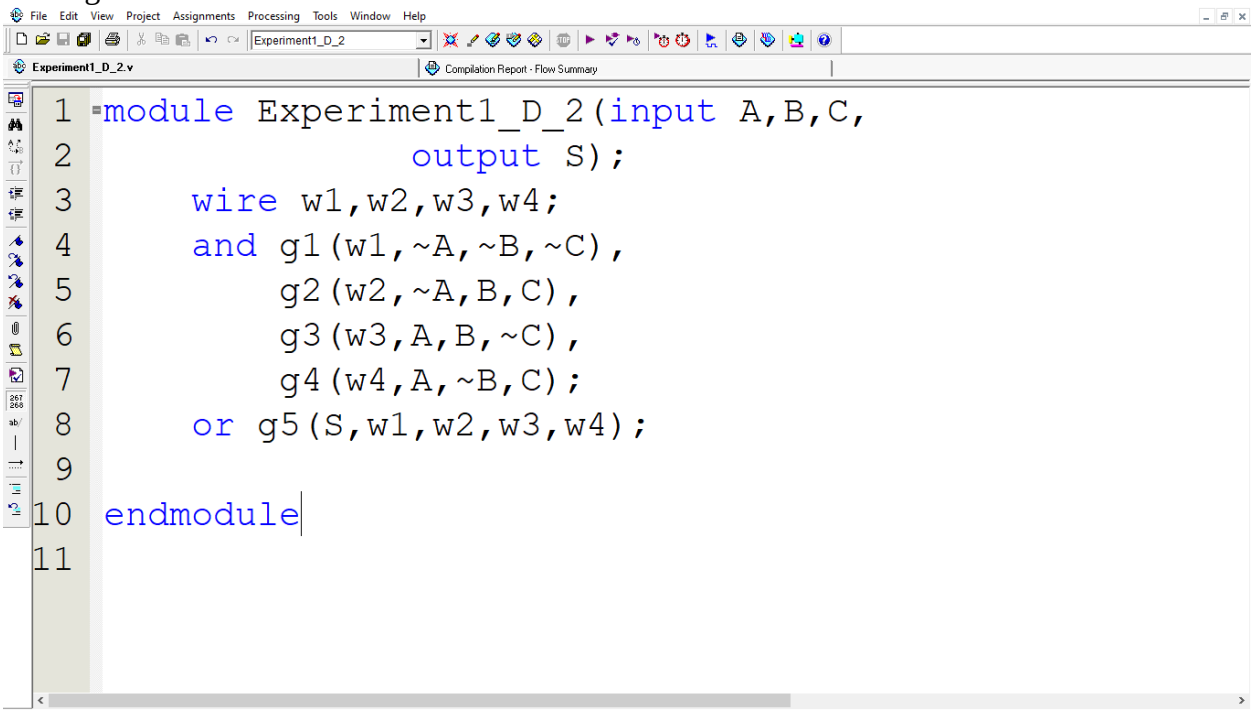

Figure 23: 3 input XNOR Gate Verilog Codes

Verilog Simulation:

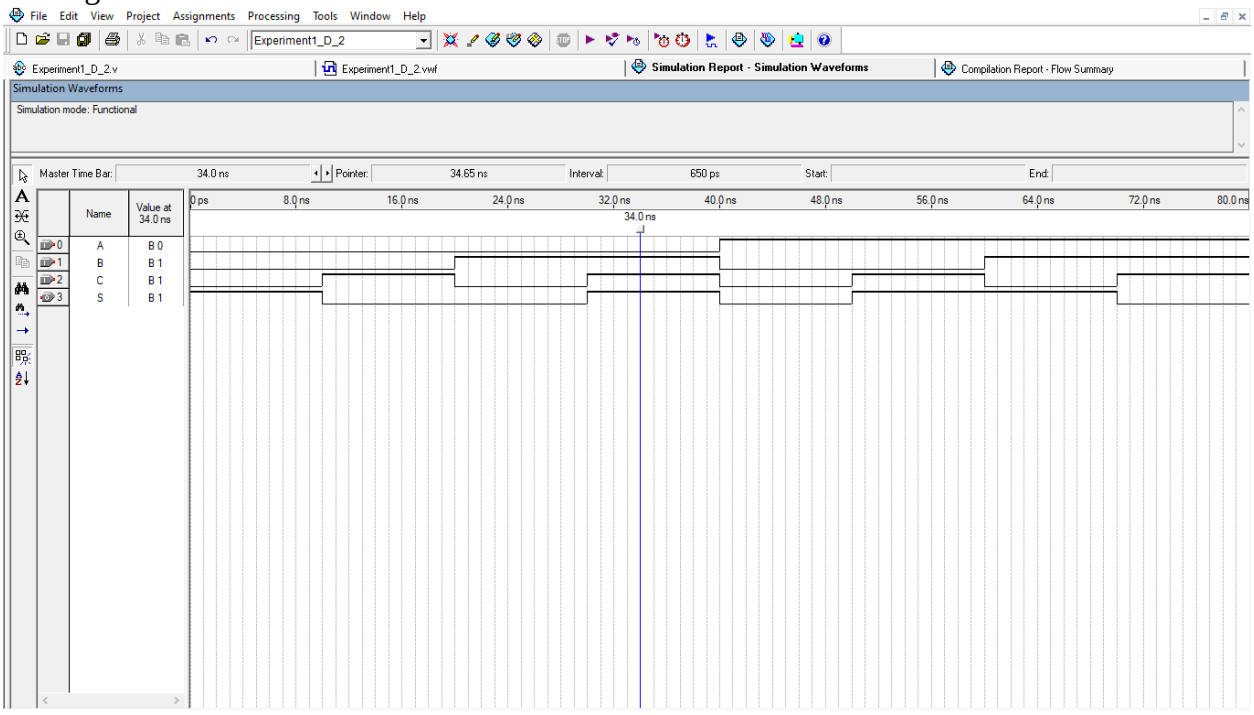

Figure 24: 3 input XNOR Gate Waveform Simulation by Verilog Codes

Conclusion: An introduction to the data sheet parameters for voltage and current ranges that characterize a logic ‘high’ or a logic ‘low’. We also learn about the connection of switches to use as logic inputs and the connection of logic outputs to LEDs. We use truth tables to verify a Boolean identity such as the distributive property. We build the circuit and test the output for all possible input combinations. For this lab, we are introduced to Verilog coding and verified with logic gates.

Reference:

- Digital Logic Design; Md Mozammel Huq Azad Khan.
- Exclusive-NOR Gate with Ex-NOR Gate Truth Table. 2020, English, W. Storr. Basic Electronics Tutorials.