Post Lab Report-01

Date: 12 March 2021	Course: CSE345
Experiment 1	Id: 2019-1-60-024
Name: Adri Saha	Course instructor: Touhid Ahmed

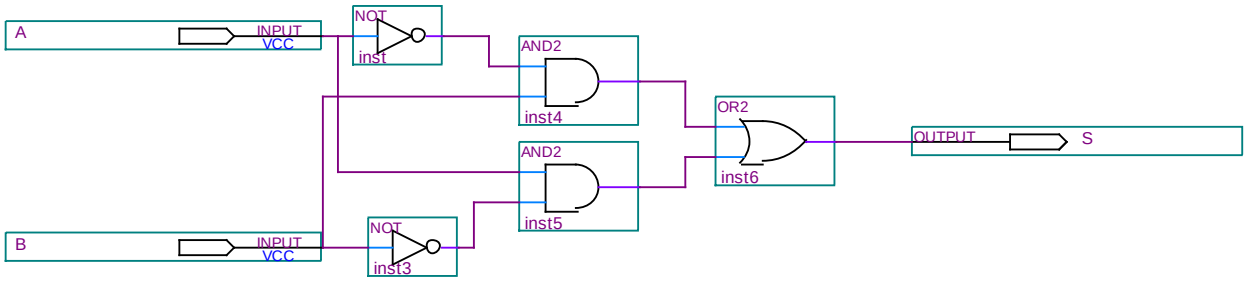
A. 2 Input XOR Gate

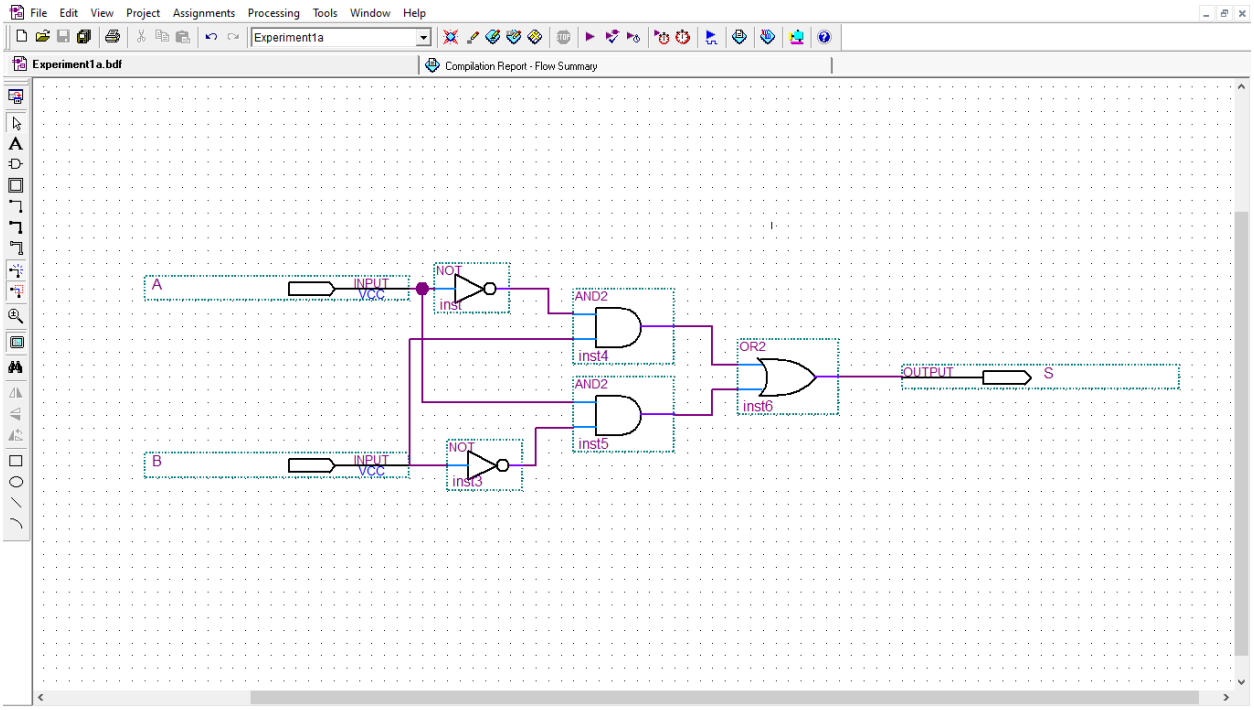
Here, A & B is input & output S

Boolean expression is:

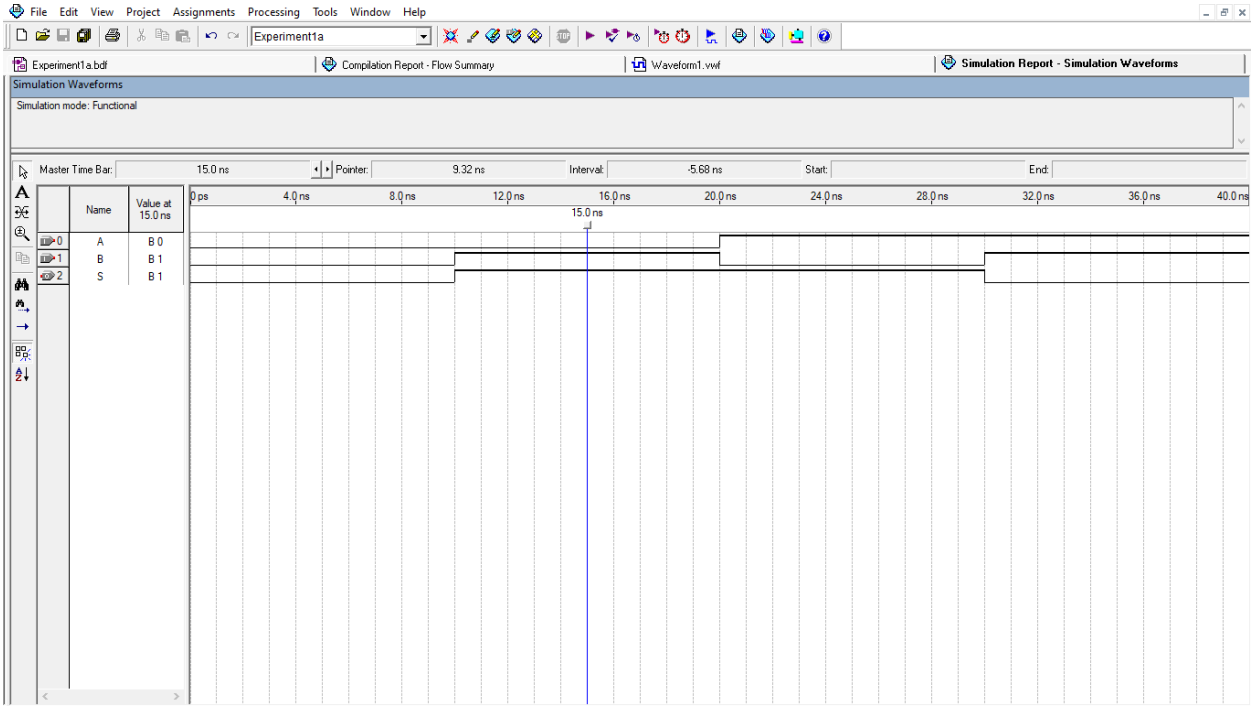
$S = (A \oplus B) = A.B' + A'.B$

Schematic Circuit:

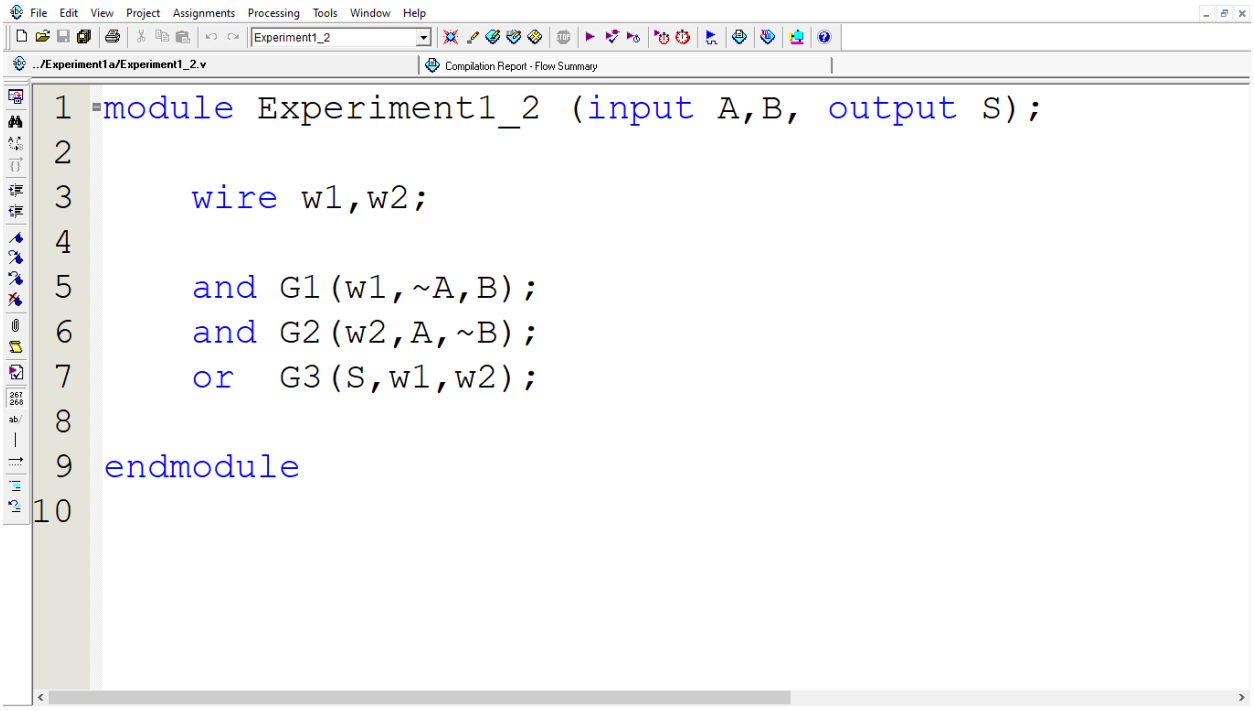




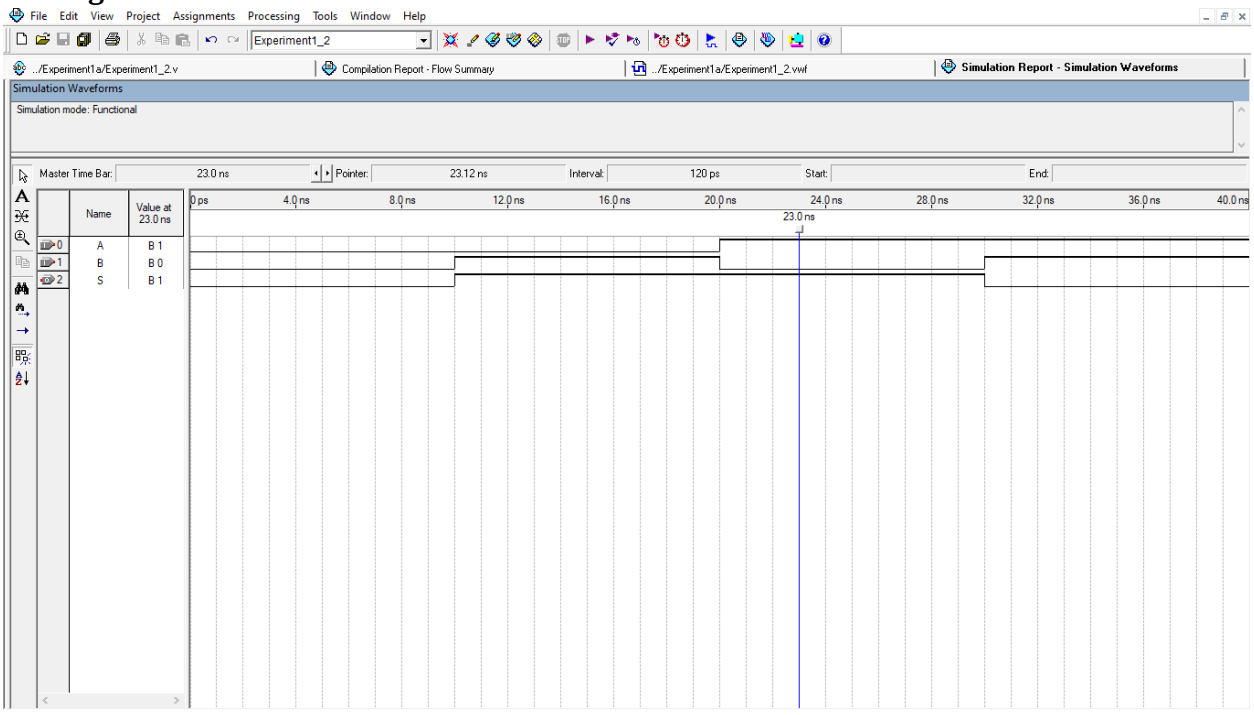
Schematic Simulation:



Verilog Codes:



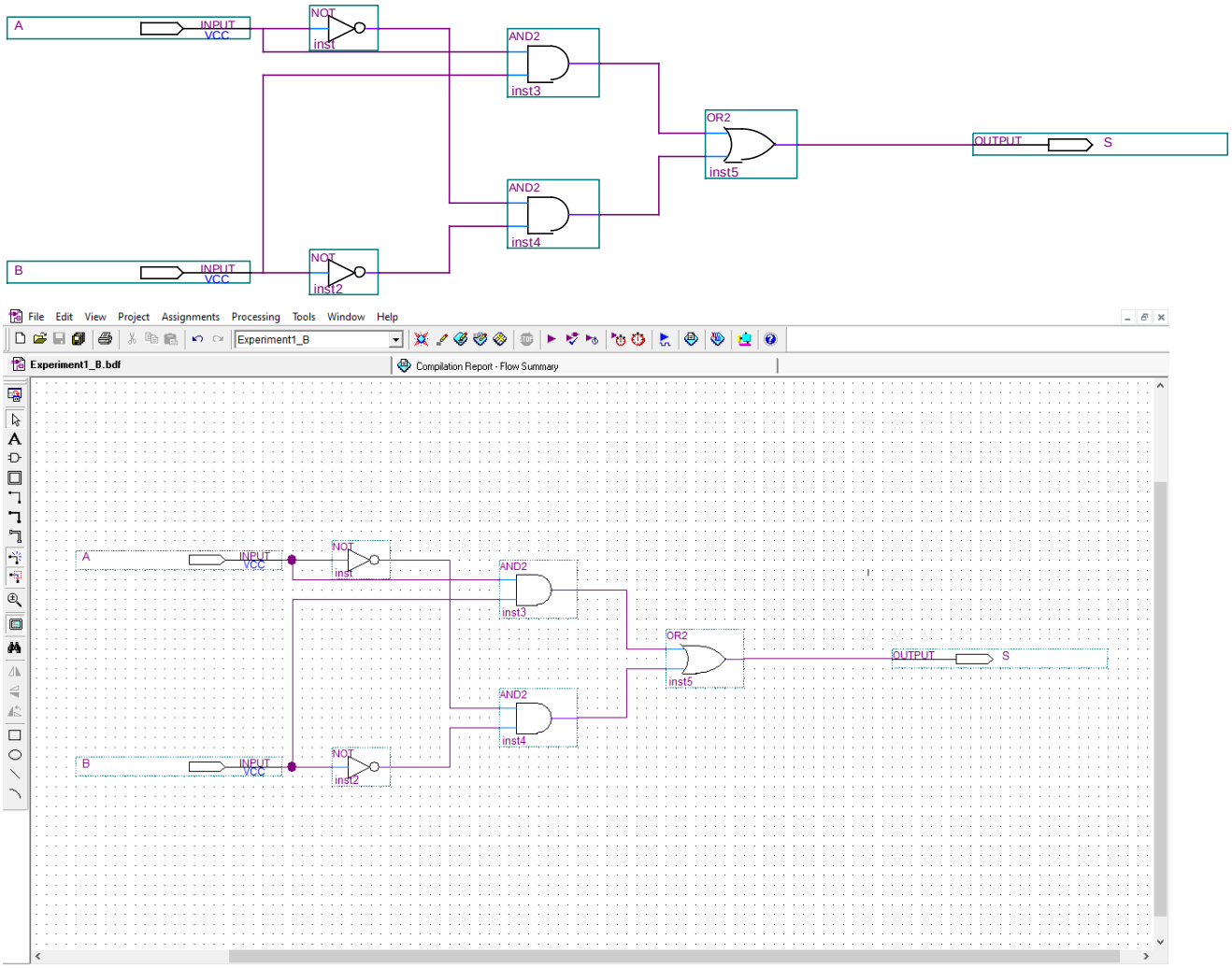
Verilog simulation:



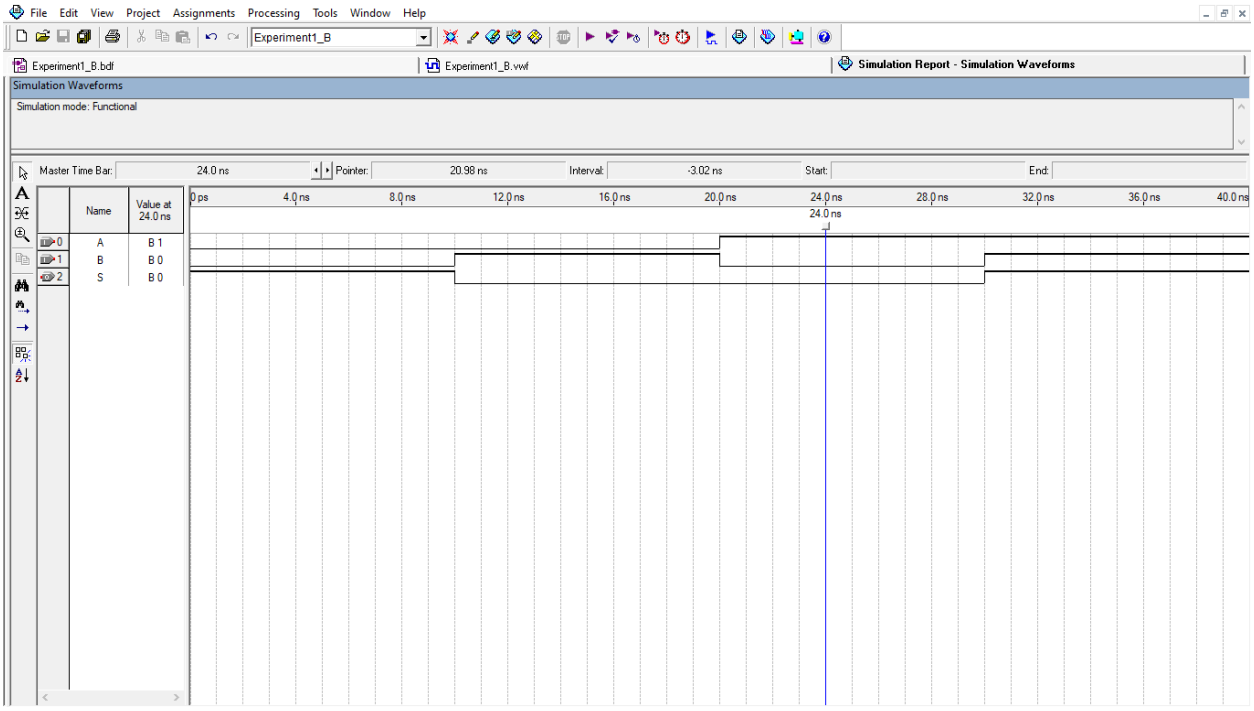
B. 2 Input XNOR Gate

Boolean expression of 2 input exclusive nor gate: Q = (A ⊕ B) **= A′.B′ + A.B**

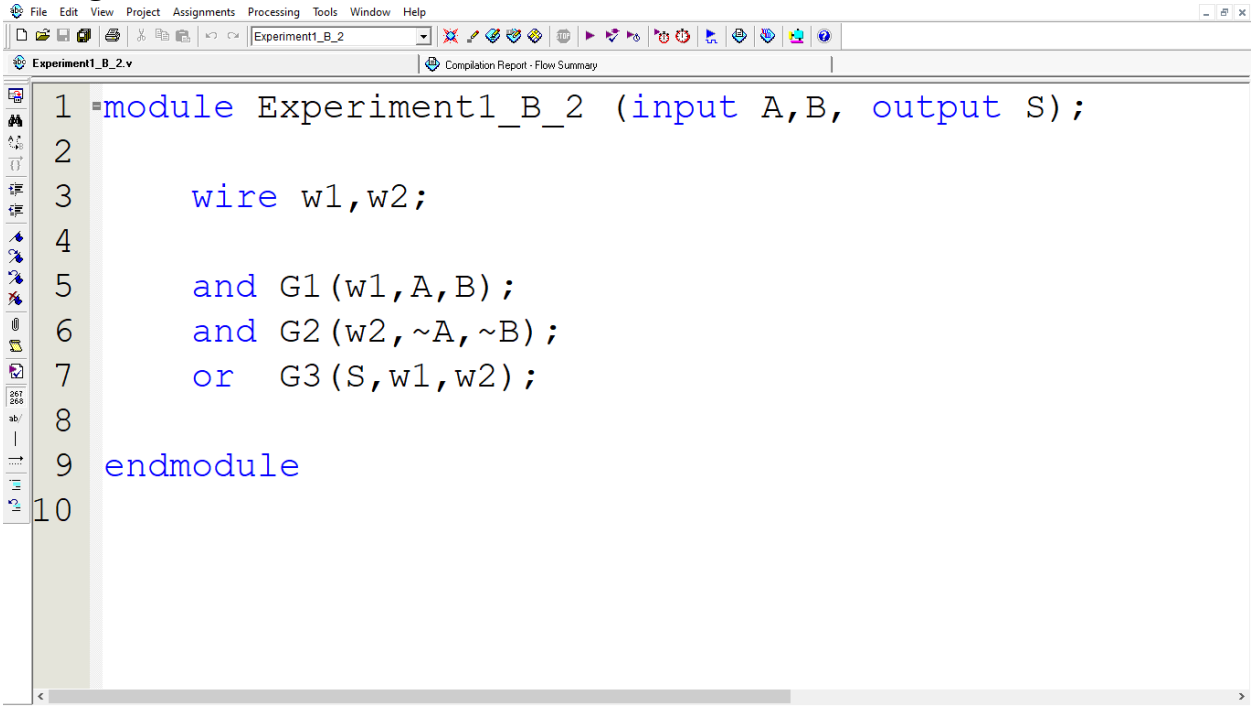
Schematic Circuit:



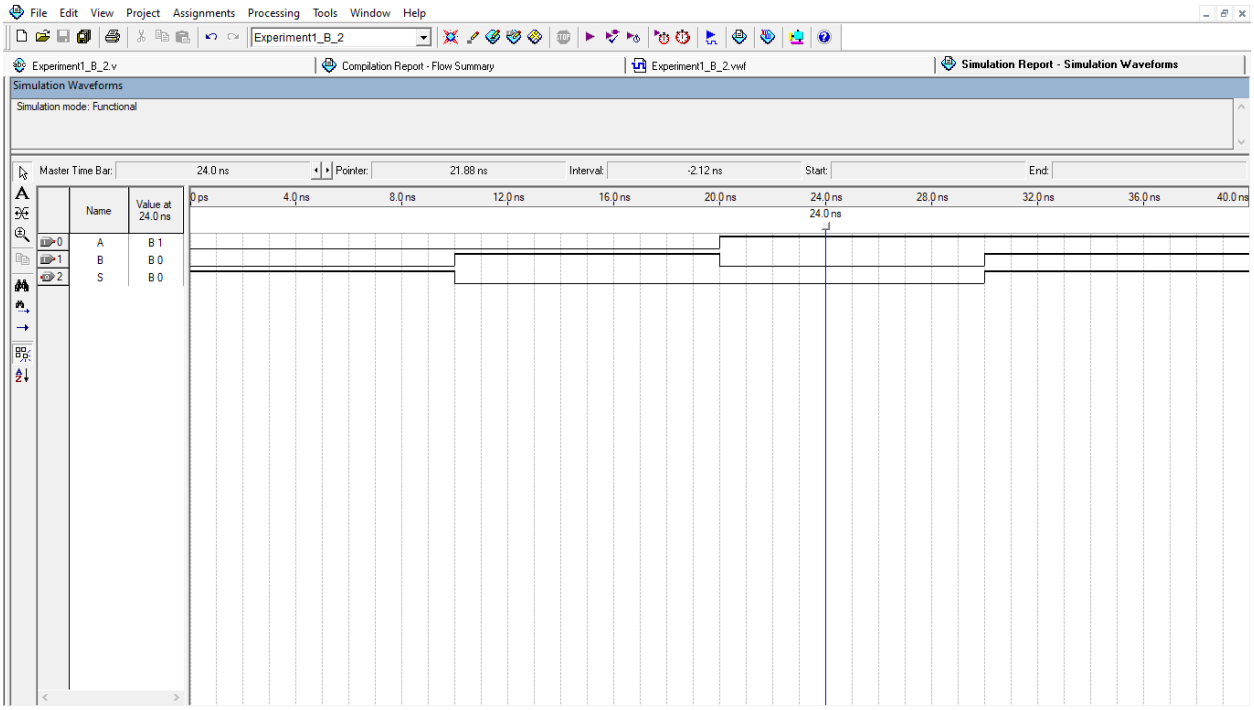
Simulation:



Verilog Code:



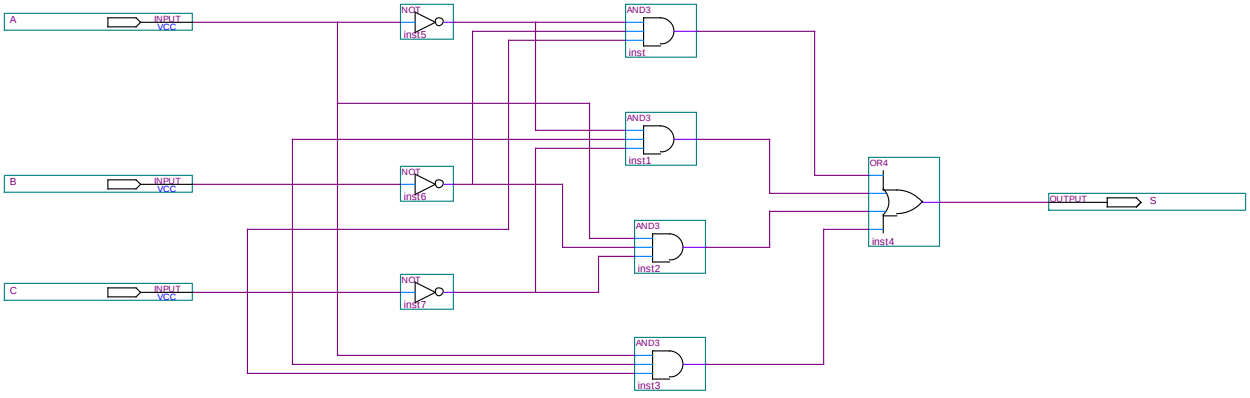
Verilog Simulation:

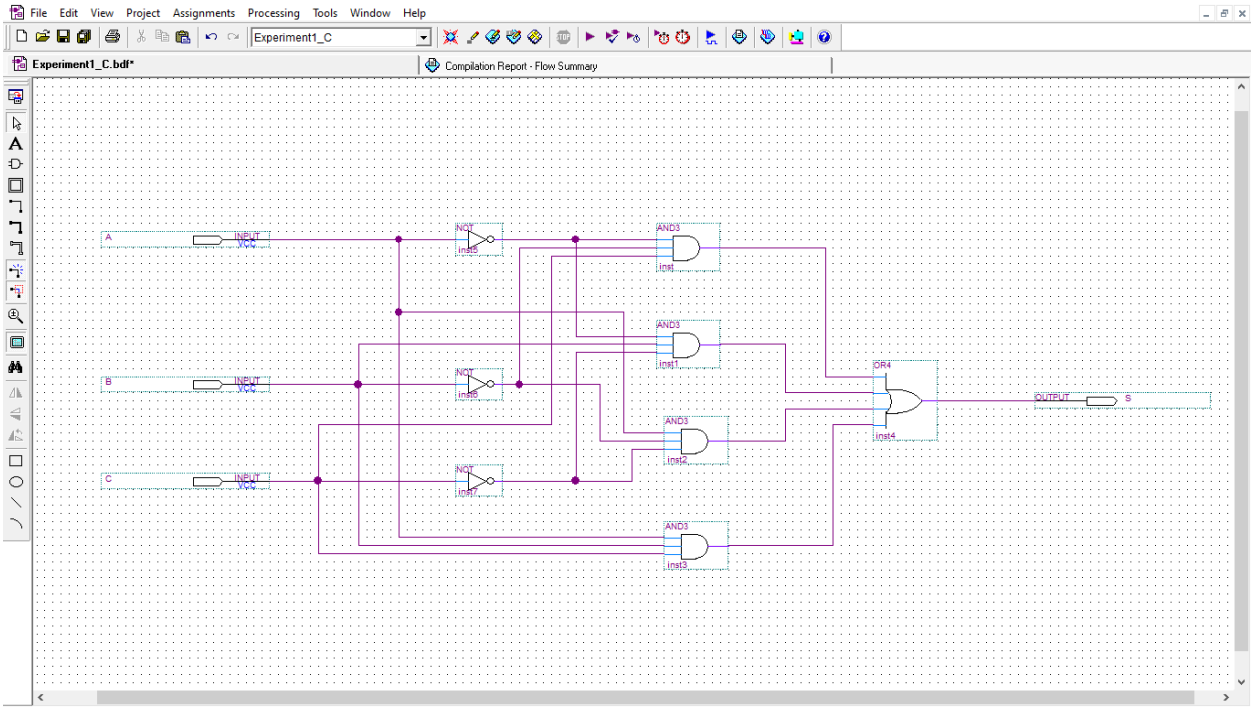


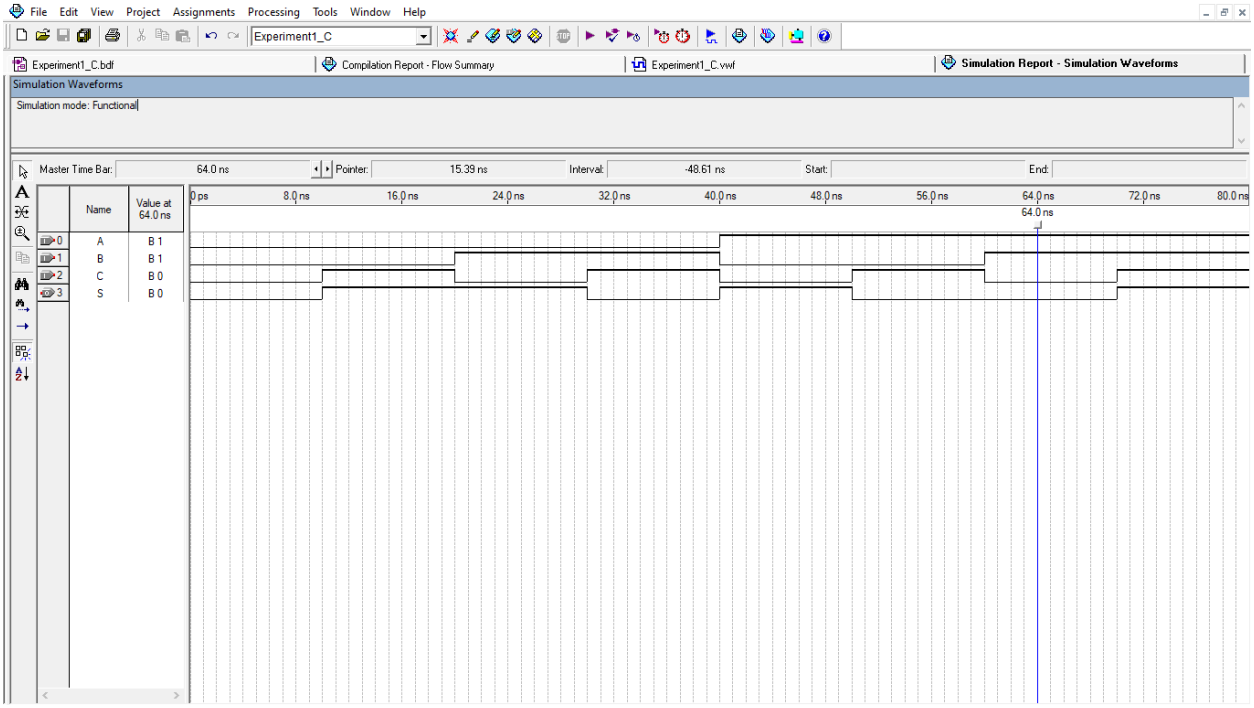
C. 3 Input XOR Gate

Boolean expression: **S = A′B′C + A′BC′ + AB′C′ + ABC**

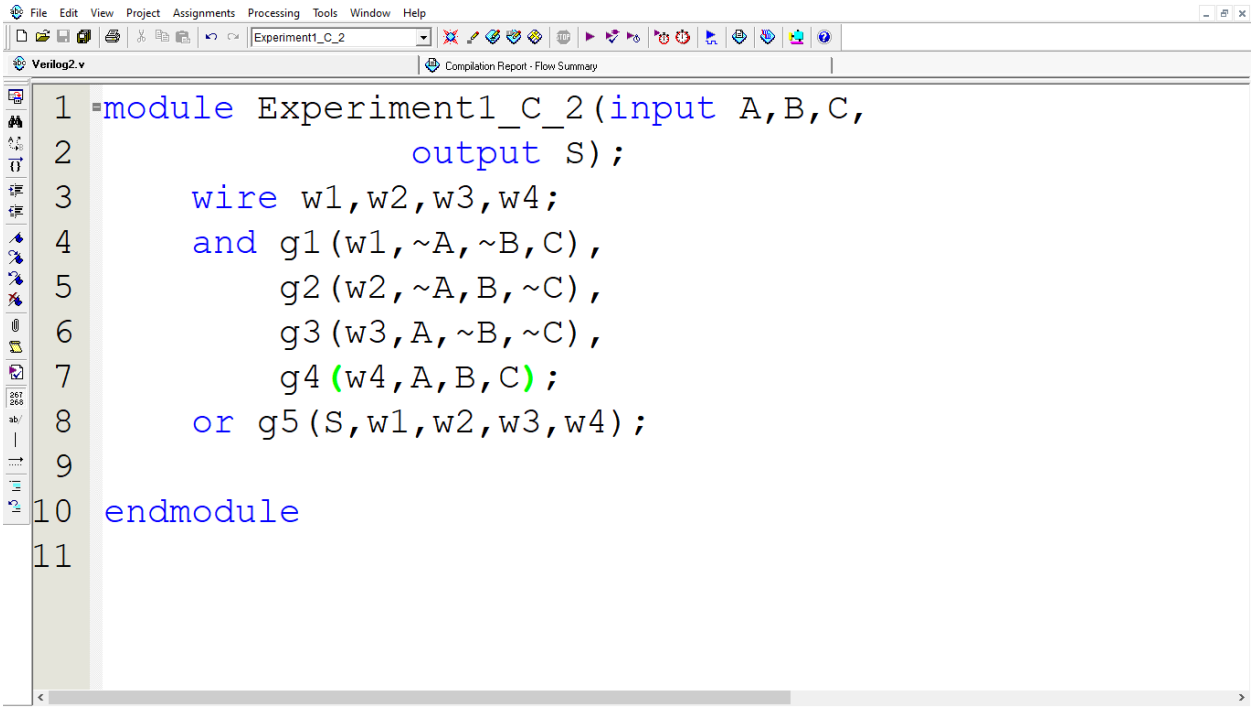
Schematic Circuit:



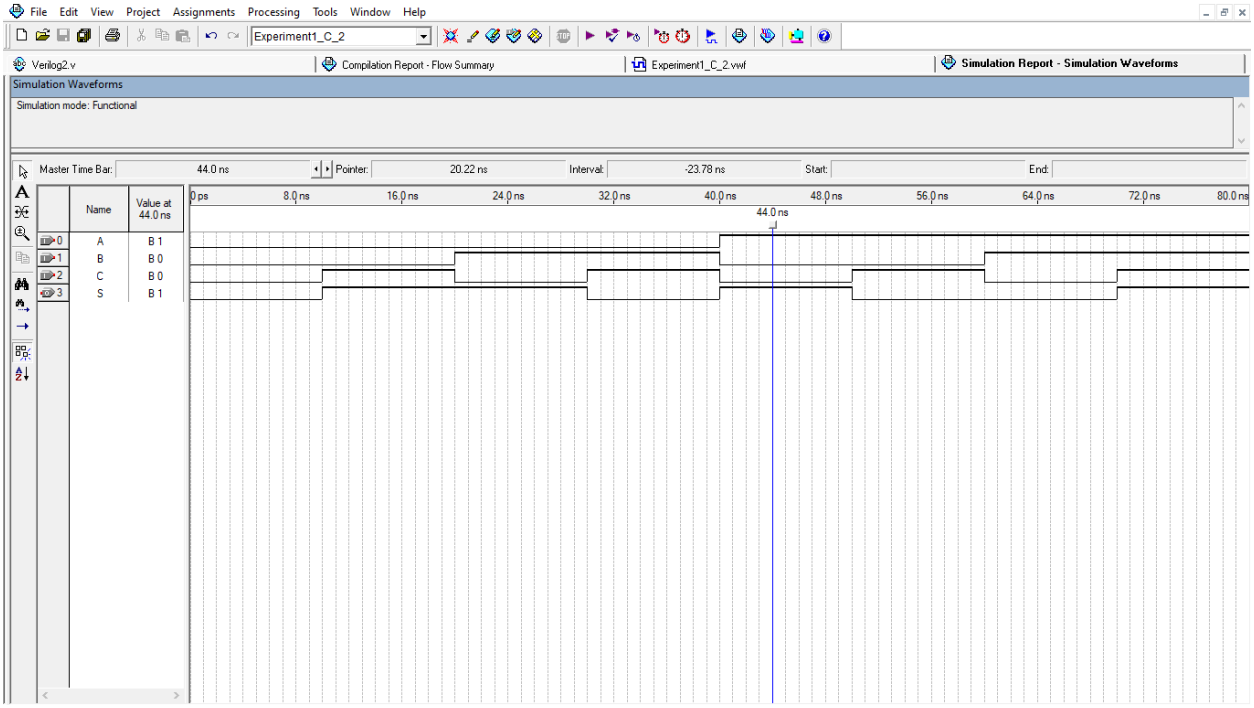




Verilog Code:



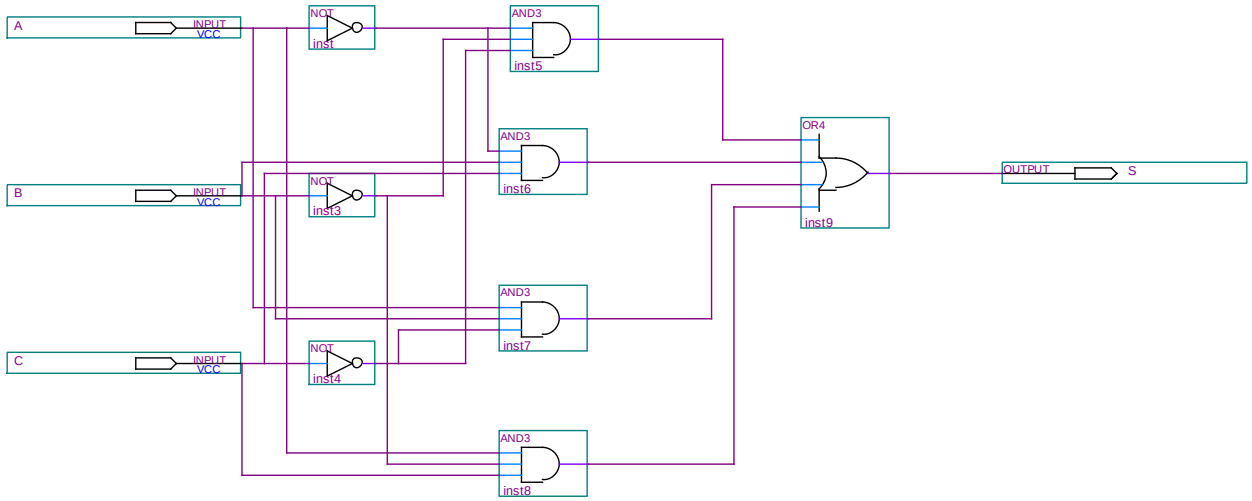
Verilog simulation:

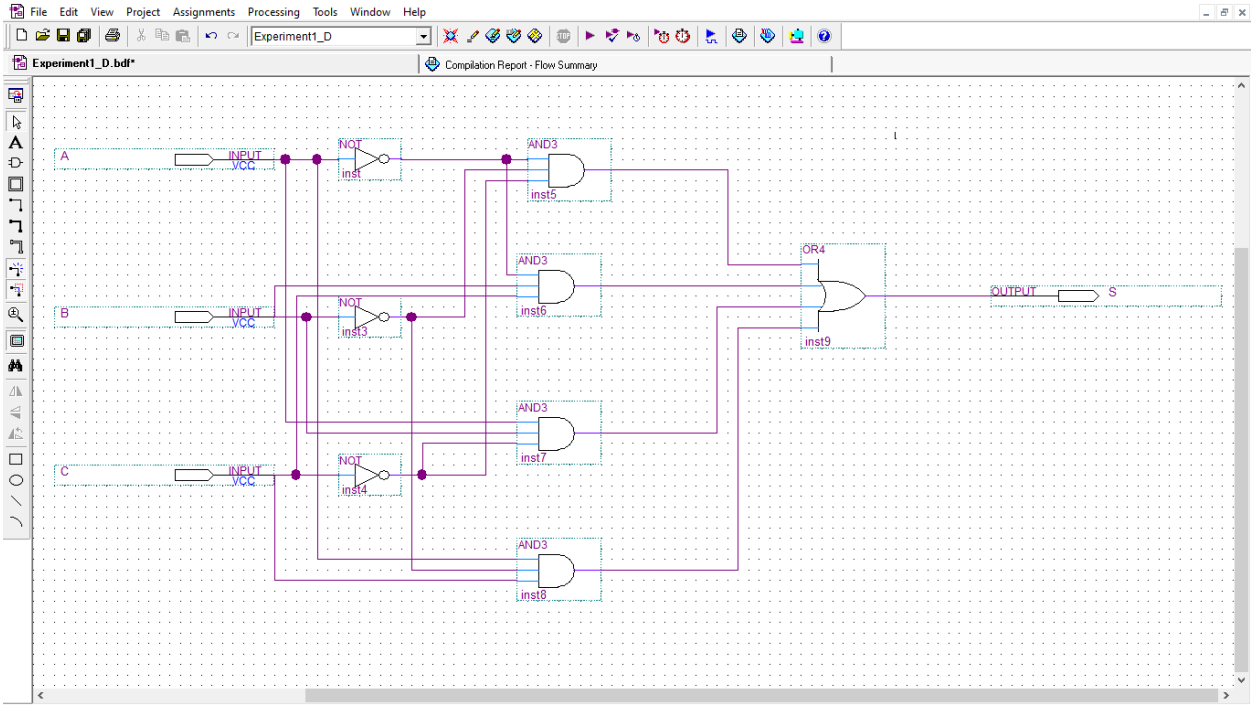


D. 3 Input XNOR Gate:

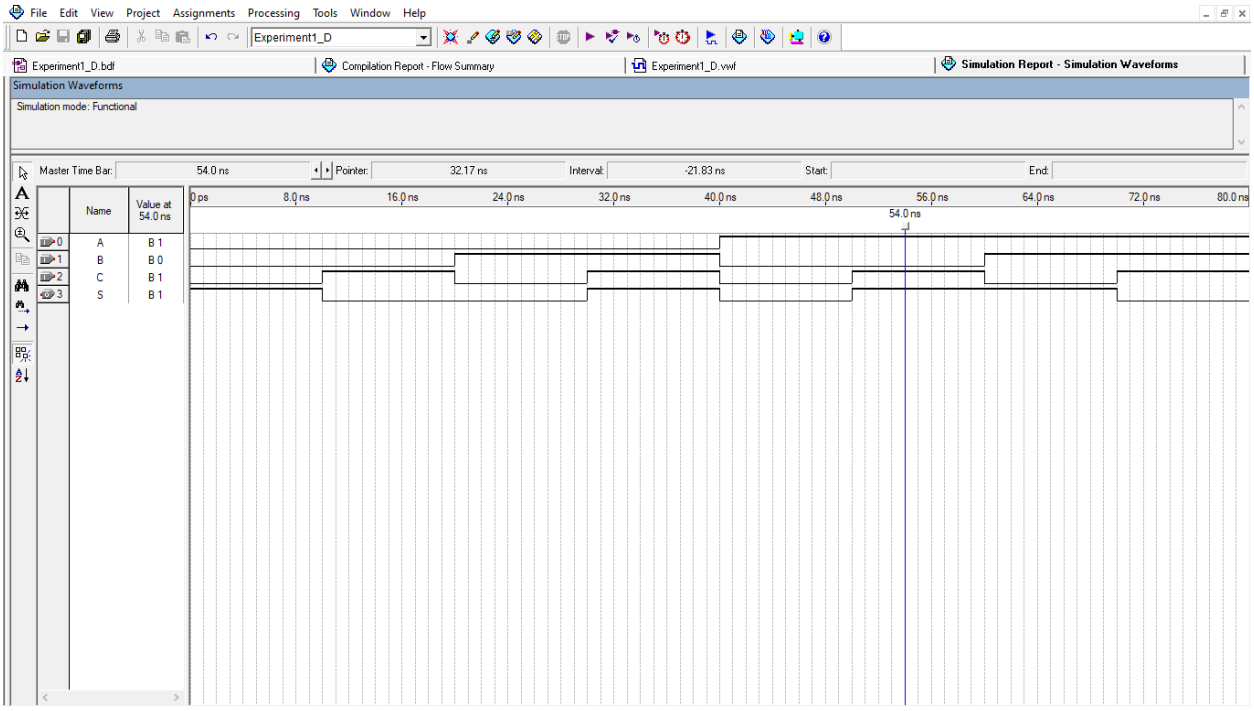
Boolean expression of: $S = AB'C + ABC' + A'BC + A'B'C'$

Schematic Circuit:

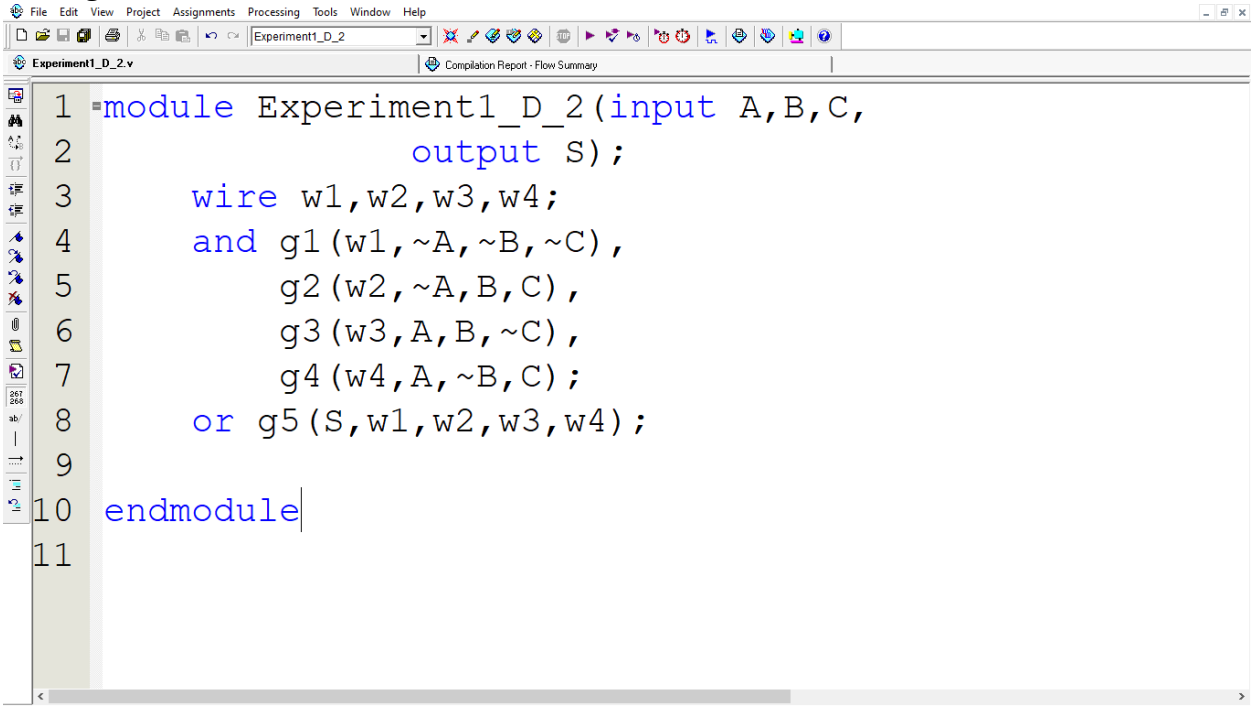




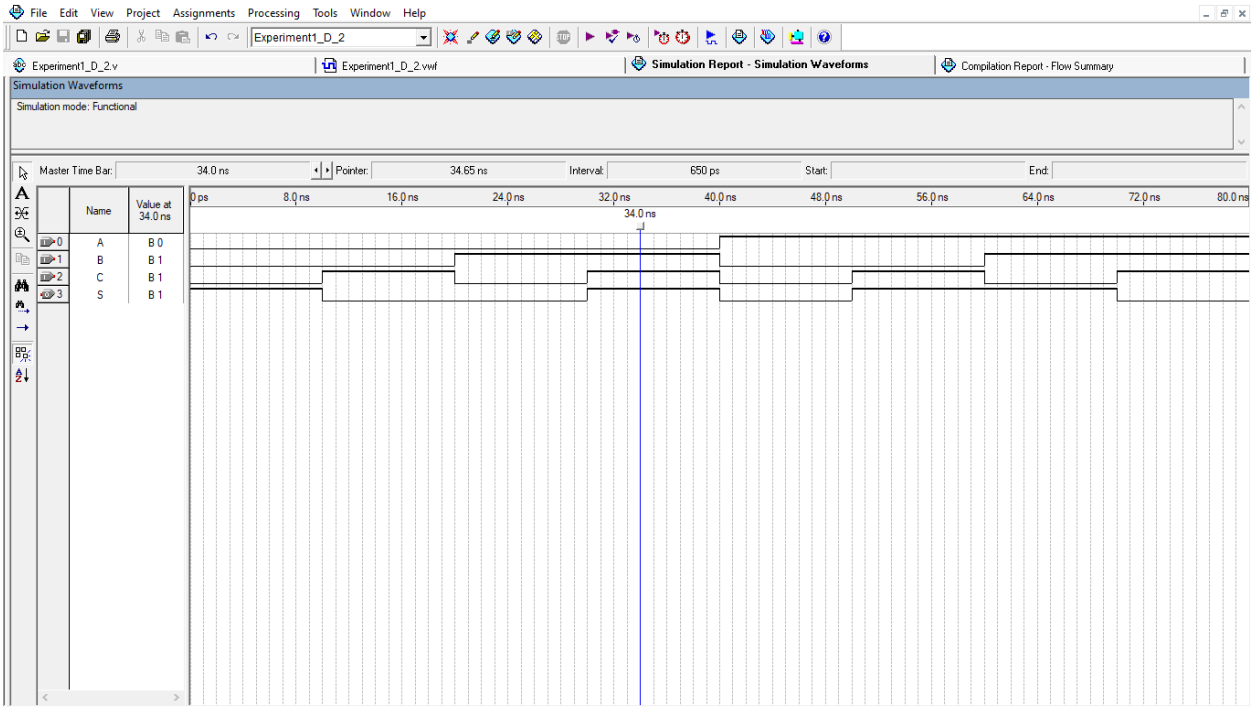
Schematic Simulation:



Verilog Code:



Verilog Simulation:


File Edit View Project Assignments Processing Tools Window Help
Experiment1_D_2
Experiment1_D_2.v
Experiment1_D_2.vwf
Simulation Report - Simulation Waveforms
Compilation Report - Flow Summary
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 34.0 ns
Pointer: 34.65 ns
Interval: 650 ps
Start:
End:
Name
Value at 34.0 ns
0 A B 0
1 B B 1
2 C B 1
3 S B 1
0 ps
8.0 ns
16.0 ns
24.0 ns
32.0 ns
40.0 ns
48.0 ns
56.0 ns
64.0 ns
72.0 ns
80.0 ns
34.0 ns