Journal of Instrumentation

An open-sorce IP-Core for Multi-Voltage Thresholding signal acquisition with FPGAs

Published by IOP Publishing for Sissa Medialab

Received: *November 3, 2023*
Accepted: *January 8, 2024*
Published: *February 23, 2024*

Topical Workshop on Electronics for Particle Physics
Geremeas, Sardinia, Italy
1–6 October 2023

An open-sorce IP-Core for Multi-Voltage Thresholding signal acquisition with FPGAs

D. Eliseev,* E. Ehlert, T. Hebbeker, M. Merschmeyer and C. Presser

III. Physics Institute A, RWTH Aachen University, Aachen, Germany

E-mail: eliseev@physik.rwth-aachen.de

Abstract: High-speed multichannel ADCs are costly and require complex FPGA or MCU firmware to communicate with them. The Multi-Voltage Thresholding (MVT) approach can replace to some extent an external ADC by harnessing the internal FPGA resources, thus reducing costs and complexity. The MVT approach needs only a few low-cost external components. The focus of the contribution is presenting an open-source IP-Core that implements the MVT approach and simplifies its implementation on a standard FPGA. The contribution also provides an overview of characterization measurements and specific calibration method. Our example application demonstrates the viability of the developed IP-Core for signal acquisition from multiple SiPMs.

Keywords: Data acquisition concepts; Electronic detector readout concepts (gas, liquid); Electronic detector readout concepts (solid-state); Optical detector readout concepts

*Corresponding author.

https://doi.org/10.1088/1748-0221/19/02/C02035

2024 JINST 19 C02035

Contents

2024 JINST 19 C02035

1 Multi-Voltage Thresholding concept basics

The Multi-Voltage Thresholding (MVT) concept has sparked interest in the PET community a decade ago [1, 2]. The MVT approach follows the similar principles as Flash-ADCs. It involves a voltage ladder for reference voltage levels and comparators for input comparison. The input analog signal is therefore "sliced" at the respective voltage levels and the information about the switching times of respective comparators is used to restore the original form of the input signal. A significant advantage of this approach is its rapid digitization capability, whereas achieving better voltage resolution requires a substantial number of comparators.

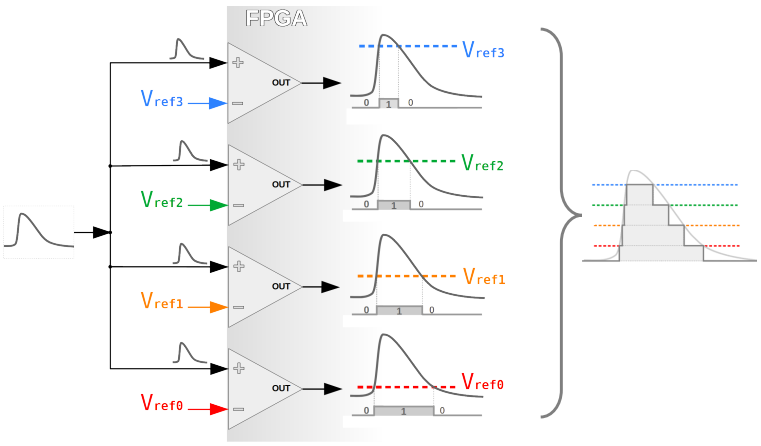


Figure 1. The concept of multi-voltage thresholding within an FPGA. The input pulse is "sliced" by the different reference voltages. The original pulse form can be restored from the comparators switching times.

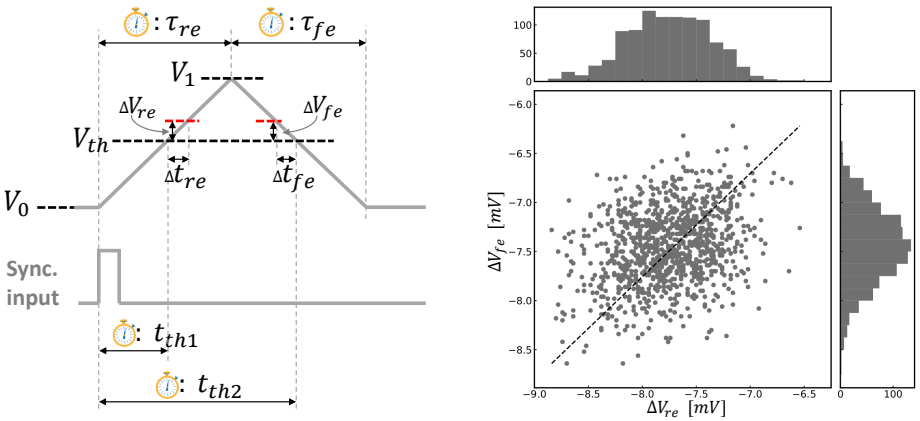
Modern FPGAs feature differential receivers for Low-Voltage Differential Signaling (LVDS) inputs which in their core contain comparators. These comparators can be utilized for MVT [1, 2] (cf. figure 1). The voltage references can be generated by slow and inexpensive multi-channel DACs. Depending on the reference voltage level, the comparators will have different transition- and on-times, for a given input signal (cf. figure 1). These transitions are precisely acquired by the proposed IP-Core and streamed out via the AXI4-Stream interface [3] as described in section 3.

2 Intrinsic biases and calibration procedure

Comparators of an FPGA are not ideal and have an intrinsic bias ΔV which can reach up to ±35 mV [4]. In order to use the comparator for the measurement purposes the bias voltage must be properly measured and compensated. It is important that the reference voltages provided for the comparators compensate the individual bias voltage of the respective comparator. A simple method for measuring the bias of a particular comparator by applying a synchronized triangle pulse with exactly known characteristics (length and amplitude) is shown in figure 2(a). We apply a threshold voltage V_{th} to the negative input of a particular comparator and measure the time when the comparator switches. The Δt_{re} and Δt_{fe} are time-shifts with respect to the times when an ideal comparator would have switched on rising- and falling edges, respectively. From the time-shifts the bias voltages ΔV_{re} (for the rising edge) and ΔV_{fe} (for the falling edge) are calculated as following:

$$\Delta V_{\text{re}} = \frac{(V_1 - V_0)}{\tau_{\text{re}}} \Delta t_{\text{re}}, \quad \Delta V_{\text{fe}} = \frac{(V_1 - V_0)}{\tau_{\text{fe}}} \Delta t_{\text{fe}}.$$

Repeating this procedure many times and plotting each calculated point in the $(\Delta V_{\text{re}}, \Delta V_{\text{fe}})$ coordinates, results in a distribution, which clearly characterizes the bias of a particular comparator (cf. figure 2(b)).

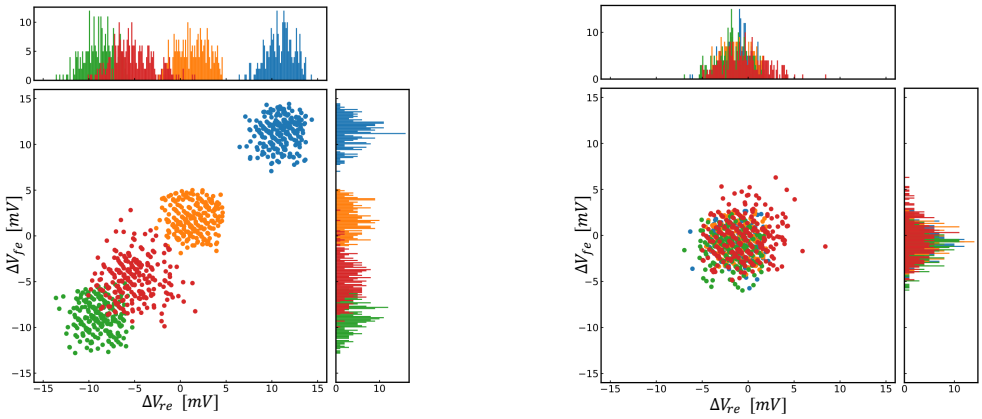


(a) (b)

Figure 2. (a): synchronized triangle pulse for measuring comparator's bias. V_{th} is set by DAC at the negative input of a comparator. Because of the intrinsic bias, the comparator switches at a slightly different voltage (shown with red dashed lines). The bias ΔV is calculated from the time difference between the expected switching time of an "ideal" comparator and the really measured switching time. (b): bias characterization for one comparator measured with 1000 triangle pulses. $\Delta V_{\text{fe}}, \Delta V_{\text{re}}$ — are bias values calculated from rising- and falling- edges respectively.

2024 JINST 19 C02035

In our IP-Core (cf. section 3), a group of four comparators is used, so the bias measurement procedure is performed on every of them, resulting in four distinct distributions (cf. figure 3(a)). The determined bias voltages are to be compensated by applying pedestals to the DAC-channels, providing reference voltages at the respective comparators. The bias measurement procedure is repeated after applying the pedestals, and results in a plot shown in figure 3(b).



(a) (b)

Figure 3. (a): bias characterization measurement for four comparators featuring four distinct distribution clusters. Each cluster corresponds to the bias of a specific comparator. (b): the same control characterization measurement after applying compensation pedestals on the DAC references of four comparators. This control measurement results in near-zero bias shift for all four channels.

3 MVT Quad IP-Core

3.1 General information

The proposed IP-Core features four sampling inputs and therefore is referred to as an MVT-Quad. The MVT-Quad IP-Core is an open-source project [5] distributed under the CC BY-SA 4.0 license. The structure of the MVT-Quad IP-Core is shown in figure 4.

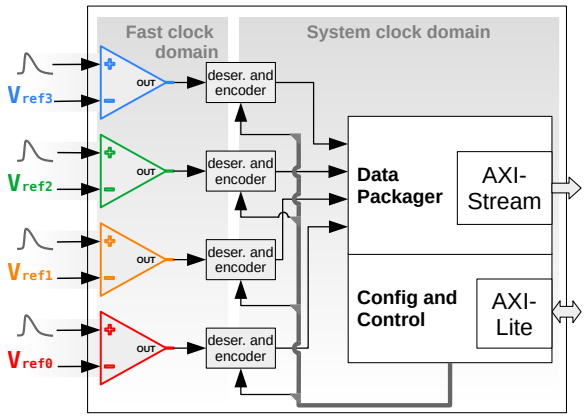


Figure 4. MVT Quad IP-Core structure.

3.2 IP-Core structure

Each of the four input comparators is followed by a block consisting of a deserializer and encoder, which are responsible for Time-to-Digital Conversion (TDC). Deserializers operate in a fast-clock domain and capture the signal transitions with a high time-resolution — $\mathcal{O}(1\,\text{ns})$. Particular time resolution depends on the system-clock frequency, because the fast clock runs phase-bound at four time the frequency of the system clock. TDCs are sampling at the double rate of the fast clock. Resulting TDC values are transferred from the encoders to the Data-Packager module. The Data-Packager module also features a 32-bit *MainCounter* which is incremented on each cycle of the system clock. The IP-Core features two interfaces: AXI4-Lite and AXI4-Stream. The AXI4-Lite interface is dedicated for interfacing internal configuration registers: for setting polarity of the comparators connected to the IP-Core and for resetting the value of the *MainCounter*. The AXI4-Stream interface streams out the acquired TDC values.

3.3 Output data format

AXI4-Stream data transmission is initiated whenever one or more comparators switch. Having at least one valid TDC-value from at least one comparator, the Data-Packager starts transmitting a sequence of 32-bit words via AXI4-Stream master interface (cf. figure 5). It starts with a word which carries the value of the system-clock based *MainCounter* register, serving as a raw time-reference. All the subsequent 32-bit payload words contain fine-grained addenda from the fast clock domain, which are related to the *MainCounter* as shown in figure 5. These words contain information on up to two transitions (rising- and falling- edges) which took place within one period of the system clock for each of the four comparators. The payload words are structured as follows: each 8 bits within the 32-bit word carry the information on the rising and falling edge transitions of one comparator. If any transition took place, the validity bit for the respective TDC-value will be set to "1". If no transitions are registered on any of the MVT Quad comparators within one period of the system clock, the AXI4-Stream transmission is ended.

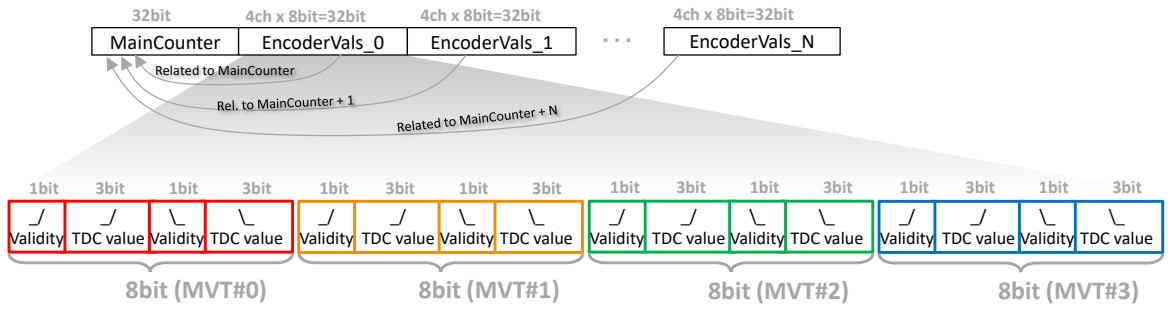
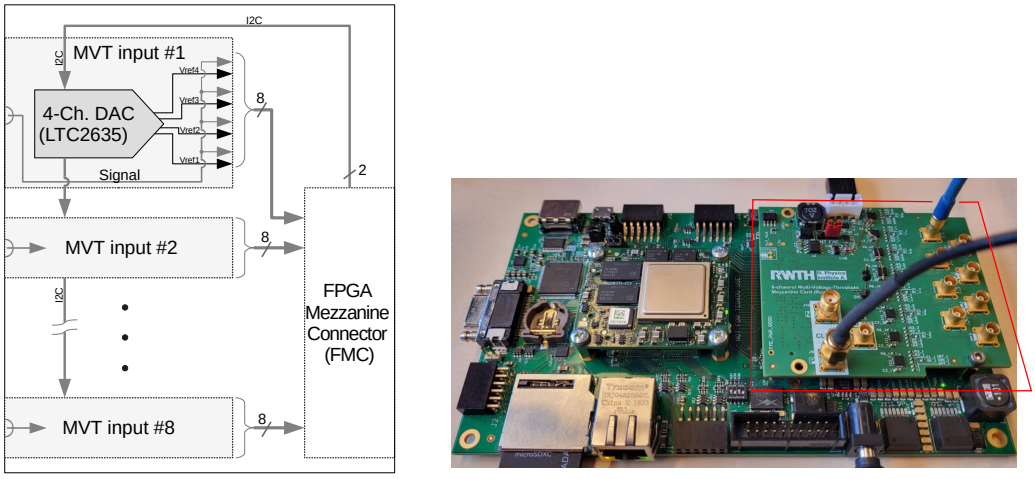


Figure 5. AXI4-Stream output data format of the MVT Quad IP-Core. The output words are 32-bit. First word in the transition is the *MainCounter* value. Subsequent 32-bit words are fine additions from the fast-clock domain. The "_/" and "_" symbols in the diagram indicate the bit-fields related to the rising- and falling edges respectively.

2024 JINST 19 C02035

4 Example application

The MVT Quad IP Core was tested with a custom FPGA Mezzanine Card (FMC) which structure is shown in figure 6. It supports eight analog inputs, using 64 FPGA pins for MVT digitization.



(a) (b)

Figure 6. (a) Block-diagram of the custom 8-channel mezzanine card for implementing the MVT. Structure of the input block circuitry is shown in details for the input block #1. All eight input blocks have the same structure, each including a 4-channel DAC respectively; (b) Photo of the board stackup, which includes the MVT mezzanine (outlined), System-On-Module and the carrier board.

Each analog input is equipped with a 4-channel 10-bit DAC (LTC2635), providing four reference voltages for the respective MVT Quad IP-Core. DAC values are loaded via the common I2C bus. The developed FMC module was tested with the System-on-Module (SoM) TE0820 [6] and the carrier module TE0701 [7]. The MVT IP-Cores are instantiated in the Programmable Logic area of the Zynq Ultrascale+ chip of the SoM. The I2C transactions for loading the values into the DACs, are driven by the application running within the Processing System of the same Zynq chip.

As for now calibration of the comparators is provided for each of the eight FMC inputs with help of the external function generator (Siglent SDG6022X). The function generator issues a triangle pulse together with a digital synchronization pulse, which is also connected to the FMC board. These procedure is repeated for each of eight inputs separately, letting us in each iteration simultaneously calibrate four comparators of the adjacent MVT-Quad.

In our example application, the system clock is chosen 100 MHz providing therefore a sampling rate of 800 MSPS for acquiring output pulses from eight SiPM frontends in a scintillator-based hodoscope.

5 Summary and outlook

We have successfully implemented and demonstrated the operation of the MVT-Quad IP-Core. The IP-Core is published and is further developed as an open-source project [5]. Looking ahead, the focus is on integration of the in-circuit generation of the calibration pulses, higher sampling rates, and expanding compatibility with various FPGA models for the MVT-Quad IP-Core.

2024 JINST 19 C02035

References

[1] D. Xi et al., *FPGA-Only MVT digitizer for TOF PET*, *IEEE Trans. Nucl. Sci.* **60** (2013) 3253.

[2] M. Pałka et al., *A novel method based solely on field programmable gate array (FPGA) units enabling measurement of time and charge of analog signals in positron emission tomography (PET)*, *Bio-Alg. Med-Syst.* **10** (2014) 41 [arXiv:1311.6127].

[3] ARM (2010), AMBA 4 AXI4-Stream Protocol, ARM IHI 0051A (ID030510).

[4] UltraScale Architecture SelectIO Resources, Datasheet UG571 v1.14, Xilinx (2022) 33.

[5] Open-Source IP-Core project for implementing Multi-Voltage Thresholding with FPGAs, https://gitlab.cern.ch/deliseev/mvt-quad-ip.

[6] Technical reference manual for TE0820 Zynq UltraScale+ MPSoC integrated SoM module., Trenz Electronic GmbH, https://wiki.trenz-electronic.de/display/PD/TE0820+TRM.

[7] Technical reference manual for TE0701 Carrier Board., Trenz Electronic GmbH, https://wiki.trenz-electronic.de/display/PD/TE0701+TRM,.

2024 JINST 19 C02035