

**AUTOMOTIVE MOSFET**

**IRF2804PbF**  
**IRF2804SPbF**  
**IRF2804LPbF**

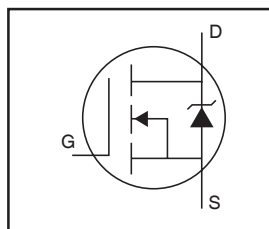
**HEXFET® Power MOSFET**

**Features**

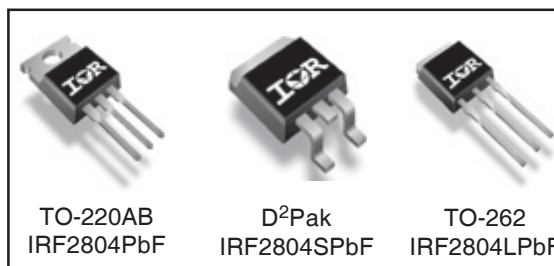
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to  $T_{jmax}$
- Lead-Free

**Description**

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



$V_{DSS} = 40V$
$R_{DS(on)} = 2.0m\Omega^{\circ}$
$I_D = 75A$



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	270	A
$I_D @ T_C = 100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$ (See Fig. 9)	190	
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	75	
$I_{DM}$	Pulsed Drain Current ①	1080	
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ②	540	mJ
$E_{AS} (tested)$	Single Pulse Avalanche Energy Tested Value ②	1160	
$I_{AR}$	Avalanche Current ①	See Fig.12a,12b,15,16	A
$E_{AR}$	Repetitive Avalanche Energy ③		mJ
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.50④	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state)⑤	—	40	

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## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

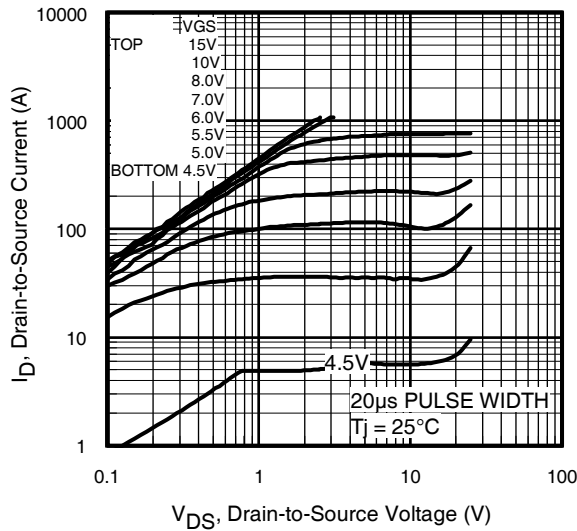
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.031	—	$V/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$ SMD	Static Drain-to-Source On-Resistance	—	1.5	2.0	$m\Omega$	$V_{GS} = 10V, I_D = 75A$ ④
$R_{DS(on)}$ TO-220	Static Drain-to-Source On-Resistance	—	1.8	2.3		$V_{GS} = 10V, I_D = 75A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	130	—	—	S	$V_{DS} = 10V, I_D = 75A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	160	240	nC	$I_D = 75A$
$Q_{gs}$	Gate-to-Source Charge	—	41	62		$V_{DS} = 32V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	66	99		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	$V_{DD} = 20V$
$t_r$	Rise Time	—	120	—		$I_D = 75A$
$t_{d(off)}$	Turn-Off Delay Time	—	130	—		$R_G = 2.5\Omega$
$t_f$	Fall Time	—	130	—		$V_{GS} = 10V$ ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	6450	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	1690	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	840	—		$f = 1.0\text{MHz}$ , See Fig. 5
$C_{oss}$	Output Capacitance	—	5350	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	1520	—		$V_{GS} = 0V, V_{DS} = 32V, f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	2210	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 32V$

## Diode Characteristics

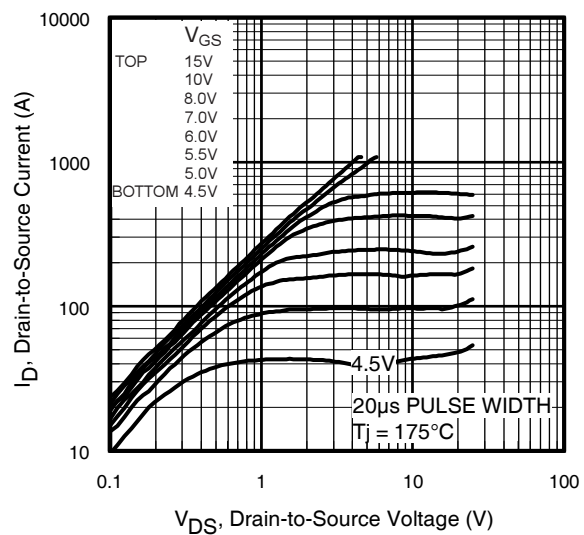
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	270	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	1080		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 75A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	56	84	ns	$T_J = 25^\circ\text{C}, I_F = 75A, V_{DD} = 20V$
$Q_{rr}$	Reverse Recovery Charge	—	67	100	nC	$di/dt = 100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

### Notes:

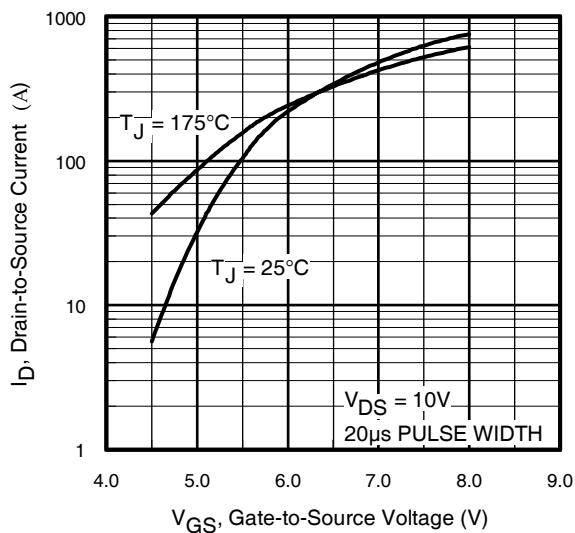
- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by  $T_{Jmax}$ ; starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.24\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 75A$ ,  $V_{GS} = 10V$ .  
Part not recommended for use above this value.
- ③  $I_{SD} \leq 75A$ ,  $di/dt \leq 220A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 1.0\text{ms}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss \text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥ Limited by  $T_{Jmax}$ ; see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑦ This value determined from sample failure population. 100% tested to this value in production.
- ⑧ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ Max  $R_{DS(on)}$  for D<sup>2</sup>Pak and TO-262 (SMD) devices.
- ⑩ TO-220 device will have an  $R_{th}$  value of  $0.45^\circ\text{C/W}$ .



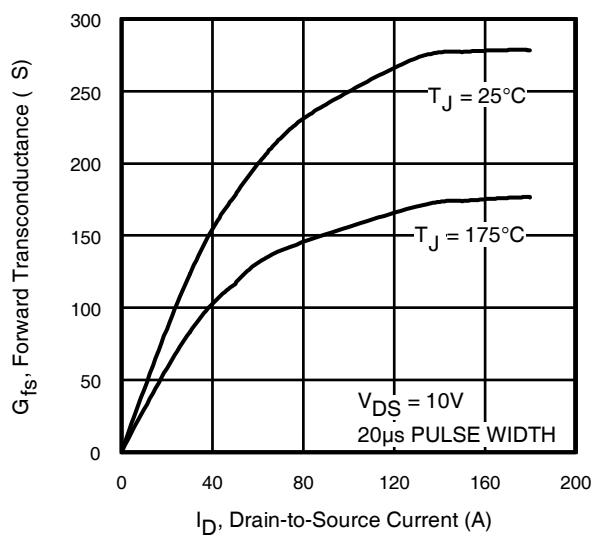
**Fig 1.** Typical Output Characteristics



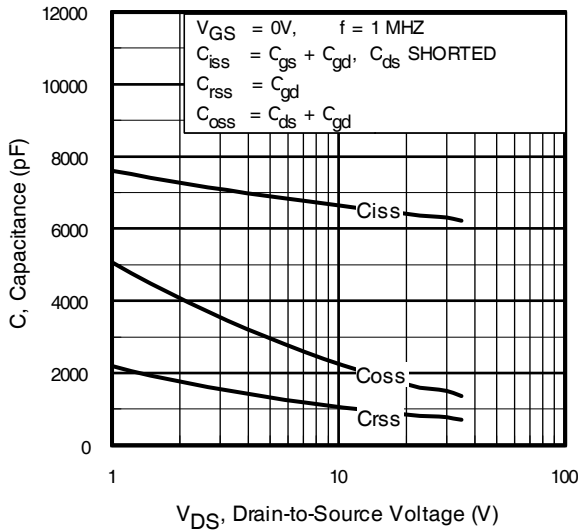
**Fig 2.** Typical Output Characteristics



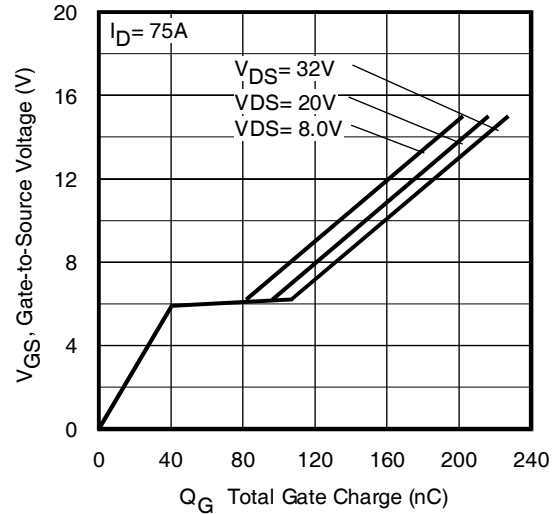
**Fig 3.** Typical Transfer Characteristics



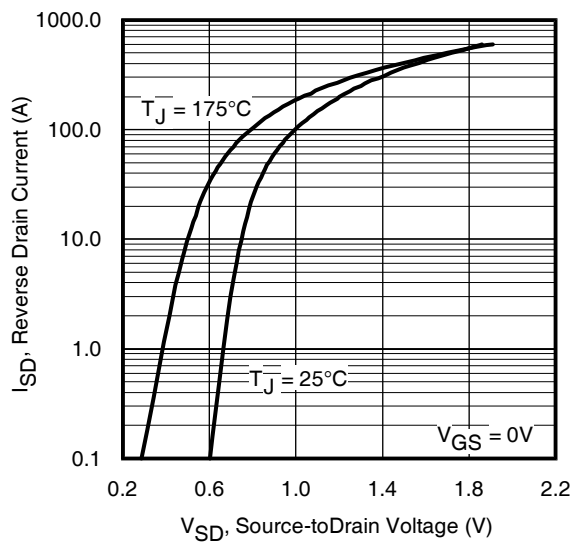
**Fig 4.** Typical Forward Transconductance vs. Drain Current



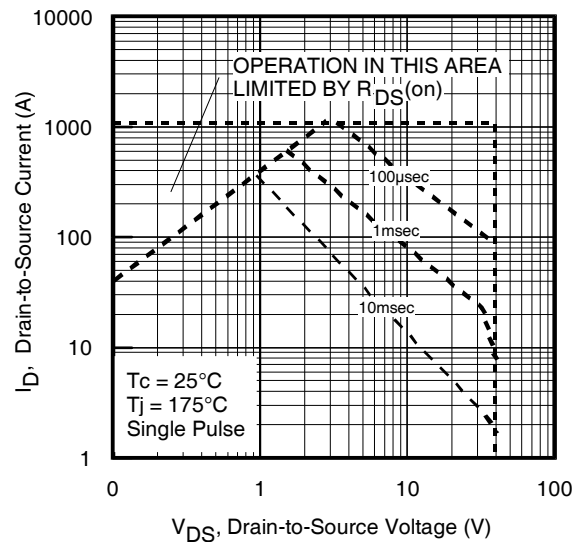
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



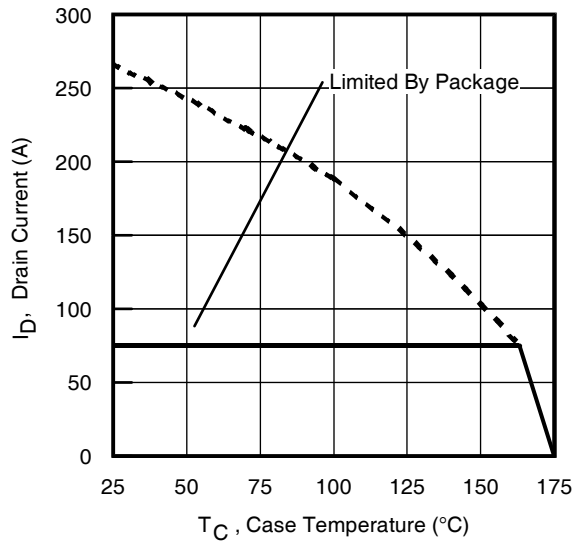
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



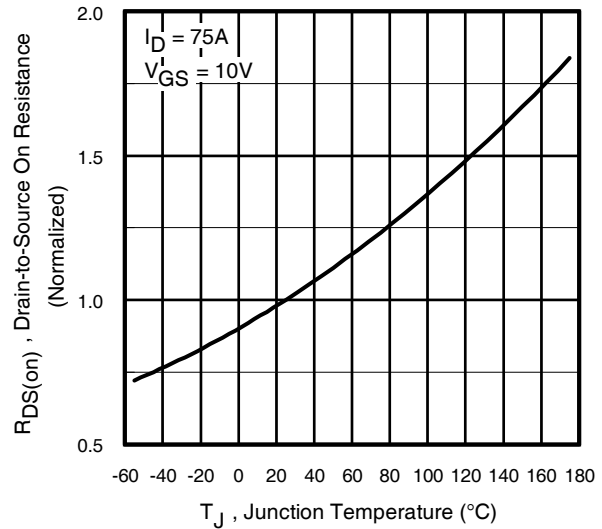
**Fig 7.** Typical Source-Drain Diode Forward Voltage



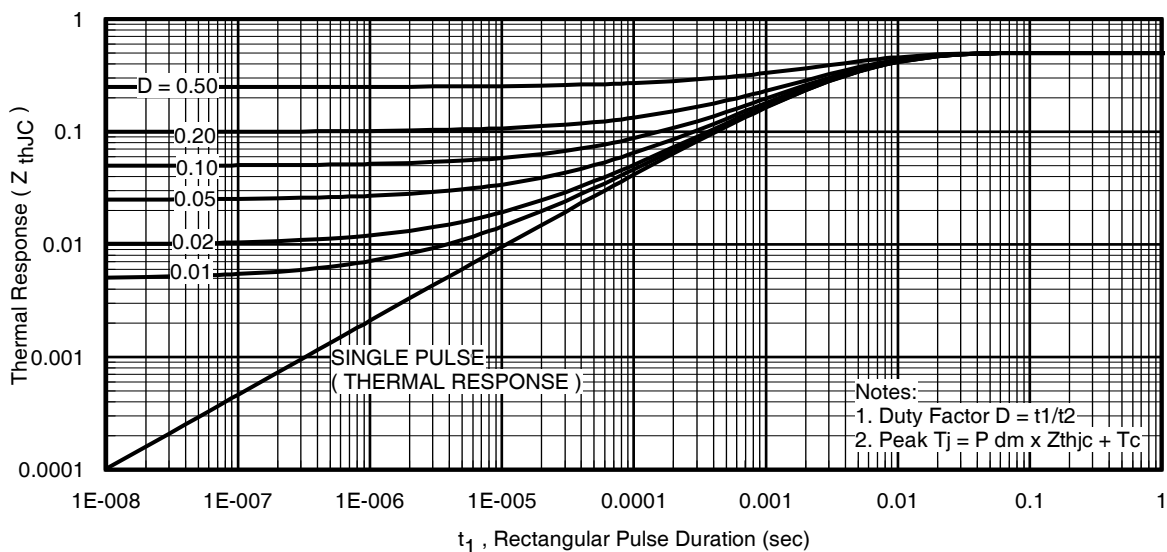
**Fig 8.** Maximum Safe Operating Area



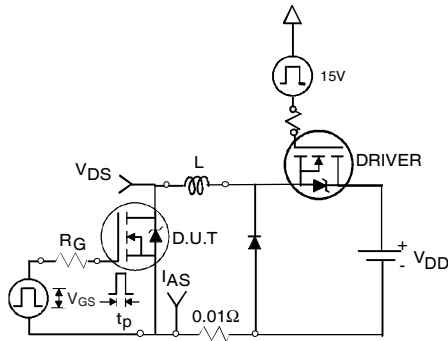
**Fig 9.** Maximum Drain Current vs. Case Temperature



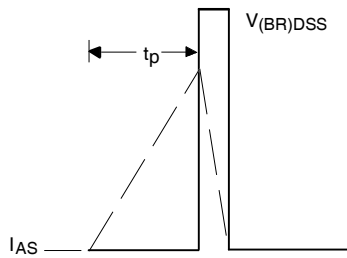
**Fig 10.** Normalized On-Resistance vs. Temperature



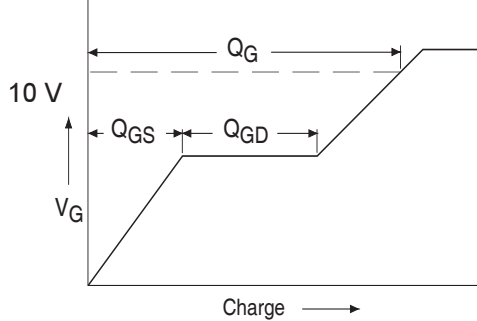
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



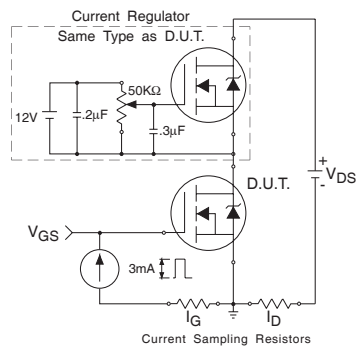
**Fig 12a.** Unclamped Inductive Test Circuit



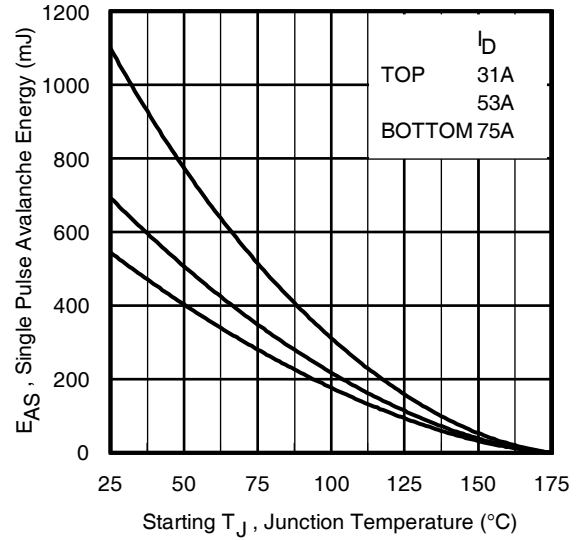
**Fig 12b.** Unclamped Inductive Waveforms



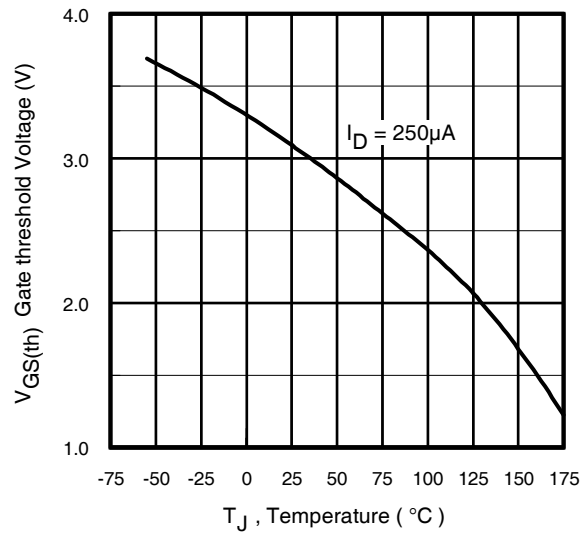
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy vs. Drain Current



**Fig 14.** Threshold Voltage vs. Temperature

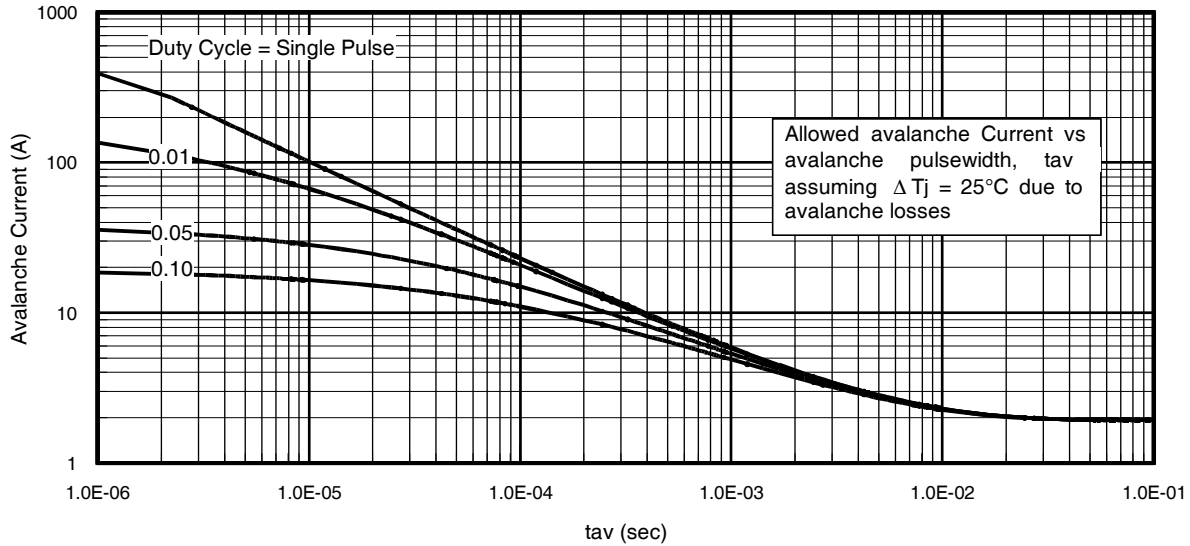


Fig 15. Typical Avalanche Current Vs. Pulsewidth

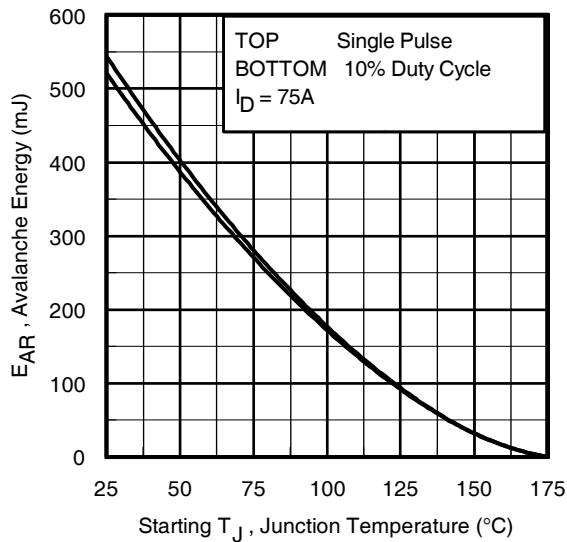


Fig 16. Maximum Avalanche Energy vs. Temperature

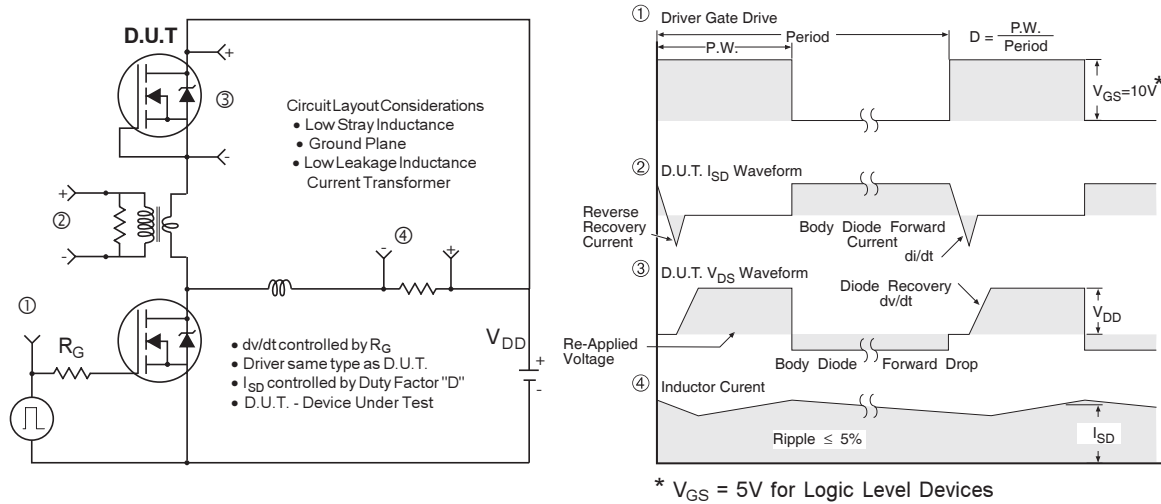
**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

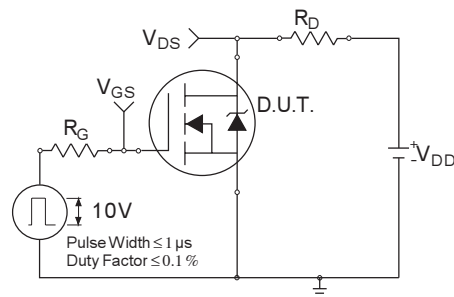
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

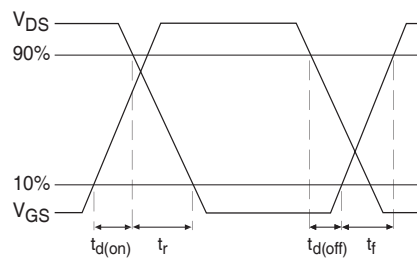
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



**Fig 18a.** Switching Time Test Circuit

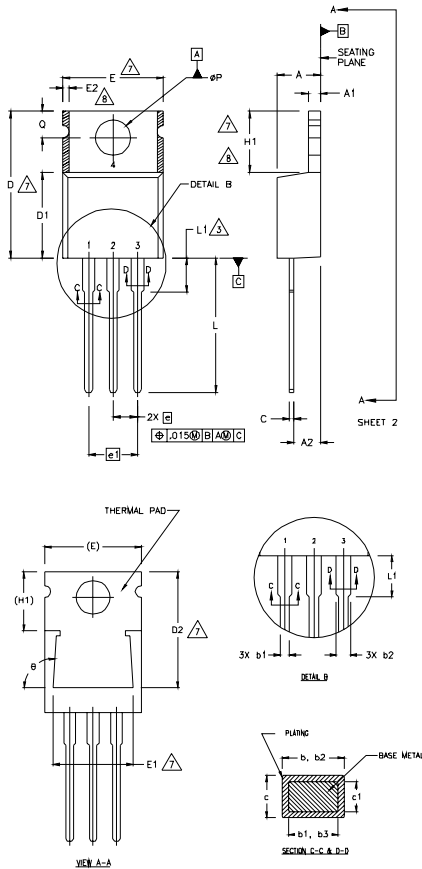


**Fig 18b.** Switching Time Waveforms



## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



### NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5 DIMENSION b1 & c1 APPLY TO BASE METAL ONLY.
- 6 CONTROLLING DIMENSION : INCHES.
- 7 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8 DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

### LEAD ASSIGNMENTS

#### HERFET

- 1- GATE
- 2- DRAIN
- 3- SOURCE

### IGBTs, CoPACK

- 1- GATE
- 2- COLLECTOR
- 3- EMITTER

### DIODES

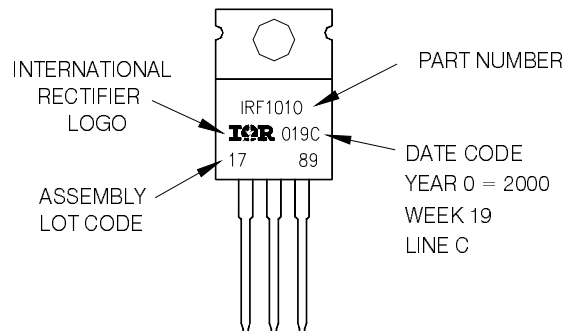
- 1- ANODE/OPEN
- 2- CATHODE
- 3- ANODE

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.82	.140	.190	5
A1	0.51	1.40	.020	.055	
A2	2.04	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.96	.015	.038	
b2	1.15	1.77	.045	.070	5
b3	1.15	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	
D	14.22	16.51	.560	.650	
D1	8.38	9.02	.330	.355	
D2	12.19	12.88	.480	.507	7
E	9.66	10.66	.380	.420	4,7
E1	8.38	8.89	.330	.350	7
e	2.54 BSC		.100 BSC		7,8
e1	5.08		.200 BSC		
H1	5.85	6.55	.230	.270	
L	12.70	14.73	.500	.580	
L1	-	6.35	-	.250	
ØP	3.54	4.08	.139	.161	3
Q	2.54	3.42	.100	.135	
ø	90°-93°		90°-93°		

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
LOT CODE 1789  
ASSEMBLED ON WW 19, 2000  
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position  
indicates "Lead - Free"

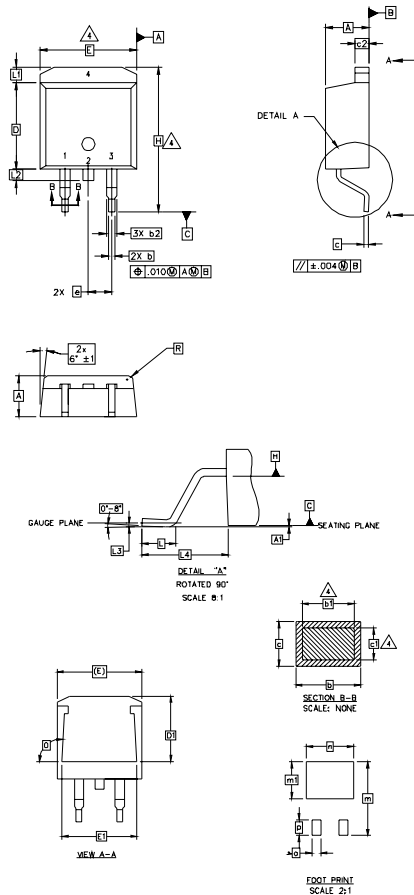


# IRF2804/S/LPbF

## D<sup>2</sup>Pak Package Outline

Dimensions are shown in millimeters (inches)

International  
**IR** Rectifier



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.78	.045	.070	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	4
c2	1.14	1.65	.045	.065	
D	8.51	9.65	.335	.380	3
D1	6.86		.270		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1		1.65		.065	
L2	1.27	1.78	.050	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
R	0.51	0.71	.020	.028	
θ	90°	93°	90°	93°	

### LEAD ASSIGNMENTS

#### HEXFET

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

#### IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

#### DIODES

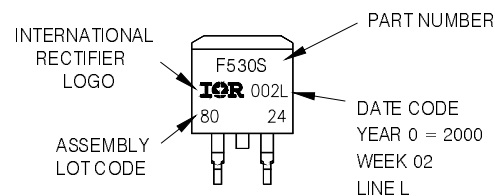
- 1.- ANODE \*
- 2, 4.- CATHODE
- 3.- ANODE

\* PART DEPENDENT.

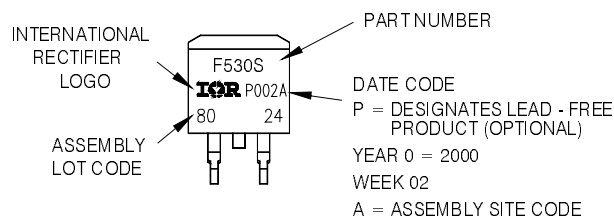
## D<sup>2</sup>Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position  
indicates "Lead - Free"

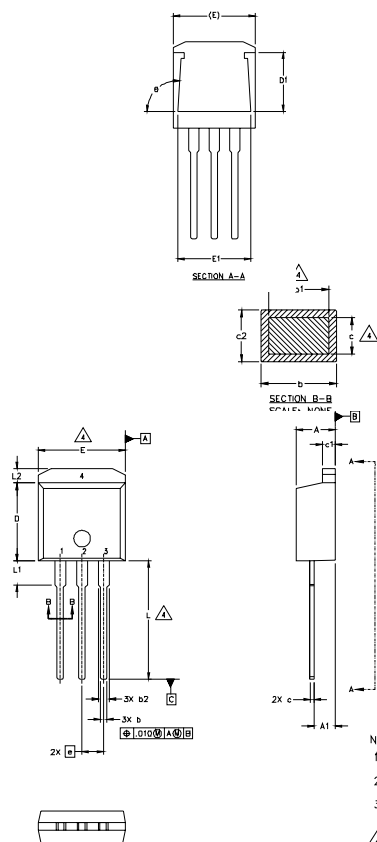


OR



## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

### LEAD ASSIGNMENTS

#### HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

#### IGBT

- 1 - GATE
- 2 - COLLECTOR
- 3 - EMITTER

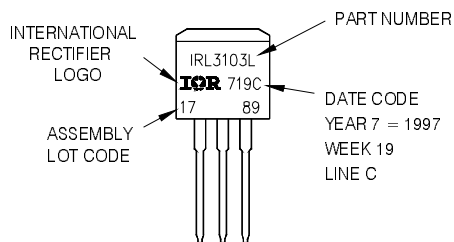
#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

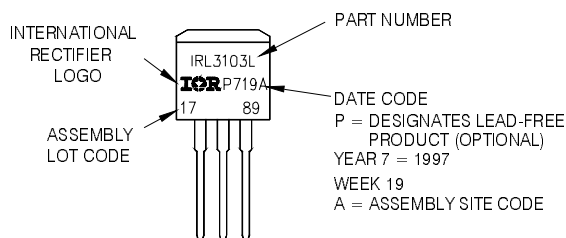
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
LOT CODE 1789  
ASSEMBLED ON VW 19, 1997  
IN THE ASSEMBLY LINE 'C'

Note: 'P' in assembly line position indicates 'Lead-Free'



**OR**

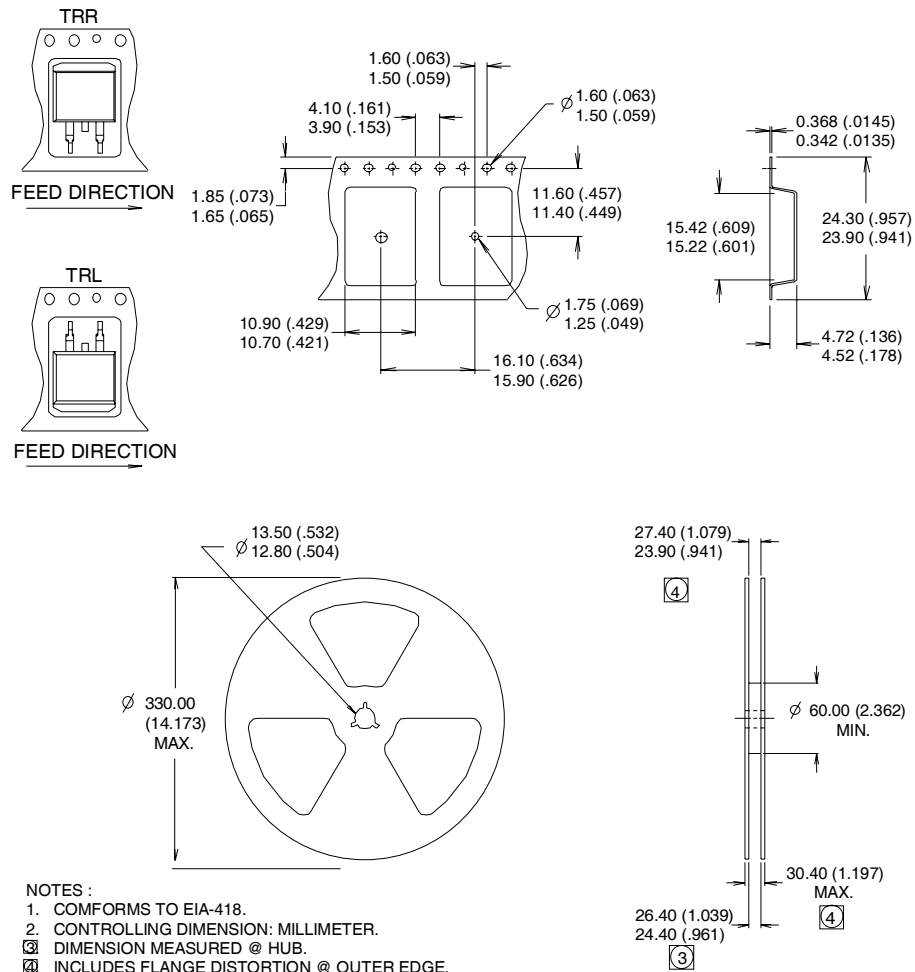


# IRF2804/S/LPbF

International  
**IR** Rectifier

## D<sup>2</sup>Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



**TO-220AB package is not recommended for Surface Mount Application.**

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Automotive [Q101] market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

Visit us at [www.irf.com](http://www.irf.com) for sales contact information. 08/05

[www.irf.com](http://www.irf.com)

Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>