1 General Description

The AS5035 is a magnetic incremental encoder with 64 quadrature pulses per revolution (8-bit resolution) and index output.

Two diagnostic outputs are provided to indicate an out-of-range condition of the magnetic field as well as movement of the magnet in Z-axis. In addition a specific combination of output states indicate a loss of power supply.

The AS5035 is available in a small 16pin SSOP package. It can be operated at either 3.3V or 5V supplies.

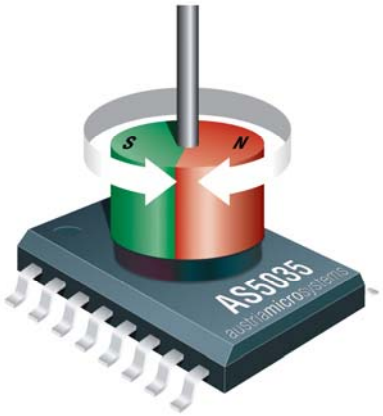

Figure 1: Typical arrangement of AS5035 and magnet

1.1 Benefits

- Complete system-on-chip, including analog front end and digital signal processing
- 2-channel quadrature and index outputs provide an alternative to optical encoders
- User programmable Zero positioning by OTP allows easy assembly of magnet
- Diagnostic features for operation safety
- Ideal for applications in harsh environments due to magnetic sensing principle
- Robust system, tolerant to magnet misalignment, air gap variations, temperature variations and external magnetic stray fields
- No calibration required

2 Key Features

Full turn (360°) contactless angular position encoder

2 quadrature A/B outputs with 64 pulses per revolution (ppr), 256 edges per revolution, 1.4° per step

Index output (one pulse per revolution)

Accurate zero position, repeatability within (0.35°)

Failure detection mode for magnet placement monitoring and loss of power supply

Wide temperature range: - 40°C to + 125°C

Small lead-free package: SSOP 16 (5.3mm x 6.2mm)

3 Applications

Industrial applications:

- Robotics
- Replacement of optical encoders
- Flow meters
- Man-machine interface

Automotive applications:

- Power seat position sensing
- Power mirror position sensing

4 Pin Configuration

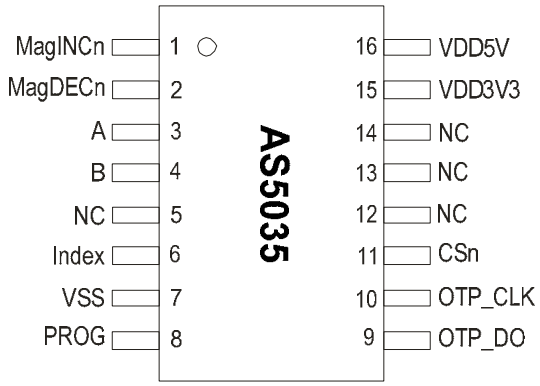

Figure 2: AS5035 Pin configuration SSOP16

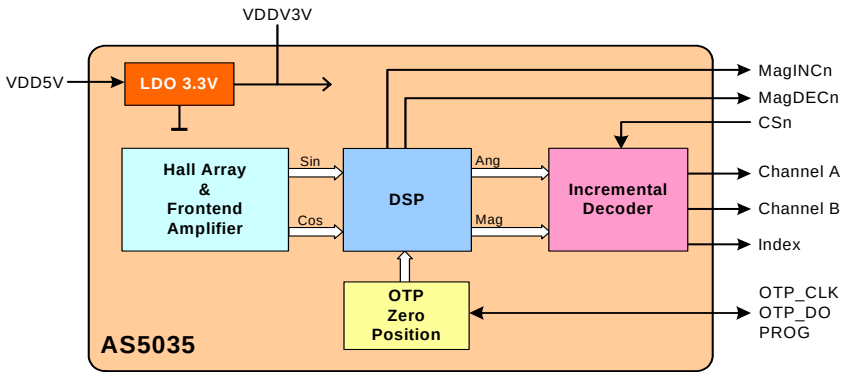

Figure 3: AS5035 Block diagram

4.1 Pin List & Description

Pin # SSOP16	Name	Type	AS5035
1	MagInc	DO_OD	Mag. Field indicator
2	MagDec	DO_OD	Mag. Field indicator
3	A	DO	Quadrature channel A
4	B	DO	Quadrature channel B
5	N.C.	test	Must be left open
6	Index	DO	Incremental Index output
7	VSS	Supply	Supply Ground
8	Prog	DI , pd	OTP Programming Input. Internal pull-down resistor (~74kΩ). Should be connected to VSS if not used
9	OTP_DO	DO_T	Data Output for Zero Position programming
10	OTP_CLK	DI,ST	Clock Input for Zero Position programming; Schmitt-Trigger input. Should be connected to VSS if not used
11	CSn	DI_ST, pu	Enable outputs A,B,I (see 5.4). Connect to VSS for normal operation
12	N.C.	test	Must be left open
13	N.C.	test	Must be left open
14	N.C.	test	Must be left open
15	VDD3V3	Supply	3V regulator output
16	VDD5V	Supply	5V positive supply input

Table 1: Pin description

DO_OD : digital output, open drain
DO : digital push/pull output
DI : digital input
ST : Schmitt-Trigger input
pu : internal pull-up resistor
pd : internal pull-down resistor
test : pin is used for factory testing, must be left unconnected

4.2 Unused Pins

Pins # 5, 8, 12, 13 and 14 are for factory testing and must be left unconnected

Pins# 8, 9 and 10 are used for OTP Zero Position Programming only. In normal operation, they can be left open or connected to VSS (pins 8 and 10 only)

5 Connecting the AS5035

5.1 Power Supply

5.1.1 5.0V Operation

Connect a 4.5V to 5.5V power supply to pin VDD5V only. Add a 1µF to 10µF buffer capacitor to pin VDD3V3

5.1.2 3.3V Operation

Connect a 3.0V to 3.6 V power supply to both pins VDD5V and VDD3V3. If necessary, add a 100nF ceramic buffer capacitor to pin VDD3V3.

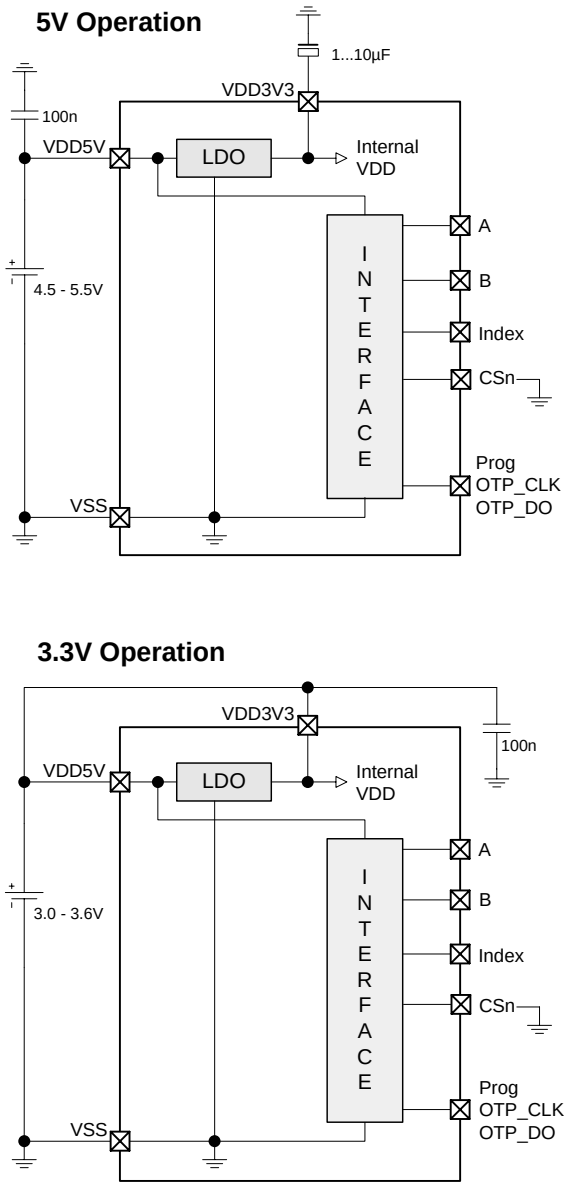

Figure 4: Connections for 5V / 3.3V supply voltages

5.2 Logic High and Low Levels

VDD5V will be either 3.0 - 3.6V or 4.5 - 5.5V, depending on configuration.

In either case, the logic levels on output pins A, B and Index will be
Vout high = VDD5V – 0.5V,

Vout low = VSS+0.4V.

The logic level on the CSn input pin will be

Vin high = VDD5V*0.7,

Vin low = VDD5V*0.3

5.3 Output Current

The available maximum output current on pins A, B and Index to maintain the Vout high and Vout low levels is

2mA (sink and source) at VDD5V = 3.0V

4mA (sink and source) at VDD5V = 4.5V

5.4 Chip Select Pin CSn

5.4.1 Without Power-up Diagnostic Feature

For standalone operation without microcontroller, pin CSn should be connected to VSS permanently. The incremental outputs will be available, as soon as the internal offset compensation is finished (within <50ms).

5.4.2 With Power-up Diagnostic Feature

A diagnostic feature is available to detect a temporary loss of power or initial power-up of the AS5035: if the CSn pin is high or left open (internal pull up resistor ~50kΩ) during power-up, the incremental outputs will remain in high state: A = B = Index = High.

This state indicates a power-up or temporary loss of power, as in normal operation A,B and Index will never be high at the same time. When Index is high, both A and B are low.

To clear this state end enable the incremental outputs, CSn must be pulled low. The incremental outputs will remain enabled if CSn returns to high afterwards.

5.5 MagInc and MagDec Indicators

These two pins are open-drain outputs with a maximum driving capability of 2mA @ 3.0V and 4mA @ 4.5V.

MagINC, (Magnitude Increase) turns on, when the magnet is pushed towards the IC, thus when the magnetic field strength is increasing.

MagDEC, (Magnitude Decrease) turns on, when the magnet is pulled away from the IC, thus when the magnetic field strength is decreasing.

If both outputs are low, they indicate that the magnetic field out of the allowed range:

MagINC	MagDEC	Description
off	off	No distance change. Magnetic Input Field OK
off	on	Distance increase (Magnet pulled away from IC)
on	off	Distance decrease (Magnet pushed towards IC)
on	on	Magnetic Input Field invalid – out of range: either too large (magnet too close) or too small (missing magnet or magnet too far away)

Table 2: Magnetic field strength diagnostic outputs

off = open-drain output transistor is off. Using a pull-up resistor, the output is high
on = open-drain output transistor is on. Using a pull-up resistor, the output is low

Both outputs MagInc and MagDec may be tied together, using one common pull-up resistor. In this case, the output will be high only when the magnetic field is in range. It will be low when either the magnet is moving in Z-axis or when the magnetic field is out of range.

6 Incremental Outputs

6.1 A, B and Index

The phase shift between channel A and B indicates the direction of the magnet movement. Channel A leads channel B at a clockwise rotation of the magnet (top view, magnet placed above or below the device) with 90 electrical degrees. Channel B leads channel A at a counter-clockwise rotation. The Index pulse has a width of 1LSB = 1.4°

6.2 Hysteresis

To avoid flickering of the incremental outputs at a stationary mechanical position, a hysteresis of 0.7° is introduced. When the direction of rotation is reversed, the incremental outputs will not change state unless the movement in the opposite direction is larger than the hysteresis. This leads to the effect that the A,B and Index pulse positions will be shifted by 0.7° when the rotational direction is reversed. This shift is cancelled again with the next reversal of direction so that the A,B and Index pulses appear always at the same position for a given rotational direction no matter how often the rotational direction is reversed (see Figure 5).

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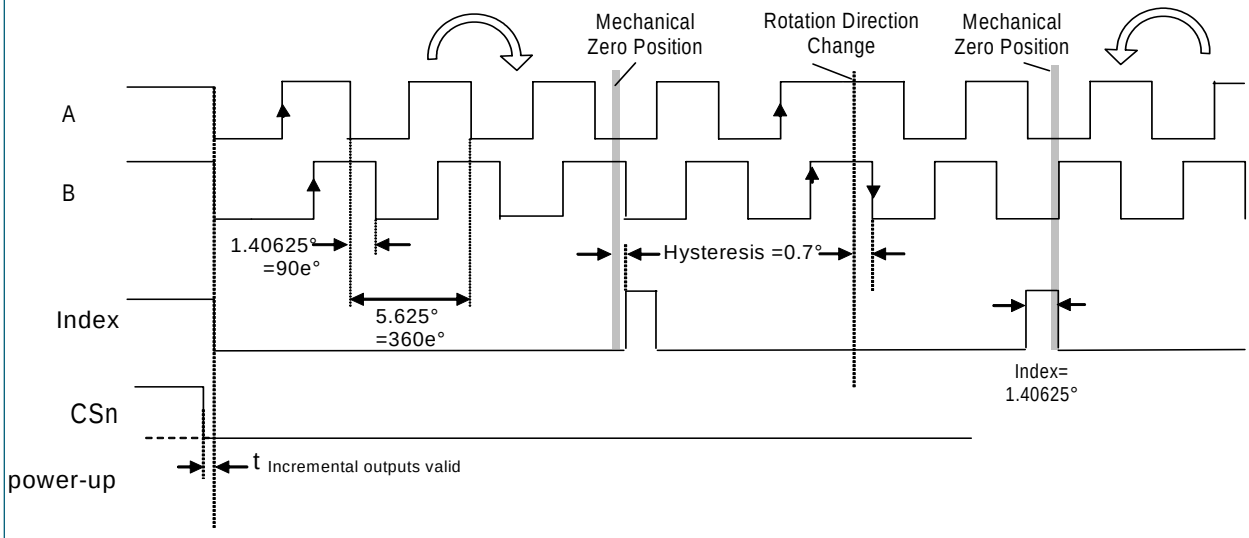


Figure 5: Incremental quadrature outputs

7 OTP Programming and Timing

OTP programming requires access to the factory settings register of the AS5035. Improper or accidental modification of the factory settings may render the chip unusable. Therefore the Zero Position and CCW programming is recommended only with austriamicrosystems proprietary hardware and software.

Note: During the programming process, the transitions in the programming current may cause high voltage spikes generated by the inductance of the connection cable. To avoid these spikes and possible damage to the IC, the connection wires, especially the signals Prog and VSS must be kept as short as possible. The maximum wire length between the V_{PROG} switching transistor and pin Prog (see Figure 6) should not exceed 50mm (2 inches). To suppress eventual voltage spikes, a 10nF ceramic capacitor should be connected close to pins Prog and VSS. This capacitor is only required for programming, it is not required for normal operation.

The clock timing t_{clk} must be selected at a proper rate to ensure that the signal Prog is stable at the rising edge of CLK (see Figure 7). Additionally, the programming supply voltage should be buffered with a 10µF capacitor mounted close to the switching transistor. This capacitor aids in providing peak currents during programming.

The specified programming voltage at pin Prog is 7.3 – 7.5V (see section 12.8). To compensate for the voltage drop across the VPROG switching transistor, the applied programming voltage may be set slightly higher (7.5 - 8.0V).

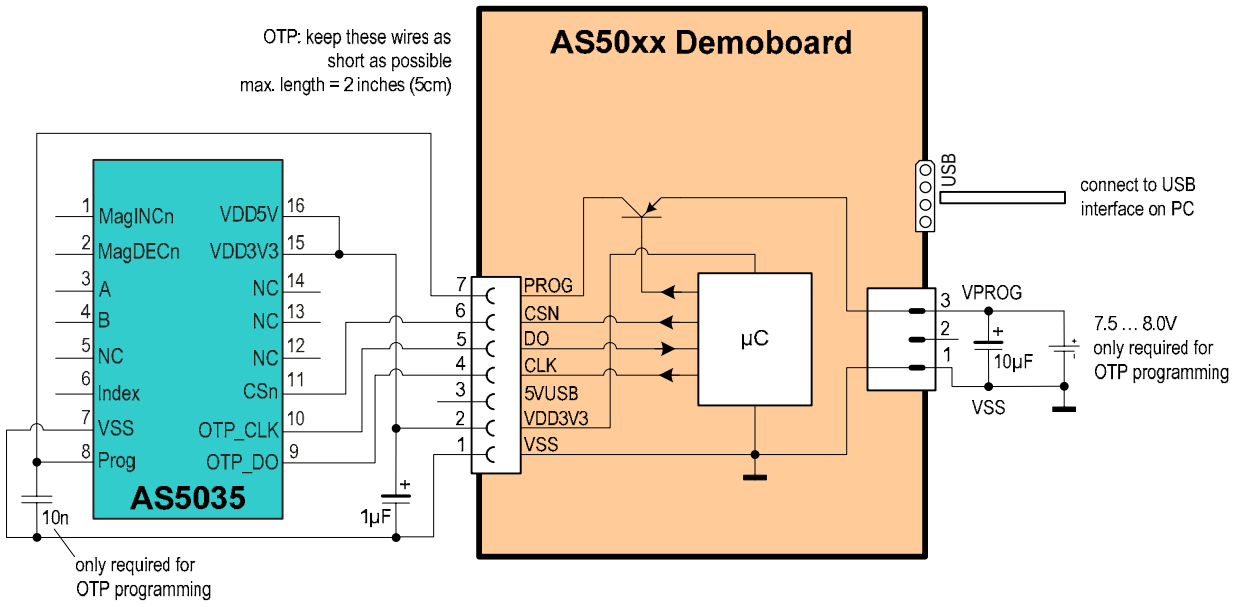


Figure 6: Hardware connection of AS5035 to AS50xx Demoboard for Zero Position Programming

7.1 Zero Position Programming

Zero Position Programming is an OTP option that simplifies assembly of a system, as the magnet does not need to be manually adjusted to the mechanical zero position. Once the assembly is completed, the mechanical and electrical zero positions can be matched by software. Any position within a full turn can be defined as the permanent new index position.

For Zero Position Programming, the magnet is turned to the mechanical zero position (e.g. the “off”-position of a rotary switch) and an automatic zero position programming is applied.

The programmability of the zero position is +/- 1.4°. In normal operation the repeatability of the position is +/- 0.35°.

7.2 CCW Bit Programming

The absolute angular output value, by default, increases with clockwise rotation of the magnet (top view). Setting the CCW-bit (see Figure 7) allows for reversing the indicated direction, e.g. when the magnet is placed underneath the IC:

CCW = 0 – angular value increases clockwise;

CCW = 1 – angular value increases counterclockwise.

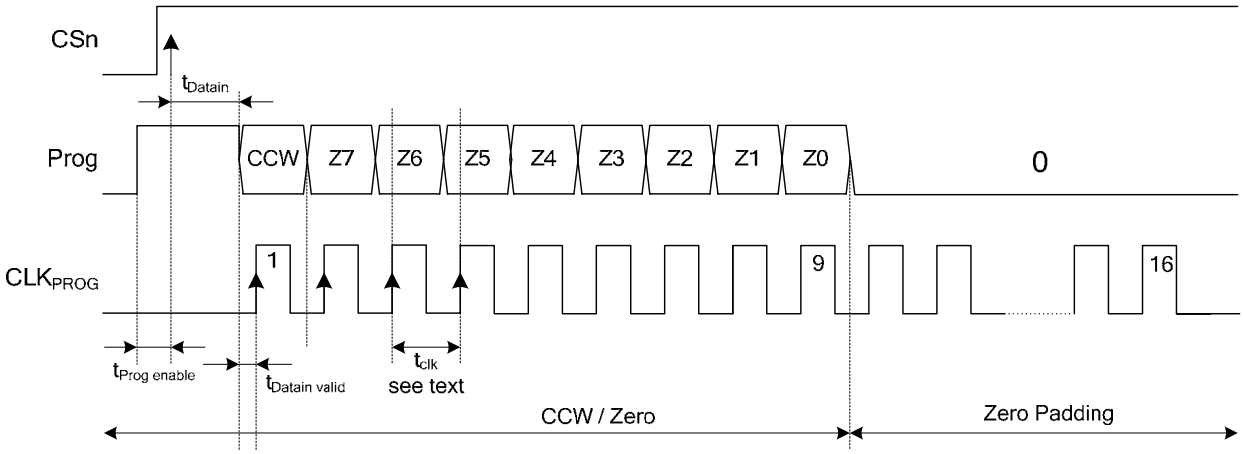


Figure 7: Programming access – write data (first section of Figure 8)

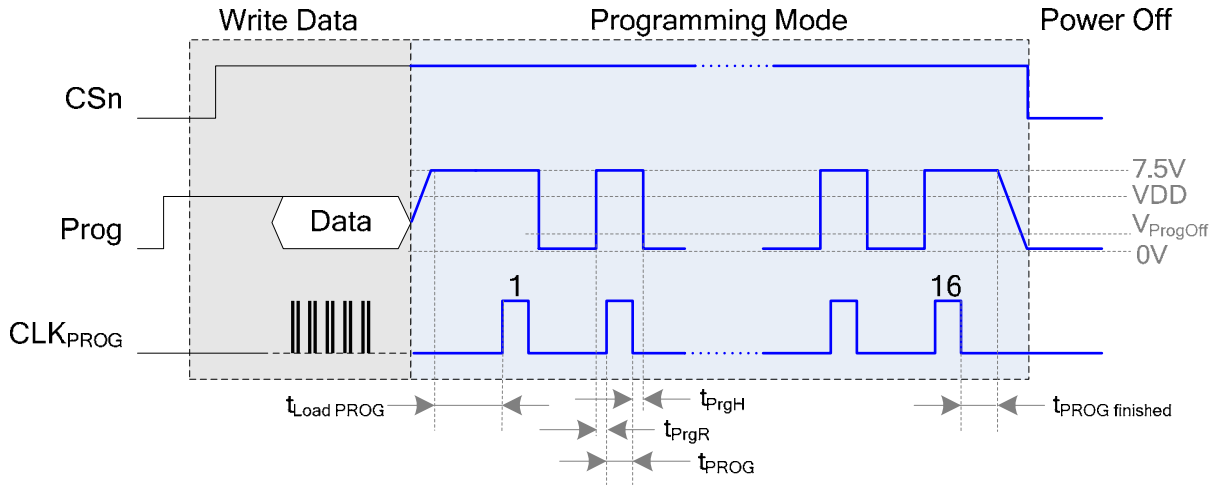


Figure 8: Complete programming sequence

7.3 Analog Readback Mode

Non-volatile programming (OTP) uses on-chip zener diodes, which become permanently low resistive when subjected to a specified reverse current.

The quality of the programming process depends on the amount of current that is applied during the programming process (up to 130mA). This current must be provided by an external voltage source. If this voltage source cannot provide adequate power, the zener diodes may not be programmed properly.

In order to verify the quality of the programmed bits, an analog level can be read for each zener diode, giving an indication whether this particular bit was properly programmed or not.

To put the AS5030 in analog readback mode, a digital sequence must be applied to pins CSn, Prog and CLK as shown in Figure 9. The digital level for this pin depends on the supply configuration (3.3V or 5V; see section 5.1).

The second rising edge on CSn (OutpEN) changes pin Prog to a digital output and the log. high signal at pin Prog must be removed to avoid collision of outputs (grey area in Figure 9).

The following falling slope of CSn changes pin Prog to an analog output, providing a reference voltage V_{ref}, that must be saved as a reference for the calculation of the subsequent programmed and unprogrammed OTP bits. Following this step, each rising slope of CLK outputs one bit of data in the reverse order as during programming(see Figure 9).

During analog readback, the capacitor at pin Prog (see Figure 6) should be removed to allow a fast readout rate. If the capacitor is not removed the analog voltage will take longer to stabilize due to the additional capacitance.

The measured analog voltage for each bit must be subtracted from the previously measured V_{ref}, and the resulting value gives an indication on the quality of the programmed bit: a reading of <100mV indicates a properly programmed bit and a reading of >1V indicates a properly unprogrammed bit.

A reading between 100mV and 1V indicates a faulty bit, which may result in an undefined digital value, when the OTP is read at power-up.

Following the 16th clock (after reading bit “ccw”), the chip must be reset by disconnecting the power supply.

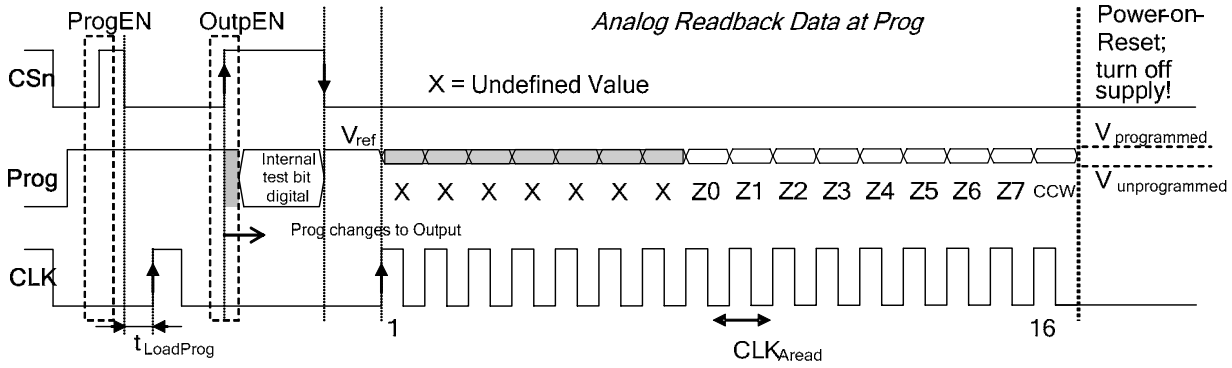


Figure 9: OTP register analog read

8 Simulation Modelling

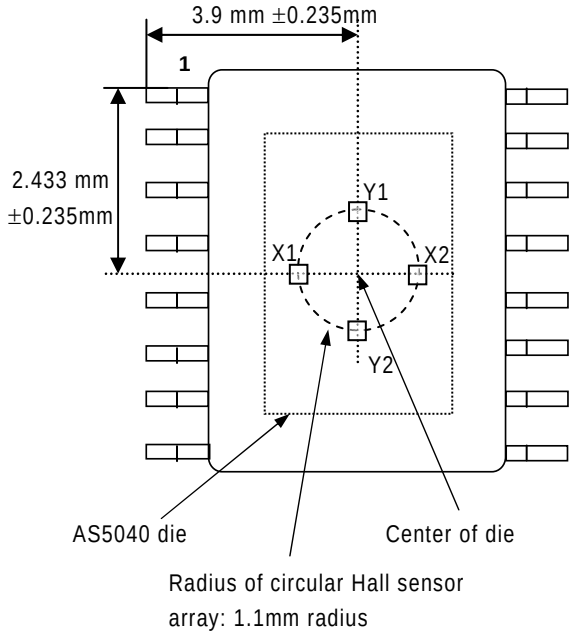


Figure 10: Arrangement of Hall sensor array on chip (principle)

With reference to Figure 10, a diametrically magnetized permanent magnet is placed above or below the surface of the AS5035. The chip uses an array of Hall sensors to sample the vertical vector of a magnetic field distributed across the device package surface. The area of magnetic sensitivity is a circular locus of 1.1mm radius with respect to the center of the die. The Hall sensors in the area of magnetic sensitivity are grouped and configured such that orthogonally related components of the magnetic fields are sampled differentially.

The differential signal Y1-Y2 will give a sine vector of the magnetic field. The differential signal X1-X2 will give an orthogonally related cosine vector of the magnetic field.

The angular displacement (Θ) of the magnetic source with reference to the Hall sensor array may then be modelled by:

$$\Theta = \arctan\frac{(Y1-Y2)}{(X1-X2)} \pm 0.5°$$

The ±0.5° angular error assumes a magnet optimally aligned over the center of the die and is a result of gain mismatch errors of the AS5035. Placement tolerances of the die within the package are ±0.235mm in X and Y direction, using a reference point of the edge of pin #1 (Figure 12)

In order to neglect the influence of external disturbing magnetic fields, a robust differential sampling and ratiometric calculation algorithm has been implemented. The differential sampling of the sine and cosine vectors removes any common mode error due to DC components introduced by the magnetic source itself or external disturbing magnetic fields. A ratiometric division of the sine and cosine vectors removes the need for an accurate absolute magnitude of the magnetic field and thus accurate Z-axis alignment of the magnetic source.

The recommended differential input range of the magnetic field strength ($B_{(X1-X2)}$,$B_{(Y1-Y2)}$) is ±75mT at the surface of the die. In addition to this range, an additional offset of ±5mT, caused by unwanted external stray fields is allowed.

The chip will continue to operate, but with degraded output linearity, if the signal field strength is outside the recommended range. Too strong magnetic fields will introduce errors due to saturation effects in the internal preamplifiers. Too weak magnetic fields will introduce errors due to noise becoming more dominant.

9 Choosing the Proper Magnet

Typically the magnet should be 6mm in diameter and 3mm in height. Magnetic materials such as rare earth AlNiCo, SmCo5 or NdFeB are recommended.

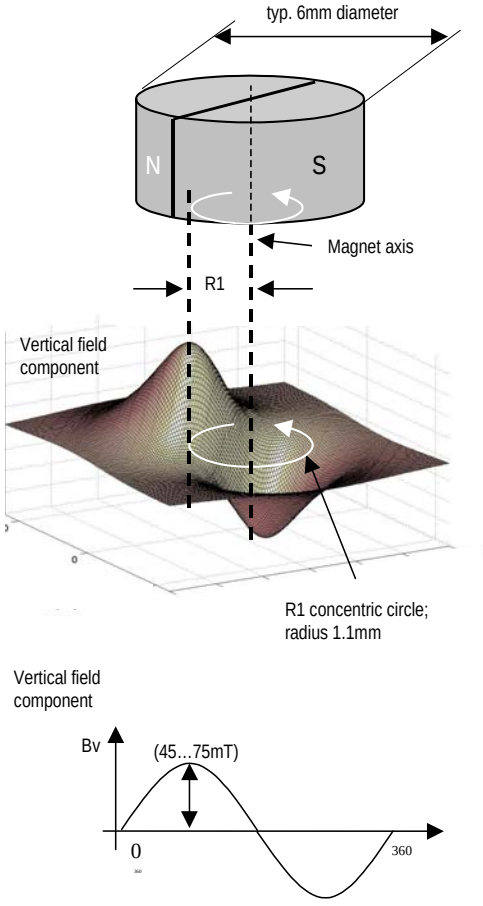


Figure 11: Typical magnet and magnetic field distribution

The magnet's field strength perpendicular to the die surface should be verified using a gauss-meter. The magnetic field B_v at a given distance, along a concentric circle with a radius of 1.1mm (R1), should be in the range of ±45mT...±75mT. (see Figure 11).

9.1 Physical Placement of the Magnet

The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the IC package as shown in Figure 12:

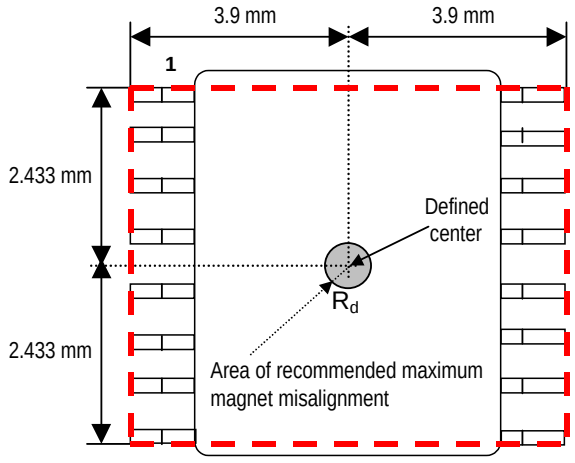


Figure 12: Defined IC center and magnet displacement radius

Magnet Placement:

The magnet's center axis should be aligned within a displacement radius R_d of 0.25mm from the defined center of the IC with reference to the edge of pin #1 (see Figure 12). This radius includes the placement tolerance of the chip within the SSOP-16 package (+/- 0.235mm). The displacement radius R_d is 0.485mm with reference to the center of the chip

The vertical distance should be chosen such that the magnetic field on the die surface is within the specified limits (see Figure 11). The typical distance "z" between the magnet and the package surface is 0.5mm to 1.8mm with the recommended magnet (6mm x 3mm). Larger gaps are possible, as long as the required magnetic field strength stays within the defined limits.

A magnetic field outside the specified range may still produce usable results, but the out-of-range condition will be indicated by MagINCn (pin 1) and MagDECn (pin 2), see 5.5.

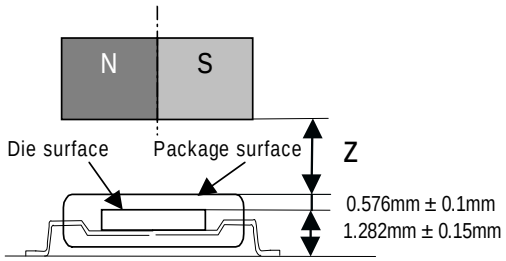


Figure 13: Vertical placement of the magnet

10 Angular Output Tolerances

10.1 Accuracy

Accuracy is defined as the error between measured angle and actual angle. It is influenced by several factors:

- the non-linearity of the analog-digital converters,
- internal gain and mismatch errors,
- non-linearity due to misalignment of the magnet

As a sum of all these errors, the accuracy with centered magnet = $(Err_{max} – Err_{min})/2$ is specified as better than ±0.5 degrees @ 25°C (see Figure 15).

Misalignment of the magnet further reduces the accuracy. Figure 15 shows an example of a 3D-graph displaying non-linearity over XY-misalignment. The center of the square XY-area corresponds to a centered magnet (see dot in the center of the graph). The X- and Y- axis extends to a misalignment of ±1mm in both directions. The total misalignment area of the graph covers a square of 2x2 mm (79x79mil) with a step size of 100µm.

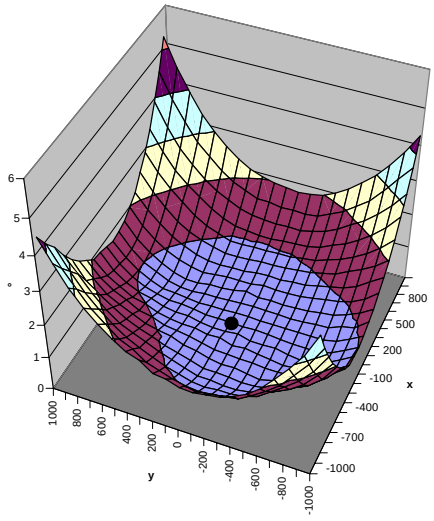


Figure 14: Example of linearity error over XY misalignment

For each misalignment step, the measurement as shown in Figure 15 is repeated and the accuracy

$(Err_{max} – Err_{min})/2$ (e.g. 0.25° in Figure 15) is entered as the Z-axis in the 3D-graph.

The maximum non-linearity error on this example is better than ±1 degree (inner circle) over a misalignment radius of ~0.7mm. For volume production, the placement tolerance of the IC within the package (±0.235mm) must also be taken into account.

The total nonlinearity error over process tolerances, temperature and a misalignment circle radius of 0.25mm is specified better than ±1.4 degrees.

The magnet used for these measurement was a cylindrical NdFeB (Bomatec® BMN-35H) magnet with 6mm diameter and 2.5mm in height.

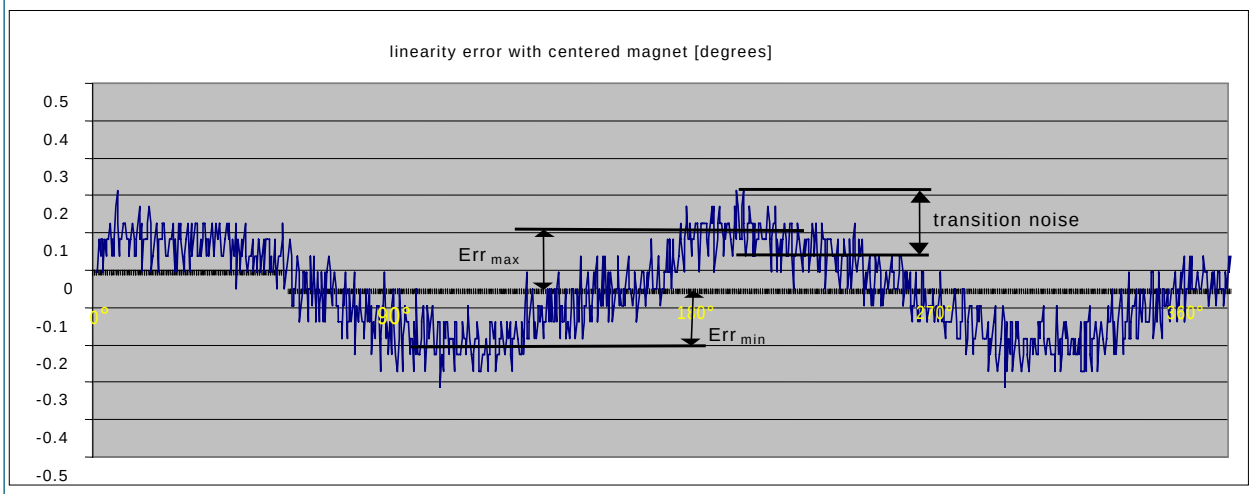


Figure 15: Example of linearity error over 360°

10.2 Transition Noise

Transition noise is defined as the jitter in the transition between two steps.

Due to the nature of the measurement principle (Hall sensors + Preamplifier + ADC), there is always a certain degree of noise involved.

This transition noise voltage results in an angular transition noise at the outputs. It is specified as 0.12 degrees rms (1 sigma)[*1].

This is the repeatability of an indicated angle at a given mechanical position.

The transition noise influences the period, width and phase shift of the output signals A, B and Index:

Parameter	Tolerance (1σ)	Tolerance (3σ)
Index Pulse width	1.406° +/-0.12°	1.406° +/-0.36°
A,B Pulse width	2.813° +/-0.12°	2.813° +/-0.36°
Period	5.625° +/-0.12°	5.625° +/-0.36°
A-B Phase shift	90e° +/-3.8e°	90e° +/-11.5e°

Table 3: Incremental signal tolerances with transition noise

e° = electrical degrees (see Figure 5)

*[*1]: statistically, 1 sigma represents 68.27% of readings, 3 sigma represents 99.73% of readings.*

The algorithm used to generate the incremental outputs guarantees no missing or additional pulses even at high speeds (up to 10,000 rpm and higher)

10.3 High Speed Operation

10.3.1 Sampling Rate

The AS5035 samples the angular value at a rate of 10k samples per second. Consequently, the incremental outputs are updated each 100µs.

At a stationary position of the magnet, this sampling rate creates no additional error.

Incremental encoders are usually required to produce no missing pulses up to several thousand rpm's.

Therefore, the AS5035 has a built-in interpolator, which ensures that there are no missing pulses at the incremental outputs for rotational speeds of up to 10,000rpm.

10.4 Output Delays

Due to the sampling rate of 10kHz, there will be a delay of up to 100µs between the time that the sample is taken until it is converted and available as angular data.
A rotating magnet will therefore cause an angular error caused by the output delay.
This error increases linearly with speed:

$$e_{sampling} = rpm * 6E^{-4}$$

At low speeds this error is small (e.g. <= 0.06° at 100 rpm).

At speeds over 586rpm, the error approaches 0.35°. The maximum error caused by the sampling rate of the ADCs is 0/+100µs. It has a peak of 0.35° at 586 rpm.

At higher speeds the error is reduced due to interpolation and the output delay remains at 200µs as the DSP requires two sampling periods (2x100µs) to synthesize and redistribute any missing pulses.

10.5 Temperature

10.5.1 Magnetic Temperature Coefficient

One of the major benefits of the AS5035 compared to linear Hall sensors is that it is much less sensitive to temperature. While linear Hall sensors require a compensation of the magnet's temperature coefficients, the AS5035 automatically compensates for the varying magnetic field strength over temperature. The magnet's temperature drift does not need to be considered, as the AS5035 operates with magnetic field strengths from ±45...±75mT.

Example:
A NdFeB magnet has a field strength of
75mT @ –40°C and a temperature coefficient of
-0.12% per Kelvin. The temperature change is from
–40° to +125° = 165K.
The magnetic field change is: 165 x -0.12% = -19.8%,
which corresponds to
75mT at –40°C and 60mT at 125°C .

The AS5035 can compensate for this temperature related field strength change automatically, no user adjustment is required.

10.5.2 Accuracy over Temperature

The influence of temperature in the absolute accuracy is very low. While the accuracy is ≤ ±0.5° at room temperature, it may increase to ≤±0.9° due to increasing noise at high temperatures.

10.5.3 Timing Tolerance over Temperature

The internal RC oscillator is factory trimmed to ±5%. Over temperature, this tolerance may increase to ±10%. Generally, the timing tolerance has no influence in the accuracy or resolution of the system, as it is used mainly for internal clock generation.

11 Failure Diagnostics

The AS5035 also offers several diagnostic and failure detection features:

11.1 Magnetic Field Strength Diagnosis

Pins #1 (MagINCn) and #2 (MagDECn) are open-drain outputs and will both be turned on (= low with external pull-up resistor) when the magnetic field is out of range. If only one of the outputs is low, the magnet is either moving towards the chip (MagINCn) or away from the chip (MagDECn).

11.2 Power Supply Failure Detection

11.2.1 MagINCn and MagDECn Pins:

These are open drain outputs and require external pull-up resistors. In normal operation, these pins are high ohmic and the outputs are high (see Table 2). In a failure case, either when the magnetic field is out of range or the power supply is missing, these outputs will become low. To ensure adequate low levels in case of a broken power supply to the AS5035, the pull-up resistors (>10kΩ) must be connected to the positive supply at pin 16 (VDD5V).

11.2.2 Incremental Outputs:

In normal operation, pins A(#3), B(#4) and Index (#6) will never be high at the same time, as Index is only high when A=B=low. However, after a power-on-reset, if VDD is powered up or restarts after a power supply interruption, all three outputs will remain in high state until pin CSn is pulled low (see 5.4.2). If CSn is already tied to VSS during power-up, the incremental outputs will all be high until the internal offset compensation is finished (within t_{PwrUp}).

Another way to detect a power supply loss is by connecting pull-up resistors to the A,B and Index pins at the receiving side (µC, control unit, etc..). If the negative power line to the sensor is interrupted, all three outputs will be pulled high by the external pull-up resistors. This unique state again indicates a failure as it does not occur in normal operation.

12 Electrical Characteristics

12.1 Absolute Maximum Ratings (non operating)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Min	Max	Unit	Note
DC supply voltage at pin VDD5V	VDD5V	-0.3	7	V	
DC supply voltage at pin VDD3V3	VDD3V3		5	V	
Input pin voltage	V_{in}	-0.3	VDD5V +0.3	V	
Input current (latchup immunity)	I_{scr}	-100	100	mA	Norm: JEDEC 78
Electrostatic discharge	ESD	± 2		kV	Norm: MIL 883 E method 3015
Storage temperature	T_{strg}	-55	125	°C	Min – 67°F ; Max +257°F
Body temperature (Lead-free package)	T_{Body}		260	°C	t=20 to 40s, Norm: IPC/JEDEC J-Std-020C Lead finish 100% Sn "matte tin"
Humidity non-condensing	r_H	5	85	%	

12.2 Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Ambient temperature	Tamb	-40		125	°C	-40°F…+257°F
Supply current	Isupp		16	25	mA	
Supply voltage at pin VDD5V Voltage regulator output voltage at pin VDD3V3	VDD5V VDD3V3	4.5 3.0	5.0 3.3	5.5 3.6	V V	5V Operation
Supply voltage at pin VDD5V Supply voltage at pin VDD3V3	VDD5V VDD3V3	3.0 3.0	3.3 3.3	3.6 3.6	V V	3.3V Operation (pin VDD5V and VDD3V3 connected)

12.3 DC Characteristics for Digital Inputs and Outputs

12.3.1 CMOS Schmitt-Trigger Inputs: OTP_CLK, CSn (CSn = internal Pull-up)

Parameter	Symbol	Min	Max	Unit	Note
High level input voltage	V_{IH}	0.7 * VDD5V		V	Normal operation
Low level input voltage	V_{IL}		0.3 * VDD5V	V	
Schmitt-Trigger hysteresis	V_{Ion-} V_{Ioff}	1		V	
Input leakage current	I_{LEAK}	-1	1	µA	CLK only
Pull-up low level input current	I_{iL}	-30	-100	µA	CSn only, VDD5V: 5.0V

12.3.2 CMOS Output Open Drain: MagINCn, MagDECn

Parameter	Symbol	Min	Max	Unit	Note
Low level output voltage	V_{OL}		VSS+0.4	V	
Output current	I_O		4 2	mA	VDD5V: 4.5V VDD5V: 3V
Open drain leakage current	I_{OZ}		1	µA	

12.3.3 CMOS Outputs: A, B, Index, OTP_DO

Parameter	Symbol	Min	Max	Unit	Note
High level output voltage	V_{OH}	VDD5V-0.5		V	
Low level output voltage	V_{OL}		VSS+0.4	V	
Output current	I_O		4 2	mA mA	VDD5V: 4.5V VDD5V: 3V

12.4 Magnetic Input Specification

Two-pole cylindrical diametrically magnetised source:

Parameter	Symbol	Min	Max	Unit	Note
Diameter	d_{mag}	4		mm	Recommended diameter: 6mm
Magnetic input field amplitude	B_{pk}	45	75	mT	Required vertical component of the magnetic field strength on the die's surface, measured along a concentric circle with a radius of 1.1mm
Magnetic offset	B_{off}		± 5	mT	Constant magnetic stray field
Field non-linearity			5	%	Including offset gradient
Input frequency (rotational speed of magnet)	f_{mag_abs}		10	Hz	Absolute mode: 600 rpm @ readout of 1024 positions (see table 6)
	f_{mag_inc}		166	Hz	Incremental mode: no missing pulses at rotational speeds of up to 10,000 rpm (see table 6)
Magnetic field temperature drift	B_{tc}	typ. – 0.035		%/K	Samarium Cobalt ReComa28
Displacement radius	Disp		0.25	mm	Max. offset between defined device center and magnet axis (see Figure 12)

12.5 Electrical System Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
Resolution	LSB		1.406		deg	Degrees / step
	RES			8 64	bit ppr	Channel A and B
Index bit width	$t_{w,Index}$		1.406		deg	= 1 LSB (see Table 3)
Integral non-linearity (optimum)	INL_{opt}			± 0.5	deg	Maximum error with respect to the best line fit. Centered magnet placement without calibration, T_{amb} =25 °C.
Integral non-linearity (optimum)	INL_{temp}			± 0.9	deg	Maximum error with respect to the best line fit. Centered magnet placement without calibration, T_{amb} = -40 to +125°C
Integral non-linearity	INL			± 1.4	deg	Best line fit = (Err_{max} – Err_{min}) / 2 Over displacement tolerance with 6mm diameter magnet, without calibration T_{amb} = -40 to +125°C
Differential non-linearity	DNL			± 0.176	deg	no missing codes
Transition noise	TN			0.12	Deg rms	rms = 1 sigma (see 10.2)
Hysteresis	Hyst		0.704		deg	
Power-on reset thresholds						
On voltage; 300mV typ. hysteresis	V_{on}	1,37	2.2	2.9	V	DC supply voltage 3.3V (VDD3V3)
Off voltage; 300mV typ. hysteresis	V_{off}	1.08	1.9	2.6	V	DC supply voltage 3.3V (VDD3V3)

12.6 Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power-up time	t_{PwrUp}			50	ms	until internal offset compensation is finished
Incremental outputs valid after power-up	$t_{Incremental\ outputs\ valid}$			500	ns	if CSn is high during power up: = Time after t_{PwrUp} from first falling edge of CSn to valid incremental outputs.
						If CSn is low during power up: Incremental outputs are valid as soon as t_{PwrUp} is expired
System propagation delay				200	µs	Calculation over two samples
Sampling rate	f_S	9.5	10	10.5	kHz	Internal sampling rate

12.7 Incremental Output Signal Tolerances

See Table 3 on page 10

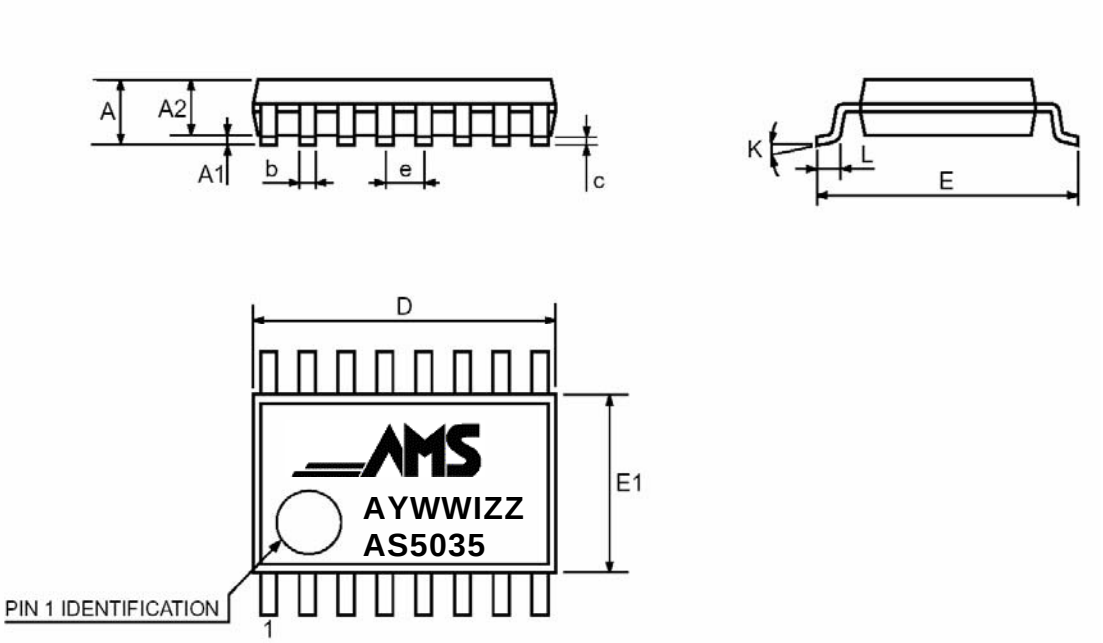
12.8 Programming Conditions

(operating conditions: T_{amb} = -40 to +125°C, VDD5V = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Programming enable time	$t_{Prog\ enable}$	2			µs	Time between rising edge at Prog pin and rising edge of CSn
Write data start	$t_{Data\ in}$	2			µs	
Write data valid	$t_{Data\ in\ valid}$	250			ns	Write data at the rising edge of CLK_{PROG}
Load programming data	$t_{Load\ PROG}$	3			µs	
Rise time of V_{PROG} before CLK_{PROG}	t_{PrgR}	0			µs	
Hold time of V_{PROG} after CLK_{PROG}	t_{PrgH}	0		5	µs	
Write data – programming CLK_{PROG}	CLK_{PROG}			250	kHz	
CLK pulse width	t_{PROG}	1.8	2	2.2	µs	During programming; 16 clock cycles
Hold time of Vprog after programming	$t_{PROG\ finished}$	2			µs	Programmed data is available after next power-on
Programming voltage	V_{PROG}	7.3	7.4	7.5	V	Must be switched off after zapping
Programming voltage off level	$V_{ProgOff}$	0		1	V	Line must be discharged to this level
Programming current	I_{PROG}			130	mA	During programming
Analog read CLK	CLK_{Aread}			100	kHz	Analog readback mode
Programmed zener voltage (log.1)	$V_{programmed}$			100	mV	V_{Ref}-V_{PROG} during analog readback
Unprogrammed zener voltage (log. 0)	$V_{unprogrammed}$	1			V	

13 Package Drawings and Markings

16-Lead Shrink Small Outline Package SSOP-16



Dimensions						
Symbol	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.73	1.86	1.99	.068	.073	.078
A1	0.05	0.13	0.21	.002	.005	.008
A2	1.68	1.73	1.78	.066	.068	.070
b	0.25	0.315	0.38	.010	.012	.015
c	0.09	-	0.20	.004	-	.008
D	6.07	6.20	6.33	.239	.244	.249
E	7.65	7.8	7.9	.301	.307	.311
E1	5.2	5.3	5.38	.205	.209	.212
e	0.65			.0256		
K	0°	-	8°	0°	-	8°
L	0.63	0.75	0.95	.025	.030	.037

Marking: AYWWIZZ

A: Pb-free Identifier

Y: Last Digit of Manufacturing Year

WW: Manufacturing Week

I: Plant Identifier

ZZ: Traceability Code

JEDEC Package Outline Standard: MO - 150 AC

Thermal Resistance $R_{th(j-a)}$:
79.4 K/W in still air, soldered on PCB

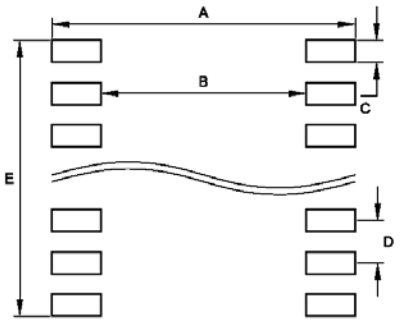
IC's marked with a white dot or the letters "ES" denote Engineering Samples

13.1 Packing Options

Delivery: Tape and Reel (1 reel = 2000 devices)
Tubes (1 box = 100 tubes á 77 devices)

Order # AS5035 for delivery in tubes
Order # AS5035TR for delivery in tape and reel

14 Recommended PCB Footprint:



Recommended Footprint Data		
	mm	inch
A	9.02	0.355
B	6.16	0.242
C	0.46	0.018
D	0.65	0.025
E	5.01	0.197

15 Revision History

Revision	Date	Description
1.2	Mar. 27, 2006	Added Prog. Conditions 12.8, added Figure 8.
1.1	Sep. 27, 2005	Update Table 3, thermal resistance of IC package and ordering information
1.0	May 6, 2005	Initial revision

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