A Rapid Serial Timing Acquisition Algorithm for Hybrid DS/FFH Packet Radio Communication

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In this article, we propose a simple, reliable, and rapid serial timing acquisition algorithm for hybrid direct-sequence and fast frequency-hopping packet radio communication systems. The proposed algorithm is designed in both the frequency domain of frequency hopping and the pseudonoise code domain of direct sequence. We provide the performance analysis for our proposed algorithm and confirm its exactness by simulation. Compared with the conventional serial search algorithm, the proposed algorithm shows much faster acquisition time while obtaining similar performance.

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I. INTRODUCTION

Spread spectrum systems such as direct-sequence (DS) and frequency-hopping (FH) are widely used in civil and military wireless communications because of their excellent properties, including antijamming, multiple access, and low probability of intercept. Hybrid DS/FH spread spectrum systems combine the advantages of both DS and FH spread spectrum systems by spreading DS signals over a number of frequencies, and these hybrid systems have gained much attention in many areas of communication [1]–[3]. Fast FH (FFH) systems, which the carrier frequency changes multiple times during the modulation of one symbol, provide extra security over slow FH (SFH) systems owing to their inherent fast hopping rate [4]. FFH systems are also becoming more attractive for commercial applications as well as military communication because of their excellent frequency diversity property and the development of a fast hopping speed direct digital synthesizer [2].

Synchronization is a critical part of all the spread spectrum systems and is the key factor affecting the performance of the system [5]. Synchronization is usually accomplished in two stages: acquisition and tracking. Acquisition is necessary in order to obtain a coarse alignment between the locally generated sequence at the receiver and the sequence of the arriving signal. Tracking is the process to achieve fine alignment within the desired synchronization error boundary. Especially, acquisition is almost always the dominant issue and the most expensive component of a complete spread spectrum system [6].

Acquisition of an FH system can be implemented by serial acquisition or parallel acquisition[1] schemes [7], [8]. The serial acquisition scheme is relatively simple to implement, but it takes a long time to achieve acquisition. In contrast, the parallel acquisition scheme can achieve acquisition more quickly, but the complexity of implementation is quite high since it requires synthesizers, filters, and correlators as the number of hopping frequencies used for acquisition, which restricts real-time implementation in practical systems [7], [9]–[11].

The increase in data traffic motivates the use of random-access packet data communication, which is used in various communication systems such as tactical military networks and wireless local area networks [12], [13]. In packet radio communication, each packet consists of a short preamble with predetermined length to aid in acquisition followed by data payload. Note that, if the receiver is unable to detect the preamble, the data payload is lost. Therefore, more reliable and accurate acquisition algorithm is required for packet radio communication. Since the preamble time for acquisition is fixed, it is important to estimate the end timing of the acquisition stage and to activate the tracking stage at the correct timing for successful synchronization.

Acquisition of hybrid DS/FFH systems needs to be achieved in both the frequency domain of FH and the

[1]The parallel acquisition is often implemented by employing a matched filter.

pseudonoise (PN) code domain of DS. Acquisition schemes for each of DS and FH system have been presented in the literature [7]–[11], [14]–[19]. However, acquisition schemes for hybrid DS/FH systems have been relatively unknown [20], and most of them are parallel-based acquisition schemes [21]–[24]. Although several serial acquisition schemes were presented, these are not suitable to packet radio communications [25], [26]. The serial acquisition scheme for hybrid DS/SFH packet radio communications is presented [5], but it is assumed that both the preamble and data payload are transmitted over one hop of SFH, which is similar to the DS system and cannot be applied to the hybrid DS/FFH system. To the best of our knowledge, the serial acquisition algorithm for hybrid DS/FFH packet radio communication systems has not been presented to date in the open literature.

In this article, we propose a novel serial timing acquisition algorithm, which has lower complexity than the parallel acquisition algorithm, for hybrid DS/FFH packet radio communication systems. We design the acquisition algorithm in both the frequency domain of FH and the PN code domain of DS. In the frequency domain, the proposed algorithm is designed to accomplish reliable acquisition under the jamming or/and channel impairment environment. In the PN code domain, a cyclic shift code is employed as the PN code, which is the core of the proposed algorithm. The proposed algorithm can be implemented using only one correlator by applying a cyclic shift code and can achieve rapid acquisition, since it does not need any additional verification logic. We provide the performance analysis for our proposed algorithm and confirm its exactness by simulation. The performance of the proposed algorithm is also analyzed by comparison with the conventional serial and parallel algorithms. Although generally ignored in the literature, the dead time that cannot transmit and receive the signal for switching to a next hopping frequency exists in practical FH systems [27]. In FFH systems, the dead time takes a significant fraction of one-hop duration due to the fast hopping rate, which can greatly affect acquisition time and probability of false alarm. Therefore, all theoretical analysis and simulations in this article are carried out, including dead time.

The rest of this article is organized as follows. Section II describes the hybrid DS/FFH system model, including the packet structure and the demodulation process. Section III describes our proposed serial acquisition algorithm in both the frequency domain and the PN code domain. Section IV provides the performance analysis, including simulation results for our acquisition algorithm. Finally, Section V concludes this article.

II. SYSTEM MODEL

A hybrid DS/FFH signal can be modeled as fast hopping DS signals according to a specific FH pattern. The transmitted symbol over one hop is spread by the PN code of DS. The PN code and the FH pattern are known *a priori* at the transmitter and the receiver. In the practical system

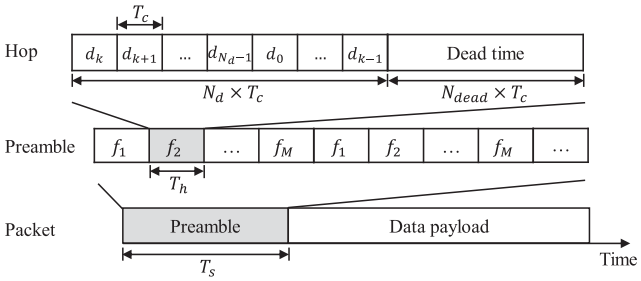


Fig. 1. Packet structure of the hybrid DS/FFH system.

design, the PN code and the FH pattern are changed at regular intervals. Note that the PN code can be generated by maximum length feedback shift register, which is called as *m*-sequence. We assume that each chip of *m*-sequence is modulated with binary phase-shift keying (BPSK). The preamble is transmitted as the hopping frequency sequence of $[f_1, f_2, \ldots, f_M]$, where M is the number of hopping frequencies used for acquisition. Then, the transmitted signal, $s(t)$, over M hopping frequencies can be written as

$$s(t) = \sum_{j=0}^{M-1} \sqrt{E_c} \sum_{i=0}^{N_d-1} b_j d_i g_c(t - iT_c - jT_h) \times \cos\left(2\pi f_{(j+1)}\left(t - jT_h\right)\right) \quad (1)$$

where E_c is the chip power, $g_c(t)$ is the chip shaping pulse, which is Nyquist pulse such as Raised Cosine and Better Than Raised Cosine pulse to eliminate the interchip interference (ICI) [28], and b_j is the transmitted symbol for one hop. In (1), N_d is the number of chips in *m*-sequence and d_i is the ith chip of the *m*-sequence with $d_i \in \{-1, 1\}$. We use a cyclic shifted *m*-sequence, which can be expressed as

$$\boldsymbol{d}_k = [d_k, d_{k+1}, \ldots, d_{N_d-1}, d_0, \ldots, d_{k-1}] \quad (2)$$

where k denotes the number of cyclically shifted chips in *m*-sequence. In the conventional method, only the *m*-sequence without cyclic shift denoted as $\boldsymbol{d}_0$ is used [6], [29]. Note that, since b_j is known *a priori* at the transmitter and the receiver in the acquisition stage and is eventually spread by *m*-sequence to obtain DS effect, we assume that b_j is "1" value for the whole acquisition time [26]. In (1), T_c is the chip duration and T_h is the hop duration. Since each hop consists of the transmitted symbol spread by *m*-sequence and the dead time, T_h can be expressed as

$$T_h = (N_d + N_{\text{dead}})T_c \quad (3)$$

where N_{dead} is the number of chips that corresponds to the dead time. The packet structure of the hybrid DS/FFH system is shown in Fig. 1, where T_s is a fixed acquisition time.

The major application of the hybrid DS/FFH spread spectrum is a tactical military network such as Link-16, which is strictly line-of-sight (LOS) communication system [30]. In LOS communication, large-scale fading is dominant, which can be compensated by power control [31]. Thus, we assume an additive white Gaussian noise (AWGN) channel in this article and can write the received signal with

coherent detection as

$$r(t) = s(t-\tau) + n(t) \tag{4}$$

where τ is a time delay of the signal and $n(t)$ is the AWGN with power spectral density $N_0/2$.

The sampling period at the receiver is T_c. In the practical system, the sampling is carried out with oversampling of T_c/N, where N indicates the oversampling rate. The error of sampling position causes ICI, which degrades the system performance even if the ICI free pulse is employed as the chip shaping pulse [32]. However, the effect of sampling error can be reduced by increasing the oversampling rate, N [12], [21], [33]. In addition, since the locking range of the tracking loop is usually $T_c/2$, a successful acquisition can be declared if the sampling error in the acquisition stage is less than $T_c/2$ [17]. Therefore, we assume that the sampling can be accomplished at the optimum sampling position in this article.

The received preamble after sampling for T_h can be expressed as

$$\boldsymbol{r}_k = \sqrt{E_c}\boldsymbol{d}_k + \boldsymbol{n} = [r_k, r_{k+1}, \ldots, r_{N_d-1}, r_0, \ldots, r_{k-1}]. \tag{5}$$

Then, we obtain $\tilde{\boldsymbol{d}}_k$ after hard decision of $\boldsymbol{r}_k$ in (5) given as

$$\tilde{\boldsymbol{d}}_k = [\tilde{d}_k, \tilde{d}_{k+1}, \ldots, \tilde{d}_{N_d-1}, \tilde{d}_0, \ldots, \tilde{d}_{k-1}], \quad \tilde{d}_i \in \{-1, 1\} \tag{6}$$

where $\tilde{d}_i$ is the decision output of d_i.

III. PROPOSED ALGORITHM DESCRIPTION

A. Acquisition in Frequency Domain

In an FH system, the preamble consists of multiple preamble pulses, and each preamble pulse is transmitted over one hop [11]. In a practical scenario, the jamming or/and channel impairment on certain frequencies needs to be considered. In that case, it is desired that the receiver carries out the acquisition process utilizing the preamble pulses of various hopping frequencies for reliable acquisition. The proposed algorithm is designed to achieve acquisition using the preamble pulses of all the M hopping frequencies.

The preamble is transmitted as the hopping frequency sequence of $[f_1, f_2, \ldots, f_M]$ and is repeated $(M+1)$ times. That is, the preamble is transmitted over $M(M+1)$ hops. Let us define $\mathcal{F}^{(x)}$ as $[F_1^{(x)}, F_2^{(x)}, \ldots, F_M^{(x)}]$, where x denotes the xth transmission of $(M+1)$ repetition transmission with $x \in \{1, 2, \ldots, M+1\}$ and $F_j^{(x)}$ indicates the xth transmitted preamble pulse over the hopping frequency j for T_h. Then, we can express the whole preamble pulse for acquisition as

$$[\mathcal{F}^{(1)}, \ldots, \mathcal{F}^{(M+1)}] = [[F_1^{(1)}, F_2^{(1)}, \ldots, F_M^{(1)}], \ldots, [F_1^{(M+1)}, F_2^{(M+1)}, \ldots, F_M^{(M+1)}]]. \tag{7}$$

Note that the acquisition time is fixed in the packet radio communication. Since the preamble is transmitted over $M(M+1)$ hops, the acquisition time, T_s, can be represented using (3) as

$$T_s = M(M+1)T_h = M(M+1)(N_d + N_{\text{dead}})T_c. \tag{8}$$

The receiver changes the frequency of its synthesizer every $(M+1)T_h$ in the sequence of $[f_1, f_2, \ldots, f_M]$. In other words, the hop duration of the receiver is $(M+1)$ times longer than the hop duration of the transmitter. Designing such FH structures of the transmitter and the receiver, we can reliably receive the M preamble pulses whose frequencies are different from each other.

As a simple example, Fig. 2 shows the proposed algorithm in the frequency domain for $M = 3$. A total of 12 preamble pulses are transmitted as the frequency sequence of $[f_1, f_2, f_3, f_1, f_2, f_3, f_1, f_2, f_3, f_1, f_2, f_3]$, which means the transmission of $[\mathcal{F}^{(1)}, \mathcal{F}^{(2)}, \mathcal{F}^{(3)}, \mathcal{F}^{(4)}]$. The receiver changes the frequency of its synthesizer every $4T_h$ in the sequence of $[f_1, f_2, f_3]$. In the general assumption that there is no prior information on the reception timing of the preamble, the receiver processes different preamble pulses according to the reception timing. Since the receiver handles M hopping frequencies, M cases occur depending on the frequency of the preamble pulse that the receiver first processes. For f_1, one case is added because there are two cases where the first processed preamble pulse at the receiver is $F_1^{(1)}$ or $F_1^{(2)}$. In this example of $M = 3$, we have four cases (Cases 1–4) according to the reception timing of the preamble, as shown in Fig. 2. The receiver processes different preamble pulses for each case because the preamble pulse corresponding to the frequency of the receiver can be processed. The first processed preamble pulses of Cases 1–4 are $F_1^{(1)}$, $F_2^{(1)}$, $F_3^{(1)}$, and $F_1^{(2)}$, respectively. We know that the receiver can reliably process the preamble pulses of three different hopping frequencies in all the cases of Fig. 2 regardless of the reception timing. We ignore the received signal over two hopping frequencies due to the degradation of correlation performance by the dead time. In this article, we use the simplest case of $M = 3$ as an example to describe our proposed algorithm.

B. Acquisition in PN Code Domain

Once the acquisition in the frequency domain is accomplished, we need to synchronize the PN code for DS despreading. We consider the correlation-based PN code synchronization, where $\tilde{\boldsymbol{d}}_k$ in (6) is correlated with m-sequence locally generated at the receiver. If the correlation value is above the threshold value, the detection of a preamble pulse is declared.

An important consideration here is that, even if the detection of a preamble pulse is obtained, we cannot acquire the current timing because the current timing depends on the reception timing of the preamble. For example, in Case 1 of Fig. 2, when the first processed preamble pulse $F_1^{(1)}$ is missed due to channel impairment and the second processed preamble pulse $F_2^{(2)}$ is detected, we are not able to determine whether the detection occurs at $F_2^{(2)}$ in Case 1 or $F_2^{(1)}$ in Case 2 because only the hopping frequency j of $F_j^{(x)}$ is known at the receiver. Note that $F_2^{(2)}$ in Case 1 and

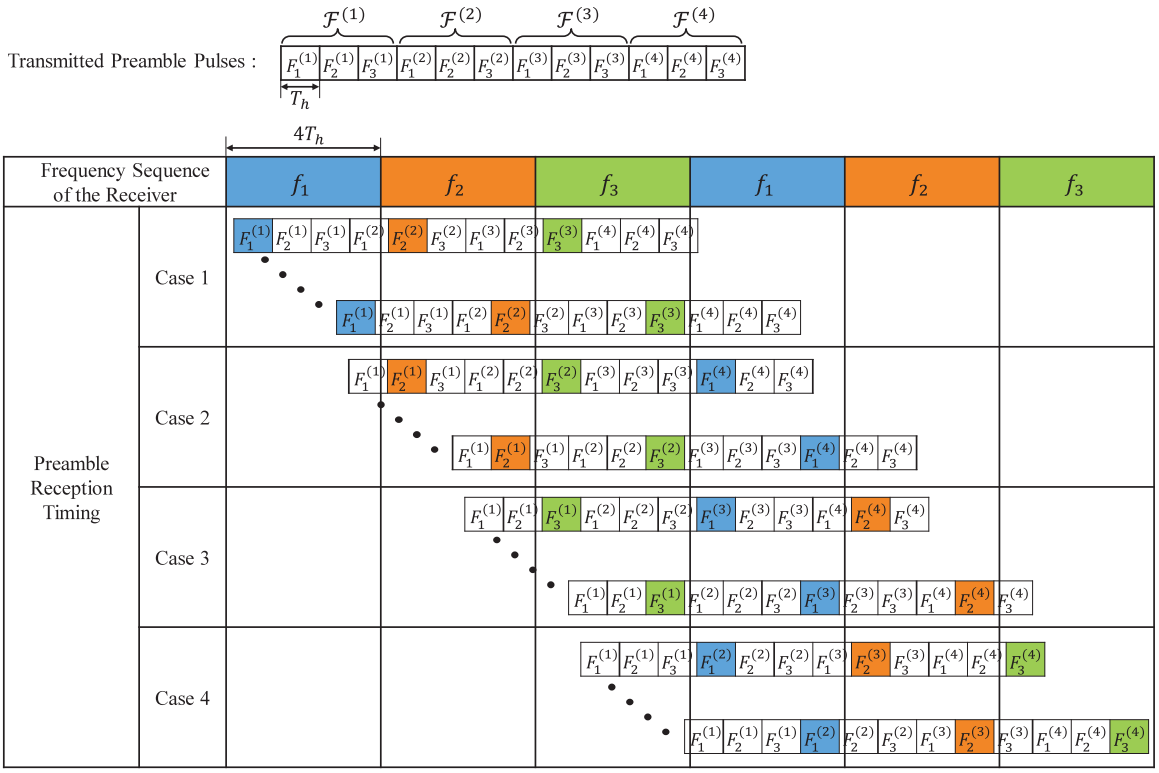


Fig. 2. Proposed acquisition algorithm in the frequency domain ($M = 3$). The preamble pulses processed by the receiver change according to the reception timing of the preamble, which is divided into four cases (Cases 1–4).

$F_2^{(1)}$ in Case 2 are the fifth and second preamble pulse of the transmitted 12 preamble pulses, respectively. Since the current timing is unknown, it is not possible to accurately estimate the end timing of the preamble. Moreover, since Cases 1 and 4 in Fig. 2 are the same from the receiver side, they cannot be distinguished even for the good channel condition.

This problem can be solved by adding an additional signal for verification after acquisition, but in this case, the acquisition time is increased, and the probabilities of detection and false alarm in an additional verification logic need to be considered. We may think of another method to transmit a different sequence for each $\mathcal{F}^{(x)}$, but the hardware complexity is increased in this case because the receiver requires $(M + 1)$ correlators and performs $(M + 1)$ correlation process simultaneously. Moreover, false alarm occurs in $(M + 1)$ correlators, which results in the increase of the probability of false alarm.

We here point out that the core of our proposed algorithm is to accurately estimate the end timing of the acquisition stage with only one correlator using a cyclic shift code of m-sequence. This method does not increase acquisition time because no additional verification logic is required. The detailed description of our proposed algorithm is as follows.

A different cyclic shifted m-sequence is transmitted for each $\mathcal{F}^{(x)}$. In other words, the transmitted m-sequence $\boldsymbol{d}_k$ in (2) changes according to x of $\mathcal{F}^{(x)}$. Table I shows the m-sequence of $\mathcal{F}^{(x)}$ depending on M, where N_s denotes the maximum cyclic shift. For example of $M = 3$, we use $[\boldsymbol{d}_0, \boldsymbol{d}_1, \boldsymbol{d}_1, \boldsymbol{d}_0]$ for preamble pulses of

TABLE I
m-Sequence of $\mathcal{F}^{(x)}$ Depending on M

M	N_s [Max. Cyclic shift]	m-sequence of $\mathcal{F}^{(x)}$
Odd	$\frac{M^2-1}{8}$	$[\mathcal{F}^{(1)}, F^{(2)}, \ldots, \mathcal{F}^{(M+1)}]$ $= [\boldsymbol{d}_0, \ldots, \boldsymbol{d}_{N_s-6}, \boldsymbol{d}_{N_s-3}, \boldsymbol{d}_{N_s-1}, \boldsymbol{d}_{N_s}, \boldsymbol{d}_{N_s}, \boldsymbol{d}_{N_s-1}, \boldsymbol{d}_{N_s-3}, \boldsymbol{d}_{N_s-6}, \ldots, \boldsymbol{d}_0]$
Even	$\frac{M(M+2)}{8}$	$[\mathcal{F}^{(1)}, F^{(2)}, \ldots, \mathcal{F}^{(M+1)}]$ $= [\boldsymbol{d}_0, \ldots, \boldsymbol{d}_{N_s-6}, \boldsymbol{d}_{N_s-3}, \boldsymbol{d}_{N_s-1}, \boldsymbol{d}_{N_s}, \boldsymbol{d}_{N_s-1}, \boldsymbol{d}_{N_s-3}, \boldsymbol{d}_{N_s-6}, \ldots, \boldsymbol{d}_0]$

$[\mathcal{F}^{(1)}, \mathcal{F}^{(2)}, \mathcal{F}^{(3)}, \mathcal{F}^{(4)}]$. The principle of the cyclic shift is to make the shift difference between adjacent $\mathcal{F}^{(x)}$s unique. For $M = 3$, since the m-sequence of $\mathcal{F}^{(1)}$ and $\mathcal{F}^{(2)}$ is $\boldsymbol{d}_0$ and $\boldsymbol{d}_1$, respectively, the shift difference is -1. In the same way, the shift difference of $\mathcal{F}^{(2)}$ and $\mathcal{F}^{(3)}$ is 0 and the shift difference of $\mathcal{F}^{(3)}$ and $\mathcal{F}^{(4)}$ is $+1$. Therefore, the shift differences between adjacent $\mathcal{F}^{(x)}$s are all different. This shift difference is reflected in the detection timing of a preamble pulse by the correlation process at the receiver, and we can use this to estimate the current timing.

Note that m-sequence locally generated at the receiver is modified from $\boldsymbol{d}_0$ in order to perform the correlation process, including the cyclic shifted chips of $\boldsymbol{d}_k$. We modify the m-sequence by adding N_s cyclic shifted chips from d_0 to d_{N_s-1} in $\boldsymbol{d}_0$, which can be written as

$$\boldsymbol{W} = [\boldsymbol{d}_0, d_0, d_1, \ldots, d_{N_s-1}]. \tag{9}$$

We show the correlation process at the receiver in the case of $M = 3$ and $N_d = 31$ for an example, as shown in Fig. 3. The received m-sequence for $[\mathcal{F}^{(1)}, \mathcal{F}^{(2)}, \mathcal{F}^{(3)}, \mathcal{F}^{(4)}]$

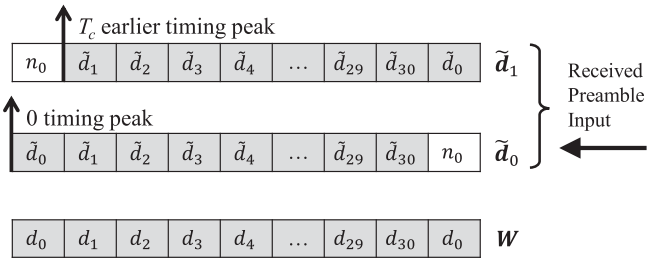


Fig. 3. Correlation process of the proposed algorithm ($M = 3$ and $N_d = 31$).

TABLE II
Acquisition LUT ($M = 3$, $N_d = 31$, and $N_{\text{dead}} = 33$)

Case	Prior Frequency	Posterior Frequency	Timing Difference [chip]	Current Timing [chip]
1	f_1	f_2	255	286
	f_1	f_3	511	542
	f_2	f_3	256	542
2	f_2	f_3	255	350
	f_2	f_1	512	607
	f_3	f_1	257	607
3	f_3	f_1	255	414
	f_3	f_2	512	671
	f_1	f_2	257	671
4	f_1	f_2	256	478
	f_1	f_3	513	735
	f_2	f_3	257	735

is $[\tilde{\boldsymbol{d}}_0, \tilde{\boldsymbol{d}}_1, \tilde{\boldsymbol{d}}_1, \tilde{\boldsymbol{d}}_0]$ as shown in Table I. In Fig. 3, the received $\tilde{d}_i$ in (6) is entered in the shift register every sampling period T_c, which is correlated with $\boldsymbol{W}$. The correlation peak of $\tilde{\boldsymbol{d}}_1$ occurs at T_c earlier in time compared with that of $\tilde{\boldsymbol{d}}_0$ as shown in Fig. 3. From the correlation process in Fig. 3, we know that the detection of $\boldsymbol{d}_k$ occurs at kT_c earlier in time than that of $\boldsymbol{d}_0$.

In the correlation between $\boldsymbol{W}$ and $\tilde{\boldsymbol{d}}_k$, the length of $\boldsymbol{W}$ is N_s chips longer than that of $\tilde{\boldsymbol{d}}_k$. Therefore, $\boldsymbol{W}$ is actually correlated with $\hat{\tilde{\boldsymbol{d}}}_k$, where $\hat{\tilde{\boldsymbol{d}}}_k$ is the vector that adds N_s elements to $\tilde{\boldsymbol{d}}_k$. Since the values of N_s elements are corrupted by AWGN, $\hat{\tilde{\boldsymbol{d}}}_k$ can be represented as

$$\hat{\tilde{\boldsymbol{d}}}_k = [[n_0, \ldots, n_{k-1}], [\tilde{\boldsymbol{d}}_k], [n_k, \ldots, n_{N_s-1}]]. \tag{10}$$

Then, the correlation value C between $\boldsymbol{W}$ and $\hat{\tilde{\boldsymbol{d}}}_k$ can be written as

$$C = \hat{\tilde{\boldsymbol{d}}}_k \boldsymbol{W}^T. \tag{11}$$

If C in (11) is greater than or equal to the threshold value, the receiver declares a pulse detection.

We obtain the current timing using the information of two detected preamble pulses and a lookup table (LUT). If two pulses are detected and the information of two detected pulses is in the LUT, the current timing can be obtained and the receiver declares the acquisition. Note that the LUT is determined depending on M, N_d, and N_{dead}. As an example for $M = 3$, $N_d = 31$, and $N_{\text{dead}} = 33$, we can make LUT as shown in Table II. Each case represents the reception timing of the preamble, which is the same as the case in Fig. 2. In Table II, we express the frequency of the prior detected preamble pulse and posterior detected preamble pulse as the prior frequency and posterior frequency, respectively. Timing difference is the difference of detection timing of two detected preamble pulses. The current timing indicates the timing at which acquisition is declared, which is the detection timing of the posterior detected preamble pulse. Note that in the LUT, the time information such as timing difference and current timing is expressed as the number of chips corresponding to the time. For example, T_s in (8) is represented as $M(M+1)(N_d + N_{\text{dead}})$.

The LUT for this example is obtained by the following calculation. When the prior frequency is f_1 and the posterior frequency is f_2 in Case 1, the time between two detected preamble pulses is $4T_h$, as shown in Fig. 2, and the corresponding timing difference is originally $4(N_d + N_{\text{dead}})$ chips. However, the preamble pulse of posterior frequency f_2, which corresponds to $\mathcal{F}^{(2)}$, is detected at one chip earlier timing because the m-sequence of the preamble pulse is $\boldsymbol{d}_1$. Therefore, the timing difference becomes $4(N_d + N_{\text{dead}}) - 1 = 255$ chips. The current timing, which is the detection timing of posterior frequency f_2, is $4(N_d + N_{\text{dead}}) + N_d - 1 = 286$ chips. The remainder of LUT can be calculated in the same way.

When the receiver detects the pulses of f_2 and f_3 sequentially without the cyclic shift code, it is not feasible to determine whether the detected pulses are $F_2^{(2)}$ and $F_3^{(3)}$ of Case 1 or $F_2^{(1)}$ and $F_3^{(2)}$ of Case 2 or $F_2^{(3)}$ and $F_3^{(4)}$ of Case 4. However, with the cyclic shift code, we can distinguish them according to whether the timing difference is 256 (Case 1) or 255 (Case 2) or 257 (Case 4), as shown in Table II. If we obtain the prior frequency, posterior frequency, and detection timing from two detected pulses, we can acquire the current timing using LUT. Then, we can estimate exactly the end timing of the acquisition stage because the current timing is known and the acquisition time is fixed. Once the current timing is obtained, the receiver increases the current timing by one every T_c period. If the current timing reaches $M(M+1)(N_d + N_{\text{dead}})$ corresponding to T_s in (8), the acquisition stage ends and the tracking stage follows. We summarize the proposed acquisition algorithm in Fig. 4, where the clock is the local timing of the receiver and is used to calculate the timing difference between two detected pulses.

IV. PERFORMANCE ANALYSIS

We consider the probability of detection, P_{d}, and the probability of false alarm, P_{fa}, for the performance of the proposed acquisition algorithm. Note that, in the packet radio communication system, P_{d} and P_{fa} for a fixed acquisition time rather than the mean acquisition time are often used as the acquisition performance metrics [8], [14], [15].

A. Probability of Detection

Note that P_{d} is the probability of obtaining the correct current timing by detecting the preamble for the acquisition time. In the proposed acquisition algorithm, the receiver can process M preamble pulses for T_s and needs to detect

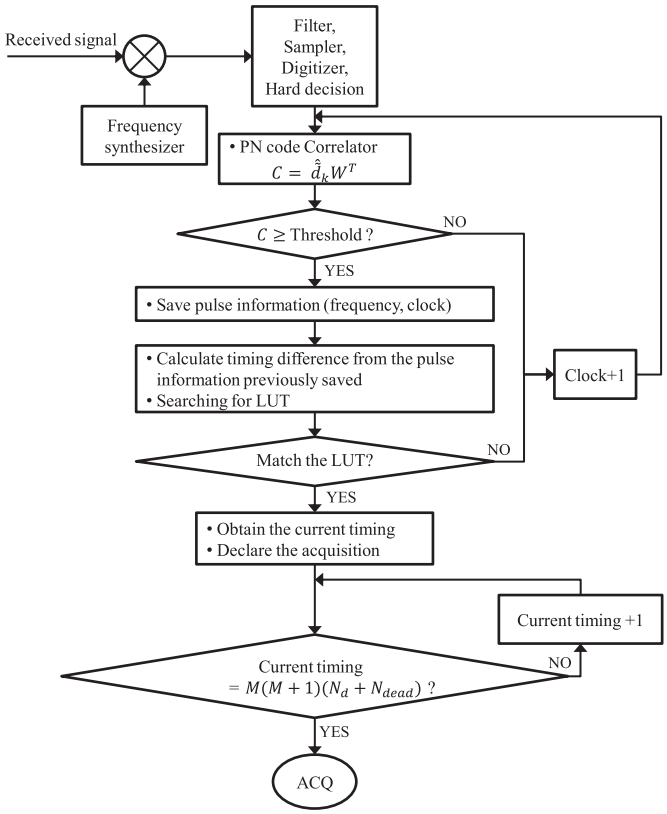


Fig. 4. Flowchart of the proposed acquisition algorithm at the receiver.

at least two pulses of the M preamble pulses for successful acquisition. Therefore, P_{d} can be represented as [17], [34]

$$P_{\mathrm{d}} = \sum_{k=2}^{M} \binom{M}{k} (P_{\mathrm{d},1})^k (1 - P_{\mathrm{d},1})^{M-k} \tag{12}$$

where $\binom{M}{k}$ denotes the binomial coefficient. In (12), $P_{\mathrm{d},1}$ is the detection probability for one preamble pulse and can be expressed as the probability that C between $\boldsymbol{W}$ and $\hat{\hat{\boldsymbol{d}}}_k$ in (11) is greater than or equal to the threshold value, Γ. Note that $\hat{\hat{\boldsymbol{d}}}_k$ comprises N_d chips of m-sequence and N_s chips of noise, as shown in (10). The error probability of N_d chips can be represented as the bit error rate for BPSK under the AWGN channel, and the error probability of N_s chips is 1/2. Let us denote the maximum number of error chips satisfying $C \geq \Gamma$ as $e_{\max}$, which can be written as

$$e_{\max} = \left\lfloor \frac{N_d + N_s - \Gamma}{2} \right\rfloor. \tag{13}$$

Denoting the number of matching chips among N_s chips as N_c, we have the number of error chips as $N_s - N_c$. Since $N_s - N_c$ errors have already occurred, the maximum number of error chips satisfying $C \geq \Gamma$ in the N_d chips of m-sequence becomes $e_{\max} - (N_s - N_c)$. Therefore, $P_{\mathrm{d},1}$ can be calculated as the probability that the number of errors in m-sequence is less than or equal to $e_{\max} - N_s + N_c$ given as [34]

$$P_{\mathrm{d},1} = \sum_{N_c=0}^{N_s} \binom{N_s}{N_c} \left(\frac{1}{2}\right)^{N_s} \sum_{k=0}^{e_{\max}-N_s+N_c} \binom{N_d}{k} (P_e)^k (1 - P_e)^{N_d-k} \tag{14}$$

where P_e is the bit error rate for BPSK under the AWGN channel given by $P_e = \frac{1}{2}\mathrm{erfc}(\sqrt{\frac{E_c}{N_0}})$ [35]. The complementary error function, $\mathrm{erfc}(x)$, is defined by $\mathrm{erfc}(x) = \frac{2}{\sqrt{\pi}} \int_x^\infty e^{-t^2} dt$ [35].

B. Probability of False Alarm

The false alarm occurs when two noise pulses instead of preamble pulses are detected and the frequencies and timing difference of the two detections are in LUT. Therefore, we only need to consider specific detection timings that satisfy the timing difference of LUT. We first calculate P'_{fa}, the probability of false alarm based on a specific chip within one hop of the receiver. It means that two different detections triggering a false alarm occur at a specific chip and a chip satisfying the timing difference of LUT from the specific chip. To derive P'_{fa}, we define $P_{\mathrm{fa},N}$ as the probability of detecting two or more pulses among N noise pulses. Then, we can express $P_{\mathrm{fa},N}$ as [34]

$$P_{\mathrm{fa},N} = \sum_{k=2}^{N} \binom{N}{k} (P_{\mathrm{fa},1})^k (1 - P_{\mathrm{fa},1})^{N-k} \tag{15}$$

where $P_{\mathrm{fa},1}$ is the detection probability for one noise pulse. Because the detection for one pulse is declared when there are no more than $e_{\max}$ errors in $N_d + N_s$ chips, $P_{\mathrm{fa},1}$ can be represented as [34]

$$P_{\mathrm{fa},1} = \sum_{k=N_d+N_s-e_{\max}}^{N_d+N_s} \binom{N_d + N_s}{k} \left(\frac{1}{2}\right)^{N_d+N_s}. \tag{16}$$

We start the calculation of P'_{fa} for $M = 3$ and generalize it for arbitrary M. For $M = 3$, the receiver processes three frequencies for T_s, and it can be divided into three cases of $[f_1, f_2, f_3]$, $[f_2, f_3, f_1]$, and $[f_3, f_1, f_2]$ depending on the frequency sequence of the receiver. Therefore, if we obtain P'_{fa} for each case, we can obtain the final P'_{fa} by calculating the average value.

Fig. 5 shows the possible false alarms in the LUT of $M = 3$ depending on the frequency sequence of the receiver for T_s. Since we only consider the specific detection timings satisfying the timing difference of the LUT, the timing difference is no longer the condition that triggers a false alarm, and the timing difference can be removed in the LUT. Note that, if the timing difference is removed in the LUT, Case $(M + 1)$ is always equal to Case 1, as shown in Fig. 5. When the receiver processes the frequencies of $[f_1, f_2, f_3]$, the eight false alarms can occur in the LUT, as shown in Fig. 5, because the frequency sequence of $[f_2, f_1]$, $[f_3, f_1]$, and $[f_3, f_2]$ cannot be detected. In Cases 1 and 4 of the LUT, P'_{fa} is the probability that two or more among three pulses of f_1, f_2, and f_3 are detected and is mapped to $P_{\mathrm{fa},3}$ in (15). In contrast, P'_{fa} in Cases 2 and 3 of

Frequency sequences of the receiver for T_s

① $[f_1, f_2, f_3]$		
Case	Prior Frequency	Posterior Frequency
1	f_1	f_2
	f_1	f_3
	f_2	f_3
2	f_2	f_3
	f_2	f_1
	f_3	f_1
3	f_3	f_1
	f_3	f_2
	f_1	f_2
4	f_1	f_2
	f_1	f_3
	f_2	f_3

② $[f_2, f_3, f_1]$		
Case	Prior Frequency	Posterior Frequency
1	f_1	f_2
	f_1	f_3
	f_2	f_3
2	f_2	f_3
	f_2	f_1
	f_3	f_1
3	f_3	f_1
	f_3	f_2
	f_1	f_2
4	f_1	f_2
	f_1	f_3
	f_2	f_3

③ $[f_3, f_1, f_2]$		
Case	Prior Frequency	Posterior Frequency
1	f_1	f_2
	f_1	f_3
	f_2	f_3
2	f_2	f_3
	f_2	f_1
	f_3	f_1
3	f_3	f_1
	f_3	f_2
	f_1	f_2
4	f_1	f_2
	f_1	f_3
	f_2	f_3

: Possible false alarms in LUT of $M = 3$

Fig. 5. Possible false alarms in the LUT of $M = 3$ depending on the frequency sequence of the receiver for T_s.

the LUT is mapped to $P_{\text{fa},2}$ in (15) as the probability that all of two pulses are detected. That is, when the receiver processes frequencies of $[f_1, f_2, f_3]$, P'_{fa} is calculated as $2P_{\text{fa},3} + 2P_{\text{fa},2}$. In the same way, when the receiver processes the frequencies of $[f_2, f_3, f_1]$ and $[f_3, f_1, f_2]$, P'_{fa} becomes $P_{\text{fa},3} + 3P_{\text{fa},2}$ in both cases, as shown in Fig. 5. Since three cases are independent, P'_{fa} for $M = 3$ is the arithmetic mean, that is, $(4P_{\text{fa},3} + 8P_{\text{fa},2})/3$. It is necessary to understand some key characteristics in order to obtain a generalized P'_{fa} from $M = 3$.

1) The frequency sequences of the receiver for T_s are a total of M cases.
   a) For $M = 3$, the frequency sequences of the receiver for T_s are three cases as $[f_1, f_2, f_3]$, $[f_2, f_3, f_1]$, and $[f_3, f_1, f_2]$.
2) In the calculation of P'_{fa}, Cases 1 and $(M + 1)$ of the LUT are always similar to each other because the timing difference is removed in the LUT. Due to this characteristic of the LUT, $P_{\text{fa},M}$ is mapped twice only if the frequency sequence of the receiver is $[f_1, f_2, \ldots, f_M]$ and $P_{\text{fa},M}$ is mapped once for the remaining $(M - 1)$ frequency sequences. Therefore, $P_{\text{fa},M}$ occurs $2 + (M - 1) = M + 1$ times.
   a) For $M=3$, $P_{\text{fa},3}$ is mapped twice for $[f_1, f_2, f_3]$ and once for the remaining $[f_2, f_3, f_1]$ and $[f_3, f_1, f_2]$. Therefore, $P_{\text{fa},3}$ occurs four times in total.
3) Both the frequency sequences of the receiver and the cases of the LUT are cyclic shift structures. If $P_{\text{fa},M}$ is mapped to Case k in the LUT, $P_{\text{fa},(M-1)}$ is mapped to Cases $(k - 1)$ and $(k + 1)$ in the LUT, and $P_{\text{fa},(M-2)}$ is mapped to Cases $(k - 2)$ and $(k + 2)$ in the LUT. Thus, $P_{\text{fa},i}$ is mapped twice for each frequency sequence of the receiver, where $2 \le i \le (M - 1)$. However, since Cases 1 and $(M + 1)$ of the LUT are similar to each other, $P_{\text{fa},i}$ is mapped three times for two frequency sequences of which $P_{\text{fa},i}$ is mapped to Case 1 or Case $(M + 1)$. Consequently, $P_{\text{fa},i}$ occurs $2(M - 2) + 3 \times 2 = 2(M + 1)$ times.
   a) For $M = 3$ and $[f_2, f_3, f_1]$ sequence, $P_{\text{fa},2}$ is mapped to Cases 1 and 3 in the LUT because $P_{\text{fa},3}$ is mapped to Case 2 in the LUT. However, since Cases 1 and 4 are similar to each other in the LUT, $P_{\text{fa},2}$ is also mapped to Case 4, resulting in a total of three mappings. We can obtain the same result in the $[f_3, f_1, f_2]$ sequence. In contrast, in the $[f_1, f_2, f_3]$ sequence, since $P_{\text{fa},2}$ is not mapped to Case 1 or Case 4, two mappings occur. Therefore, $P_{\text{fa},2}$ for $M = 3$ occurs $2 + 3 \times 2 = 8$ times

Accordingly, we can express P'_{fa} for M as

$$P'_{\text{fa}} = \frac{1}{M}\left((M+1)P_{\text{fa},M} + 2(M+1)\sum_{i=2}^{M-1} P_{\text{fa},i}\right). \quad (17)$$

Note that P'_{fa} in (17) is calculated for one chip among the $(M + 1)(N_d + N_{\text{dead}})$ chips corresponding to the one-hop duration of the receiver. Then, we can obtain P_{fa} using (17) as

$$P_{\text{fa}} = 1 - (1 - P'_{\text{fa}})^{(M+1)(N_d+N_{\text{dead}})-N_{\text{dead}}}. \quad (18)$$

Note in (18) that we remove the dead time period, N_{dead}, in the one-hop duration of the receiver because the receiver does not process the received signal for the dead time.

C. Performance Comparison

We present the performance of the proposed algorithm by comparing it with the conventional serial and parallel schemes. We here modify the conventional serial and parallel schemes to be applied to hybrid DS/FFH systems for comparison with our proposed scheme.

1) *Conventional Serial Search Algorithm:* In a DS system, the conventional serial search algorithm detects the preamble using the correlation between the received sequence and the locally generated sequence at the receiver. If a correlation value does not exceed a threshold value, the receiver adjusts the timing by T_c/N and repeats this process [6], [36]. Actually, N is set to 2 or more, but N is assumed to be 1 for simplicity. The conventional serial search algorithm of the DS system needs to be extended to take into account FH in a hybrid DS/FFH system. When the preamble pulses of M hopping frequencies are transmitted, the dwell time for the correlation process at the receiver needs to be MT_h so that the receiver can process M hopping frequencies. In the general assumption that there is no prior information on the reception timing of the preamble, the receiver needs to repeat the timing adjustment and correlation process $M(N_d + N_{\text{dead}})$ times, which is the number of chips corresponding to the dwell time of MT_h, to synchronize the PN code for the worst case. Therefore, the transmission for the preamble pulses of M hopping frequencies needs to be repeated $M(N_d + N_{\text{dead}})$ times and thus $[\mathcal{F}^{(1)}, \mathcal{F}^{(2)}, \ldots, \mathcal{F}^{(M(N_d+N_{\text{dead}}))}]$ is transmitted. Then, the acquisition time is given by

$$T_s = MT_h \times M(N_d + N_{\text{dead}}) = \{M(N_d + N_{\text{dead}})\}^2 T_c. \quad (19)$$

The same result can be obtained for the acquisition time of the conventional serial search algorithm in a FH system

when extended to a hybrid DS/FFH system. The conventional serial search algorithm of the FH system typically aims to synchronize within a fraction of one hop between the frequency of the receiver and the frequency of the received signal [6], [7]. If a correlation result does not pass a test, the receiver slips the phase of the frequency pattern, and the next test is repeated. However, the synchronization of the hybrid DS/FFH system needs to be accomplished within a PN code in one hop to obtain the gain of DS spreading. Therefore, the slip unit of the frequency pattern needs to be T_c/N. If the correlation is performed for MT_h in order to process M hopping frequencies for $N = 1$, the acquisition time can be expressed as (19).

The ratio between T_s of the proposed algorithm in (8) and T_s of the conventional serial search algorithm in (19) can be represented as

$$\alpha = \frac{M(M+1)(N_d + N_{\text{dead}})T_c}{\{M(N_d + N_{\text{dead}})\}^2 T_c} = \frac{M+1}{M(N_d + N_{\text{dead}})}. \quad (20)$$

From (20), we figure out that the proposed algorithm can greatly reduce the acquisition time to $\frac{1}{48}$ of the conventional serial search algorithm in the case of $M = 3$, $N_d = 31$, and $N_{\text{dead}} = 33$. The reduction effect of acquisition time rises as N_d and N_{dead} increase. In addition, the proposed algorithm can accurately estimate the end timing of the acquisition stage by applying a cyclic shift code, whereas the conventional serial search algorithm is not able to know which of the repeatedly transmitted preamble pulses has been detected.

In the conventional serial search algorithm, the acquisition can be declared when the correlation value for dwell time of MT_h is above the threshold value. Then, we can express P_{d} and P_{fa} of the conventional serial search algorithm as [34]

$$P_{\text{d}} = \sum_{k=\Lambda}^{MN_d} \binom{MN_d}{k} (1-P_e)^k (P_e)^{MN_d-k}$$
$$P_{\text{fa}} = 1 - \left(1 - \sum_{k=\Lambda}^{MN_d} \binom{MN_d}{k} \left(\frac{1}{2}\right)^{MN_d}\right)^{M(N_d+N_{\text{dead}})} \quad (21)$$

where Λ denotes the minimum number of matching chips among MN_d chips in order to exceed the threshold value. Note in (21) that the number of chips corresponding to dwell time of MT_h is $M(N_d + N_{\text{dead}})$, but N_{dead} is excluded from the calculation of correlation value.

2) *Conventional Parallel Algorithm:* The conventional parallel algorithm of an FH system is described in [6] and [19]. The envelop detector of the conventional parallel algorithm needs to be modified to the correlation-based PN code detector in order to obtain the gain of DS spreading. In the conventional parallel algorithm, the receiver can process the preamble pulses of all the M hopping frequencies simultaneously because the receiver takes M synthesizers, filters, and correlators, as shown in [6] and [19]. Therefore, acquisition can be obtained by the reception of only $\mathcal{F}^{(1)}$, which means the transmission of M preamble pulses. Then, the acquisition time can be written as

$$T_s = MT_h = M(N_d + N_{\text{dead}})T_c. \quad (22)$$

The acquisition time of the conventional parallel algorithm in (21) is $(M+1)$ times shorter than that of the proposed algorithm in (8).

In the conventional parallel algorithm, the acquisition is achieved in two steps, where a different threshold value is used in each step. In the first step, if the correlation value of the PN code detector of each branch exceeds the threshold value, the output of the PN code detector is "1," otherwise, "0." In the second step, the acquisition is declared when the sum of output of all the M PN code detectors exceeds the threshold value. Thus, we can represent P_{d} and P_{fa} of the conventional parallel algorithm as [34]

$$P_{\text{d}} = \sum_{k=\Upsilon_2}^{M} \binom{M}{k} (P'_{\text{d}})^k (1-P'_{\text{d}})^{M-k}$$
$$P_{\text{fa}} = 1 - \left(1 - \sum_{k=\Upsilon_2}^{M} \binom{M}{k} (P'_{\text{fa}})^k (1-P'_{\text{fa}})^{M-k}\right)^{M(N_d+N_{\text{dead}})} \quad (23)$$

where Υ_2 indicates the threshold value of the second step and P'_{d} and P'_{fa} are the probabilities that the output of each PN code detector is "1" by preamble and noise, respectively. Since the PN code detector is the correlator with N_d chips, we can easily obtain P'_{d} and P'_{fa} as [34]

$$P'_{\text{d}} = \sum_{k=\Upsilon_1}^{N_d} \binom{N_d}{k} (1-P_e)^k (P_e)^{N_d-k}$$
$$P'_{\text{fa}} = \sum_{k=\Upsilon_1}^{N_d} \binom{N_d}{k} \left(\frac{1}{2}\right)^{N_d} \quad (24)$$

where Υ_1 denotes the minimum number of matching chips among N_d chips in order to exceed the threshold value of the first step. Note that, since the received signal is divided into M branches for the parallel scheme, the input power of each branch is reduced by a factor of $1/M$. Thus, P_e in (24) needs to be modified as $P_e = \frac{1}{2}\text{erfc}(\sqrt{\frac{E_c}{MN_0}})$ [35].

3) *Comparison Results:* In this article, we set the performance criterion to $P_{\text{d}} = 0.999$ (probability of miss, $P_{\text{m}} = 1 - P_{\text{d}} = 10^{-3}$) at $P_{\text{fa}} = 10^{-4}$ as an example [8]. For $M = 3$, $N_d = 31$, and $N_{\text{dead}} = 33$, P_{m} of the proposed algorithm in (12) and the conventional algorithms in (21) and (23) are shown in Fig. 6. Note that P_{fa} is determined by the correlation threshold value. Since the correlation value is discrete due to the digital correlation, P_{fa} is also discrete and is set close to 10^{-4}.

For $P_{\text{m}} = 10^{-3}$, the conventional serial search algorithm is about 2 dB lower in E_c/N_0 than the proposed algorithm, as shown in Fig. 6. However, assuming the same acquisition time, we can repeat the acquisition process of the proposed algorithm 48 times as in (20). If we newly define the acquisition as the original acquisition occurs Γ' or more times in 48 repetitions, $P_{\text{d}}^{\text{rep}}$ and $P_{\text{fa}}^{\text{rep}}$ can be expressed using

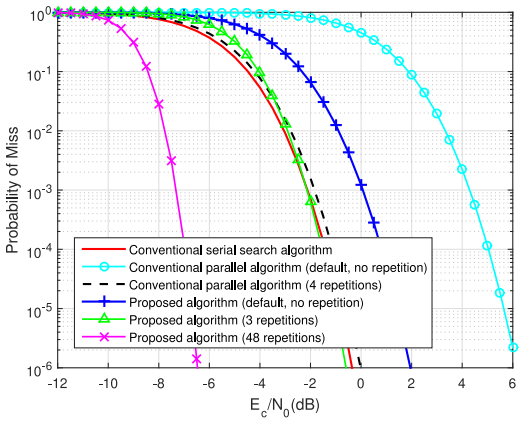


Fig. 6. Comparison of probability of miss between proposed algorithm and conventional algorithms for $M = 3$, $N_d = 31$, and $N_{\text{dead}} = 33$.

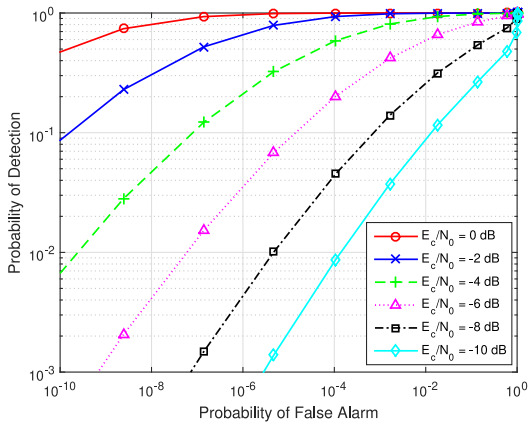
(12) and (18), respectively, as [34]

$$P_{\text{d}}^{rep} = \sum_{k=\Gamma'}^{48} \binom{48}{k} (P_{\text{d}})^k (1-P_{\text{d}})^{48-k}$$
$$P_{\text{fa}}^{rep} = \sum_{k=\Gamma'}^{48} \binom{48}{k} (P_{\text{fa}})^k (1-P_{\text{fa}})^{48-k}. \quad (25)$$

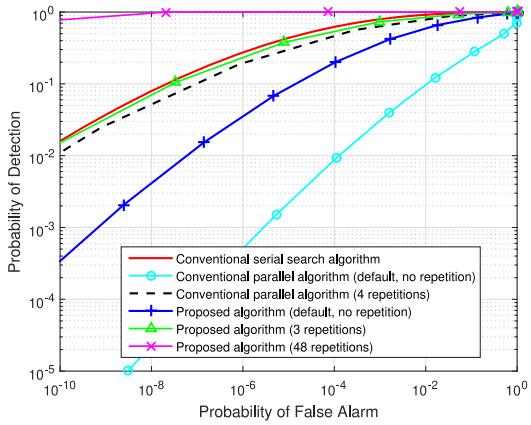
Fig. 6 shows that the proposed algorithm with 48 repetitions is about 5 dB lower in E_c/N_0 than the conventional serial search algorithm for $P_{\text{m}} = 10^{-3}$. The proposed algorithm with three repetitions and the conventional serial search algorithm have similar P_{m} performance, as shown in Fig. 6, which indicates that the proposed algorithm can reduce the acquisition time to 1/16 of the conventional serial search algorithm while obtaining similar P_{m} performance.

The proposed algorithm is about 4 dB lower in E_c/N_0 than the conventional parallel algorithm for $P_{\text{m}} = 10^{-3}$, as shown in Fig. 6, while the acquisition time of the conventional parallel algorithm is four times faster than that of the proposed algorithm. The proposed algorithm is about 2 dB higher in E_c/N_0 than the conventional parallel algorithm with four repetitions assumed same acquisition time. However, the parallel algorithm requires the synthesizers, filters, and correlators corresponding to the number of hopping frequencies, which restricts the real-time implementation in the practical system. Compared with the parallel algorithm, our proposed serial algorithm has particular advantages in hardware limited systems such as tactical military network using drone and weapon data link.

We also carry out the performance comparison of the proposed algorithm and the conventional algorithms using receiver operating characteristic (ROC) curves. Fig. 7(a) shows the ROC curves of the proposed algorithm for different E_c/N_0 with $M = 3$, $N_d = 31$, and $N_{\text{dead}} = 33$. As shown in Fig. 7(a), the area under the curve of the ROC curve increases as E_c/N_0 increases. For $M = 3$, $N_d = 31$, and $N_{\text{dead}} = 33$, the ROC curves of the proposed algorithm and the conventional algorithms are shown in Fig. 7(b). As shown in Fig. 7(b), we can see that the performance of P_{d} in ROC curves is better in the order of the proposed algorithm



(a)



(b)

Fig. 7. ROC curves of the proposed algorithm and the conventional algorithms. (a) ROC curves of the proposed algorithm depending on E_c/N_0 for $M = 3$, $N_d = 31$, and $N_{\text{dead}} = 33$. (b) Comparison of the ROC curve between proposed algorithm and conventional algorithms for $M = 3$, $N_d = 31$, $N_{\text{dead}} = 33$, and $E_c/N_0 = -6$ dB.

with 48 repetitions, the conventional serial search algorithm, the proposed algorithm without repetition, and the conventional parallel algorithm without repetition, which is consistent with the comparison result of P_{m} in Fig. 6. We summarize the performance comparison results between the proposed algorithm and the conventional algorithms in Table III.

D. Simulation Results

The simulation for the proposed acquisition algorithm is carried out to confirm the exactness of our performance analysis. The number of hopping frequencies is chosen as $M = 3$ and 5 for an example. The number of chips in m-sequence is set to $N_d = 31$ and 63, whereas dead time is fixed at $N_{\text{dead}} = 33$. In Figs. 8 and 9, we check the exactness of the analytical results of P_{d} and P_{fa}. The four points in the rectangle shown in Fig. 9 represent the Γ and P_{fa} values used in the simulation for P_{d} in Fig. 8. From Figs. 8 and 9, we know that the theoretical analysis and simulation results agree with each other well in all cases, which confirms the accuracy of our performance analysis. The performance

TABLE III
Performance Comparison Results Between the Proposed Algorithm and the Conventional Algorithm

	Acquisition time [hop]	Required E_c/N_0 for $P_m = 10^{-3}$ at $P_{fa} = 10^{-4}$ ($M = 3, N_d = 31$ and $N_{dead} = 33$)	Hardware complexity
Conventional serial search algorithm	$M^2(N_d + N_{dead})$	-2 dB	Low (One synthesizer, filter, and correlator)
Conventional parallel algorithm (default)	M	4 dB	High (M synthesizers, filters, and correlators)
Conventional parallel algorithm (4 repetitions)	$4M$	-2 dB	High (M synthesizers, filters, and correlators)
Proposed algorithm (default)	$M(M+1)$	0 dB	Low (One synthesizer, filter, and correlator)
Proposed algorithm (3 repetitions)	$3M(M+1)$	-2 dB	Low (One synthesizer, filter, and correlator)
Proposed algorithm (48 repetitions)	$48M(M+1)$	-7 dB	Low (One synthesizer, filter, and correlator)

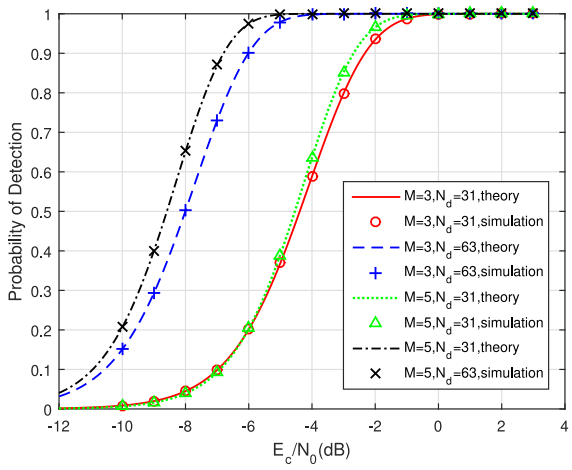


Fig. 8. Comparison of the theoretical P_d and the P_d obtained by simulation for various M and N_d.

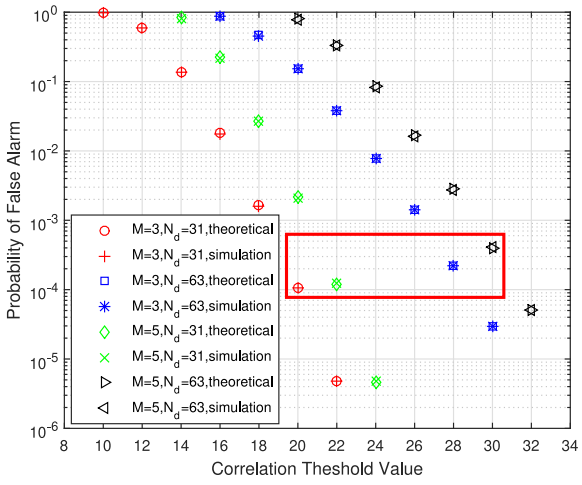


Fig. 9. Comparison of the theoretical P_{fa} and the P_{fa} obtained by simulation depending on the correlation threshold value Γ for various M and N_d.

of P_d is greatly affected by N_d, whereas M has relatively little effect on performance of P_d. However, M needs to be considered in terms of antijamming and frequency diversity as well as performance of P_d. Therefore, we can adjust N_d for the performance of P_d and M for antijamming and frequency diversity.

V. CONCLUSION

A simple, reliable, and rapid serial timing acquisition algorithm for hybrid DS/FFH packet radio communication systems has been proposed in this article. A serial acquisition scheme requires only one synthesizer, which can reduce the hardware complexity of the system compared with a parallel acquisition scheme. In the frequency domain, we proposed the acquisition algorithm to process the preamble pulses of all the hopping frequencies for reliable acquisition under the jamming or/and channel impairment environment. In the PN code domain, we applied the cyclic shift code as the PN code, which is the core of our proposed algorithm. With the cyclic shift code, the proposed algorithm can accurately estimate the end timing of the acquisition stage using only one correlator and can achieve rapid acquisition. The performance analysis indicates that the proposed algorithm significantly reduces the acquisition time compared with the conventional serial search algorithm.

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