A half adder is a combinational logic circuit that adds two 1-bit binary numbers and outputs the sum and carry bits. It is the simplest of all adder circuits and is the building block of more complex adders, such as full adders and ripple carry adders.

The half adder operation can be represented by the following equation:

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S = A XOR B
C = A AND B
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where:

- S is the sum bit
- C is the carry bit
- A is the first input bit
- B is the second input bit

The half adder operation can be implemented using basic gates such as XOR and AND gates. The XOR gate implements the addition operation for binary digits, where a "1" is generated in the Sum output only when one of the inputs is "1". The AND gate generates a "1" in the Carry output only when both inputs are "1".

Here is a truth table for a half adder:

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0

A	B	S	C
1	1	0	1

As you can see, the Sum output is the LSB of the result, while the Carry output indicates whether there was a carry-over from the addition of the two inputs.

Half adders are used in a variety of applications, such as:

- Adding two binary digits in a computer's central processing unit (CPU)
- Generating checksums for data transmission and storage
- Designing combinational logic circuits

Half adders are simple and efficient circuits that are essential for many digital devices.