

CAN RECEIVER

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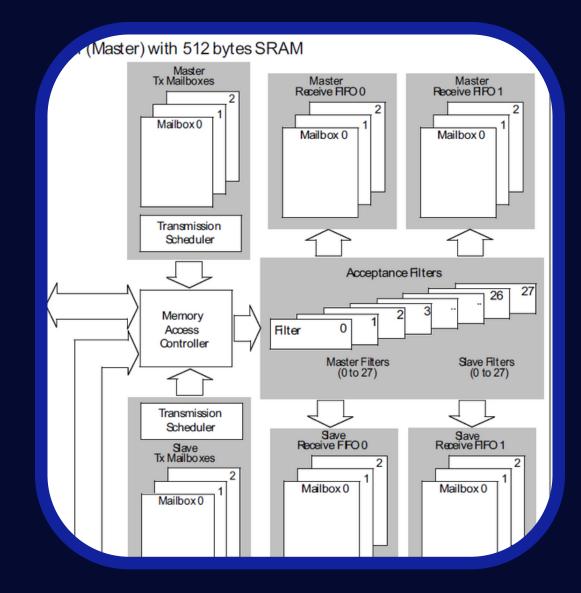
FEATURES

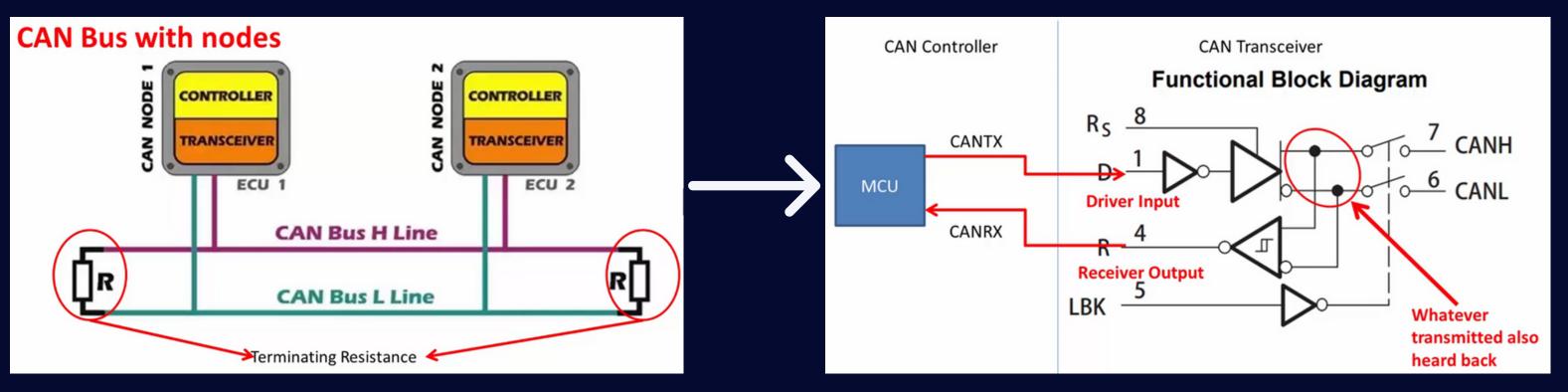
- 2 recieve FIFOs with 3 stages
- Scalable filter banks:
 - 28 filter bakns shared between CAN1 and CAN2
- Identifier list feature
- Configurable FIFO overrun
 - Time Stamp on OF reception

RXPATH

To understand reception we need to know the **PATH** that a message takes from the **BUS** to the **MCU**.

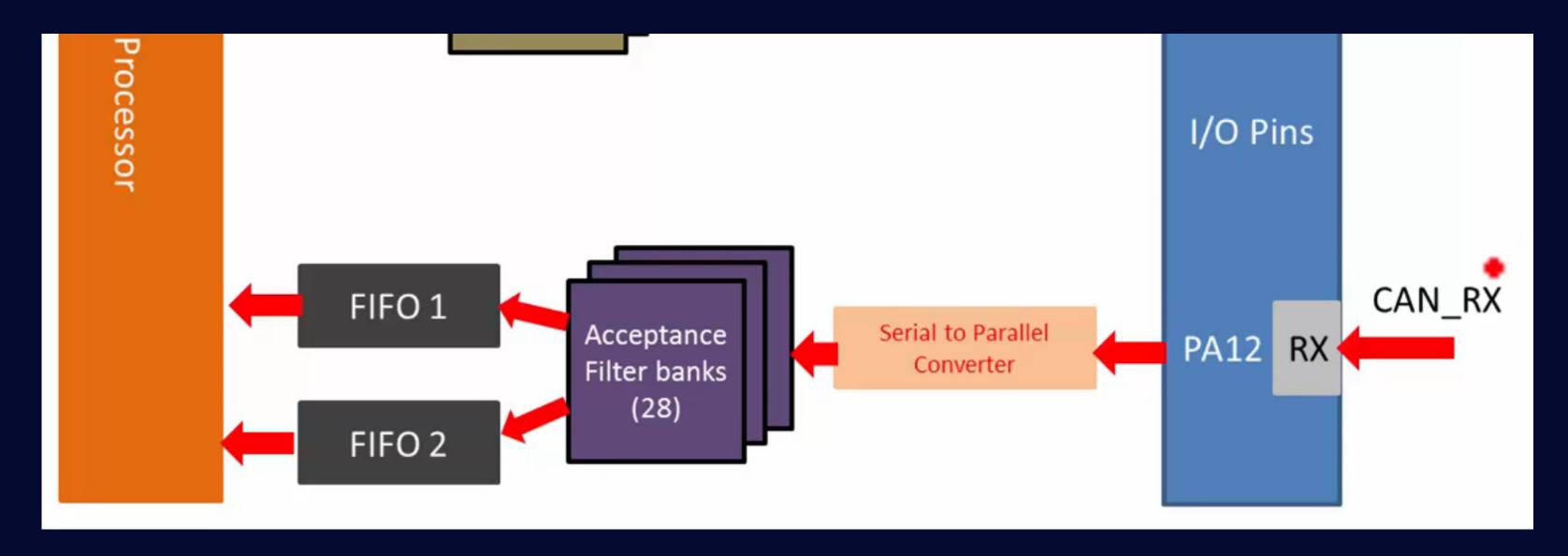
CAN BUS -> TRANSRECIVER -> CAN CONTROLLER (bxCAN)







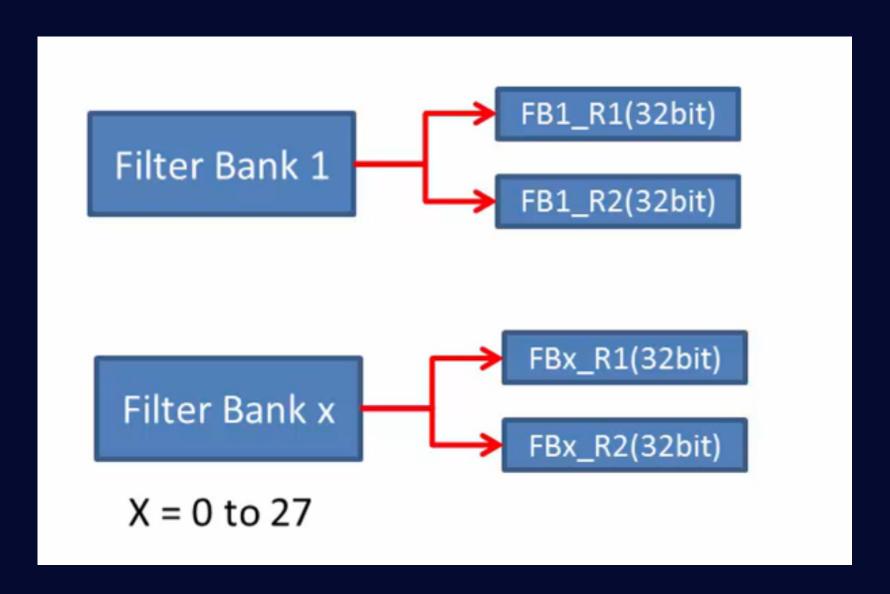
The bxCAN RX PATH - Filtering



Filter banks is a hardware mechanism that can be programmed to ignore and discard certain CAN frames and allow other to pass on to the FIFOs.

There are 28 filter banks for CAN1&2 each with 2 32-bit registers

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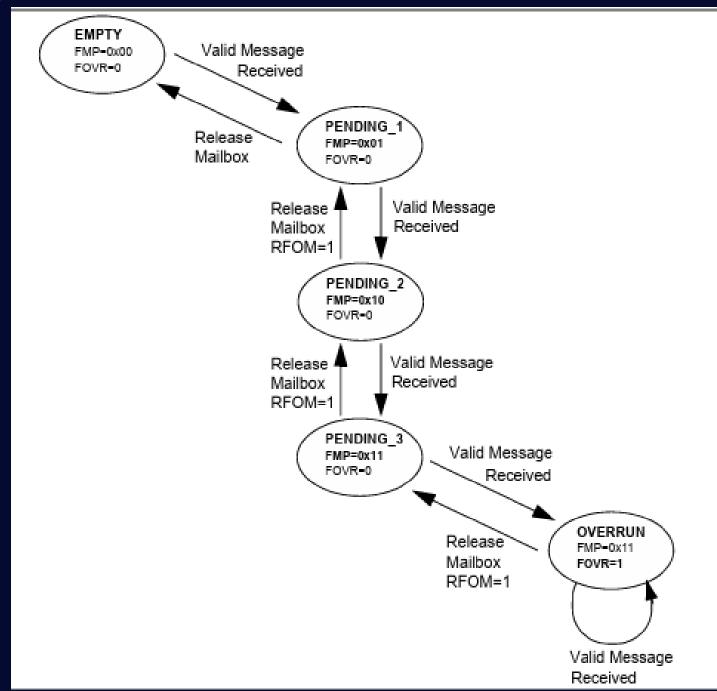
Examples:

Accept only extented id frames

Accept only indentifiers with hex value 0x02

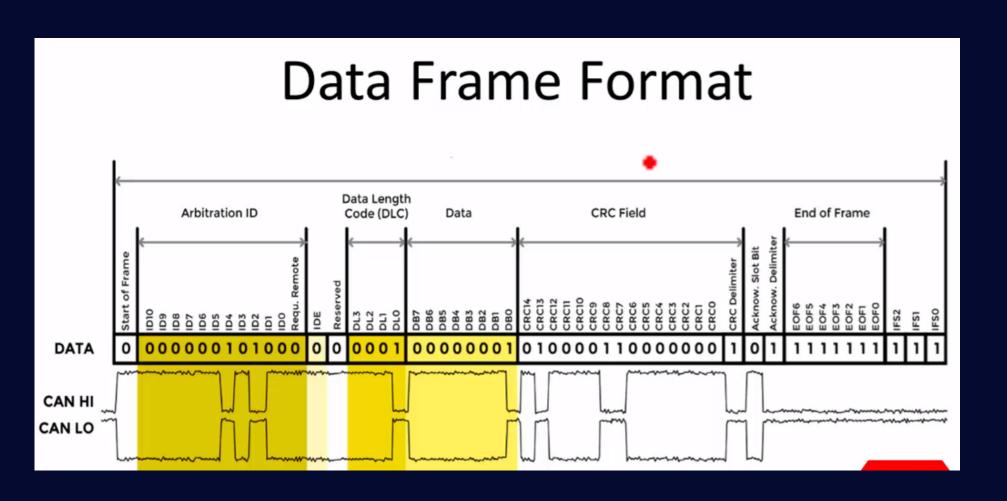


- For recieving we have 2 FIFOs (First in-First Out),
 these are used to store incomming messages.
- 3 complete messages can be stored at each
- Managed completely by hardware.
- Reception Handling is more complex than the Transmission
 - The application accesses the messages stored in the FIFO throught the FIFO output mailbox.
 - The important bit is the acknowledge field
 - When a message is stored, it becomes available in the FIFO output mailbox.
 - Once the software handle the message, the software must release the FOM, activating the CAN_RFR Reg to make the incoming message available.



- We can say that a message is valid when recieved according to the CAN protocol.
- The acknowledge field is controlled by the recieving node, the state of this field will tell us the outcome.
- The important bit is the acknowledge field

Offset to receive mailbox base address (bytes)	Register name
0	CAN_RIXR
4	CAN_RDTxR
8	CAN_RDLxR
12	CAN_RDHxR



• Depending on which register the mailbox is stored, we have a different offset to set to the software to read.

