



CHIPATHON 2025 PROJECT PROPOSAL

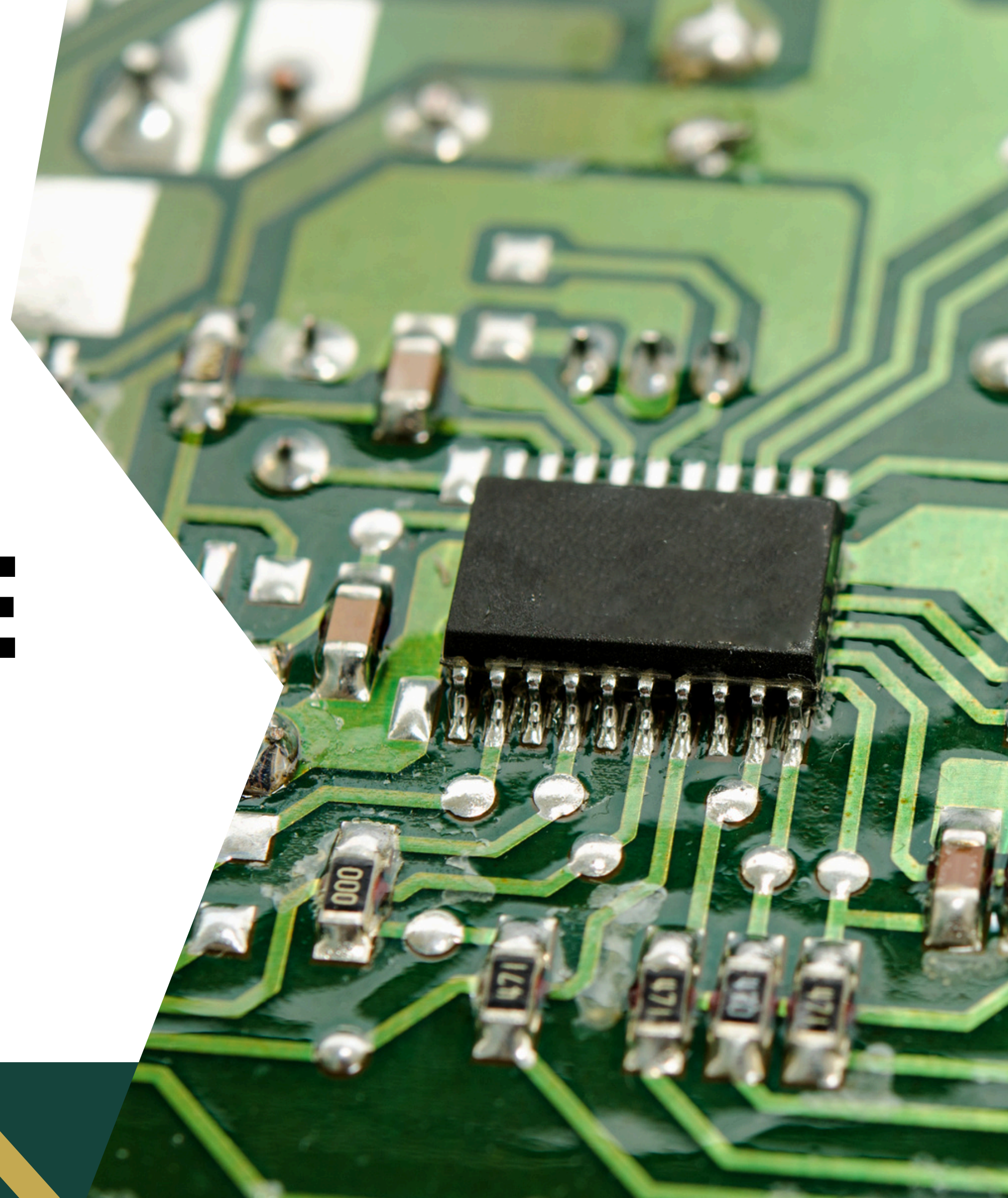


TRACK B

AOI & OAI GATE

by ChipiChapa Team

XXXXX



Background

- In this chipaton, our team will make 4 standard cells library, that is AOI211, OAI211, AOI221, and OAI221.
- We make these AOI dan OAI cells for fundamental cell of further macro cells like arithmetic cells and multiplexer.
- For the reference of performaces (delay, power, etc), we use performance from standard cells gf180mcu with 5v VDD, and make some goal prediction from those 5v standard cells (tweaking the delay time, power, etc from 5v and predict how it works for 3v3).

Functionality

In this chipaton, our team will make 4 standard cells library, that is AOI211, OAI211, AOI221, and OAI221.

AOI211

AOI211 is a standard cells with 4 input that has boolean expression:

$$Y = !((A1 \& A2) | B1 | C1)$$

AOI221

AOI221 is a standard cells with 5 input that has boolean expression:

$$Y = !((A1 \& A2) | (B1 \& B2) | C1)$$

OAI211

OAI211 is a standard cells with 4 input that has boolean expression:

$$Y = !((A1 | A2) \& B1 \& C1))$$

OAI221

OAI221 is a standard cells with 5 input that has boolean expression:

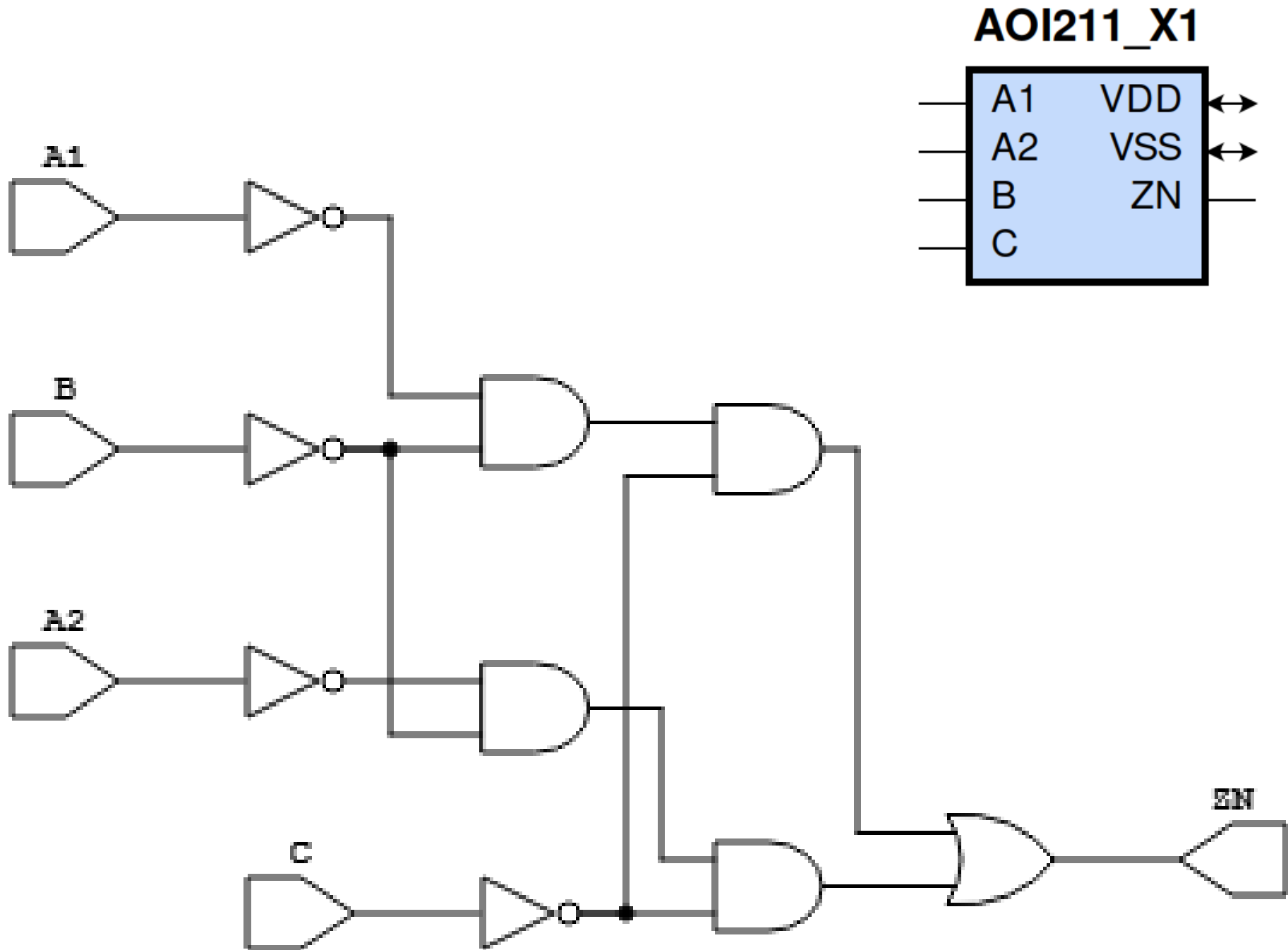
$$Y = !((A1 | A2) \& (B1 | B2) \& C1)$$

General Format & Specification

LIBRARY	gf180mcu_osu_sc_9t3v3
CELLS	<div>1. AOI 211 : <u>gf180mcu_osu_sc_gp9t3v3_aoi211_1</u></div> <div>2. OAI211: <u>gf180mcu_osu_sc_gp9t3v3_oai211_1</u></div> <div>3. AOI221: <u>gf180mcu_osu_sc_gp9t3v3_aoi221_1</u></div> <div>4. OAI221: <u>gf180mcu_osu_sc_gp9t3v3_oai221_1</u></div>
DRIVE STRENGTH	1X
TRACK	9 Track
VDD	3.3V

Block Diagram & Schematic - AOI211

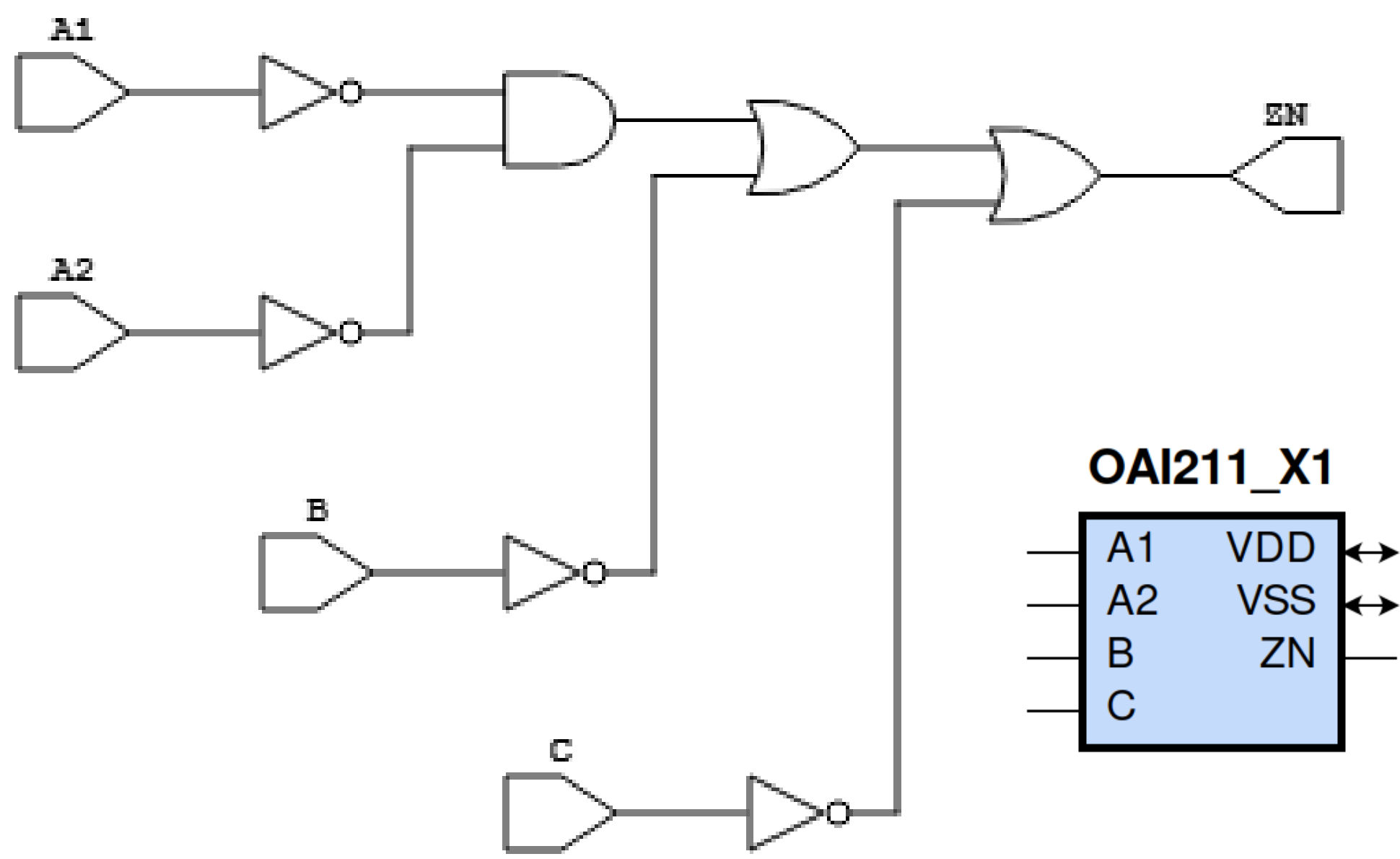
Gate Level



Specification	Target
Area	<35 μm^2
Input Capacitance	<0.01 pF
Delay	<0.40 ns
Output Load	0.001 pF
Dynamic Energy	<0.4 $\mu\text{W}/\text{MHz}$
Leakage Power	<0.2 nW

Block Diagram & Schematic - OAI211

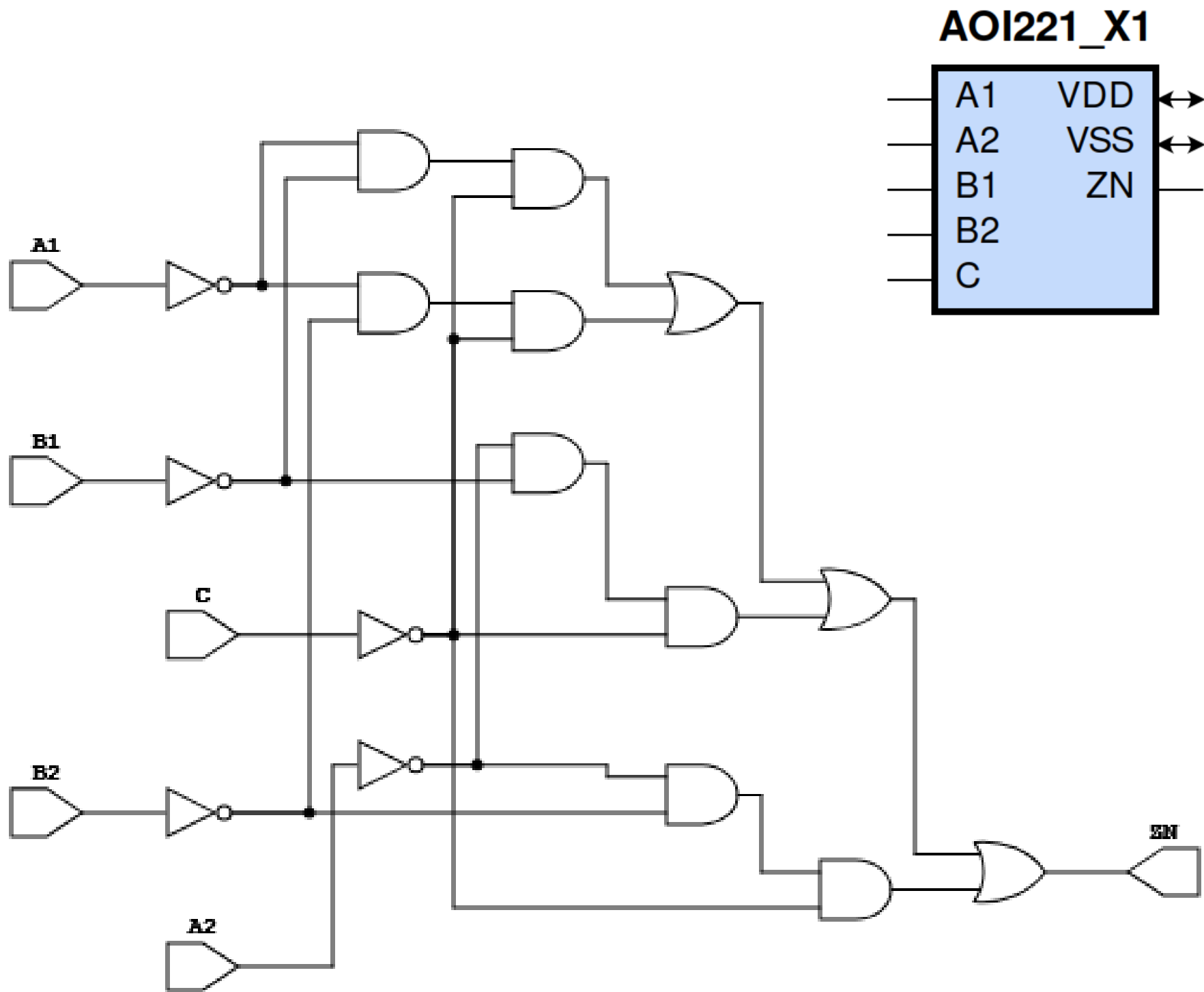
Gate Level



Specification	Target
Area	<35 μm^2
Input Capacitance	<0.01 pF
Delay	<0.40 ns
Output Load	0.001 pF
Dynamic Energy	<0.4 $\mu\text{W}/\text{MHz}$
Leakage Power	<0.2 nW

Block Diagram & Schematic - AOI221

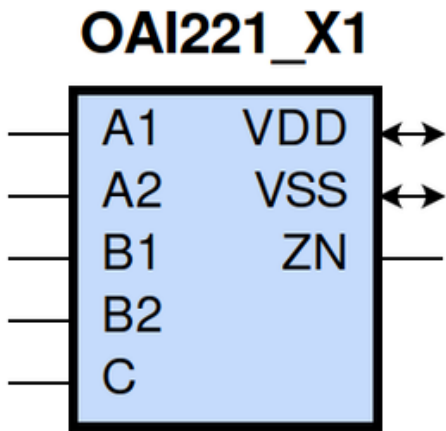
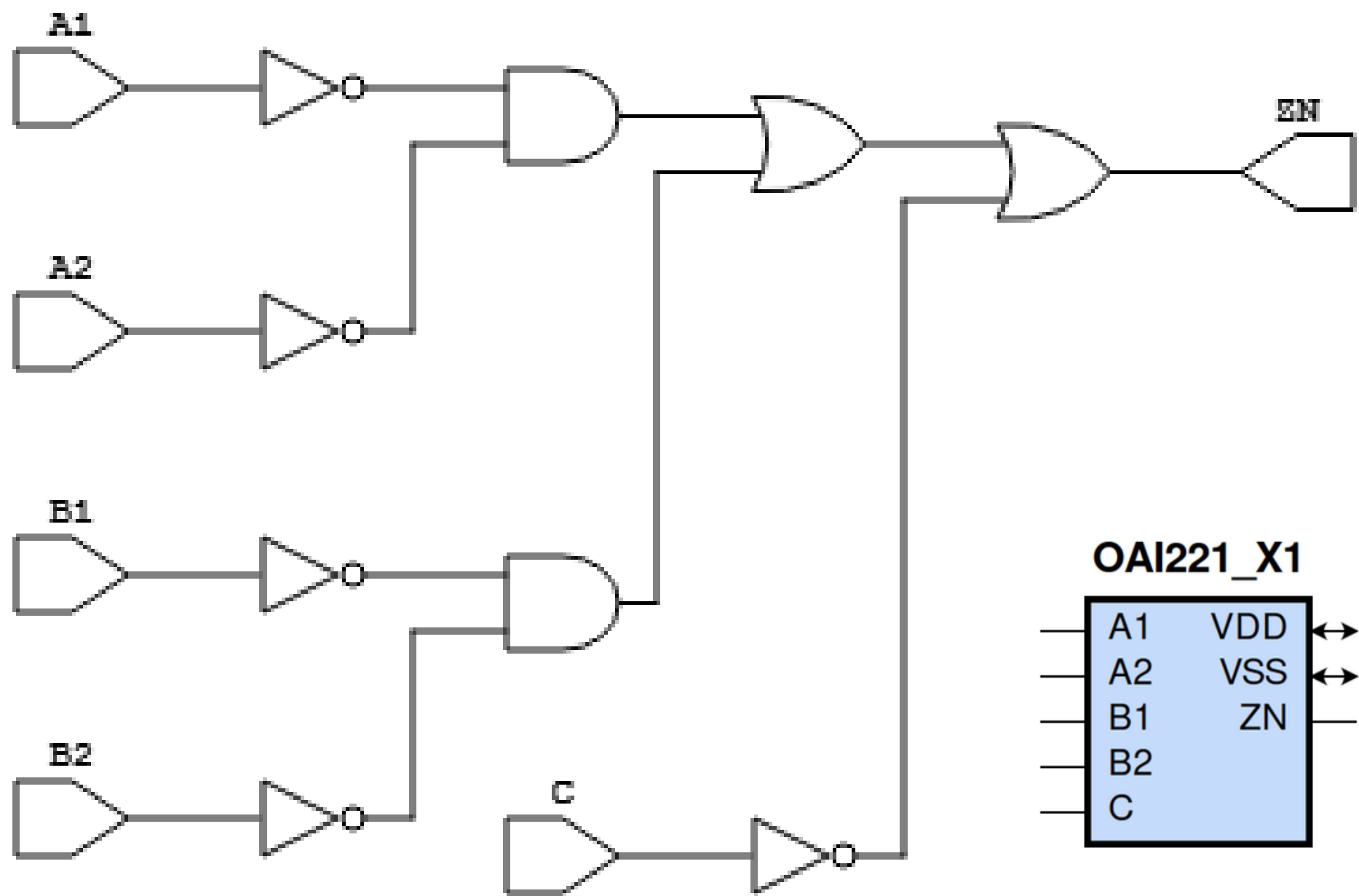
Gate Level



Specification	Target
Area	<40 μm ²
Input Capacitance	<0.01 pF
Delay	<0.90ns
Output Load	0.001 pF
Dynamic Energy	<0.4 μW/MHz
Leakage Power	<0.2 nW

Block Diagram & Schematic - OAI221

Gate Level



Specification	Target
Area	<40 μm^2
Input Capacitance	<0.01 pF
Delay	<0.90ns
Output Load	0.001 pF
Dynamic Energy	<0.4 $\mu\text{W}/\text{MHz}$
Leakage Power	<0.2 nW

Task Distribution

Member Name	Rafi Ihsan Alfathin	Saputra Yudika Marpaung	Adrian Sami Pratama	Muhammad Nabil Raihan
Block will be working on	AOI211	OAI211	AOI221	OAI221
Task Detail	<ol style="list-style-type: none">1.Design schematic with XScem2.Simulation with ngspice3.Layouting, DRC, and LVS with Klayout/Magic4.Generate parasitic RC with Magic5.Characterizing the cell with Charlib/Libretto	<ol style="list-style-type: none">1.Design schematic with XScem2.Simulation with ngspice3.Layouting, DRC, and LVS with Klayout/Magic4.Generate parasitic RC with Magic5.Characterizing the cell with Charlib/Libretto	<ol style="list-style-type: none">1.Design schematic with XScem2.Simulation with ngspice3.Layouting, DRC, and LVS with Klayout/Magic4.Generate parasitic RC with Magic5.Characterizing the cell with Charlib/Libretto	<ol style="list-style-type: none">1.Design schematic with XScem2.Simulation with ngspice3.Layouting, DRC, and LVS with Klayout/Magic4.Generate parasitic RC with Magic5.Characterizing the cell with Charlib/Libretto

Project Timeline

[illegible]



THANK YOU

link to our github : ChipiChapa Github Repo Link:
https://github.com/AdrianSPratama/SSCS-Chipaton-2025_ChipiChapa?tab=readme-ov-file

