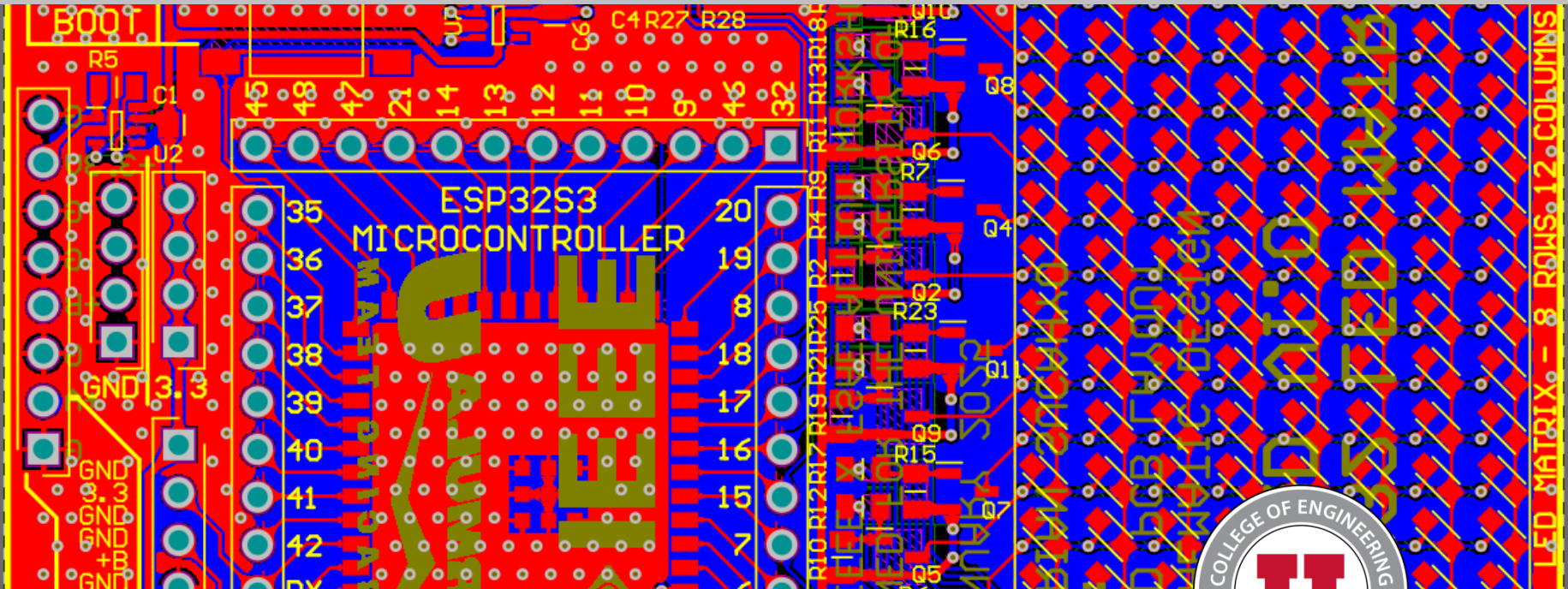


IEEE X FSAE PCB Design Workshop: (Week 04)

Intermediate Printed Circuit Board Design (LED Matrix)



Hosted By: Adrian Sucahyo and Nick Howard



Announcements

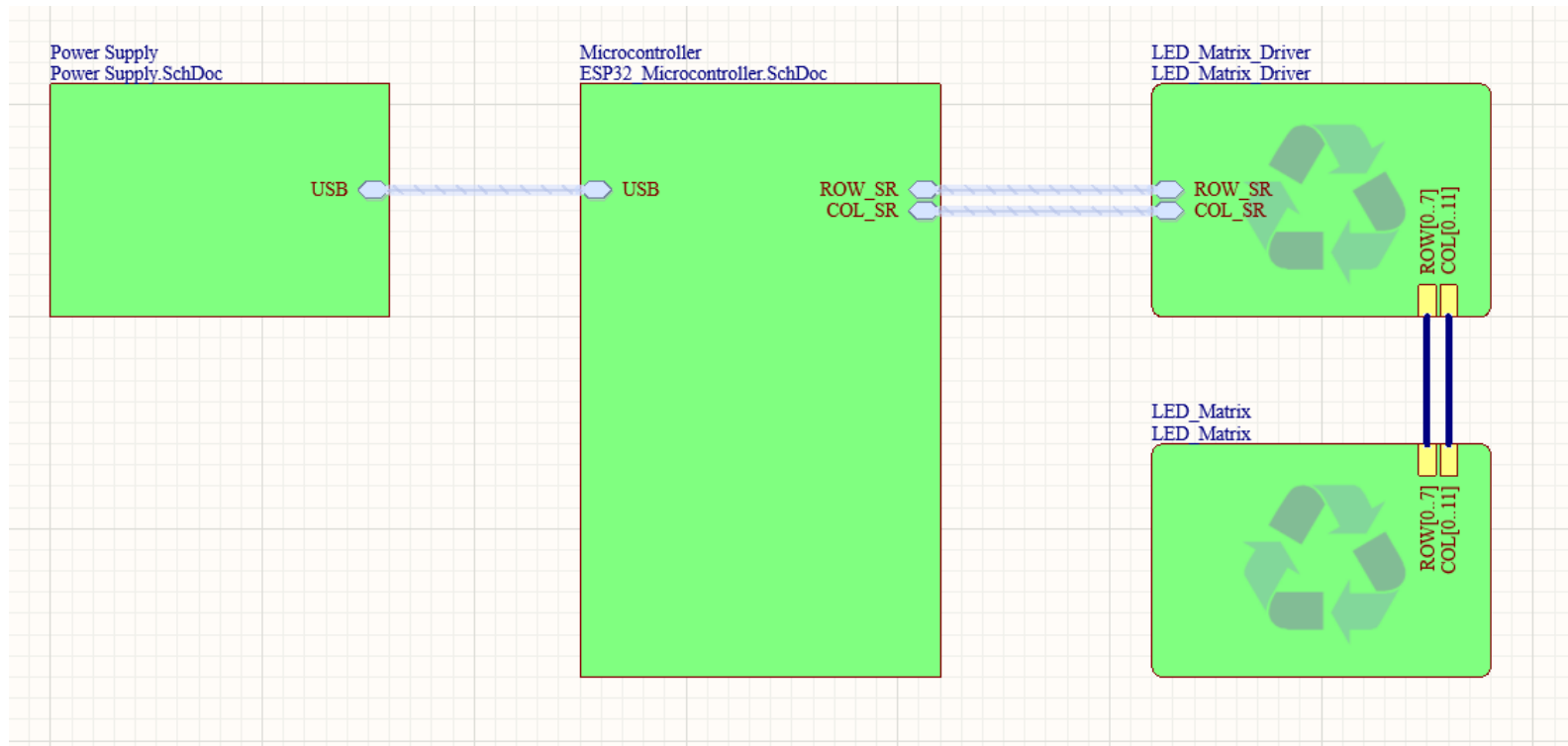
PCB Design Submissions

- Soft Deadline: March 1st
- Hard Deadline: March 4th

Next Week

- Food, Work Time, and Design Reviews
- Any other topics of interest?
 - Will send out a survey

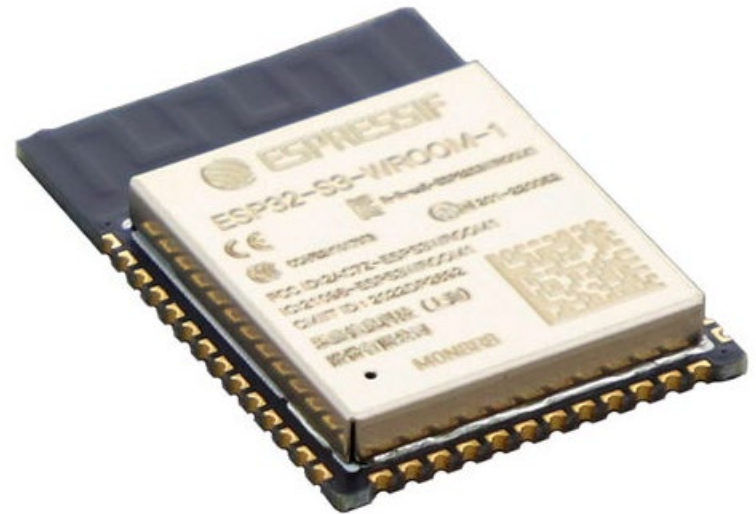
Project Review



- Hierarchical Design of the LED Matrix
- Introduction to ESP32 Microcontrollers

Microcontroller Review

- LED Matrix based on ESP32S3
 - Simple to design around
 - Beginner friendly development env.
 - (Arduino or esp-idf)
 - More advanced than ATMEGA328p
 - Many additional features
 - WiFi
 - Bluetooth
 - USB OTG



ESP32S3 Module

- We don't want to focus on designing an ESP32S3 microcontroller circuit from scratch.
 - Many extra components
 - Sensitive data lines
 - Someone has already designed it for us
- Use the ESP32S3 Module!

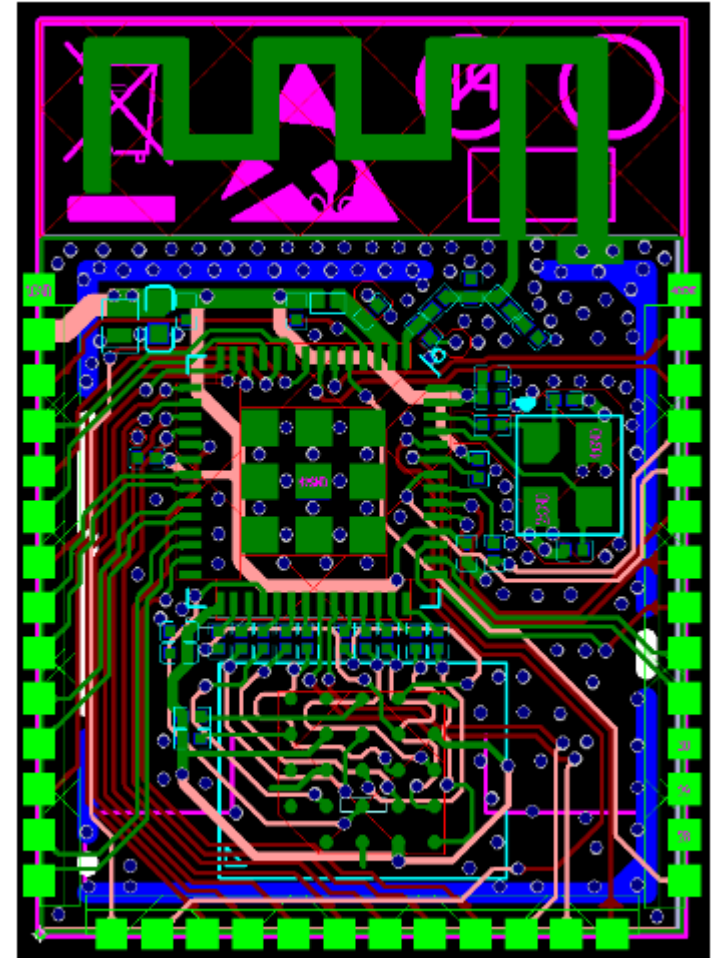
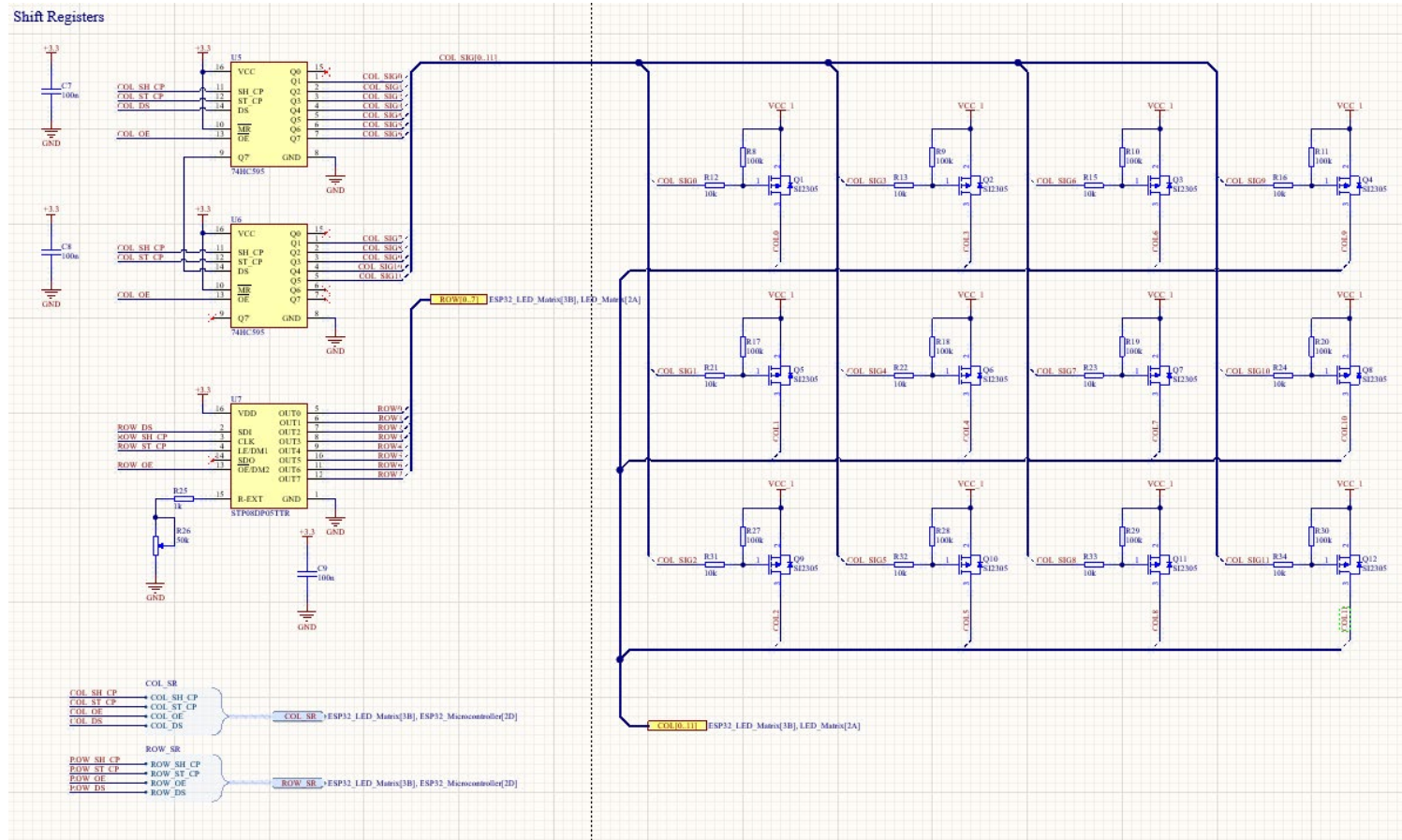


Fig. 1: ESP32-S3 Reference PCB Layout

LED Matrix Driver Review



- Driver provides the current to power all LEDs
- Uses shift registers to minimize input on GPIO

Layout and Placement

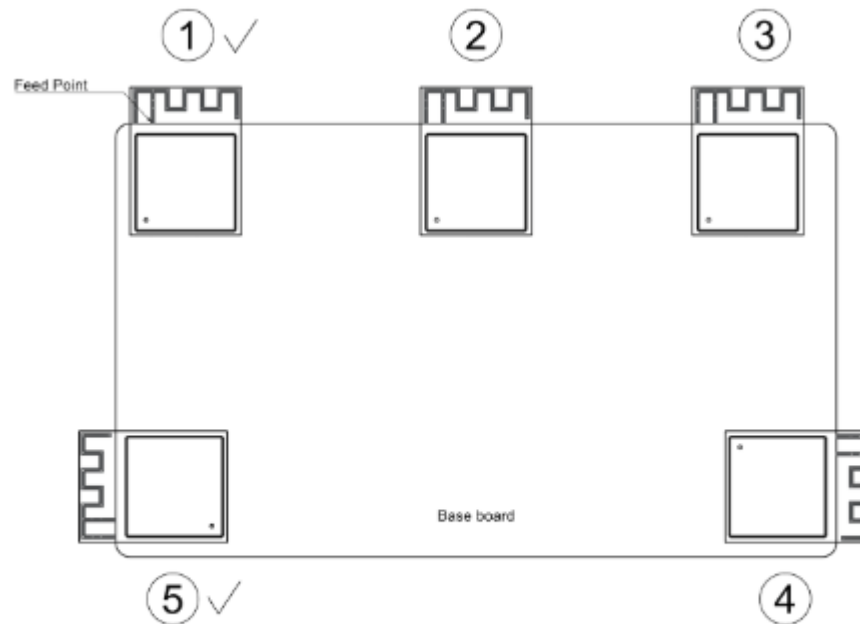


Fig. 3: Placement of ESP32-S3 Modules on Base Board (antenna feed point on the left)

- The ESP32S3 has an antenna that needs to be placed correctly to function.
- The antenna portion of the module hanging.

Layout and Placement

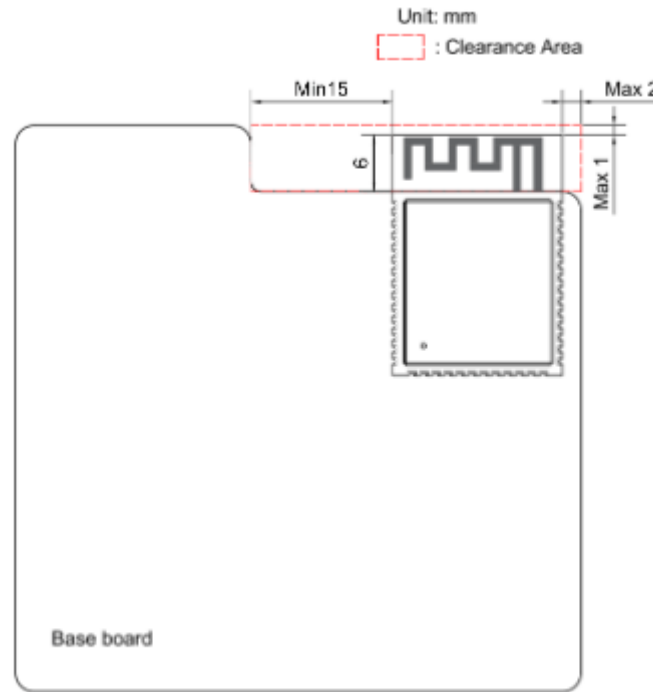
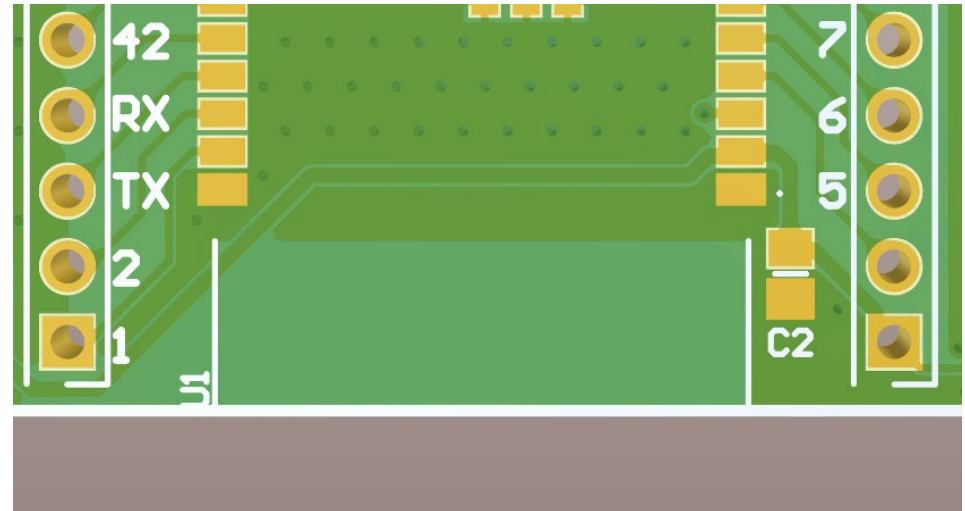
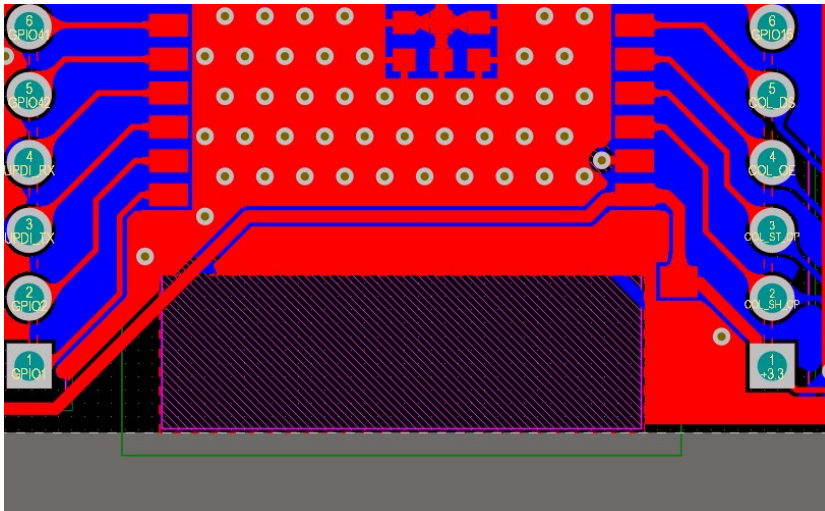


Fig. 4: Keepout Zone for ESP32-S3 Module's Antenna on the Base Board

- A board cutout is also appropriate for the antenna.
- Note: We will not be using this method (antenna is exposed and could be broken off)

Keepout Regions

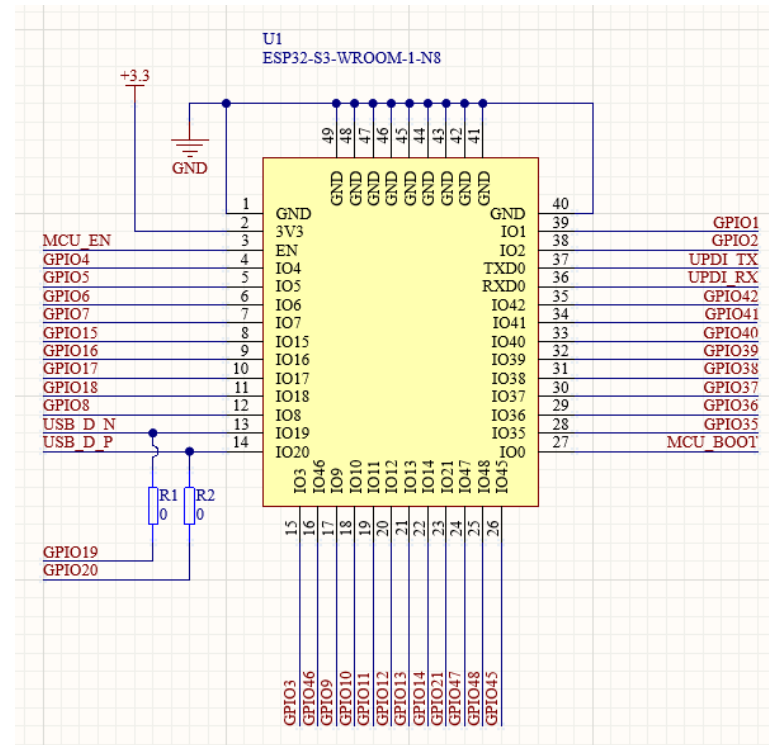


- The antenna portion of the module may be placed completely on the board, however there must be no GND plane below.
- Use Keepout regions to facilitate this.

Important Pins / GPIO

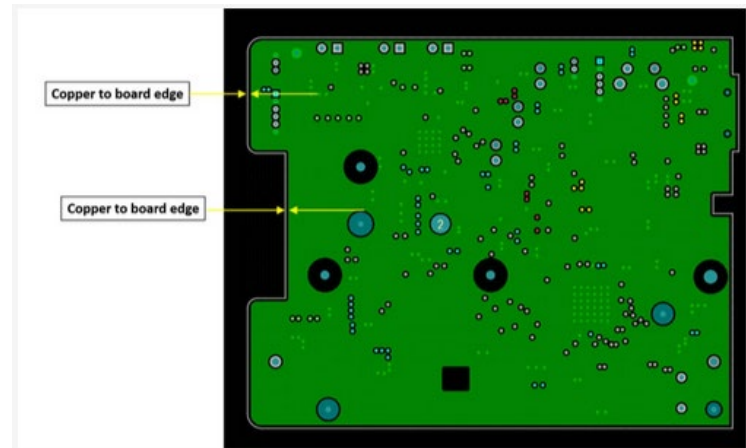
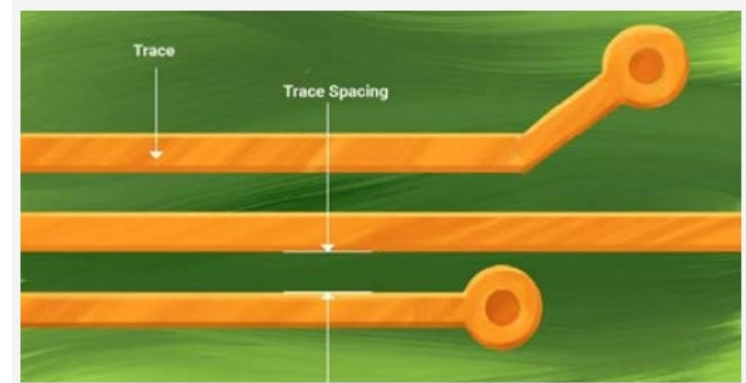
- PIN 3
 - MCU Enable
- PIN 13 and 14
 - USB- and USB+ (respectively)
- PIN17
 - Boot Mode Bootstrapping Pin
- PIN 36 and 37
 - UART RX and TX (respectively)

Note: These refer to physical pins, not GPIO Number



PCB Manufacturing – DFM and DRC

- DRC (Design Rule Check) Analysis is for checking that the minimum requirements can be met.
- DFM (Design for Manufacturing or Design for Manufacturability) Analysis is a process undertaken to ensure that the PCB layout has minimal problems.
 - Attempts to minimize problems to be encountered during manufacturing and / or assembly.
- Some aspects that might be checked are:
 - Drill Hole Size
 - Drill to Copper Clearance
 - Trace Spacing
 - Solder Mask Clearance



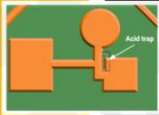
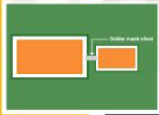


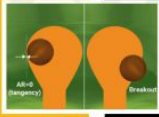



DFM vs DRC

Why do I need to use both?

- DRC's goal is to detect any discrepancies or errors.
 - Any errors found in the DRC verification will be present in all manufactured boards.
- DFM's goal is to identify any aspects that could lead to issues later on during the manufacturing process.
 - Errors found in the DFM may appear in some boards during the manufactured lifetime.
 - This could manifest as variability in the manufacturing process.
 - Accounting for DFM can reduce cost and complexity.
 - Key for later production stages

Image credit: Sierra Circuits

<https://www.protoexpress.com/blog/dfm-issues-pcb-manufacturing/>

SIERRA CIRCUITS		8 Common DFM Errors and Ways to Avoid Them	
Type of the DFM errors		Description	Techniques to avoid the defect
01. Acid trap		» 90° trace bends result in acid traps during the etching process	» Keep the trace bending angle at 45° adjacent to the pads
02. Solder mask slivers		» Slivers are small, floating wedges of solder. They get affixed to copper features forming an antenna and induce interference	» Provide at least 4 mil solder dam between the adjacent pads
03. Starved thermals		» Voids between the thermals and the planes/pads can minimize the heat concentration required for soldering process	» Avoid placing components or other traces directly above or below thermal vias
04. Insufficient antipad (clearance pad) diameter		» Through-holes without adequate clearance pads connect all voltage planes and cause short circuit	» Make the antipads 16 mil larger than the drilled hole size
05. Annular ring tangency and breakout		» Insufficient annular ring width results in tangency and breakout	» For a 1 mil annular ring: Pad width on outer layers: 6 mil Pad width on inner layers: 7 mil » For a 2 mil annular ring: Pad width for all layers: 7 mil
06. Layer shorting		» Inadequate clearance between copper features and board edges leads to short between adjacent layers	» Have at least 10 mil of clearance between the copper features and board edges
07. Solder bridges		» Tight clearance between the solder mask and copper pads results in solder bridge	» Minimum solder mask web: Green: 4 mil Other colors: 5 mil
08. Overlapping silkscreen		» Inappropriate text clearance from the solder mask causes the silkscreen to overlap with the adjacent one or coincide with the SMT pad	» Maintain 4.5 mil of standard spacing between silkscreen text and solder mask

Gerber Files

- Gerbers (or Gerber Files) are the files sent to the manufacturer that will be used to make the boards
- Engineers at the fab review files for manufacturability and then send it off to production.
- Gerber files can be generated from EDA software but needs to be reviewed by us before sending it off.
- There are other versions of PCB design files such as:
 - Gerber X2
 - OBB++

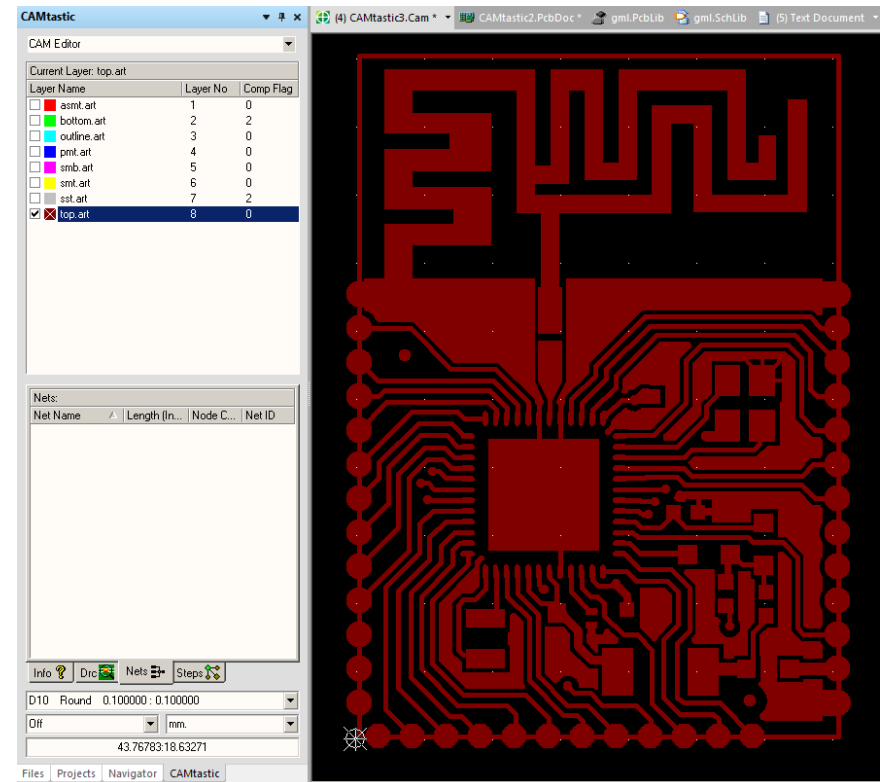
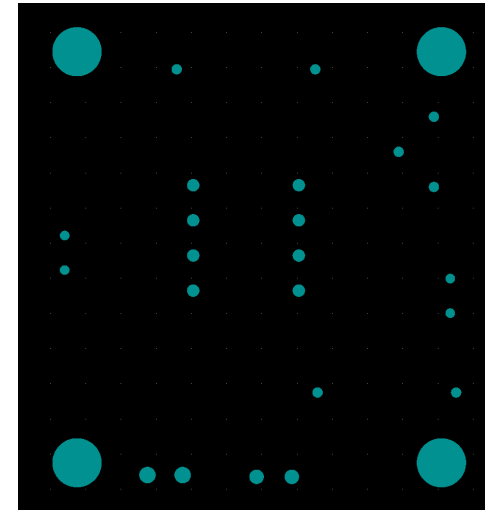


Image credit: One Thesis
<https://www.onethesis.com/gerbers-to-footprint/>

NC Drill Files

- NC Drill Files contain the information for the drill holes of the PCB.
 - These are generated separately from the Gerber Files but are just as necessary for the manufacturing process.

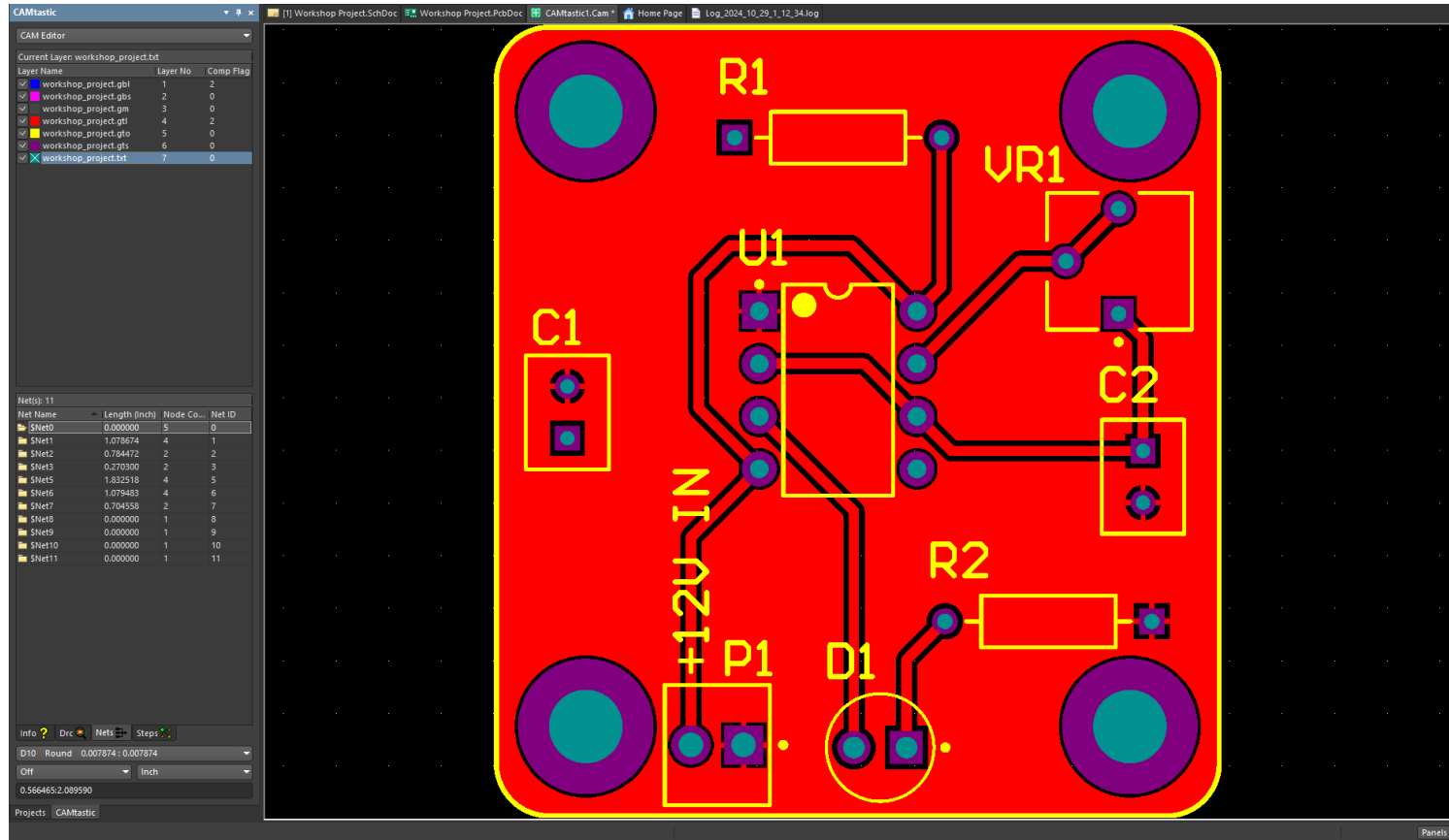


NCDrill File Report For: Workshop Project.PcbDoc 10/29/2024 1:09:38 AM

Layer Pair : Top Layer to Bottom Layer
ASCII RoundHoles File : Workshop Project.TXT

Tool	Hole Size	Hole Tolerance	Hole Type	Hole Count	Plated	Tool Travel
T1	28mil (0.7mm)		Round	4	PTH	1.29inch (32.82mm)
T2	30mil (0.75mm)		Round	7	PTH	2.02inch (51.35mm)
T3	35mil (0.9mm)		Round	8	PTH	0.90inch (22.86mm)
T4	41mil (1.05mm)		Round	2	PTH	0.10inch (2.54mm)
T5	47mil (1.19mm)		Round	2	PTH	0.10inch (2.54mm)
T6	140mil (3.556mm)		Round	4	PTH	3.24inch (82.30mm)
Totals				27		
Total Processing Time (hh:mm:ss) : 00:00:00						

Altium CAM Viewer / CAMTastic



- Altium has a built-in CAM viewer and editor called CAMTastic which can be used to verify design files.
- CAMTastic isn't very intuitive to use but can be useful to verify designs files within Altium.

Questions?

Questions?

Other Topics for Today

- Design Reuse Schematics
- Microcontroller Layout Guidelines (ESP32)
- Rooms / Grouping
- Exporting Gerber Design Files
- Work Time and Design Review / Discussion

- Free Work Time and Design Reviews

Download Today's Project Files

Navigate to the workshop GitHub and
download today's files listed under
Week04

<https://github.com/AdrianSucahyo/IEEE-PCB-Workshop-Resources-2025>