

# Low-Power Amplifier-Discriminators for High Time Resolution Detection

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**Abstract**—Low-power amplifier-discriminators based on a so-called NINO architecture have been developed with high time resolution for the readout of radiation detectors. Two different circuits were integrated in the NINO13 chip, processed in IBM 130 nm CMOS technology. The LCO version (Low Capacitance and consumption Optimization) was designed for potential use as front-end electronics in the Gigatracker of the NA62 experiment at CERN. It was developed as pixel readout for solid-state pixel detectors to permit minimum ionizing particle detection with less than 180 ps rms resolution per pixel on the output pulse, for power consumption below 300  $\mu$ W per pixel. The HCO version (High Capacitance Optimization) was designed with 4 mW power consumption per channel to provide timing resolution below 20 ps rms on the output pulse, for charges above 10 fC. Results presented show the potential of the LCO and HCO circuits for the precise timing readout of solid-state detectors, vacuum tubes or gas detectors, for applications in high energy physics, bio-technologies or medical imaging.

**Index Terms**—CMOS circuits, detector instrumentation, fluorescence spectroscopy, high energy physics instrumentation, photodetectors.

## I. INTRODUCTION

THE quest of knowledge in High Energy Physics (HEP) requires constant improvement of radiation detectors time-resolution (now in the range of tens of picoseconds). The most stringent time requirements are met for detectors measuring the transit-time of relativistic particles in order to identify the particles momentum and energy. This particle identification technique is done with Time Of Flight detectors (TOF), such as the TOF detector of the ALICE experiment at CERN. This detector comprises Multi-gap Resistive Plate Chambers (MRPCs) [1] read out by electronic circuits called NINO. These front-end channels produce Low Voltage Differential Signals (LVDS) with less than 25 ps rms time jitter [2] and are read-out by time to digital converters [3]. An overall time-resolution of about 50 ps rms is achieved with this readout [4]. For future experiments, TOF detectors with ultra high-time resolution below 10 ps could moreover be expected with the use of Micro-Channel Plate detectors (MCP) and dedicated electronics, as already shown in [5].

In addition, higher time-resolution has also to be achieved with solid-state particle detectors, in order to be combined with high spatial resolution, radiation hardness and material budget.

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This will be mandatory for tracking in different future experiments to be built [6], as for example in the NA62 experiment at CERN. This experiment proposes to measure the very rare kaon decay  $K^+ \rightarrow \Pi^+ \nu \bar{\nu}$  at the CERN SPS [7] and requires tracking of the 400 GeV/c proton beam with 1 GHz total rate within minimum material budget. This so-called “Gigatracker” [8] will comprise hybrid pixel detectors with a pixel size of  $300 \times 300 \mu\text{m}^2$ . It will provide measurements of beam particles direction, momentum and time with a resolution below 150 ps rms in order to separate close-in-time tracks with good efficiency. However, while solid-state hybrid pixel detectors have reduced in the past decade position resolutions down to few tens of microns, their time resolution hasn’t kept pace and needs to be improved. In comparison to standard pixel detectors, different electronic architectures have to be developed to build a time-resolved pixel detector. The readout chip has thus to integrate low-power high time-resolution amplifier-discriminators in each pixel and to perform internal time to digital conversion of the timing information delivered by each pixel. In that way, digital information of the time and position of each track can be driven out of the pixel detector. In this context, we have studied the possibility to integrate in each pixel of such detector a circuit based on the NINO architecture successfully used in the ALICE experiment. However, complete re-design of the circuit had to be done to implement this architecture as front end readout of pixel detectors. This involved dramatic reduction of power consumption (2 orders of magnitude) and strong reduction of noise and of minimum detectable charge (1 order of magnitude). These reductions are potentially attainable thanks to the low detector capacitances involved in pixel detectors (few hundred femtofarads compared to few picofarads for vacuum tubes or gas detectors). This developed circuit, referred to as LCO (Low Capacitance Consumption Optimization), is integrated in the NINO13 chip designed in a 130 nm CMOS technology.

Improvement of the radiation detection time-resolution is also required for medical imaging and biotechnologies, and the different time-resolved techniques developed for HEP already proved to have a high potential for such applications. The NINO circuit developed for the ALICE experiment [2] already showed interesting potential for the readout of solid-state photon detectors for Positron Emission Tomography (PET) [9]. It also permits to readout MCP photomultipliers and to enhance performance in event timing and detector throughput for photon counting [10]. Applications in life science utilizing time resolved spectroscopy, particularly in the growing field of proteomics, could greatly benefit from these performance enhancements [10]. A second circuit based on the NINO architecture was thus developed to address multi-channel very high

TABLE I  
PERFORMANCE OF THE NINO CIRCUIT IN 250 nm CMOS TECHNOLOGY

NINO 250 nm CMOS technology	
Peaking time	1 ns
Noise (with detector)	< 5000 e <sup>-</sup> rms
Front edge time jitter	10 to 25 ps rms
Power consumption	30 mW / channel
Discriminator threshold	20 to 100 fC
Input resistance	30 to 100 Ω

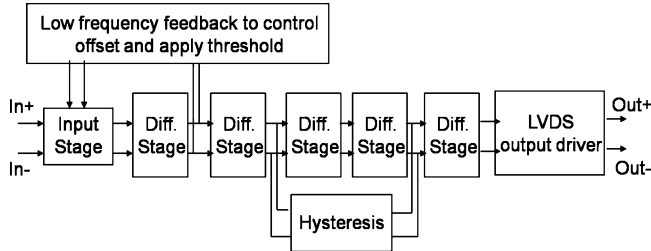


Fig. 1. Block diagram of the NINO architecture used for the LCO and HCO circuits.

time-resolution readout of detectors with few picofarads capacitance, such as photo-detectors. This amplifier-discriminator, called HCO (High Capacitance Optimization), is also integrated in the NINO13 chip and is a direct optimization of the NINO circuit from a 250 nm to a 130 nm CMOS technology.

## II. THE NINO LOW-POWER AMPLIFIER DISCRIMINATOR

The LCO and HCO amplifier-discriminators that we designed are based on the so-called NINO architecture, which was first implemented in a 0.25 μm CMOS technology. Performances of this first circuit based on the specific NINO technique are summarized in Table I and detailed in [2].

This readout technique, detailed in [2] and shown in Fig. 1, is fully differential in order to obtain a large immunity against power supply noise and ground noise and the circuit can be efficiently used in differential or single ended mode.

The input currents are sensed by the input current-to-voltage converter which is based on a balanced common gate cascode stage, enabling a low input resistance on each circuit input [2]. For the readout of MRPC or of photomultipliers, which have high capacitance (> 2 pF), this low input resistance (down to 30 Ω for the HCO circuit) permits to achieve high bandwidth, low crosstalk and to minimize signal reflection (by matching the circuit input to the resistance of the transmission line connecting the detector to the circuit). In pixel detectors, connection of the sensor to the circuit is via a bump bond and the load capacitance is of few hundreds femtofarads so that a higher input resistance can be used (around 2 kΩ for the LCO circuit), lowering the power consumption.

The transimpedance stage outputs have an imposed DC offset acting as threshold as the differential signal is then amplified by 5 cascaded differential amplifiers. These stages provide a sufficient gain to reach signal saturation so that the circuit operates as a discriminator. The threshold is set by a voltage difference applied externally on two symmetrical inputs, acting on the DC

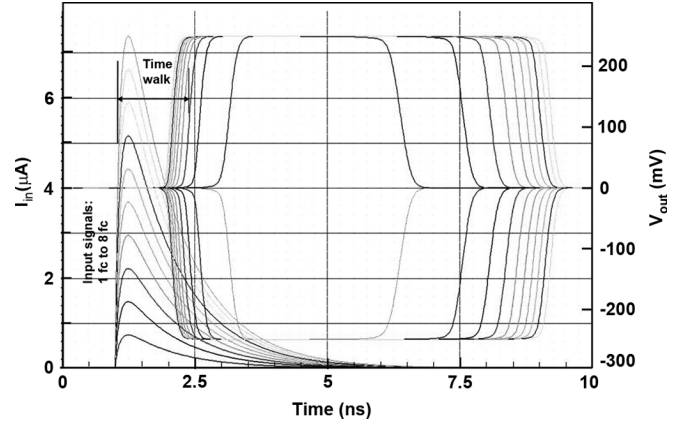


Fig. 2. Illustration of the NINO differential outputs: simulations of the LCO circuit for input charges varying from 1 fC to 8 fC. Pulse width increases and time walk decreases for increasing input charge.

stabilization feedback circuit and setting the DC voltage difference at the output of the transimpedance stage. This low-frequency feedback circuit is also used as the common mode rejection ratio circuit. A positive loop feedback circuit can also be enabled to add a small hysteresis on the discriminator threshold. Finally, a Low Voltage Differential Signals (LVDS) driver permits to have NINO outputs compatible with any LVDS receiver.

The NINO architecture enables the generation of LVDS pulses for a given input current and can be approximated as a time over threshold technique [9]. The output pulse width increases for increasing input currents, as a result of the increasing saturation time of the differential amplifiers. Moreover, the time walk between the input signal time and the output pulse leading edge also varies as a function of the input current, decreasing for increasing charges, i.e., for increasing pulse width. These variations in the LVDS output signals are illustrated in Fig. 2 by simulation results obtained on the LCO circuit for input charges varying from 1 fC to 8 fC.

The pulse width information hence permits to retrieve the input signal charge and to correct time walk variations induced by input currents with different amplitudes (even for a large dynamic scale). The LVDS receiver has therefore to provide the timing measurement of both leading and trailing edges in order to retrieve the exact timing and the input charge.

## III. NINO LCO CIRCUIT

### A. Towards a Time-Resolved Pixel Detector

A challenging pixel Gigatracker system has to be developed for the NA62 experiment at CERN [8]. It will be made of 3 stations, with a surface of about 12 cm<sup>2</sup> each. Tracking will be done by hybrid pixel detectors, with a pixel cell dimension of 300 μm × 300 μm. The hit rates in the centre of the beam of 50 MHz/cm<sup>2</sup> and the timing precision around 100 ps per pixel result in a large output data rate of more than 4 Gbit/s/chip. Radiation levels are expected to be 10<sup>5</sup> Gy and 2 × 10<sup>14</sup> cm<sup>-2</sup> 1 MeV neutron equivalent fluence each running year. In order not to degrade the momentum resolution a very low material budget of 0.45% X<sub>0</sub> is targeted, imposing a pixel chip thinned down to 100 μm and a thin silicon or diamond sensor (150 to

200  $\mu\text{m}$  thickness), pushing the discrimination sensitivity of the front-end electronics to be around 1 fC.

The NA62 collaboration has chosen to evaluate two different architectures in the R&D phase for the development of the time-resolved pixel chip. A first architecture, the pixel TDC solution, implements both the analog and digital signal processing inside the pixel cell [11]. The other solution, the “End of Column” (EOC) architecture, integrates only the analog readout in the pixel, signals being sent via transmission lines to EOC peripheral circuits for digital processing. This second approach avoids the use of high speed clock in the active pixel array and allows separation of digital signals from the analog front-end, minimizing the digital crosstalk and reducing the level of single event upset protection. However, this architecture imposes to transmit high speed pulses on up to 13.5 mm, while keeping timing precision to 100 ps without disturbing low noise electronics in the pixel cells.

The LCO circuit was designed to study the possibility to implement a discriminator based on the NINO architecture as front-end electronics for a time-resolved pixel detector, for use in the EOC solution. In comparison to the NINO circuit (Table I), requirements are a power consumption below 350  $\mu\text{W}$  per pixel, a discrimination threshold around 1 fC and a time resolution below 150 ps rms. Circuit optimization was done in a 130 nm CMOS technology, targeting the sensor readout with a load capacitance on the channel of 300 fF (including sensor and parasitic capacitances at the circuit input). All transistors dimensions and biases were strongly reduced in comparison to the NINO circuit. For example, the width of the common gate input transistor was decreased from 640  $\mu\text{m}$  down to 8  $\mu\text{m}$  while the biasing current decreases from 1.5 mA to 15  $\mu\text{A}$ . This strong scaling-down of the circuit permits to attain low-power consumption of 250  $\mu\text{W}$  (2 orders of magnitude reduction), at the price of a higher input resistance ( $\sim 2 \text{ k}\Omega$ ) whose impact on the timing performance is limited thanks to the low load capacitance. The LCO channel layout fits in 180  $\mu\text{m} \times 35 \mu\text{m}$ , leaving enough space in the pixel for the transmission lines needed for the EOC pixel chip solution. The circuit threshold is set by a voltage difference applied externally on two symmetrical inputs.

### B. Electrical Characterizations

Performance of the LCO circuit was first evaluated with input currents generated by applying voltage steps to 100 fF injection capacitances integrated in the chip between the input pads and the channels inputs. The voltage pulses have 800 ps rise time and 8 ps rms time precision with respect to the generator output trigger. These tests permit to analyze the performance of the LCO circuit for a low load capacitance of around 200 fF (similar conditions of operation than expected in the NA62 pixel chip).

The time difference between the leading edge of the LVDS output pulse and the trigger output of the pulse generator is referred to as  $t_{\text{lead}}$  in the following, and the time difference between the trailing edge and the trigger as  $t_{\text{trail}}$ . These time differences were measured for different input voltage amplitudes, i.e., for different input charges. For each input charge, a set of 1000 measurements of ( $t_{\text{lead}}$ ,  $t_{\text{trail}}$ ) was acquired, and data was

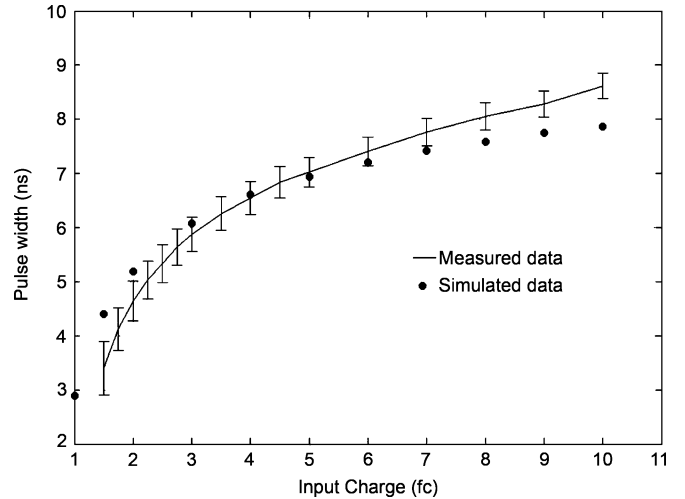


Fig. 3. LCO channel output pulse width for different input charges.

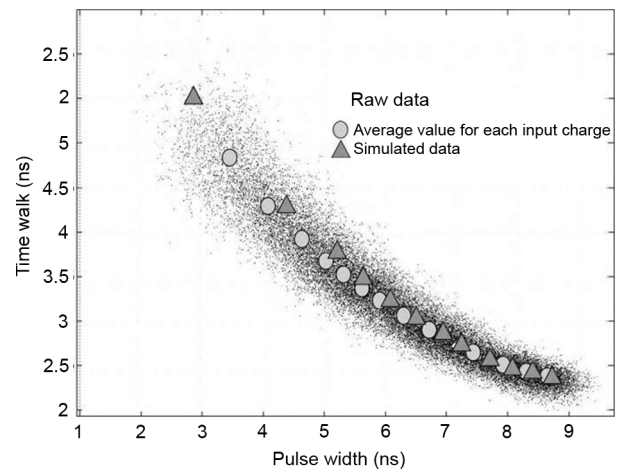


Fig. 4. Variations of the LCO channel output pulse leading edge time walk as a function of the output pulse width.

recorded for charges varying from 1 fC to 10 fC. The pulse width, time-walk and time precision on both leading edge and pulse width are therefore measured. The output pulse exhibits 800 ps rising and falling times. The pulse width ( $t_{\text{trail}} - t_{\text{lead}}$ ) varies from 2.5 ns for 1.5 fC input charge to 8.5 ns for 10 fC. These experimental results are shown in Fig. 3 with error bars corresponding to the pulse width uncertainty for each charge (at  $\pm 3\sigma$ ). Results are well fitted by simulations done for a 200 fF input load capacitance.

The LCO output pulse leading edge time  $t_{\text{lead}}$  depends on the input signal amplitude, as shown in Fig. 2. All the  $t_{\text{lead}}$  time measurements acquired for the different input charges are displayed in Fig. 4 as a function of the measured pulse width, together with the mean time walk measured for each charge (i.e., mean time walk for a mean pulse width).

Time walks presented in Fig. 4 include systematic walk due to the propagation of the signal to the oscilloscope and a variable time walk  $t_{\text{lead\_var}}$  due to the signal formation in the electronic channel, decreasing for increasing input current amplitude. These time variations are contained in about 2 ns for input charges varying from 1 fC to 10 fC. From the average time walk

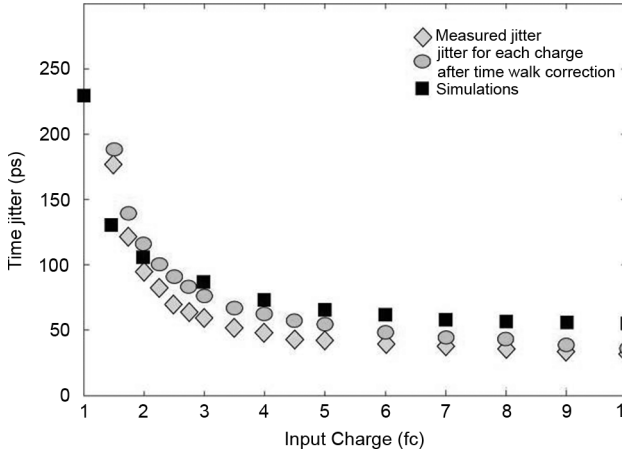


Fig. 5. LCO channel timing precision.

measured for the different input signal amplitudes, it is possible to retrieve an equation defining the average relation between time-walk variation  $t_{\text{lead\_var}}$  and pulse width. This relation  $t_{\text{lead\_var}} = f(t_{\text{trail}} - t_{\text{lead}})$  permits to obtain from the data set  $(t_{\text{lead}}, t_{\text{trail}})$  the absolute  $t_{\text{lead\_var}}$  information. It therefore allows correcting for the time-walk variations, so that  $(t_{\text{lead}} - t_{\text{lead\_var}})$  is used as absolute measured time information. This technique permits to have high-time resolution even for input signals amplitude varying on a large dynamic scale.

Time precision attained with the LCO circuit is shown in Fig. 5. The time jitter on the output pulse rising edge was first retrieved from each input charge measurements. This represents the jitter measured for signals with similar charge at the circuit input (referred to as measured jitter in Fig. 5). Measurements show a time resolution of 50 ps rms for charges above 4 fC and an increasing time jitter for lower charges ( $\sim 150$  ps rms at 1.5 fC). The global time precision reached with the LCO circuit for any input signal amplitude is then retrieved from the relation between mean time-walk and pulse width. The systematic time walk induced by the signal propagation time is not taken into account in this study, as we focus on the event time fluctuations. The arrival time of the signal  $t_{\text{event}}$  is thus obtained from any set of data  $(t_{\text{lead}}, t_{\text{trail}})$  by:  $t_{\text{event}} = t_{\text{lead}} - f(t_{\text{trail}} - t_{\text{lead}})$ . This permits to get the precision in the time information  $t_{\text{event}}$  for any set of measurements, even with large dynamic scale in input signal amplitudes. The time walk correction technique was applied to all the raw data and the event time precision was then analyzed for each set of measurements obtained for a particular charge. This permits to estimate the uncertainty in the time information  $t_{\text{event}}$  for a given input charge. The results are presented in Fig. 5 and referred to as time jitter after time walk correction.

The uncertainty in the measured and corrected time information is of about 175 ps rms for a 1.5 fC input charge and down to around 50 ps rms for charges above 4 fC. The global time precision which can be attained for a particular application will then depend on the statistical distribution of the input signals amplitude, as low charge signals exhibit higher time uncertainty than signals with a charge higher than 4 fC. Measurements presented in Fig. 5 demonstrate that for applications with event charges of 1.5 fC and more, the time precision reached by the LCO can be expected between 50 and 175 ps rms for a 200 fF capacitance.

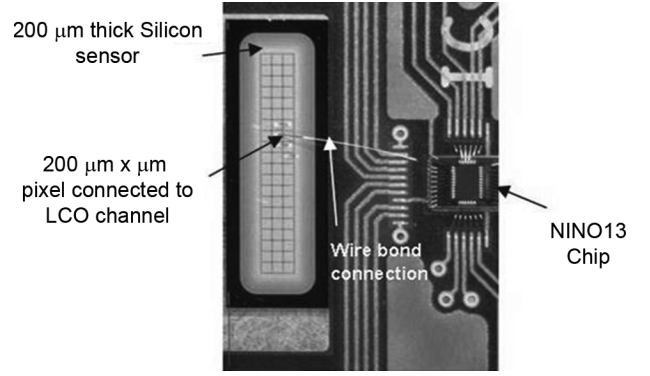


Fig. 6. A 200  $\mu\text{m}$  thick p-in-n silicon sensor with a  $300 \mu\text{m} \times 300 \mu\text{m}$  pixel wire-bonded to a LCO channel of the NINO13 chip.

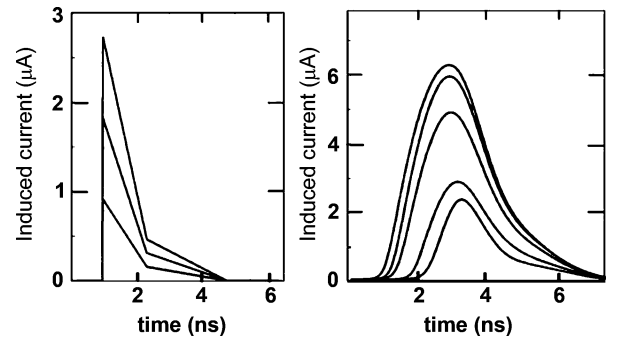


Fig. 7. Expected induced signals in a 200  $\mu\text{m}$  thick p-in-n silicon sensor. Left: for a Minimum ionizing particle (MIP), Right: for the 1060 nm laser pulses used in the experiment, for different laser biases.

### C. Tests With a 200 $\mu\text{m}$ Thick Silicon Sensor

The NA62 sensor baseline is a 200  $\mu\text{m}$  thick pixelated p-in-n silicon sensor which will be bump bonded to the final pixel ASIC. A first sensor was tested, with one of the  $300 \mu\text{m} \times 300 \mu\text{m}$  pixels wire-bonded to a LCO circuit (Fig. 6). Tests were carried out using a 1060 nm pulsed laser so that free carriers are generated homogeneously through the sensor thickness, as it will be the case for the 400 GeV/c protons to be tracked in the NA62 experiment.

A fast signal creation is required for the silicon sensor so that it has to be operated close to saturation velocity. For particles creating quasi-simultaneously free carriers equally distributed all along their tracks through the sensor, the induced current will exhibit very fast rise time corresponding to the generation time of the carriers. This maximum amplitude of the signal corresponds to the maximum number of carriers drifting at their saturation velocity.

While generated carriers drift and get collected at the sensor electrodes, the induced current decreases due to the reduced amount of moving charge. The signal decay shows a fast component caused by electrons and a longer decay due to the holes (Fig. 7). The sensor is expected to provide full charge in about 4 ns when operated at saturation velocity. In our tests, the induced currents are moreover shaped by the laser pulse form. Laser pulse shapes were measured and integrated in the calculations of induced signals. These signals from the silicon sensor under the pulse excitation are displayed in Fig. 7.

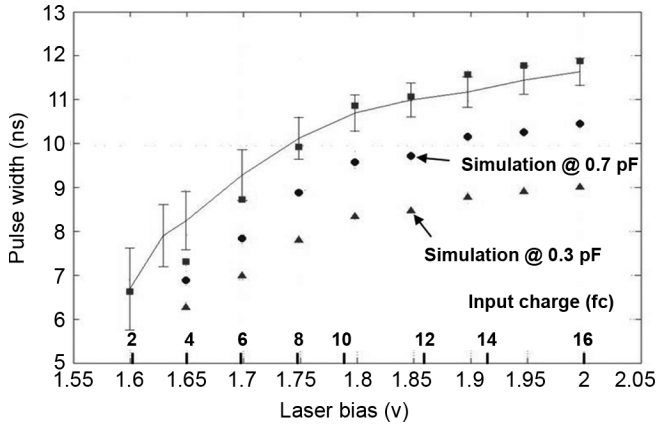


Fig. 8. LCO channel output pulse width for different laser pulses, i.e., different input charges. Measurements are compared to simulations carried out for 1.2 pF, 700 fF and 300 fF loading capacitance.

The connection from the pixel diode to the circuit introduces high parasitic capacitances, as it is done via a wire bond onto a pad integrated in the chip. This bond pad has to be designed large enough to allow the wire bonding and introduces about 0.7 pF parasitics. These tests are done with higher load capacitance than it will be the case for the pixel chip. The bump-bonding of the sensor allows the design of smaller pads on the integrated circuit, leading to a parasitic capacitance of about 50 fF, for a total load capacitance of 200 to 300 fF. A simulation work was therefore done after the measurements to estimate what will be the LCO performance for a load capacitance of 200 to 300 fF.

Measurements were done for different laser biases, corresponding to different input charges (Figs. 7 and 8). For each laser bias, about 1000 measurements of the time information ( $t_{\text{lead}}$ ,  $t_{\text{trail}}$ ) on the output pulses were acquired. The pulse width was shown to vary from 6.5 ns to 11.5 ns for charges varying from 2 fC to 16 fC. These experimental results are well fitted by circuit simulations using the calculated signals shown in Fig. 7 and a load capacitance on the LCO circuit of 1.2 pF (Fig. 8). Further simulations were done using similar input signals but reduced load capacitances of 700 fF and 300 fF, clearly showing the strong impact of the load capacitance on the LCO performance.

An increased input capacitance slows down the input signal as it pushes the input pole to be the circuit dominant pole. The signal amplitude is thus lowered and becomes longer. High load capacitance therefore gives rise to a reduced minimum charge which can be detected and to longer output pulse width, as seen in Fig. 8. The channel noise also is increased so that together with the signal shaping it leads to higher time jitter. This is seen in Fig. 9 where measurements of the time jitter on the pulse leading edge are displayed for the different input signals, together with simulations for an input load capacitance of 1.2 pF, 700 fF and 300 fF.

The time jitter measured with the experimental set-up is thus higher than the one which will be attained in the pixel chip configuration. The simulations permit to well fit the measured data for a 1.2 pF input capacitance, so that further simulations based on the same input signals still permit to show the time jitter of the LCO circuit in the pixel chip case (i.e., for about 300 fF

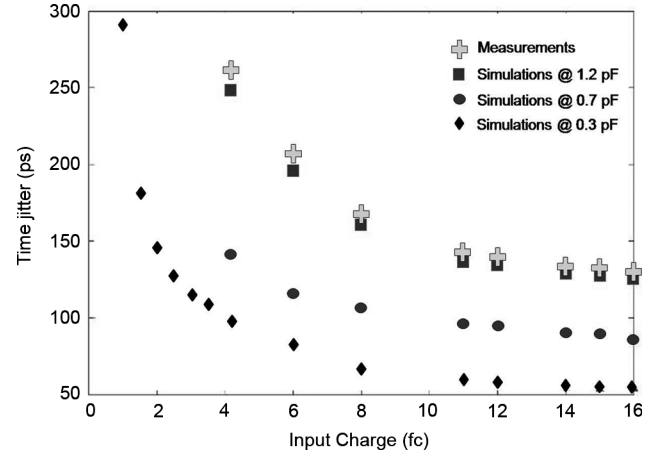


Fig. 9. Time jitter on the LCO channel output voltages for different laser pulses, i.e., different input charges. Measurements are compared to simulations carried out for 1.2 pF, 700 fF and 300 fF loading capacitance.

input capacitance). These measurements and simulations therefore show a performance of the LCO circuit, for signal shapes originating from silicon sensor operated at saturation velocity, close to the electrical characterizations previously done. It is thus possible to conclude from these different studies that the LCO circuit, in the pixel detector configuration, can provide time precision of about 170 ps rms at 1.5 fC (minimum detected charge) down to about 50 ps rms for higher charges.

Signal shape plays an important role in the minimum detected charge, in the pulse width and in time jitter. After radiation induced degradation of the sensor, ballistic effect might affect signal to noise ratio of the electronic pixel channel. Possible alternative of sensors are being studied, such as diamond sensors [12]. The LCO circuit could also be an interesting amplifier-discriminator solution for a hybrid pixel detector using 3D silicon sensors, which could also lead to higher induced signal speed [13].

#### IV. NINO HCO CIRCUIT

The HCO circuit was developed for the direct readout of detectors such as MRPC, MCP-PMT, or SiPM, i.e., detectors with a high capacitance of 5 pF to 20 pF, providing more than 10 fC per event, and capable of very high time resolution. This development was motivated by the successful use of the NINO chip for the readout of such detectors and for applications in high energy physics, fluorescence lifetime imaging and medical imaging. However, there is a need for these applications of a higher channel density and of lower power consumption [10] to permit multi-channel high-time resolution readout of the detectors, as the present circuit integrates 8 channels for a consumption of 20 mW per channel.

The HCO channel represents a direct optimization from a 0.25  $\mu\text{m}$  to a 0.13  $\mu\text{m}$  CMOS technology. The transistors sizes and biases were scaled down to permit lower power consumption for similar timing performance. The HCO channel consumption is of about 5 mW, i.e., a factor 4 reduction in comparison to the 0.25  $\mu\text{m}$  circuit. The input resistance of the HCO channels was kept low (around 50  $\Omega$ ) because of the detectors

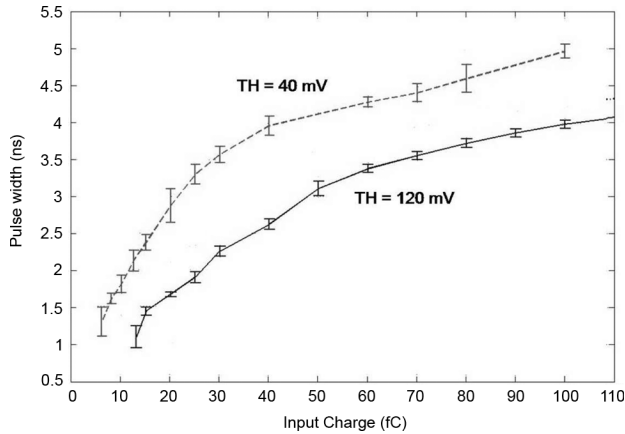


Fig. 10. HCO channel output pulse width for different input charges.

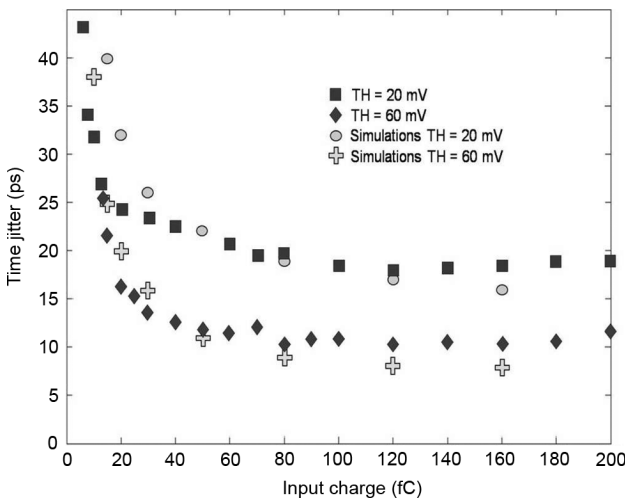


Fig. 11. HCO channel: Measured and simulated time jitter on the output pulse leading edge as a function of the input charge.

high capacitance. The circuit is powered at 1.2 V and necessitates 2 external resistances to set the input resistance and the output current.

Electrical characterizations of the HCO were done using 1 pF injection capacitance mounted on the PCB holding the NINO13 chip, so that the tests were carried out for a load capacitance of about 4 pF. The generated test currents last about 800 ps. The HCO differential outputs are LVDS (500 mV differential pulses), with about 600 ps rising and falling times. The measured pulse widths as a function of the input charges are displayed in Fig. 10 for different circuit threshold values. A minimum charge of 10 fC can be detected, giving rise to an output pulse width of about 1.25 ns. The pulse width increases with the input charge and a pulse of 4 ns to 5 ns is seen for an input charge of 100 fC.

Timing performance of the HCO channel is shown in Fig. 11, with the time jitter measured on the output pulse leading edge as a function of the input signal charge.

The time jitter measurements for the two different threshold values are well fitted by the circuit simulations. The HCO channel exhibits below 20 ps rms at 20 fC and down to about 10 ps rms for charges higher than 60 fC. As the pulse generator

TABLE II  
PERFORMANCE OF THE LCO AND HCO CIRCUITS DEVELOPED IN 130 NM CMOS TECHNOLOGY AND INTEGRATED IN THE NINO13 CHIP

NINO13 CHIP in 130 nm CMOS technology		
Performance	LCO	HCO
Power consumption	250 $\mu$ W / channel	4 mW / channel
Discriminator threshold	1.5 to 5 fC	10 to 100 fC
Peaking time	800 ps	600 ps
Input resistance	2 k $\Omega$	30 to 100 $\Omega$
Front edge jitter	175 to 50 ps rms	25 to 6 ps rms
Detectors readout	Time-resolved hybrid pixel detectors	MRPC, Vacuum tubes (MCP-PMT), Solid-state photodetectors (SiPM...)
Applications	High Energy Physics (NA62)	HEP, Biotechnologies, Medical Imaging

itself gives about 8 ps rms variations between the pulse trigger and the test pulse, one can expect about 6 ps rms time jitter for 100 fC and higher input charges.

## V. CONCLUSION

Low-power amplifier-discriminators based on the so-called NINO architecture were designed in a commercial 130 nm CMOS technology. This development follows the successful use of the NINO circuit designed in a 0.25  $\mu$ m technology. This circuit is widely used in the Alice experiment at CERN and under development in many different other fields of applications. The two adaptations presented, the LCO and HCO circuits, prove to have interesting potential and widen the perspectives of applications of the circuit readout technique. The HCO circuit targets multi-channel readout of high capacitance detectors such as MRPC, vacuum tube detectors (MCP-PMT) or solid-state photodetectors (SiPM, APD...), while the LCO addresses the development of front-end electronics for a time-resolved hybrid pixel detector. Performances of the two designed circuits are summarized in Table II.

Both circuits have LVDS outputs, with the output pulse width varying as a function of the input charge. This pulse width information permits to both retrieve the input signal amplitude and to correct for time-walk variations, so that high-time resolution can be attained even for input signals varying on a large dynamic scale. Strong scaling down of the existing circuit permitted the development of the ultra low power LCO circuit (250  $\mu$ W/channel), able to readout bump-bonded silicon or diamond sensors with a time jitter between 175 and 50 ps rms. The technology change also permitted the development of the HCO channel with down to 6 ps rms time precision for 5 mW power consumption per channel. This circuit enables multi-channel readout in a more compact way for high capacitance detectors, principally for applications in biotechnologies [11] or medical imaging [10].

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## REFERENCES

- [1] A. Akindinov *et al.*, "The multi-gap resistive plate chamber as a time-of-flight detector," *Nucl. Instrum. Methods Phys. Res. A*, vol. A456, no. 1–2, pp. 16–22, 2000.
- [2] F. Anghinolfi, P. Jarron, F. Krummenacher, E. Usenko, and M. C. S. Williams, "NINO: An ultrafast low-power front-end amplifier discriminator for the time-of-flight detector in the ALICE experiment," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 5, pp. 1974–1978, Oct. 2004.
- [3] J. Christiansen, High Performance Time to Digital Converter [Online]. Available: [http://tdc.web.cern.ch/tdc/hptdc/docs/hptdc\\_manual\\_ver2.2.pdf](http://tdc.web.cern.ch/tdc/hptdc/docs/hptdc_manual_ver2.2.pdf)
- [4] E. Scapparone, "The time-of-flight detector of the ALICE experiment," *J. Phys. G: Nucl. Part. Phys.*, vol. 34, pp. S725–S728, 2007.
- [5] J. Va'vra, "A high-resolution TOF detector—A possible way to compete with a RICH detector," *Nucl. Instrum. Methods Phys. Res. A*, vol. A595, no. 1, pp. 270–273, 2008.
- [6] J. E. Brau, "The science and challenges for future detector development in high energy physics," in *Proc. SNIC Symp.*, Stanford, CA, Apr. 3–6, 2006.
- [7] A. Ceccucci, *Future of Kaon Experiments*. Moscow, Russia: ICHEP, 2006, pp. 798–802.
- [8] G. Dellacasa *et al.*, Pixel Readout Architecture for the NA62 Gigatracker, TWEPP Sep. 26, 2008.
- [9] F. Powolny *et al.*, "Development of a new photo-detector readout technique for PET and CT imaging," *Nucl. Instrum. Methods Phys. Res. A*, vol. A561, no. 1–2, pp. 329–332, 2007.
- [10] J. Lapington *et al.*, "A multi-channel high-time resolution detector for high-content imaging," *Nucl. Instrum. Methods Phys. Res. A*, to be published.
- [11] M. Fiorini *et al.*, "The P326 (NA48/3) Gigatracker: Requirements and design concept," *Nucl. Instrum. Methods Phys. Res. A*, vol. A572, pp. 290–291, 2007.
- [12] H. Frais-Kölbl, E. Griesmayer, H. Kagan, and H. Pernegger, "A fast low-noise charged-particle CVD diamond detector," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3833–3837, Dec. 2004.
- [13] A. Kok *et al.*, "3D detectors—State of the art," *Nucl. Instrum. Methods Phys. Res. A*, vol. A560, pp. 127–130, 2006.