

# Booting Nios® II from Quad Serial Configuration (EPCQ), Cyclone V GX Starter Kit.

Written by: Holguer A. Becerra

## 1) Quartus Configuration:

- 1) Open and modify the <project>.qsf file with a text editor and add the following lines:

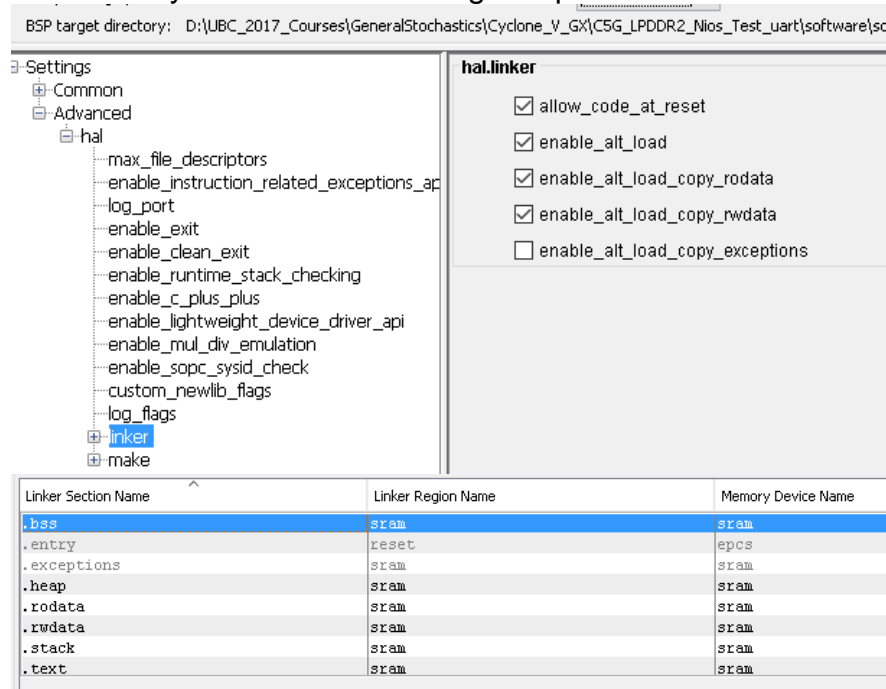
```
set_global_assignment -name STRATIXV_CONFIGURATION_SCHEME  
"ACTIVE SERIAL X1"  
set_global_assignment -name ENABLE_INIT_DONE_OUTPUT ON
```

- 2) Delete the “db” and “incremental\_db” folder if it is needed.
- 3) Open your Qsys Project.
- 4) Ensure the Nios II’s reset vector is pointing at EPCS/EPCQ Controller.
- 5) Ensure the Nios II’s Exception Vector is pointing at the memory of your preference, sram, lpddr2, or memory on chip.
- 6) Generate your Qsys design.
- 7) Compile your design with Quartus.

## 2) Open Nios II IDE.

- a. Create a new project.
- b. Right-click on the folder and go to Nios II-> BSP Editor.
- c. Make sure you have the following setup.

BSP target directory: D:\UBC\_2017\_Courses\GeneralStochastics\Cyclone\_V\_GX\C5G\_LPDDR2\_Nios\_Test\_uart\software\sd



Linker Section Name	Linker Region Name	Memory Device Name
.bss	sram	sram
.entry	reset	epcs
.exceptions	sram	sram
.heap	sram	sram
.rodata	sram	sram
.rwdata	sram	sram
.stack	sram	sram
.text	sram	sram

- d. Generate the BSP, and exit

- e. Right -Click and Build the software.

### 3) Open Nios II Command Shell.

- a. Go to the folder in which <software>.elf is stored.
- b. Type the following lines (it might change on yours) on the console:

First

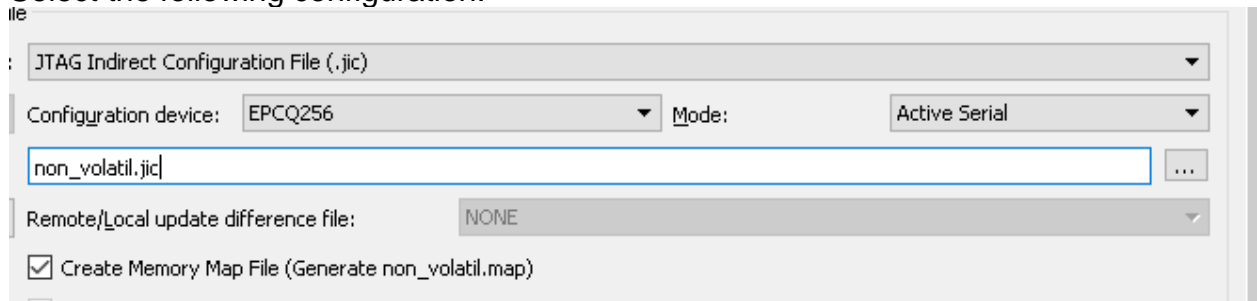
```
noiguer@adrixcorp /cygdrive/d/UBC_2017_Courses/GeneralStochastics/Cyclone_V_GX/C5G_LPDDR2_Nios_Test_uart/software/sd_card_test
$ elf2flash --input="D:/UBC_2017_Courses/GeneralStochastics/Cyclone_V_GX/C5G_LPDDR2_Nios_Test_uart/software/sd_card_test/sd_card_test.elf" --output=sw.flash --epcs verbose
```

Third:

```
$ nios2-elf-objcopy -I srec -O ihex sw.flash sw.hex
```

### 4) Generating non\_volatil.jic file and programming the EPCQ.

- a. Go to Quartus and then File->Conver Programming Files...
- b. Select the following configuration:



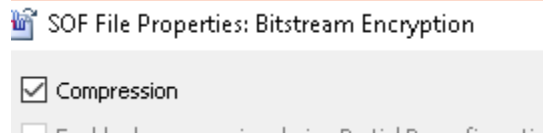
- c. Press on Flash Loader, then on "Add Device.." and then Select Cyclone V -> 5CGXF5C6, and press ok.

File/Data area	Properties	Start Address
Flash Loader		
5CGXF5C6		

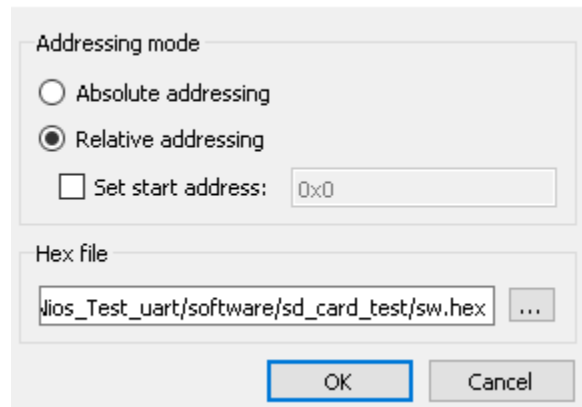
- d. Press on SOF Data, then press on Add File, and Select your <quartus>.sof file.

SOF Data	Page_0	<auto>
C5G_LPDDR2_Nios_Test.sof	5CGXF5C6F27	

- e. Press on the <quartus>.sof file, press properties, and enable compression, and press on ok.



- f. Press on “Add Hex Data..”, select the “sw.hex” file which was generated in the step 3, and enable “Relative addressing”.



- g. At the end, you might have something like the following (The same order).

Input files to convert			
File/Data area	Properties	Start Address	
Flash Loader			
5CGXFC5C6			
Hex Data	Relative addressing	<auto>	
sw.hex			
SOF Data	Page_0	<auto>	
C5G_LPDDR2_Nios_Test.sof	5CGXFC5C6F27		

- h. Press on “Generate”.
- i. Open Quartus Programmer, and make sure you have the board connected to the USB.
- j. Press on “Add File...”, select the non\_volatil.jic file, enable “program/configure”.
- k. Finally, press on “Start”.
- l. In order to check everything works fine, restart your board.
- m. Nios II should be running.

You can find the jic file and the solution in the following link

<https://github.com/Adrizcorp/FPGAs/tree/master/Cyclone%20V%20GX%20Starter%20Kit/Booting%20Nios%20II%20Example> .

