File structure
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The zip file contains the code listing, SOPC component files, C files, DE2 amendment files, and hardware and software image files. It is organized as follows:

- chapter_lisitng: It contains the listings of HDL codes and C codes. The files are organized in chronological order.
- chu_ip_drv: It contains the C driver (.c and .h) files of IP cores in Parts III and Part IV. Since the driver files are not integrated with HAL, the corresponding files must be manually copied to the software application project directory when a core is used in a Nios II system.
- chu_ip_vlog: It contains the Verilog files (.v) and SOPC component files (.tcl) of IP cores in Parts III and Part IV. Each subdirectory contains the files for one core. The chu_avalon_fifo directory contains no IP core but includes the FIFO files of Chapter 5, which are used by the chu_avalon_ps2 and chu_avalon_audio cores. The IP cores can be integrated into SOPC Builder by following the procedure in Section 17.10.1. Altera Component Editor v10.1 sp1 was used for the development.
- chu_ip_vlog_de2: The codes in the book are targeted for the DE1 board. Minor modifications are needed for the DE2 board. This directory contains the modified codes. Detailed use is explained in the pdf file within the directory.
- de1_build: It contains the FPGA configuration file of the comprehensive Nios II system in Section 17.10.2 and software image files for the DE1 board. These files can be used for quick demo or software development. Note that the files can only be used for the DE1 board. Detailed use is explained in the pdf file within the directory.
- de2_build: It contains the FPGA configuration file of the comprehensive Nios II system in Section 17.10.2 and software image files for the DE2 board. These files can be used for quick demo or software development. Note that the files can only be used for the DE2 board. Detailed use is explained in the pdf file within the directory.